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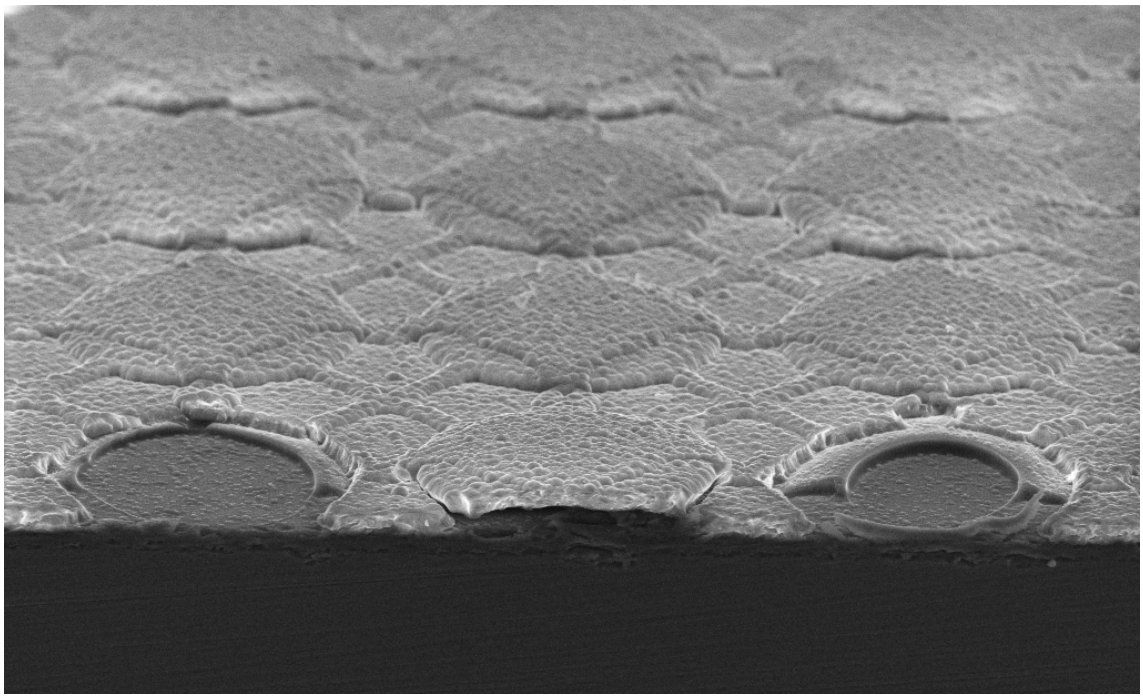

Capacitive micromachined ultrasonic transducer (cMUT) for biometric applications

Thesis for the Degree of Erasmus Mundus Master of Nanoscience and Nanotechnology

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Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden, 2012

KATHOLIEKE UNIVERSITEIT LEUVEN

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Capacitive micromachined ultrasonic transducer (cMUT) for biometric applications

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Abstract
Biometric devices (such as fingerprint sensors, iris scanners, face recognition systems etc.) are becoming more and more popular in areas where personal identification is required - migration control, physical access, online banking etc. Nowadays the most used biometric sensor is a fingerprint scanner which provides a good combination of accuracy, size and price. However, fingerprint recognition is not always successful in case of sweaty/dirty fingers and the accuracy rate can fall down to 80-90% which is not enough for high-security applications. The solution of this problem can be found in combining fingerprint pattern with other biometric data inside the finger (vein pattern or bone geometry). It can be achieved using ultrasound imaging technique and capacitive micromachined ultrasonic transducer (cMUT) is a good choice to perform these measurements. The main advantage of cMUT is ideal design compatibility with the fingerprint sensor based on capacitive method - a product of Fingerprint Cards AB (FPC) which participates as an industrial partner in this project. Modeling and fabrication of a cMUT array was done using the top interconnect layers of the CMOS technology which can be integrated in the process line of the FPC fingerprint capacitive sensor. Thus, it will be possible to create a multi-modal biometric device with an ability to acquire both fingerprint pattern and additional biometric features (vein pattern, bone geometry).

Keywords: biometrics, fingerprint, capacitive sensor, cMUT, CMOS

Contents

Chapter 1

Introduction

Biometrics is a field that studies person identification based on their biological features. According to the IBM 5-year prediction of 2011 biometric sensors will become dominating among other types of identification [1]. Just imagine how great it would be to replace bank cards, home and car keys, e-mail and Facebook passwords, for instance, with a fingerprint which is impossible to lose or forget.

There is a great number of biometric techniques that use different biological features (e.g. fingerprint, vein, iris, face, voice etc.). Probably, the most famous and well-known among them is fingerprint recognition. It has been known since 19^{th} century and actively used in criminal investigation. Nowadays fingerprint scanners are a must in embassies and migration control offices, for example, in the USA or Sweden. Many laptops and some smartphones are embedded with portable fingerprint swipe sensors which allow password-free logging in.

Chapter 2

Background

2.1 Fingerprint sensing

This Master thesis project has been done as an industrial collaboration with the biometrics company Fingerprint Cards AB (Gothenburg, Sweden) - one of the leader in production of fingerprint sensors (see Fig. 2.1 and Fig. 2.2).

Figure 2.1: Capacitive area fingerprint sensor FPC 1011F (with permission from Fingerprint Cards AB)

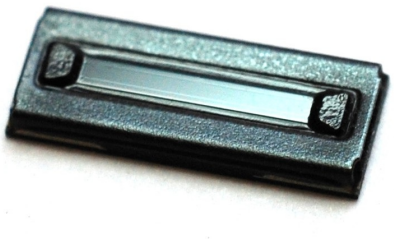


Figure 2.2: Capacitive swipe fingerprint sensor FPC 1080A (with permission from Fingerprint Cards AB)

The fingerprint sensing technique used by Fingerprint Cards (FPC) is based on the capacitive method [2]. The sensor consists of an array of electrodes and when a finger is placed on top, the voltage bias is applied between electrodes and skin creating artificial capacitors. By measuring capacitive difference between ridges and valleys a fingerprint pattern can be resolved

(see Fig. 2.3).

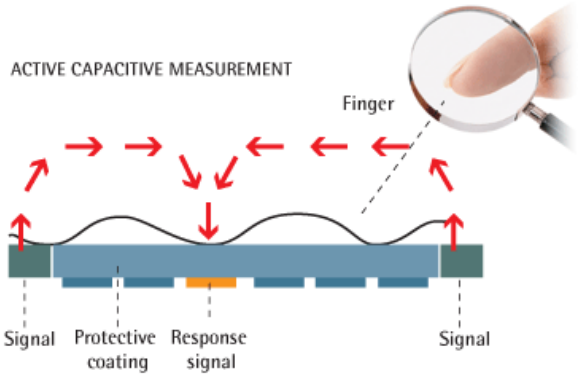


Figure 2.3: Capacitive fingerprint sensing method (with permission from Fingerprint Cards AB)

This method provides good image quality in most cases, however, sometimes it doesn't work very well. For example, in very humid environment people can have sweaty fingers which reduce the capacitive difference between ridges and valleys and result in poorer image contrast. Dirty fingers also have a negative effect on the image quality due to the same reason. In the worst cases the accuracy can drop up to 80-90% and is unacceptable for high-security applications (e.g. online banking). Therefore, a solution must be found that will eliminate the problem of sweaty/dirty fingers.

So far only one company Lumidigm has succeeded with resolving wet/dirty fingers [3]. Their technique is called multispectral imaging - an optical method that uses different wavelengths to scan several skin layers [4]. If the surface of the fingerprint is sweaty/dirty, then the pattern can be obtained from the underlying layers which have the same pattern but are not influenced by air humidity. But the sensor itself is complicated and has bulky optics which makes it very hard to integrate with mobile devices compared to small Si-based capacitive sensors.

So the challenge of creating a compact fingerprint sensor which can efficiently resolve sweaty/dirty fingers still remains unsolved. The goal of this thesis work is to suggest and evaluate such solution.

2.2 Multi-modal biometric sensing

The experience of Lumidigm showed that obtaining more biometric data can sufficiently improve the identification accuracy. This approach is called multi-modal biometric sensing and covers not only fingerprints but also all other biometric features [5]. One example of this technique can be a system that identifies a person based on both fingerprint and iris which already exists on the market [6]. However, these devices are very bulky and not suitable for mobile applications.

Multi-modality can also be applied to improve accuracy of the compact capacitive fingerprint sensor by introducing another type of biometric sensor. It might be one more fingerprint sensor but based on a different method (optical, thermal, piezoelectric etc.) or a biometric device obtaining biometric information inside the finger such as vein pattern or bone geometry [7].

The first approach is more straight-forward and has high level of maturity because figerprint sensors are developed commercial products. The idea of having several fingerprint devices combined into one dual fingerprint sensor was first introduced in [8]. It was shown to have higher accuracy rate compared to a single fingerprint scanner. Nevertheless, the problem of sweaty/dirty fingers affects all fingerprint sensing methods in smaller or larger extent and it is impossible to completely overcome it.

Therefore, a biometric device that can resolve individual biological features inside the finger (vein pattern and bone geometry) seems more promising because these features do not depend on environment conditions such as air humidity. On the other hand this kind of devices are still being developed and for some of them miniaturization is problematic.

2.3 Biometric methods overview

For the evaluation of the best technique several candidates were considered - infrared, thermal and ultrasound methods.

Infrared method can be used for imaging veins inside the finger as hemoglobin in blood is opaque to the near-infrared light ($\approx$ 800 - 1000 nm) [9]. The main

advantage of this technique is a good image quality of vein pattern but the drawback is the design which requires both light source and a camera - it makes it bulky and very hard to scale down.

Thermal method overcomes the design problem and can be made planar as it uses thermoelectric sensors which measure temperature gradient between different structures. It can be used to resolve both the fingerprint and finger vein pattern [10]. However, the drawback of this technique is isotropic heat spread which blurs the picture and leads to poor image quality.

Ultrasound method has similar pros and cons compared to thermal method. During ultrasound imaging a signal is sent in tissues and echoes from different structures are received. The device can be made planar and information about finger vein pattern as well as bone geometry can be obtained [11]. Due to acoustic scattering of ultrasound waves, the problem with blurred image still remains and has to be solved.

Regarding all advantages and disadvantages it was decided to proceed with ultrasound method as it can be realized using compact planar device architecture and provides both vein pattern and bone geometry biometric data combined with capacitive detection of the fingerprint pattern.

2.4 Ultrasound sensor cMUT

Most of the ultrasound sensors nowadays are represented by piezoelectric transducers. They have high working frequency and high output pressure providing good image quality. However, they suffer from the acoustic impedance mismatch between the transducer and soft tissues which gives weaker output signal due to reflections. Also fabrication of piezoelectric transducers can be problematic upon downscaling because the damping material has to fill the space between them and its conformal deposition is hardly achievable.

An attractive alternative to piezoelectric transducers has been developed over the last years and is called capacitive micromachined ultrasonic transducer (cMUT) [12]. cMUT produces ultrasound waves through mechanical vibrations of a membrane separated with a gap from the substrate. The membrane is actuated electrostatically by electrodes embedded in its struc-

ture.

2.5 cMUT vs. capacitive fingerprint sensor

2.5.1 Functional similiarities

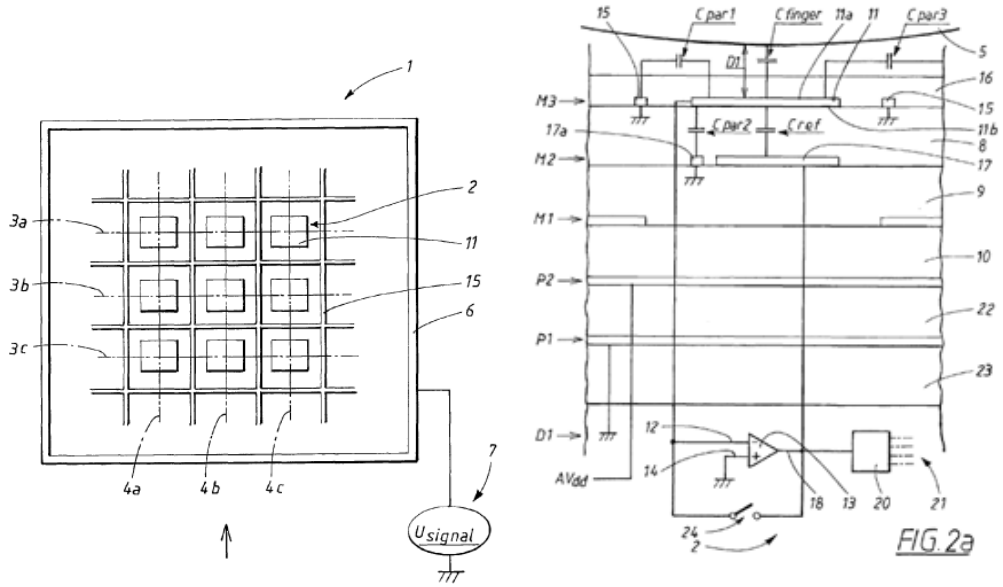
The structure of cMUT plays a crucial role in creating a multi-modal biometric sensor. The top cMUT electrode can perform capacitive measurements just as the capacitive fingerprint sensor does and at the same time it can also be used for ultrasound imaging of the structures inside the finger (veins or bones). This idea is new and has never been presented before.

2.5.2 Geometrical similarities

Dimensions of the cMUT and the capacitive fingerprint sensor elements are very similiar to each other. The capacitive FPC sensor consists of square electrode array (see Fig. 2.4a) having 50 μm pitch size (distance between the centers of two adjacent electrodes) [13] [14]. The cMUT size ranges from 10 to 100 μm providing different ultrasound frequency and can be fit to the pitch size of the capacitive sensor [15]. Also cMUT membranes can have different shapes (square, circular, hexagonal) but the shape of the top electrode does not dependend on it and can be set to square mimicking the capacitive sensor.

2.5.3 Material similarities

The capacitive fingerprint sensor is fabricated as a part of a CMOS substrate where top metal layer is patterned as an electrode array (see Fig. 2.4b) [13]. Therefore, in order to integrate cMUT with CMOS substrate one has to use the same materials for cMUT fabrication that looks feasible.



(a) (b)

Figure 2.4: Capacitive fingerprint sensor design: a) top view, b) side view (with permission from Fingerprint Cards AB)

2.6 cMUT fabrication overview

As was mentioned previously the future cMUT should be integrated with the fingerprint sensor which is fabricated as a part of a CMOS wafer. Because capacitive fingerprint sensing method requires very low parasitic capacitance of the system, short interconnects from the sensing electrodes to the driving and readout electronics is needed which can be achieved through CMOS integration. CMOS transistors act as pre-amplifiers and signal processing units while the top interconnect layer works as an electrode for fingerprint sensing.

There are several methods of cMUT fabrication and integration with CMOS technology.

The first one uses wafer bonding of separately fabricated cMUT chips with a CMOS substrate [15]. Through-silicon vias (TSV) and solder bumps are used to connect a cMUT wafer to CMOS contact pads. The main advantage of this method is no limitation for the processing temperature of a cMUT as

it is fabricated separately from the CMOS wafer. However, the complexity of this process increases the cost of the final device which is an issue for biometric devices.

During the second approach called monolithic post-processing a cMUT is fabricated directly on top of the CMOS wafer [16] [17]. Compared to the wafer bonding this method is cheaper but has thermal budget limitations (400-450°C) as Al interconnects of CMOS substrate can easily diffuse through insulation layers.

The last method is called monolithic co-processing and a cMUT is fabricated during the CMOS proces [18]. It is the cheapest way to fabricate a cMUT and the maturity of the optimized CMOS technology is used as a benefit. But the main disadvantage is unability to change materials or layer thicknesses which are a part of CMOS fabrication.

All pros and cons of the above mentioned methods are summarized in Table 2.1.

Fabrication method	Advantages	Disadvantages
Wafer bonding	no thermal budget limits	expensive and complex
Monolithic post-processing	cheaper than wafer bonding	thermal budget limits
Monolithic co-processing	the cheapest method, CMOS process maturity	geometry and material restrictions

Table 2.1: cMUT fabrication methods

The choice of the method was mostly dictated by the cost of the sensor. It is very important for biometric sensor to be as cheap as possible to compete with other companies sensor solutions. Moreover, preserving the structure of the capacitive fingerprint sensor will save the optimization expenses. Regarding all arguments we picked up the monolithic co-processing method to proceed forward.

2.7 Monolithic co-processing

As a CMOS substrate usually contains multiple layers above the Si wafer one has to choose this stack of layers to be used for cMUT fabrication.

One of the possibilites of making cMUT is using the bottom layers of CMOS process. For example, On Semiconductor 1.5 μm 2-polysilicon 2-metal n-well CMOS technology was used in [19]. The cMUT bottom electrode was made in a poly-Si gate layer while the sacrificial and top electrode were defined in first and second Al interconnect layers. The access to the sacrificial layer was done through vias and the top interconnect layer. Before etching of the sacrificial layer CMOS contact pads should be protected by photoresist or any other material. Due to large features the photolithography was not required and screen printing was used for photoresist deposition and patterning. Afterwards the sacrificial layer was etched away following by photoresist stripping and sealing of the holes by PECVD SiO_2 with shadow masking of the CMOS contact pads.

As one can see from the fabrication steps no additional photolithography was used which keeps the cost of the cMUT the same as the cost of a CMOS wafer. However, using bottom CMOS layers is not practical because the effective area of the wafer is shared by CMOS circuitry and a cMUT. In this way it is impossible to create a high density array of cMUT required for integration with the fingerprint sensor.

To overcome this problem a cMUT can be fabricated using not the bottom but rather top layers of the CMOS substrate. For instance, TSMC 0.35 μm 2-polysilicon 4-metal CMOS technology was used in [20]. Here both electrodes and the sacrificial layer were taken as Al interconnect layers. After the fabrication of the CMOS wafer etching holes were opened in the passivation layer and the sacrificial layer was etched away realizing a membrane. Sealing of holes was done by deposition of SiO_2 and afterwards CMOS contacts were opened.

In this work the latter approach of using CMOS top layers for cMUT fabrication will be followed with some modifications which will be discussed later.

Chapter 3

cMUT design and fabrication

3.1 Photolithography mask design

The photolithography technique was used for patterning layers of the cMUT. The layout for a set of five masks was created using Tanner EDA L-Edit software.

The masks (see Fig. 3.1) are square glass plates and have size 5" corresponding to the 4" wafer size as the most compatible with the fabrication tools that will be used in the MC2 cleanroom of the department of Microtechnology and Nanoscience where where the processing was done.

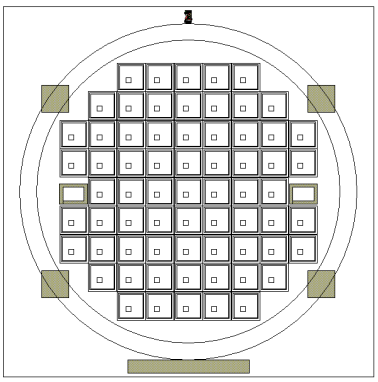


Figure 3.1: Mask design

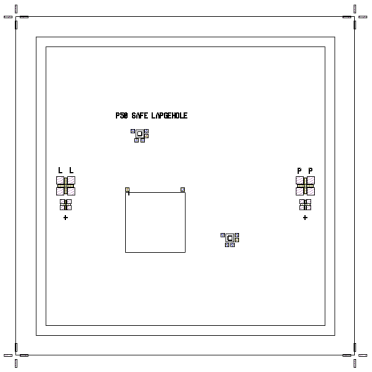


Figure 3.2: Chip design

The inner circle represents the 5 mm offset for wafer handling with tweezers. Five rectangles act as rough alignment marks for aligning mask to the

pattern on the wafer. Fine alignment marks are placed in two rectangular areas on the left and right sides of the wafer surrounded by a framebox (see Fig. 3.3). They allow alignment accuracy up to 1 μm using the lower aligning crosses. Below the alignment marks "Photolitho" pattern can be found for checking the exposure resolution (see Fig. 3.4). 8.5 mm square chips which contain cMUT elements can be seen on the wafer.

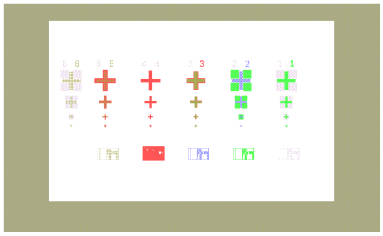


Figure 3.3: Fine alignmente marks in the framebox

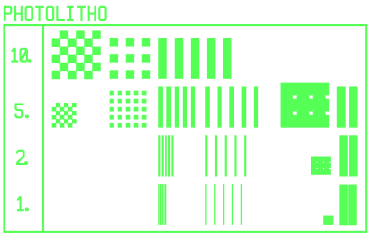


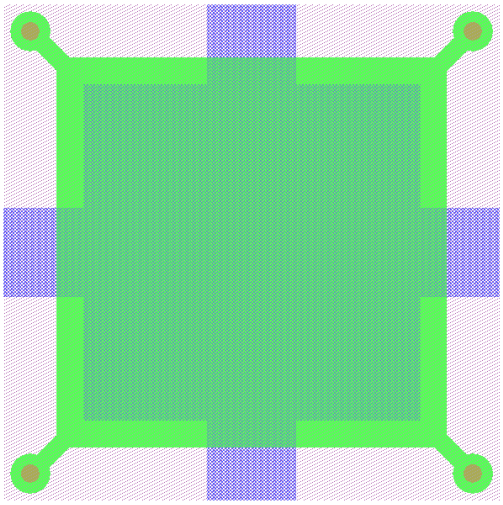
Figure 3.4: "Photolitho" pattern for the resolution check

The chip (see Fig. 3.2) includes the name for distinguishing different designs, two small regions with individually addressable cMUT elements, one big region with an array of cMUT elements addressable at the same time, alignment marks for a possibility to align mask with individual chips after wafer dicing and crosses in the chip corners working as dicing alignment marks.

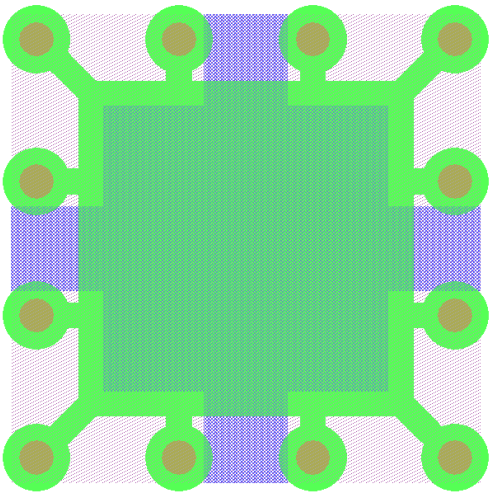
3.2 cMUT designs

Several designs of cMUT cells has been made to evaluate the most suitable one. Square and circular cMUT elements with small and large holes were analyzed (see Fig. 3.5). The general design with small holes represents examples from literature, however, safe designs with more etching ports and larger holes were also included.

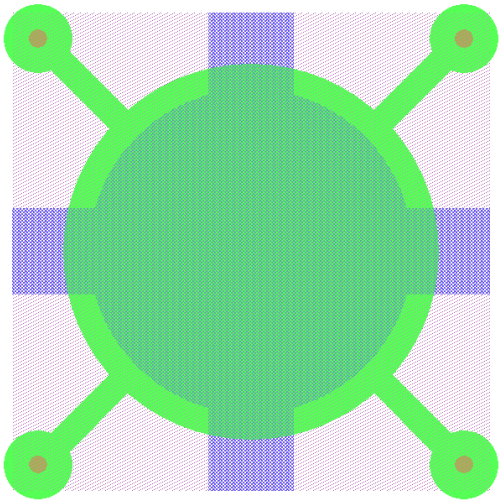
The bottom electrode (purple stripes) is covering the whole area below the membrane. Array of cMUT has one common bottom electrode with one contact pad. Individual cMUT also have a common bottom electrode which is grounded.



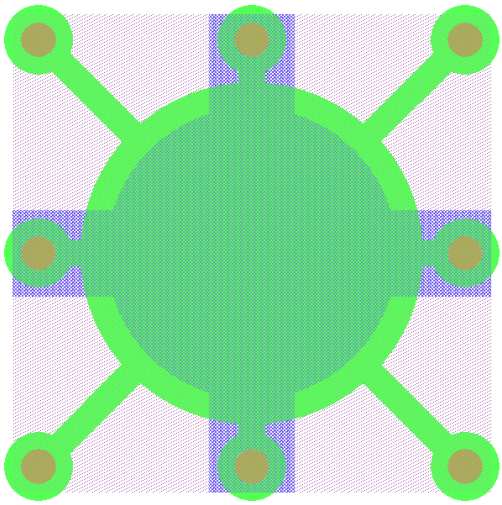
(a) Square cMUT with small holes (general design)



(b) Square cMUT with more and larger holes (safe design)



(c) Circular cMUT with small holes (general design)



(d) Circular cMUT with more and larger holes (safe design)

Figure 3.5: cMUT designs

Sacrificial layer (green) which forms a gap after etching actually defines a cMUT membrane area. It was set to 44 μm (diameter for circular membrane and edge for square membrane) for designs with small holes and 40 μm for safe designs with large holes. These dimensions were picked in order to fit the pixel pitch (distance between center points of two neighbour elements) 50 μm of the FPC fingerprint sensor. Platforms for holes have diameter 8 μm except for the square cMUT with small holes (4.5 μm). The width of etching channels is 3 μm except the square cMUT with small holes (2 μm).

The etching holes (red) are placed in the middle of sacrficial layer platforms. Small holes have diameter 2 μm while large holes have 4 μm.

The top electrode (blue) diameter is 38 μm and 34 μm for general and safe designs respectively. The interconnecting lines are 10 μm wide. It is worth noting that the top electrode is not limited to the circular shape and can be optimized according to the capacitive measurement needs.

All cMUT dimensions are summarized in Table 3.1.

	General design	Safe design
Membrane	44 μm	40 μm
Platform for etching holes	4.5 μm (square), 8 μm (circular)	8 μm
Etching channels width	2 μm (square), 3 μm (circular)	3 μm
Etching holes	2 μm	4 μm
Top electrode	38 μm	34 μm
Interconnects width	10 μm	10 μm

Table 3.1: cMUT dimensions

Finally, the last mask was designed to open contact pads (100 μm squares) for bottom and top electrodes.

3.3 Fabrication process plan

To illustrate all the fabrication steps a schematic process plan was created (see Fig. 3.6).

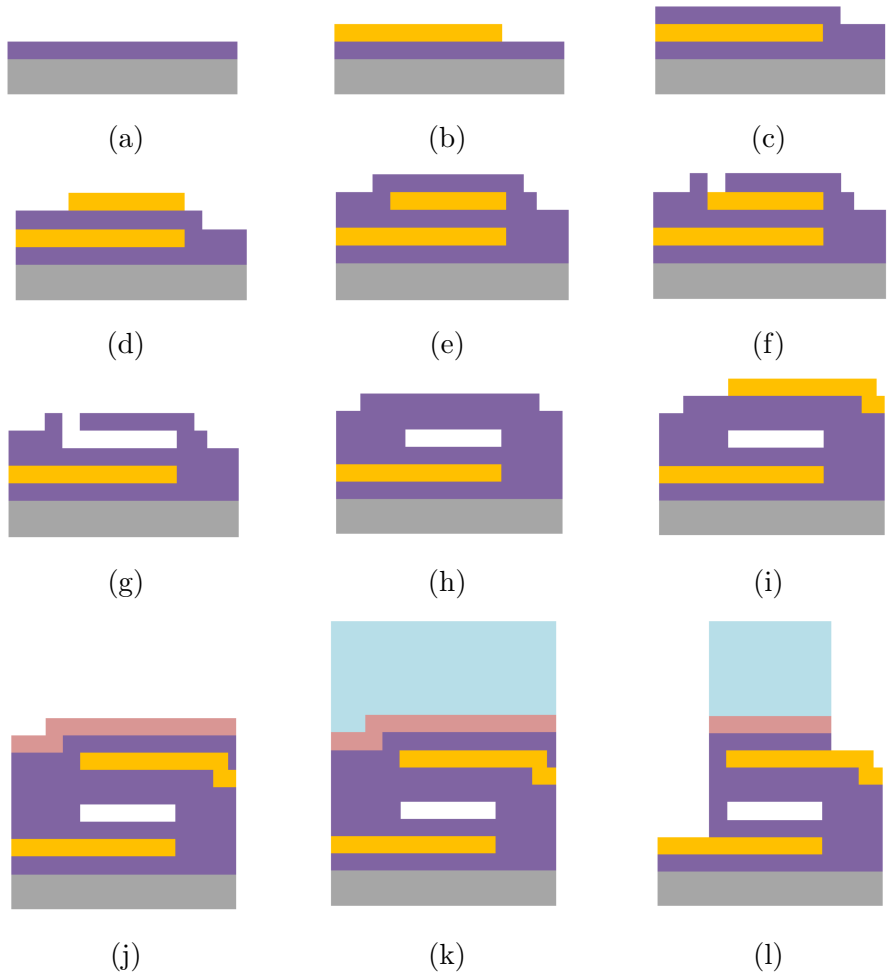


Figure 3.6: Schematic fabrication process plan of cMUT

As far as experiments require only the top layers and not the full CMOS wafer which is expensive, it was decided to choose virgin Si wafers as a starting substrate and make the cMUT from the same layers as in CMOS technology (TSMC 0.18 μm 1-poly 4-metal) used for fabrication of the FPC fingerprint capacitive sensor.

At first, one needs PECVD SiO_2 deposited on the Si wafer for insulation and improved adhesion of Al (Fig. 3.6a). During the next processing step Al is sputtered and patterned with photolithography to form bottom electrodes along with their contact pads (Fig. 3.6b).

Afterwards the insulation layer of PECVD SiO_2 should be deposited (Fig. 3.6c) to protect the bottom electrode during etching of the Al sacrificial layer which is sputtered later and patterned with photolithography (Fig. 3.6d).

To form a future membrane PECVD SiO_2 is deposited on top of sacrificial layer (Fig. 3.6e). Access to the sacrificial layer is made by etching holes in membrane which is done with photolithography and dry plasma etching (Fig. 3.6f).

So far all process steps were the same as in the CMOS process where Al layers are metal interconnects, PECVD SiO_2 - dielectric layers and etching holes - via holes for connecting metal layers.

The next fabrication step is not included in CMOS process but it is necessary for creating membranes. This step is etching of sacrificial layer which releases a membrane and creates a gap (Fig. 3.6g). During this step it is very important to keep all other via holes protected with photoresist so that the main interconnects are not etched away. This process step is CMOS-compatible and after membrane release photoresist can be stripped away.

Sealing of the membranes can be done through the next CMOS step which is deposition of W (tungsten) vias. In this work, this step was not included because of its complexity and the fact that holes are far from the membranes so their sealing will not influence the performance. Instead of W the holes were sealed by one more deposition of PECVD SiO_2 (Fig. 3.6h). Two depositions of SiO_2 were estimated to have the same total thickness of SiO_2 CMOS insulation layer.

Finally the last Al layer was sputtered and patterned with photolithography to form the top electrode and its contact pads (Fig. 3.6i). The passivation of the structure was done by PECVD of SiO_2 and Si_3N_4 (Fig. 3.6j). The Si_3N_4 layer is used in CMOS process to protect the structures from ambient contamination of Na^+ and K^+ ions that can easily diffuse inside and create local charging which affects reliability.

If one would like to use a cMUT for capacitive measurements of a fingerprint the electrostatic discharge (ESD) protection is needed. It increases the distance between the electrode and the skin thus decreasing the electric fields which reduces the possibility of discharge. This protective ESD coating can be fabricated by FPC for a final optimized structure (Fig. 3.6k). However, as a good approximation of the ESD coating one can also use SU8 photoresist which has very close mechanical and electrical properties.

The last step is opening the contacts to perform measurements of the structure (Fig. 3.6l). In the case of using a real CMOS wafer, this step is not needed because the electrodes will be connected to the CMOS transistors and can be contacted with through-silicon vias.

3.4 Processing issues

During the processing several problems can occur that has to be taken into account.

- Wafer bending: Because of the high compressive stress and high thickness of the PECVD SiO_2 (several μm) deposited on the wafer it experiences bending. It leads to bad contact between the wafer and the chuck of the lithography tool which gives vacuum leaks and can result in wafer stiction to the mask during contact mode exposure. It can be solved by depositing the same amount of SiO_2 on the backside of the wafer to compensate the stress.

- Hillocking of Al: Upon heating Al experiences compressive stress due to high difference between thermal expansion coefficient of Al ($23.1 \cdot 10^{-6}$ °C^{-1}) compared to Si ($2.6 \cdot 10^{-6}$ °C^{-1}) or SiO_2 ($0.55 \cdot 10^{-6}$ °C^{-1}).

This effect is more pronounced at grain boundaries where the diffusion of Al is much faster. This problem can be solved by adding some Cu in Al which results in precipitation of Cu at grain boundaries decreasing the Al diffusion and preventing hillock formation.

- Double exposure: During photoloithography on Al layer the UV light that passes photoresist is reflected back from the mirroring Al surface which results in double exposure of the photoresist. By reducing twice the time of exposure one can solve this problem.

- CF_4 residues: Opening the holes in the SiO_2 membrane for etching the sacrifcial layer is done by Reactive Ion Etching in CF_4 plasma. If the power is too high then the CF_4 resiues will be deposited on the surface. It will passivate the surface and make it impossible for the furher etching. It can be solved by adding 10% of O_2 to CF_4 gas. O_2 will react with CF_4 releasing F^+ ions and decrease the number of CF_4 residues.

- Membrane stiction: During membrane release capillary forces act on the membrane and while drying it can collapse leading to the stiction. This problem can be solved by making a membrane thicker so it can withstand the capillary forces or increase the gap so the water is dried faster and the membrane has more space to bend before actual contact with substrate. Also critcal point and freeze drying are widely used as a solution.

- SU8 delamination: In case of using SU8 photoresist to mimick the ESD protection layer one has to consider stress issues which occur during SU8 cooling after baking. Shrinking of the SU8 film leads to high tensile stress which creates cracks and delamination. This problem can be solved by optimization of the baking temperatures and time.

3.5 Fabrication process

The starting substrate was a new 4" Si wafer taken from the storage box. In this case the cleaning procedure was not required.

The first insulation layer of 1.38 μm SiO_2 was deposited using STS PECVD tool. The process was done in low frequency plasma (350 kHz) and the film had compressive stress of $2.49 \cdot 10^9$ dyn/cm^2. To compensate the wafer bending the SiO_2 layer of the same thickness was deposited on the backside of the wafer.

After that 0.53 μm of Al (bottom electrode) was sputtered with FHR MS150 tool. This thickness exactly matches the one used during the CMOS process for the FPC fingerprint sensor As was mentioned pure Al results in hillocking upon heating and is not used in CMOS technology anymore. Instead the alloy of Al with 1-2% Cu is the material for CMOS interconnects which minimizes these negative effects. However, in this work the reliability issues are not critical and pure Al was taken as a metal layer.

The bottom electrode is defined by patterning the Al layer with photolithography. A photoresist primer HMDS for improved adhesion and positive photoresist S1813 (1.2 μm) were spun on top of the wafer with Spinner SST20. To evaporate the solvent and harden the photoresist soft baking of the wafer was done on the hot plate for 2 minutes at 110°C . Afterwards the wafer was loaded to the Mask Aligner MA6 and exposed to UV light through the mask for bottom electrode. The recommended exposure time for S1813 is usually 10 seconds but regarding the issue of double exposure the time was reduced to 5 seconds and gave good results. Development of the exposed resist was performed in the standard developer MF-319 and then "Photolitho" pattern was checked in the optical microscope to determine the obtained resolution. If the resolution is sufficient enough then the photoresist goes through hard baking to stabilize and harden its structure.

After the photoresist is patterned and hard baked, the wafer is put into the Al etchant which is composed from phosphoric acid H_3PO_4 (dissolves Al_2O_3), nitric acid HNO_3 (oxidizes Al), acetic acid CH_3COOH (for wetting and buffering) diluted in H_2O. The etching time 3 min was calculated ac-

cording to the etching rate 200 nm/min adding some extra time (up to 30 seconds) to make sure that Al is etched away on the whole wafer. Further inspection in the microscope is required to verify that Al was etched away. After etching the photoresist should be stripped in hot resist remover Shipley 1165 for 10 minutes at 65°C.

It is very important that no resist residues are left on the wafer before PECVD deposition. Therefore the wafer is placed in O_2 plasma for 2 minutes to remove any possible resist residues. Afterwards another insulation layer (front side) and stress compensation layer (back side) of 1.38 μm PECVD SiO_2 were deposited using the same parameters as the first time.

It was followed by sputtering 0.53 μm of Al (sacrificial layer) and patterning it with photolithography using the same recipe as described above.

The membrane layer of 0.69 μm PECVD SiO_2 was deposited on top of patterned sacrificial layer and etching holes were defined with photolithography. It was noticed that 2 μm holes for general design are very hard to define especially with a thick photoresist although photolithography for 4 μm was successfull. Also alignment should be done very accurately with 2 μm precision or better to match the platforms of sacrifcial layer.

Making holes in SiO_2 membrane with wet etching (in HF acid solution) is not recommended because of the underetch and very fast etching rate which is hard to control. Taking this into account dry etching (in CF_4 plasma) was considered to be a better option. To reduce the problem of CF_4 residues the recipe with additional 10% O_2 gas was chosen. However, during dry plasma etching the photoresist which protects the remaining parts of the wafer is also etched away by CF_4 as well as O_2. The etch rate for the photoresist can be several times higher than for SiO_2. To be sure that no SiO_2 except holes will be etched away a thick photoresist is required. For this purpose positive photoresist AZ 4562 (7 μm) was chosen. Because of higher thickness the processing parameters are different: soft bake was performed for 3 minutes at 100°C, exposure time was increased up to 20 seconds and hard bake was done for 60 minutes at 120°C.

Before etching the holes in SiO_2 membrane the etch rate of SiO_2 in CF_4 + 10% O_2 plasma was estimated. Test 2" Si wafer covered with PECVD

SiO_2 was put in RIE tool for 15 seconds. The thickness of PECVD SiO_2 was measured before and after dry plasma etching with Woollam ellipsometer and the etch rate of PECVD SiO_2 was calculated to be 160 nm/min.

Regarding the estimated etch rate the time needed to etch 0.69 μm of SiO_2 is equal to 4 minutes 30 seconds. Adding some extra time to make sure that all holes will be opened and considering the fact that etching in small holes takes more time than on the unpatterned wafer the etching time was set to 8 minutes. Then the wafer was put into Al etchant for 20 minutes to check if the holes were opened successfully and Al is etched away. After confirming it the wafer was put in the Al etchant again over the night because the Al etch rate is very slow 200 nm/min comparing to the lateral dimensions of the membrane - 20-30 μm from the etching holes till the center of the membrane.

The problem of stiction can occur during the drying of the membranes. It happened during experiments with thinner test membranes (0.4 μm) (see Fig. 3.7) but was not observed with cMUT membranes (0.69 μm). It was also noticed that circular test membranes are more resistant to stiction than square ones due to better spreading of stress. The necessary procedure after Al etching and rinsing in water is rinsing the wafer in isopropanol (IPA) which dries very fast. Also placing the wafer in oven (90°C) for 1 minute increases the drying speed which reduces the risk of membrane collapsing.

It was noticed that the underlying layers of Al covered by SiO_2 were also etched partially and it can be explained by bad quality of the PECVD SiO_2 containing micropores (see Fig. 3.8).

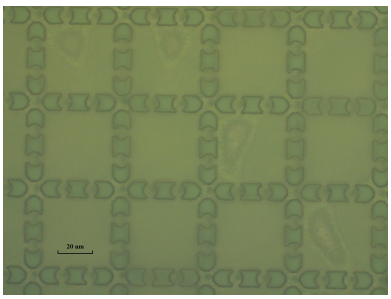


Figure 3.7: Collapsed membranes recognized by optical rings

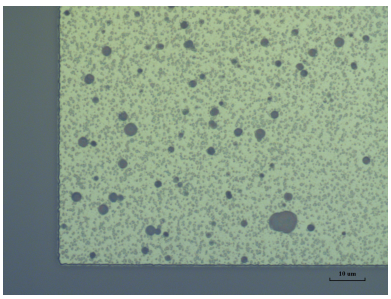


Figure 3.8: Etched Al layer due to micropores in PECVD SiO_2

The holes were sealed during the next deposition of 0.69 μm PECVD SiO_2 resulting in total thickness 1.38 μm of insulation layer. The stress compensation layer was not deposited anymore because the vacuum quality of the wafer chuck was not very important as the following lithography steps were done in soft contact mode (to minimize the risk of membrane collapsing).

0.53 μm Al layer for the top electrode was sputtered and patterned with photolithography (the same recipe as for the bottome electrode and sacrificial layer).

Passivation of the whole structure was done by deposition of 1.15 μm PECVD SiO_2 and 0.6 μm PECVD Si_3N_4.

The lamination should have been performed with FPC protective coating but because of its temporary unavailability SU8 was picked as an alternative coating. SU8 is a negative epoxy-based photoresist which stays on the wafer after processing and has similiar electrical and mechanical properties to the FPC coating. SU8 was deposited on the wafer using syringe (instead of pipette) due to its high viscosity and then spin-coated to the average thickness 32 μm which was measured with profilometer. The standard recipe from Microchem was taken for the lithography of the SU8. 2 minutes prebake with lower temperature (65°C) was followed by 6 minutes soft bake at higher temperature (95°C). The exposure time (30 seconds) was optimized to achieve the required exposure energy dose (150-160 mJ/cm^2) for the current resist thickness. It was followed by post-exposure bake (PEB) for 2 minutes at 65°C and for 5 minutes at 95°C. The PEB is needed to fully cross-link the exposed parts of the photoresists as UV exposure only initiates this process which is extremely slow at room temperature. The development for 10 minutes with continuous agitation was performed afterwards.

SU8 is shrinking during the cooling after post-exposure bake and high tensile stress occurs at the corners which leads to cracks and delamination (see Fig. 3.9). To reduce this problem PEB process should be optimized to minimize the stress. This optimization was not fully realized and contacts were not opened for further measurements due to the lack of time.

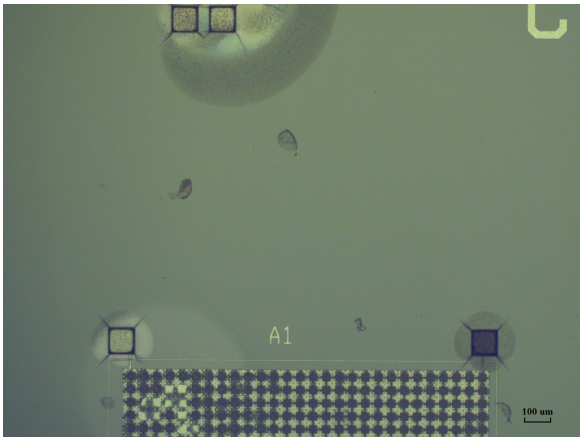


Figure 3.9: Cracks and delamination of SU8 after development

3.6 Membrane characterization

Several chips were cut in the middle of the membrane array and inspected with scanning electrone microscope (SEM). One can clearly see the multi-layer cMUT structure raising above the surface (see Fig. 3.10). Most of the membranes were ripped off along the sawing line which can be seen on the figure. However, some of them survived and the gap is clearly seen from another angle (see Fig. 3.11).

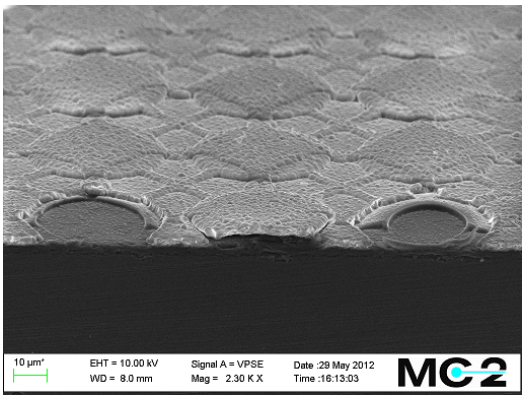


Figure 3.10: SEM picture of the cMUT array

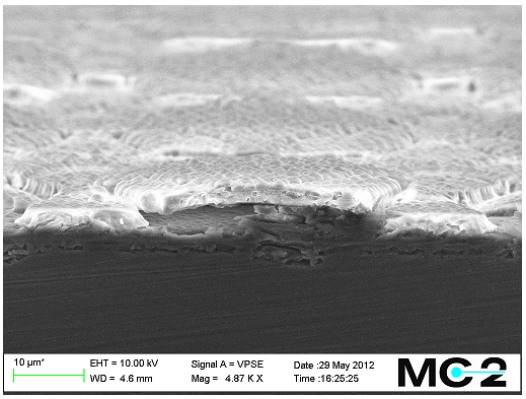


Figure 3.11: SEM picture of the cMUT membrane

Chapter 4

cMUT modeling

If one would like to use cMUT for vein or bone imaging, several parameters of the device should be calculated. They include resonance frequency and quality factor which were simulated using Finite Element Method (FEM) modeling software Comsol Multiphysics [21].

4.1 Vein imaging

Vein imaging with ultrasound is usually done by Doppler method [22]. It is based on the ultrasound frequency shift due to blood motion. An ultrasound wave is sent at a certain angle towards the blood stream and the reflected signal is recorded from which one can extract the Doppler frequency shift

$$f_d = f_i - f_r = \frac{2f_i \ v \ \cos(\theta)}{c} \tag{4.1}$$

where f_i is an ultrasound frequency of the incident wave, f_r - ultrasound frequency of the reflected wave, v - blood stream velocity, θ - angle between an incident wave and blood stream direction, c - speed of ultrasound.

From the Doppler frequency shift the blood stream velocity and its direction can be calculated and finger veins can be imaged.

As was mentioned the Doppler method requires a particular angle of the ultrasound towards the blood stream in vein. In our design the cMUT is placed directly below the finger and the incident wave is perpendicular to its

surface which means $\theta = 90°$ and $f_d = 0$ for all blood stream velocities. To overcome this problem phase delay beam steering has to be used [22].

During the beam steering transducers in the array are excited not simultaneously but with a delay which creates an ultrasound beam in a different direction depending on a delay profile. Therefore, an incident wave can be sent at a particular angle towards blood stream.

The second cMUT will be needed to detect the reflected wave from the vein and its field of view should overlap with the cMUT that sends the signal [11].

Moreover, cMUT should have high working frequency f_i to get sufficient Doppler shift f_d (see Eq. 4.1). Also the ultrasound pulse (high frequency signal, typically MHz) should be long enough to be able to extract the Doppler shift (low frequency signal, typically kHz). For a long pulse one needs a cMUT with low damping and therefore high quality factor Q.

4.2 Bone imaging

Bones can be visualized through pulse-echo method [22]. The ultrasound pulse is sent inside the finger and then the reflected signal from the bone (echo) is recorded. The echo from the bone can be recognized by its large amplitude compared to echoes from other tissues.

For the pulse-echo ultrasound method two parameters are important: lateral and axial resolution. The targeted lateral and axial resolutions in this work will be 0.35 mm and 0.1 mm respectively. These values were shown to be sufficient for ultrasound transducers to recognize different objects inside the hand (bones, muscle tissues and veins) [23]. Distances between these objects and their depth were used to identify people.

4.2.1 Lateral resolution

Lateral resolution is the first cMUT feature of interest. It is defined as the minimal distance between two objects on the axis perpendicular to the wave propagation that can be resolved. It depends on the beam width and is the

best at the focal point of the ultrasound beam. For a focused transducer lateral resolution can be estimated as [24]

$$Lateral = \lambda \cdot f_{number}(\text{focused transducer}) \tag{4.2}$$

where f_{number} is a ratio of the focal distance to the transducer diameter d. For an unfocused transducer f_{number} is fixed and is equal to $d/4\lambda$ which results in

$$Lateral = d/4(\text{unfocused transducer}) \tag{4.3}$$

In this work the cMUT is unfocused and the transducer diameter is 44 μm (general design) and 40 μm (safe design) resulting in a lateral resolution of 11 μm and 10 μm respectively.

4.2.2 Axial resolution

Axial resolution is the minimal distance between two objects on the axis of wave propagation that can be resolved. It can be calculated as [22]

$$Axial = 1/2 \cdot SPL \tag{4.4}$$

where SPL is Spatial Pulse Length defined as

$$SPL = \lambda \cdot (\text{number of cycles}) \tag{4.5}$$

It means that if two objects are separated by the distance less than 1/2 SPL, the signal reflected back from the second object will overlap with the signal reflected from the first one. Therefore, it wont be possible to distinguish these objects.

One can clearly see that good axial resolution comes with short SPL and hence short wavelength of ultrasound λ which requires high working frequency of a cMUT. Also the number of pulses should be taken into account which depends on the damping of a cMUT. The details about damping will be described in the section about quality factor Q.

4.3 Resonance frequency

In order to achieve the axial resolution of 0.1 mm the resonance frequency of the cMUT should be not lower than 12 MHz - it is going to be the target value.

Resonance frequency depends on both geometry and material properties of the cMUT. For a clamped circular membrane it can be given as [25]

$$\omega_0 = \frac{2.95\ t}{a^2}\sqrt{\frac{E}{\rho\ (1-\nu^2)}} \tag{4.6}$$

where t is the membrane thickness, a - its radius, E - the Youngs modulus of the membrane material, ρ - its density and ν - its Poissons ratio. This equation is valid only for a cMUT made from one material and it is not applicable to our cMUT structure which is multi-layer. Nevertheless, it gives a good picture on how and which parameters influence the resonance frequency.

To get the resonance frequencies of multi-layer cMUT membrane numerical simulations are required. Comsol Multiphysics was used for this purpose as one of the best Finite Element Method (FEM) modeling software which can couple different physics phenomena (for instance, mechanics and electrostatics in our case).

Both circular and square cMUTs were modeled to get the first eigenfrequency mode using Electromechanics interface (MEMS module). It includes Structural Mechanics, Electrostatics and Moving Mesh interfaces pre-coupled together. All domains by default are assigned to Electrostatics interface and it was kept untouched. DC voltage was set to zero and membrane was actuated only by AC voltage.

Structural Mechanics interface represented by Linear Elastic Model node was assigned to the membrane domains. Axial Symmetry node was set by default for a circular membrane (2D axisymmetric model), however, Symmetry node needed to be included for a square membrane (3D model). Outer edge boundaries of a membrane were modified with Fixed Constraint node.

Bottom electrode and its insulation domains were assigned with Fixed

Mesh node and boundaries of air domain with Prescribed Mesh Displacement. It is worth noting that Prescribed Mesh Displacement should be set to zero only in the normal direction to the boundary axis.

First, Eigenfrequency study was performed with circular membrane and multi-layer structure shown in the Fig. 4.1 and material properties stated in the Table 4.1. This cMUT membranes were described in the paper [17] and its resonance frequency was also estimated through modeling. The paper value stated 21.6 MHz while new simulations with Comsol showed 23.5 MHz which deviates by 10%. The reason might be in different values used for Cr and Al as well as slightly different boundary conditions which are not specified in the original paper.

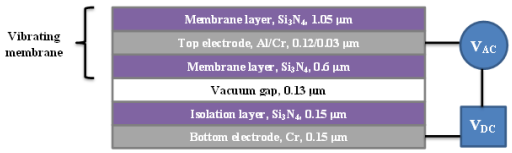


Figure 4.1: Test cMUT verification model

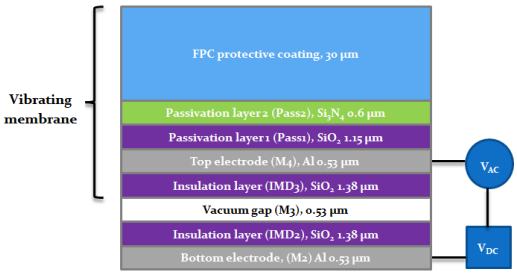


Figure 4.2: cMUT-in-CMOS model

	Cr	PECVD Si_3N_4	Al
Density, kg/m3	7150	2040	2700
Young's modulus, GPa	279	110	70
Poisson's ratio	0.21	0,253	0,35
Relative permittivity	1	6.3	1

Table 4.1: Material properties for test cMUT

	Al	PECVD SiO_2	PECVD Si_3N_4
Density, kg/m3	2700	2300	2500
Young's modulus, GPa	70	85	160
Poisson's ratio	0.33	0,25	0,253
Relative permittivity	1	5	7

Table 4.2: Material properties for cMUT-in-CMOS model

After the verification was performed the same Eigenfrequency study was done for square and circular membranes of new design (see Fig. 4.2). The safe design cMUT were not included in simulations as their size 40 μm is very close to the general design 44 μm. Material properties of different layers were collected in Table 4.2 and this data was taken both from the Comsol material library and MIT material database [26]. The material properties of FPC coating were not mentioned due to their confidential status.

The first eigenmodes are clearly recognized (see Fig. 4.3 and Fig. 4.4) and the simulated data is collected in Table 4.3.

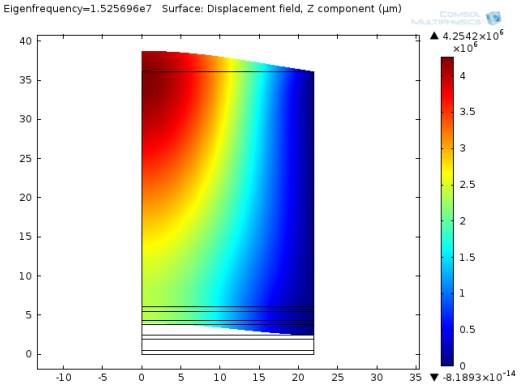


Figure 4.3: Circular cMUT with protective FPC coating, $f_0 = 15.2$ MHz

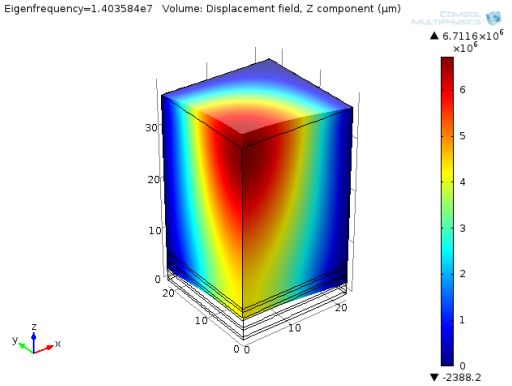


Figure 4.4: Square cMUT with protective FPC coating, $f_0 = 14$ MHz

	Circular cMUT	Square cMUT
With FPC coating	15.3 MHz	14 MHz
Without FPC coating	22.7 MHz	20 MHz

Table 4.3: cMUT resonance frequencies

The reason why the resonance frequency with FPC coating is smaller than without it is because of very small Young's modulus of this coating compared to its density. It results in added mass without additional spring constant which decreases the resonance frequency.

Nevertheless, all results show very good values of resonance frequency which are all above the targeted value of 12 MHz.

As the cMUT is fabricated in the CMOS process, layer materials and thicknesses are fixed which puts limitations on the design. However, lateral dimensions can be changed, for example, the diameter of a membrane - by decreasing it twice the resonance frequency increases 4 times according to the equation (4.6). For example, one can imagine design where two membranes are placed under one electrode which will keep lateral resolution the same but increase axial resolution 4 times.

4.4 Quality factor

The quality factor Q is a number which shows the damping rate of the system. It can be defined as

$$Q = 2\pi \frac{E_{\text{stored}}}{W_{\text{cycle}}} \tag{4.7}$$

where E_{stored} is the total energy of the system and W_{cycle} is the loss during one cycle due to damping. This definition is very inconvenient to work with as it is hard to calculate values of E_{stored} and W_{cycle}. Instead, the other definition of the quality factor Q is often used which is based on the frequency response of the resonator. It can be written as

$$Q = \frac{f_0}{\Delta f} \tag{4.8}$$

where f_0 is the resonant frequency and Δf is the bandwidth of this resonance peak at the amplitude which is -3 dB lower $(1/\sqrt{2})$ than the resonance amplitude.

The high Q means low damping and the structure will keep resonating for quite a while even in the absence of an excitation force. On the contrary, low Q results in strong damping and vibration amplitude dies very fast. Obviously, for a short SPL and hence better axial resolution one would like to have strongly damped system with a low quality factor Q.

Before creating a model one has to find out the main damping mechanisms in cMUT vibrations. They include air damping, damping through supports,

thermo elastic damping (TED) etc.

Air losses occur due to acoustic waves emitted by a cMUT which carry away the energy. This damping mechanism is the most significant among others. For a circular membrane it can be estimated as [27]

$$Q_{\text{air}} \approx \frac{(2\pi f_0 t\rho)}{Z_{\text{air}}} \tag{4.9}$$

where t is the thickness of a membrane, ρ is its density and Z_{air} is the acoustic impedance of air which is proportional to air pressure P. This rough estimation gives a value of 17.7/MHz and depends on the resonance frequency. To get precise results numerical analysis is required.

As a verification a cMUT membrane consisting of crystalline silicon from the reference [27] was studied and compared for Q_{air}. The diameter of the membrane was set to be 40 μm and thickness 0.5 μm. Material properties for Si were taken from Comsol material database and are as following: Young's modulus 170 GPa, Poisson's ratio 0.28, density 2329 kg/m^3.

Membrane was assigned with Solid Mechanics interface (2D axisymmetric model) and its edges were put to Fixed Constraint node. Edge Boundary Load of 1 N/m^2 was taken arbitrarily and was applied to the upper boundary in z-direction. The value of exciting Boundary Load isn't important for evaluating the Q-factor - it will only influence the magnitude of displacement.

Air domain of hemi-sphere was built on top of the membrane and assigned with Pressure Acoustics (Frequency Domain) interface. It is important that part of this hemi-sphere was chosen as Perfectly Matched Layer (PML) (see Fig. 4.5) which model environment and eliminate all acoustic wave reflections by their attenuation. Only with PML it is possible to calculate Q-factor, otherwise the resonance peak will aim at constantly increasing displacement which is the case for undamped system.

The coupling between Solid Mechanics and Pressure Acoustics interface was made at the upper edge of the membrane. In Solid Mechanics it was realized by adding a Boundary Load with "Load defined as force per unit area" in Load type and "Acoustic Load per unit area (acpr/pam1)" in Load. In Pressure Acoustics the Normal acceleration node for this boundary was

selected, “Acceleration” in Type, “Acceleration (solid/lemm1)” in Acceleration.

The Frequency Domain study was performed around estimated resonance frequency of 5.2 MHz. Results of the frequency analysis can be seen on Fig. 4.6.

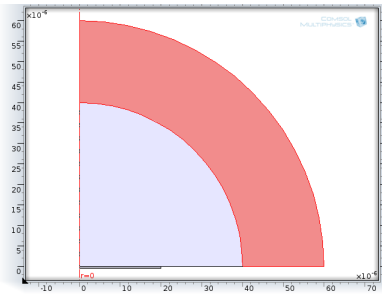


Figure 4.5: Geometry of test structure and Perfectly Matched Layer (PML)

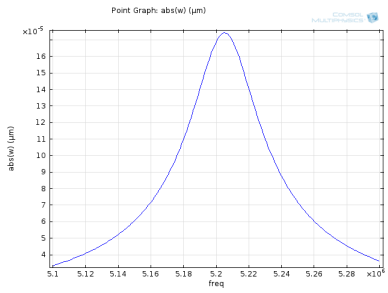


Figure 4.6: Frequency analysis of test structure, $Q_{air} = 180$

The calculated Q_{air} is 180 and is equal to the one from the referenced paper [27]. The analytical Q_{air} is 90 (also in agreement with reference) and is twice smaller than the numerical one, however, one has to remember that it is an approximate value and can be used only for rough estimation.

After successful verification test, the same model was applied to our cMUT structure. Test membrane was replaced by cMUT stack and Electromechanics interface was used instead of Solid Mechanics. Results can be seen in Table 4.4

	Circular cMUT	Square cMUT
With FPC coating	6955	6438
Without FPC coating	2951	2505

Table 4.4: cMUT Q-factor due to air losses

One can notice that Q_{air} for cMUT membranes without FPC coating is lower due to smaller total thickness of the membrane which can be deduced from the equation (4.9).

The results from quality factor show that the modeled cMUT cannot be used for bone imaging with pulse-echo ultrasound method due to low

damping and long spatial pulse length which gives bad axial resolution. On the other hand, it is possible to perform vein imaging with Doppler method for which low damping is preferrable.

Also bone imaging could be done with Doppler method if the finger is swiped across the sensor which is exactly the case for swipe fingerprint sensor.

Chapter 5

Conclusion and future work

It was shown that multi-modal biometric approach can be a possible solution for increased accuracy of the fingerprint capacitive sensor. Ultrasonic method and cMUT as an ultrasonic device can be integrated in the fingerprint sensor preserving the ability of capacitive fingerprint sensing and adding ultrasound vein/bone imaging. This integration method is included in CMOS process and will add almost no additional cost for the final device.

The fabrication experiments showed that making cMUT is relatively easy process with specified dimensions of CMOS substrate and available materials although basic processing issues has to be taken into account.

cMUT modeling results proved that it can be used for vein imaging and bone imaging can be performed for swipe sensor.

The future work should also cover the cMUT model with finger load on top of a cMUT which will result in more realistic values for resonance frequency and quality factor. Also fabrication of cMUT using CMOS substrate should be realized and both capacitive and ultrasound biometric measurements should be performed.

Appendix A

cMUT processplan

Process Plan for CMUT

Materials: 4" Si wafer

1. **<u>RCA clean</u> (Equipment: Wetbench, tool no. 651, Ulf Sodervall) (optional)**
    - Standard clean 1 (SC1)
    - Standard clean 2 (SC2)
2. **<u>Insulation layer</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of SiO_2: recipe LfSiO (low frequency 350 kHz), 31 min 30 sec, target thickness = 1380 nm, deposition rate = 0.73 nm/sec
3. **<u>Stress compensation layer</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of SiO_2: backside of the wafer, recipe LfSiO, 31 min 30 sec, target thickness = 1380 nm, deposition rate = 0.73 nm/sec
4. **<u>Bottom electrode</u> (Equipment: Sputter - FHR MS150, tool no. 400, Henrik Frederiksen)**
    - Sputtering of Al: 265 sec, target thickness = 530 nm, deposition rate = 2 nm/sec
5. **<u>Lithography</u> (Equipment: SST20 Resist Spinner and MA 6 Mask Aligner, tools no. 214 and 205, Johan Andersson)**
    - Primer: HMDS, 30 sec, 3000 RPM
    - Photoresist: S1813, 30 sec, 3000 RPM, 1.2 μm
    - Soft bake: hot plate, 2 min, 110 °C
    - Exposure: Mask #1 (Bottom electrode), 5 sec (due to double exposure!), Hard contact
    - Develop: MF-319, 1 min 30 sec (till "bleeding" stops)
    - Developer removing: QDR (quick dump rinse), N_2 gun
    - Look at the "PhotoLitho" pattern in the microscope to check the development
    - Hard bake: oven, 30 min, 120 °C
6. **<u>Bottom electrode patterning</u> (Equipment: Wetbench, Ulf Sodervall)**
    - Al wet etch: SUNCHEM Al Etchant, 3 min (till Al is etched), 40°C, etch rate 200 nm/min
    - Etchant removing: QDR, N_2 gun
    - Check etching in the microscope
    - Resist removing: Shipley 1165 bath, 10 min, 65°C
    - Cleaning removal residues: acetone bath, 30 sec
    - Cleaning acetone: QDR, N_2 gun
7. **<u>Resist residues removing</u> (Equipment: Plasma etch - Plasma Therm BatchTop RIE m/91, tool no. 418, Göran Alestig)**
    - RIE (Reactive Ion Etching) of resist: gas O_2, 2 min, 100 W (recipe "str02m_a"), etch rate = 700 nm/min
8. **<u>Insulation layer</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of SiO_2: recipe LfSiO, 31 min 30 sec, target thickness = 1380 nm, deposition rate = 0.73 nm/sec
9. **<u>Stress compensation layer</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of SiO_2: backside of the wafer, recipe LfSiO, 31 min 30 sec, target thickness = 1380 nm, deposition rate = 0.73 nm/sec
10. **<u>Sacrificial layer</u> (Equipment: Sputter - FHR MS150, tool no. 400, Henrik Frederiksen)**
    - Sputtering of Al: 265 sec, target thickness = 530 nm, deposition rate = 2 nm/sec
11. **<u>Lithography</u> (Equipment: SST20 Resist Spinner and MA 6 Mask Aligner, tools no. 214 and 205, Johan Andersson)**

- Primer: HMDS, 30 sec, 3000 RPM
- Photoresist: S1813, 30 sec, 3000 RPM, resist thickness = 1.2 µm
- Soft bake: hot plate, 2 min, 110 °C
- Exposure: Mask #2 (Sacrificial layer), 5 sec (due to double exposure!), Hard contact
- Develop: MF-319, 1 min 30 sec (till "bleeding" stops)
- Developer removing: QDR, N_2 gun
- Look at the "PhotoLitho" pattern in the microscope to check the development
- Hard bake: oven, 30 min, 120 °C

12. **<u>Sacrificial layer patterning</u> (Equipment: Wetbench, Ulf Sodervall)**
    - Al wet etch: SUNCHEM Al Etchant, 3 min (till Al is etched), 40°C, etch rate = 200 nm/min
    - Etchant removing: QDR, N_2 gun
    - Check etching in the microscope
    - Resist removing: Shipley 1165 bath, 10 min, 65°C
    - Cleaning removal residues: acetone bath, 30 sec
    - Cleaning acetone: QDR, N_2 gun
13. **<u>Resist residues removing</u> (Equipment: Plasma etch - Plasma Therm BatchTop RIE m/91, tool no. 418, Göran Alestig)**
    - RIE of resist: gas O_2, 2 min, 100 W (recipe "str02m_a"), etch rate = 700 nm/min
14. **<u>Membrane layer</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of SiO_2: recipe LfSiO, 15 min 45 sec, target thickness = 690 nm, deposition rate = 0.73 nm/sec
15. **<u>Lithography</u> (Equipment: SST20 Resist Spinner and MA 6 Mask Aligner, tools no. 214 and 205, Johan Andersson)**
    - Primer: HMDS, 30 sec, 3000 RPM
    - Photoresist: AZ 4562, 30 sec, 3000 RPM, resist thickness = 7 µm
    - Soft bake: hot plate, 3 min, 100 °C
    - Exposure: Mask #4 (Etching holes), 20 sec (due to double exposure!), Hard contact
    - Develop: MF-322, 3 min (till "bleeding" stops)
    - Developer removing: QDR, N_2 gun
    - Look at the "PhotoLitho" pattern in the microscope to check the development
    - Hard bake: oven, 60 min, 120 °C
16. **<u>Holes etching</u> (Equipment: Plasma etch - Plasma Therm BatchTop RIE m/91, tool no. 418, Goran Alestig)**
    - RIE (Reactive Ion Etching) of SiO_2: gas CF_4 + 10% O_2, 8 min, 250 W (recipe cf4x250W), etch rate = 160 nm/min
17. **<u>Sacrificial layer etching</u> (Equipment: Wetbench, Ulf Sodervall)**
    - Al wet etch: SUNCHEM Al Etchant, 20 min, 40°C, etch rate = 200 nm/min
    - Etchant removing: QDR, N_2 gun
    - Check etching in the microscope
    - Al wet etch: SUNCHEM Al Etchant, 10 hours, 40°C, etch rate = 200 nm/min
    - Anti-stiction rinsing: QDR, 1 min in isopropanol (IPA) beaker, N_2 gun
    - Drying: oven, 90°C, 1 min
18. **<u>Holes sealing</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of SiO_2: recipe LfSiO, 15 min 45 sec, target thickness = 690 nm, deposition rate = 0.73 nm/sec
19. **<u>Top electrode</u> (Equipment: Sputter - FHR MS150, tool no. 400, Henrik Frederiksen)**

- Sputtering of Al: 265 sec, target thickness = 530 nm, deposition rate = 2 nm/sec

20. **<u>Lithography</u> (Equipment: SST20 Resist Spinner and MA 6 Mask Aligner, tools no. 214 and 205, Johan Andersson)**
    - Primer: HMDS, 30 sec, 3000 RPM
    - Photoresist: S1813, 30 sec, 3000 RPM, resist thickness = 1.2 µm
    - Soft bake: hot plate, 2 min, 110 °C
    - Exposure: Mask #3 (Top electrode), 5 sec (due to double exposure!), Soft contact
    - Develop: MF-319, 1 min 30 sec (till "bleeding" stops)
    - Developer removing: QDR, N_2 gun
    - Look at the "PhotoLitho" pattern in the microscope to check the development
    - Hard bake: oven, 30 min, 120 °C
21. **<u>Top electrode patterning</u> (Equipment: Wetbench, Ulf Sodervall)**
    - Al wet etch: SUNCHEM Al Etchant, 3 min (till Al is etched), 40°C, etch rate = 200 nm/min
    - Etchant removing: QDR, N_2 gun
    - Check etching in the microscope
    - Resist removing: Shipley 1165 bath, 10 min, 65°C
    - Cleaning removal residues: acetone bath, 30 sec
    - Cleaning acetone: QDR, N_2 gun
22. **<u>Passivation layer 1</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of SiO_2: recipe LfSiO, 26 min 15 sec, target thickness = 1150 nm, deposition rate = 0.73 nm/sec
23. **<u>Passivation layer 2</u> (Equipment: PECVD - STS, tool no. 303, Göran Petersson)**
    - Deposition of low-stress Si_3N_4: recipe MfSiN (mixed frequency 350 kHz and 13.5 MHz), 1 hour, target thickness = 600 nm, deposition rate = 9.4 nm/min
24. **<u>Lamination and lithography</u> (Equipment: SST20 Resist Spinner and MA 6 Mask Aligner, tools no. 214 and 205, Karl Lundahl, Fingerprint Cards)**
    - Photoresist: SU-8 2035 (negative), spinning programme "SU-8 2035", resist thickness = 32 µm
    - Pre-bake: 2 min, 65°C
    - Soft bake: 6 min, 95°C, leave cool down
    - Exposure: Mask #5 (Contacts), 30 sec, Soft contact
    - Post-exposure bake 1: 2 min, 65°C
    - Post-exposure bake 2: 5 min, 95°C, leave cool down
    - Develop: mr-Dev 600, 10 min
    - Developer removing: rinsing in IPA beaker!, N_2 gun
    - Look at the contacts in the microscope to check the development
25. **<u>Contact pad opening</u> (Equipment: Plasma etch - Plasma Therm BatchTop RIE m/91, tool no. 418, Goran Alestig)**
    - Reactive Ion Etching (RIE) of Si_3N_4 and SiO_2: gas CF_4 + 10% O_2, 25 min, 250 W (recipe cf4x250W), etch rate = 160 nm/min
26. **<u>Dicing</u> (Equipment: Dicing saw - Disco DAD3350, tool no. 1011, Mahdad Sadeghi)**
    - Wafer dicing in chips
    - Cleaning residues: DI (de-ionized) water, N_2 gun

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