
# Slew Rate Control Optimisation for Gate Driver Circuit of NPC Multilevel Inverter

Master's thesis in Sustainable Electric Power Engineering and Electromobility

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CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2023
www.chalmers.se

Master's thesis 2023

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Master's Thesis 2023
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Printed by Chalmers Reproservice
Gothenburg, Sweden 2023

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# Abstract

Electric Vehicles (EVs) introduce unique challenges in managing Electromagnetic Interference (EMI) due to the coexistence of high and low voltages within confined spaces. At the same time, there is the need for increased efficiency of the propulsion system in order to increase the range of the EV, which means application of high-switching-speed power electronics and the introduction of wide-bandgap technologies. The overarching objective of this study is to attain optimal EMI levels within the EV's electromagnetic environment by exploring the application of multilevel inverters (MLI) based on wide-bandgap switches and optimized gate driver design with a central focus on better EMI performance and energy efficiency.

The proposed approach involves refining switching techniques of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) to strike a balance between switching rates and EMI generation. Rapid switching, while reducing losses, can lead to increased switching transients and magnetic fields, which contribute to EMI. A pivotal element of this research is the design of a gate driver circuit with controlled slew rates, specifically tailored for The Neutral Point Clamped (NPC) converter. Each switch in the inverter has been prefixed with a custom gate driver as per its slew rate.

The investigation commences with a meticulous analysis of a three-level inverter, encompassing diverse driver circuit simulations. Subsequently, the developed gate driver design is implemented in a 3-level inverter configuration. This choice aligns with multilevel inverter principles, enabling efficient operation at higher voltage levels compared to traditional two-level inverters. NPC converter topology, widely embraced in machine drive applications, forms the bedrock for these experiments.

To assess the efficacy of the proposed solution, a rigorous evaluation of modulators, including Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation (SVM), is executed through comprehensive simulations. This examination hinges on their capability to curtail EMI across the electromagnetic spectrum. Following assessment of switching techniques, a system level loss distribution analysis is done to map which switches have more concentration of switching losses. Accordingly, a unique gate driver design is proposed for each switch, and improvements in EMI magnitude and switching losses are noted.

In sum, this research endeavours to refine EV systems by orchestrating advanced switching techniques and tailored gate driver designs. By doing so, it aspires to bring down EMI to optimal levels and unlock a future of seamless electric mobility.

Keywords: EMI, NPC, MLI, Gate driver, switching losses, wide-bandgap switches, slew rate control, Space Vector Modulation (SVM)

# Acknowledgements

Completion of a project within the stipulated deadlines can always be a challenge, but we found aid and encouragement from multiple corners which made accomplishing this feat much more manageable- a tough and long road still, but paved well.

We would like to take this opportunity to extend our sincere gratitude to our supervisors Dr. Georgios Mademlis, Dr. Raik Orbay and Mr. Kooros Moabber for their guidance, support and patience. Without their positive words and constant backing at several steps of this project, the successful completion of our thesis would have been unimaginable. We are thankful also to our manager Mr. Fredrik Niklasson for allowing us the opportunity to be a part of this forward-looking project and for being as approachable as he has been time and again.

We extend a vote of thanks to our examiner Prof. Yujing Liu for being understanding and assisting us with constructive criticism and valuable insights. We deeply value his years of experience in the industry and academia, which has played a significant role in the timely fulfillment of our project objectives.

People live and thrive only with the blessings, love, and care of their loved ones, and we for one, are no exception. We move about carrying in our hearts the incredible debt to our families for being a source of inspiration and for always being by our sides through the ebbs and flows of this thesis project.

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Gothenburg, Sweden
August 2023

# List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

| | |
|---|---|
| EMI | Electromagnetic Interference |
| MLI | Multilevel Inverters |
| NPC | Neutral Point Clamped |
| PWM | Pulse-Width Modulation |
| SPWM | Sinusoidal Pulse Width Modulation |
| SVM | Space Vector Modulation |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| PMOS | Positive channel MOSFET |
| NMOS | Negative channel MOSFET |
| SiC | Silicon Carbide |
| FFT | Fast Fourier Transformation |
| THD | Total Harmonic Distortion |
| EV | Electric Vehicle |
| DPT | Double Pulse Test |
| HV | High Voltage |
| LV | Low Voltage |
| BMS | Battery Management System |
| Li-ion | Lithium-ion |
| CSI | Current Source Inverters |
| VSI | Voltage Source Inverters |

# Contents

# 1
# Introduction

Mobility throughout the world is shifting to electric propulsion. Every new Electric Vehicle (EV) in the market aims to outdo the one it succeeds with better performance, more distance per charge, and faster charging times. The necessity to pack in more sophisticated functionalities means packaging in the same space has to be tighter- the demand for more efficient systems in ever-smaller footprints is increasing. Another problem that plagues systems which have so many sub-systems working in tandem with each other simultaneously is Electromagnetic Interference, specially the EMI radiated because of antennas- placed intentionally or as a result of poor design of power electronics. An EV is a confined space where the high voltage and the low voltage sub-systems are in close proximity to each other. There's a high probability that if proper design guidelines are not followed to keep the EMI at a minimum, the numerous wired and wireless communication systems will be affected.

Thus, design and fabrication of systems with minimum possible footprint, an optimal amount of EMI, minimal losses, and increased energy efficiency is incredibly desirable.

## 1.1 Background

An EV is a complicated engineering product and specifically a Battery Electric Vehicle (BEV) can pose certain unique challenges that come with packaging a number of High-Voltage (HV) and Low-Voltage (LV) components around each other. The HV system includes the motors, the battery pack, power electronic converters- either DC-DC or DC-AC, or both. The LV system is inclusive of all the electronics and controllers- the motor controller, battery management system- (BMS), communication harness, sensor network among several other crucial hardware and software devices. In some cars, an on-board charger is also included. Efficient functioning of all the listed and unlisted components is essential and ensures that an EV functions as intended.

### 1.1.1 Battery Pack

The battery pack is the power-house of an EV. It consists of several modules of individual cells grouped together. The cells- most commonly based on chemistries based

on Lithium-ion (Li-ion) technology- are connected to each other in series and in parallel. The performance, and driving range are determined by the cells used in the battery pack. Different cell chemistries have different properties and behave in their unique manner under similar circumstances. Hence, we obtain varying performance and characteristics from different types of cells. The cells can be classified into the following categories on the basis of how the electrodes, separator, electrolyte, and the active material are packaged [1]-

- Cylindrical cells: The cell has everything rolled and packed into a cylindrical construction. Looks like a regular AA battery. The dimensions may or may not be similar, though. Most common cells are 18mm in diameter, 65 mm in height or 21mm in diameter, 70 mm in height.
- Pouch cells: The internals of the cell are stacked on top of each other and encased into a aluminium-coated plastic film.
- Prismatic cells: These cells have the constituents of the cell either rolled or stacked but packaged into a rigid cuboidal structure.

The most common elements used in formulating active materials for the different chemistry cells are: Lithium, Manganese, Nickel, Cobalt, Aluminium, Iron, Phosphorus, Titanium among others. On the basis of chemistries the most common Lithium-ion cells are:

- NCA: Nickel Cobalt Aluminium cells.
- LCO: Lithium Cobalt Oxide cells.
- NMC: Nickel Manganese Cobalt cells.
- LFP: Lithium Ferrous Phosphate cells.
- LTO: Lithium Titanium Oxide cells.

Each chemistry and construction has its own set of pro and cons and hence their own use-cases where the respective cell type is suited the best. Also, the future scope involves steering towards Solid State Batteries- they have solid electrolytes as opposed to liquid electrolytes in current Li-ion batteries- due to their superior energy and power densities.

To cool or heat the cells as per the ambient conditions, an Heating Ventilation and Air Conditioning (HVAC) system is also placed in the pack. The complete system also includes the BMS to monitor and measure a variety of parameters ont he battery pack.

### 1.1.2 Converters

Most commonly there are two kinds of converters in the car- DC-DC and DC-AC.

The DC-DC converter takes the DC voltage from the battery and generates an output to meet the supply requirements of everything apart from the traction system. This includes all the auxiliary devices like the active sensors, the infotainment

console, Electronics Control Unit (ECU), and other accessories and as well as the BMS, controllers, and other essential embedded systems. In this sense, the DC-DC converter is the main LV system supply.

The DC-DC converter utilises the buck concept to step down the input from traction voltage to LV supply voltage. Additionally, galvanic isolation may be provided to separate the input and the output sides of the converter for safety. This is done by using the either Full-bridge, Flyback or Forward topology, when required. [2]

The DC-AC converter or the Inverter is used to convert the DC battery voltage to AC voltage to power the motor. The inverter along with the motor and the battery pack forms the traction system, which essentially is everything that requires HV to operate. The motor and the inverter by themselves form the electric drive system, which is the main focus of this thesis. The upcoming sections and chapters cover inverters in more detail, with a special focus on the correlation with their relevance in the thesis.

### 1.1.3 Motor

The electric motor is the driver of the EV. It can be either DC or AC. Most commonly in EVs, an AC motor is used due to supreme performance, robust control, cost-effectiveness, and efficient regenerative braking capabilities. It receives supply from the battery pack via the inverter. For the operation of the motor it also needs to interface with the controller which is a part of the LV system. An AC electric motor can be of different types, all of which have been used in one or the other EV. A brief summary is as follows [3]:

- Induction Motor (IM): Works on the principle of electromagnetic induction. They are known to be rugged, and reliable in operation, and are also economical due to absence of any rare earth magnets and a simple construction. The control is challenging and the torque-speed curve does not yield efficient operation throughout the speed range.
- Permanent Magnet Synchronous Motor (PMSM): This motor relies on permanent magnets in its rotor to lock itself with the magnetic field generated by the stator. Presence of rare earth material makes it expensive but has superior control and performance characteristics.
- Synchronous Reluctance Motor: This motor is finding more and more traction among EV manufacturers as it overcomes a few of the cons of the PMSM. For example, it is free of magnets and works on the basis of magnetic fields generated by the stator and the rotor by aligning the rotor with the path of the least reluctance. However, it has noise and vibration, and performance issues due to which it has not seen a more widespread application.

### 1.1.4 BMS and Controllers

The Battery Management System is crucial for the safe operation of the battery pack. It monitors the voltage, current and temperature values pertaining to each cell in the pack. It then ascertains that the operating conditions with regard to each parameter is met and no thresholds are crossed, and if they are the protection circuits are engaged and the battery pack is disconnected from the system. This was isolation is maintained as a precautionary measure.

The motor controller is responsible for managing the operation of the electric motor. It controls the power, RPM, torque output, and direction of the motor as per the requirement. It takes input from several sensors regarding the motor position, speed, current drawn, and temperature, after which the control algorithm processes the sensor data to guide the operation of the motor. This device also works to protect and isolate the motor and the battery system from each other- provision for overcurrent, over-temperature, short circuit protections is in place, alongside current and voltage limiters.

### 1.1.5 Miscellaneous LV

The harness that runs along the length and breadth of the automobile is a crucial hardware. It carries all the signals from the sensors to controllers. Many of these signals are critical for the operation of the vehicle. The communication between any two or more ports may happen using CANbus, ethernet, UART, isoSPI or other serial protocols.

Since, all this is in close proximity to the HV components, the potential of Radio-Frequency (RF) coupling is high. The EMI generated by these HV devices must be minimised for this reason [4].

### 1.1.6 Electromagnetic Interference

EMI is the disturbance in the transmission of a signal caused due to an electromagnetic radiation emitted by another device operating in the vicinity. The effect of EMI from a foreign device can vary from being a minor disturbance in the signals, to severe system malfunction and yielding of unintended results. Minor EMI inflictions can be dealt with the use of filters and shielding, however it should be a standard practice to design systems around EMI considerations to increase the robustness and reliability of the system. [5]

There are industrial standards which are adhered by all manufacturers in the field of application of power electronics and electric machines. These standards limit the amount of permissible radiated EMI which is emitted from a vehicle. The vehicle has to obtain the standard and clear the certification in order to be eligible to be sold in the open market. These standards are often quite specific to each market, that it, to each country. The most prevalent standard is the UNECE R10, and there

are several other region-specific standards formulated as per local norms. [6]

There are no legal standards, per se, limiting the amount of EMI present on the interior of the vehicle, however, it is still monitored and limited stringently by individual manufacturers using their internal standards. This is done to effect an optimal system performance, especially when the sensitive components like antennas, sensors, and wirless communications. [4] [6] Such standards are often labelled as 'Customer Satisfaction Requirements'.

EMI can be roughly segregated into two types [7]-

- Radiated EMI: The EMI which gets transmitted from one device to another via media like air are classified as radiated EMI. It is most commonly leakage electric and magnetic fields that cause such disturbances.
- Conducted EMI: When the transmission of EMI takes place via wires and conduits, then it is termed as conducted EMI. It can creep into the system via cables and PCB traces and other shared connections. In the system it manifests itself as voltage and current ripples of a very high frequency.

Then there is the interaction between the radiated and the conducted components of EMI. The conducted EMI generates a magnetic field of its own owing to the current and the voltage, and their ripples in the conductors. This adds to the total radiated EMI. An electrical system has signals, switches and power connections present, and several EMI waves with different frequencies and amplitudes are existent in the system [8] [9]. The most common causes can be summarised as follows:

- Fast switching: As the technology evolves, we are seeing attempts at faster and faster switching using SiC and GaN based Field Effect Transistors (FET) because of higher efficiency, lower switching losses, and smaller overall system footprint.
- Clock signals: These are generally high frequency and contribute to EMI.
- Power supplies: High current can lead to generation of electromagnetic (EM) waves which can act as noise in surrounding systems.
- Wiring: Poor harness design can lead to formation of loops and act as antennas which can radiate unwanted EMI and hamper efficient operation.
- External sources: EM waves from high voltage power lines and radio towers and nearby wireless devices can have an effect on a sensitive system and make it susceptible to EMI.

Being an issue of grave concern in modern electrical systems, there are certain measures that are taken to mitigate the problem to an extent. After the application of specific measures it is still mandatory to conduct an EMC test to make sure the EMI is within certain thresholds and compliance is maintained. [8] [9] There are certain limitations to additional measures that need to be put on place to account for an increased EMI in the system.

- Shielding: Sensitive components are often shielded using conductive material to safeguard against any stray EMI that may affect the operation negatively. Shielding all the components would make the system quite expensive and add to the service-ability of the system- it would be cumbersome and time-consuming to troubleshoot and repackage everything together. It can have leakage points due to low quality termination and lifetime degradation.

- Filtering: Having filters designed into the system is an essential practice to take care of unwarranted signals in the circuits. However, they are quite heavy and bulky, which means they require a lot of space. This would make the footprint of the device larger contrary to industry-wide attempts. Filters are also limited regarding the frequencies they can absorb, and EMI tends to have a wide frequency range. Accommodating filters to absorb most of the EMI would be infeasible. Also, the size of the filters increases with the frequency it is designed for.

- Grounding: It aids in sending all the EMI to the ground. Improper grounding can lead to formation of ground loops which emulate an antenna, as the current which should have been grounded is now circulating in the system in a loop. This will exacerbate the interference amount in the system. Grounding has to be short and highly conductive, and packaging restrictions can make this difficult.

- Isolation: Proper distancing between the HV and the LV components can bring down the mutual and detrimental influence they have on each other. Isolation means appropriate spacing the system, and requires space, which there is a dearth of in an environment like an EV. Transformers and optocouplers are the most common choices and can add system complexities, bulk and signal deterioration problems.

- Harnessing: Careful system design and harness design can go a long way in minimising the EMI occurrence in the system. Effective and optimal component placement could be a challenge as the space in an EV is already constricted. Packaging restrictions are an added challenge. Additionally, at high frequencies, component placement and mitigation of EMI via ideal electrical design becomes an even greater obstacle.

The variety of reasons are why inherent design solutions that aid in limiting the EMI and increasing energy efficiency in the system, while still being compact in footprint, light in weight, and economical to produce, are crucial for the development of next-generation traction systems for future EVs.

### 1.1.7 Solution

The aforementioned issues and challenges in totality are a clear sign pointing towards one clear fix- application multi-level inverters utilising wide band-gap power

switches.

MLIs have several advantages over the traditional two-level inverter. There is a detailed description and comparisons in Chapter 2 of this report, so in-a-nutshell, MLI offer better harmonic performance, higher efficiency and better quality voltage waveform. Wide band-gap devices have high electron-mobility which allows them to undergo faster switching at higher frequency with lower conduction and switching losses, as well as more robust performance at higher temperature. They also have a significantly smaller footprint than regular Silicon-based semiconductor devices

When we combine them both, that is, a functioning MLI using wide band-gap semiconductor devices would be an ideal solution to tackle EMI and efficiency problems. To be precise, Silicone-Carbide (SiC) type wide band-gap switches are utilised to design a Neutral-Point Clamped MLI. The aims of the study are to achieve high efficiency operation of the inverter designed, with reduced EMI generation. One major challenge that poses is that both the aims are in direct contradiction with each other. While high efficiency operation calls for a high frequency and densely packed design, low EMI generation required slower switching rates and well-isolated individual components in the design. Therefore, to be able to utilise the strengths presented by the wide band-gap technology, an alternate method to obtain reduced EMI levels with efficient packaging has been devised. This problem statement is the precise birthing place of this thesis project. To attain the mentioned goals, a custom variable slew-rate gate driver has been ideated for each group of switches in the inverter with a unique power-loss distribution.

### 1.1.8 Slew-Rate

The Slew-Rate (SR) is the rate of change of a parameter with respect to time. Or more precisely in this case, it can be defined as the rate of change of voltage across the switch with respect to time. It quantifies how quickly the voltage climbs or falls while switching ON or OFF of a switch. It is measured most commonly in V/$\mu$s or in V/ns. It can represented as below:

$$SR = \frac{\Delta V}{\Delta t} \tag{1.1}$$

The SR is directly proportional to the frequency response of the circuit- higher the SR, higher the frequency signal can be handled by the circuit. However, a high SR also translates into higher overshoot and ringing. A rapidly rising voltage waveform is highly likely to overshoot from the new steady state value, although briefly, and generates high frequency oscillations while stabilising. This is termed as ringing, and this is the genesis of conducted EMI. High- speed switching requires higher slew rates, and hence a remedial circuit is designed to placate the EMI that takes place as a byproduct.

## 1.2 Aim

The aim of this project is to design a variable slew-rate gate driver for 3 phase NPC inverter, which will reduce the switching losses by eliminating EMI caused by fast switching transient.

## 1.3 Scope

The thesis project will focus on simulation study related to designing of a variable slew-rate controlled gate driver for a 3-phase 3-level NPC converter. Different topologies of gate drivers will be studied and the main focus will be to limit the generation of EMI during switching transients of MOSFETS using slew-rate control.

Based on the literature study, variable slew-rate controlled gate driver is selected, which is implemented in NPC converter. The variable slew-rate gate driver is selected to control the switching transients during turn-ON and turn-OFF of MOSFETs. The gate driver is designed with 4 driver MOSFETs- 2 PMOS to control turn-ON region of power MOSFET, and 2 NMOS to control turn-OFF region of power MOSFET. To derive the switching characteristics of the power MOSFET, Double Pulse Test (DPT) is simulated in LTSpice. Based on the derived switching characteristics, a 3-phase MLI is designed on PLECS, modulation techniques like SPWM and SVM are compared and implemented to reduce the switching losses due to EMI. PLECS is further utilised to run system level simulations and map the loss concentration in all the switches. Conduction and switching losses are studied. This is done to be able to design a gate driver with higher SR for switches with higher losses and ringing, and another gate driver with lower SR for switches with lower losses and ringing.

As the project is focused on designing the gate driver for an inverter, other aspects like battery model, or the motor model are not considered instead the input to the inverter model is a steady DC source. The losses related to battery are not considered. The motor is modelled as a current source and the losses of the electrical machine are also not considered.

## 1.4 Outline

The initial phase of the thesis was focused on literature study. It was essential to educate ourselves about exploring the scope of the thesis. Several research papers were scoured through to get insights into gate driver topologies and how each one behaved under different operating conditions and would serve our purpose the best. In parallel, modulation techniques were also studied and a holistic understanding of application of multiple switching methods was obtained. Simulations were run with a combination of our selections and the best system performance was observed

on parameters like efficiency, noise in the output, and desired slew rate and gate resistance.

After the gate driver topology and modulation strategy were zeroed down on, system level simulations were run and loss distribution among all the switches in the NPC converter was noted. This was done for a variety of operating conditions- varying the modulation index of the modulator, the load current, and the type of load. Frequency response of each gate driver was also studied to ensure steady operation.

A custom gate driver with a unique slew rate was designed for each pair of switch showing unique characteristics. In most cases the two switches in each phase on the extreme ends had identical responses, while the two on the inside had similar responses- as is obvious with a 3-phase 3-level inverter operation.

# 2

# Inverters

An inverter converts direct current and voltage into alternating current and voltage for the electrical machine (EM). It accomplishes this by modulating sinusoidal waveforms using high-frequency switching of power semiconductors. As a result, it produces the three phases of sinusoidal current that are 120°phase-shifted required to enable the EM to produce an output torque. The frequency of the produced waveforms determine the speed of rotation of the EM, while the amplitude determines the motor power or torque.

## 2.1 Types based on Source

Voltage source inverters (VSI) are where the inverter works as voltage source. This is the most common inverter, and has a relatively higher efficiency. Whereas, current source inverter (CSI) controls the current output, needs very big inductance, and has a lower efficiency, which is why a VSI is chosen for this project.

### 2.1.1 Current Source Inverters

When the inverter's input is a constant DC current source, the inverter is referred to as a current source inverter. The current source inverter (CSI) receives stiff current from the DC source when the DC source has a high impedance. Stiff current is typically produced using a large inductor or closed-loop-controlled current. The ensuing stiff current wave is unaffected by the load. The switching states of the switches in the inverter and the DC source entirely dictate the AC output current [10].

### 2.1.2 Voltage Source Inverters

When an input source with a constant DC voltage is used, the inverter is referred to as a voltage source inverter (VSI). A rigid DC voltage source serves as the input to the voltage source inverter. When a DC voltage source is stiff, it signifies that its impedance is zero. A stiff voltage is achieved by adding a capacitor between the positive and the negative terminals of the DC supply. Practically, DC sources have a very low impedance. The assumption is that VSIs are powered by ideal voltage sources with very low impedance sources. The switching states of the inverter and the applied DC source only define the AC output voltage [10]. Stiffness of voltage

implies that the voltage does not change with change in load, and the VSI is able to maintain a constant output load voltage even in varying operating conditions with variations in load impedance.

## 2.2 Types based on Levels in Output Voltage

### 2.2.1 Two-level Inverters

The most popular and straightforward inverter topology utilised in electric car applications is a three-phase two-level Inverter. It converts a DC voltage source into AC voltage, which is then delivered to the load- a machine that runs on electricity- via it. Six semiconductor switches make up this topology, and each switch incorporates an anti-parallel diode to allow current to flow in the other direction. Two levels of output voltage, $+V_{dc}$ and $-V_{dc}$ can be obtained from this inverter in its phase-to-ground voltage.

Because of its lightweight, compact, and relatively good performance, the three-phase two-level VSI is the standard inverter structure used in small-scale systems [11], especially in powertrain design where small size is crucial. It consists of six semiconductor switches $S1-S6$ (either IGBTs or MOSFETs) whose switching times are intuitively selected to achieve the demanded fundamental voltage amplitude and frequency. Each switch consists of anti-parallel diodes, $D1-D6$ that provide free-wheeling paths for negative inductive currents when the switch is turned on [12] [13]. Its output consists of three identical waveforms that are phase-shifted by 120° from each other. The input to the inverter usually referred to as the dc-link, consists of a power source, $V_{dc}$ (battery in this case), and the DC-link capacitor, $C$.

### 2.2.2 Multilevel Inverters

It is a power electronic device that generates an output phase to ground voltage with more than two levels by using additional switching devices. The elementary concept of an MLI is to utilise one or several DC sources to generate a staircase voltage waveform which resembles an AC wave. It is a power electronic device which provides a solution to achieve higher power by making use of more switching devices to produce an output phase to ground voltage with more than two levels. An n-level MLI will be able to produce 'n' number of voltage levels in its phase-to-ground output voltage waveform. It has several advantages when compared to the Two-level Inverter (TLI). As the number of levels is increased, a more sinusoidal voltage waveform can be realised using a lower switching frequency - at the same level of harmonics - when compared to the TLI. This helps in reducing the THD. As the number of levels increases, the voltage across each switch also goes down. This reduces the switching losses and Electromagnetic interference (EMI) in the MLI. Hence, it is able to deliver an improved power quality and higher voltage capability The sequence of switching is determined by the gate driver, which in turn is part of the modulator [14] [15]

.
An MLI offers several advantages over a conventional two-level VSI using a high-frequency PWM technique. It is superior to the two-level VSI in several ways. When compared to the two-level VSI, a more sinusoidal voltage waveform can be realised when the number of levels is raised at a lower switching frequency. This aids in lowering THD. The voltage across each switch decreases as there are more levels. By doing this, the switching losses and EMI in the MLI are decreased. As a result, it has the capacity to produce higher voltages and better power quality. These advantages can be summarised as follows: [14] [15] [16] [17]

1. Staircase waveform quality
   (a) MLI generate output voltage with low distortion.
   (b) Reduced *dv/dt* stresses on each switch.
   (c) EMC performance is enhanced. Lower Total Harmonic Distortion (THD).

2. Common-mode (CM) voltage
   (a) MLI converters produce CM voltage of lower amplitude.
   (b) Motor bearing stresses connected to the MLI can be reduced.
   (c) CM voltages can be eliminated using advanced modulation strategies.

3. Input current
   (a) Input current ripple is reduced. Added bulky filters are not required.
   (b) In general, lower levels of EMI are found.

4. Switching frequency
   (a) MLI converters can operate at both fundamental and high switching frequencies.
   (b) The Lower the frequency, the lower the switching losses and the higher the efficiency.

It has a few disadvantages as well. A greater number of semiconductor switches are needed. Each switch also requires an associated gate driver circuit, all of which in combination makes the system complicated and expensive.

Determining the number of levels in a multilevel inverter is one of the most crucial decisions because it influences many other sizing considerations and control strategies. The main distinctions between an MLI and a two-level inverter are the trade-offs in determining how many levels will be required, as well as the benefits and complexity of having various voltage levels accessible. The total voltage-blocking capacity of the active devices in each phase leg is unaffected by the number of levels because fewer device ratings can be used. The following are some advantages of using more levels in a diode-clamped inverter: [15]

1. There is less voltage stress across each device. Lower voltage-rated active devices and dc link capacitors (which can occasionally be significantly less expensive and more readily available) can both be employed.

2. Due to the reduced *dv/dt* during each switching, the inverter will have a lower EMI.
3. The waveform's output will have more steps or degrees of freedom, allowing it to more closely resemble a reference waveform.
4. An inverter with fewer levels and a higher device switching frequency will produce the same results as one with fewer levels and a lower individual device switching frequency. Or, to obtain a better waveform, the switching frequency can be maintained at the same level as in an inverter with fewer levels.

The following are the drawbacks of employing more levels than what is necessary:

1. The complexity of the control increases as the number of layers increases.
2. If blocking diodes employed in the inverter had the same rating as the active devices, the number would increase significantly.

Several varying MLI topologies have been devised over the years considering the variety of applications that each is supposed to serve. High or medium-voltage industrial drives, interfacing with renewable power systems, grid-side transmission systems and traction drives are a few of the applications for which MLI have been designed specifically. MLI can be of the following types-

- Flying capacitor Inverter
- Cascade H-bridge Inverter
- Diode clamped/Neutral Point clamped Inverter

## 2.3 Flying Capacitor Inverter

The circuit topology of the Flying Capacitor Multilevel (FCMLI) has DC side capacitors in a ladder structure, where the voltage across each of the capacitors is different. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform [16].

For an n-level FCMLI, $(n-1)$ capacitors are used with $2(n-1)$ switching devices. The voltage across each capacitor is $(V_{dc})/(n-1)$. As the flying capacitors are charged to their respective voltage levels, they provide the additional voltage levels by performing the correct switching strategy. Hence, as the number of levels increases, the number of capacitors will also significantly increase which could make the device bulky. It is important to also consider the size of flying capacitors to have lower voltage ripple for the flying capacitors as well [14].

For a three-level FCMLI, the additional zero level is achieved by making use of flying capacitors. This topology has two different switching states to produce the zero-voltage level. Hence, both these switching states must be equally used to ensure that the corresponding switches are evenly stressed.

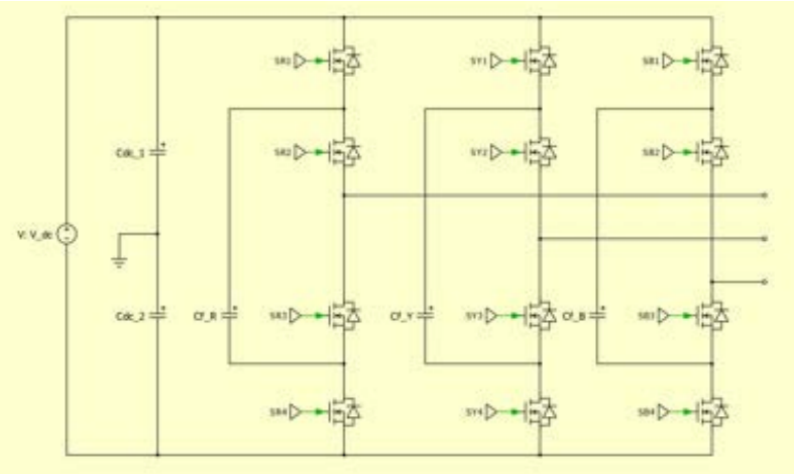


**Figure 2.1:** Flying-capacitor Multilevel Inverter

The DC voltage is split into two by the DC-link capacitors, which is $V_{dc}/2$. The flying capacitors shall also have a voltage of $V_{dc}/2$. Switches 1 and 2 are on to produce the positive voltage. For the FCMLI, the two zero-switching states need to happen alternatively. This automatically provides voltage balancing for the flying-capacitors present in each phase leg. In one of the zero-switching state cases, the voltage produced due to the DC-link capacitor is opposed by the flying capacitor and the capacitor goes into a charging state. In another case, the voltage produced due to the second DC-link capacitor is opposed by the flying-capacitor and the capacitor goes into a discharging state. Switches 3 and 4 turn on to produce the negative voltage. The voltage across all switches shall now be only $V_{dc}/2$ [20].

This topology often finds application in electric vehicle drives, solar inverters, and static VAR compensators [21]. One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. The FCMLI does not require all switches that are on, that is, in a conducting state, to be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [17]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated into the control system for balancing the voltages across the various levels [19]. It presents the following advantages and disadvantages: [18]

Advantages

- The voltage level of the capacitors can be balanced as phase redundancies are available.
- Flow of real and reactive power can be controlled.
- The large number of capacitors enables the inverter to ride through short-duration outages and deep voltage sags.
- Reduces $dV/dt$ stress across the device.
- Additional switching states help to maintain charge balance in the capacitors.

Disadvantages

- Control to track the capacitor voltage levels is complicated.
- Precharging all the capacitors to the same voltage level is cumbersome.
- Start-up is complex.
- Switching utilization and efficiency are poor for real power transmission.
- The large number of capacitors is more expensive and bulkier than clamping diodes in multilevel diode-clamped converters.
- Packaging is also more difficult in inverters with a high number of levels.

## 2.4 Cascade H-bridge Inverter

The Cascaded H-bridge Multilevel Inverter (CHBMLI) has an H-bridge inverter as a sub-module with individual DC sources for each phase leg. This enables three different voltage levels in its phase-to-ground voltage.

Each separate DC source is connected to a single-phase full-bridge or H-bridge inverter. Three different voltage outputs - $+V_{dc}$, 0, and $-V_{dc}$ - can be generated by each inverter level utilising different combinations of switches available between the DC source and the AC output. The AC outputs of each inverter level are connected in series. Hence, the synthesised voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels 'm' in a cascade inverter is defined by $m = 2s + 1$, where 's' is the number of separate DC sources. [17]

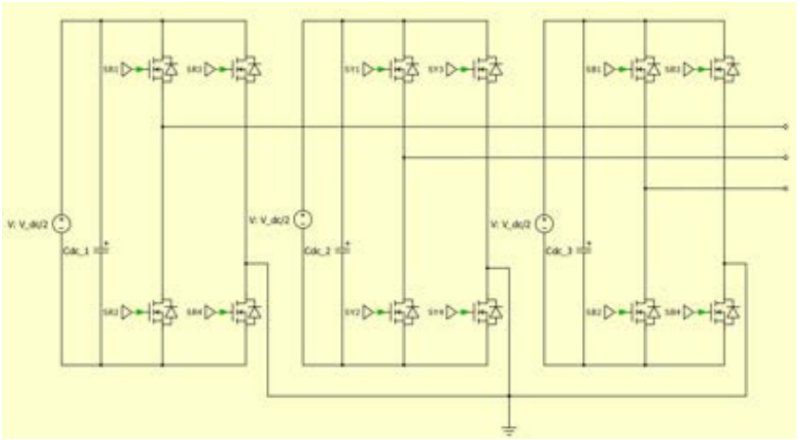


**Figure 2.2:** Cascaded H-bridge Multilevel Inverter

To get an n-level CHBMLI, 'n' sub-modules will need to be used in series for each phase and $2(n-1)$ switches will be required for each phase. The voltage stress across each switch depends on the DC source of the sub-module. It can be extended to higher levels easily due to its modular structure. This topology requires individual DC sources for each sub-module. It does not need additional components such as diodes or capacitors used in the previous topologies. For a three-level CHMI, the additional zero level is achieved by using individual DC sources in each phase leg to produce the three different voltage levels. The individual DC sources have a voltage

of $V_{dc}/2$ which is half in value compared with the DC sources in other topologies. Like the FCMLI topology, this topology also has two different switching states to produce the zero-voltage level and both these switching states are equally used.

Often utilised in motor drives, and fuel-cell-based systems, but also to connect battery systems and photovoltaic systems to the grid [21]. The DC source present in each phase leg will also have DC-link capacitors. Switches 1 and 4 are on to produce the positive voltage. The output is in parallel connection to the DC-link capacitor. The two zero-level switching states are either the top two switches or the bottom two switches can be closed, which makes the output in short circuit condition to produce the zero voltage level. Switches 2 and 3 are on to produce the negative voltage level. The output is connected in parallel but with reversed polarities. The voltage across all switches shall now be only $V_{dc}/2$ [14] [19]. The advantages to this topology of MLI are as follows: [18]

Advantages
- Easy packaging and storage.
- Produce common mode voltage, stress is reduced.
- Low distortions in the input current.
- Low distortions in the input current.
- Operates at both fundamental switching frequencies.
- Total harmonic distortion is very low in the output waveform without any filter circuit

Disadvantages
- Separate DC sources are required for each of the H-bridges.
- Limited application - to products with multiple separate DC sources.
- Complex controller is required due to the amount of capacitors

## 2.5 Neutral Point Clamped MLI

To produce the additional voltage levels at the output in its phase-to-ground voltage, the Neutral Point Clamped Multilevel Inverter (NPC MLI), also known as a Diode-Clamped Multilevel Inverter, uses clamping diodes. Each phase of the inverter shares a common DC bus. The DC bus is divided into six levels by five capacitors. The voltage across each capacitor is $V_{dc}$, and each switch goes through a voltage stress limited to $V_{dc}$ through the clamping diodes [16].

For an n-level NPC MLI, $(n-1)(n-2)$ clamping diodes are used across each phase leg, $(n-1)$ capacitors on the DC bus - also called DC-link capacitors; and $2(n-1)$ switching devices in each phase [22]. As the DC-link capacitors are charged to their respective voltage levels, they provide the additional voltage levels by performing the correct switching strategy. For a three-level NPC MLI, the additional zero level is achieved by making use of clamping diodes. The DC voltage is split into two by the DC-link capacitors, which is $V_{dc}/2$. Switches 1 and 2 are on to produce the

positive voltage. Two zero-level switching states are obtained when either switch 2 or 3 conducts depending on the current direction. For a positive current, the switch 2 conducts and for a negative current, the switch 3 conducts. Switches 3 and 4 are on to produce the negative voltage. For all the cases, based on the current direction, either the switch conducts or the anti-parallel diodes conduct. For example, a positive current switches 1 and 2 conduct but for a negative current the anti-parallel diodes conduct. The voltage across all switches shall now be only $V_{dc}/2$. [17] [19]

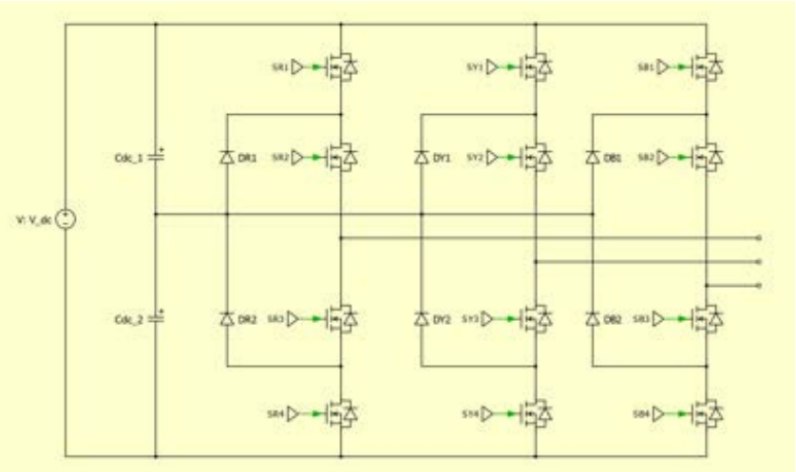


**Figure 2.3:** Neutral Point Clamped Multilevel Inverter

One application of the multilevel diode-clamped inverter is an interface between a high-voltage DC transmission line and an AC transmission line. Another application would be as a variable speed drive for high-power medium-voltage (2.4 kV to 13.8 kV) motors. Static VAR compensation is an additional function which several authors have proposed for the diode-clamped converter [21]. The main advantages and disadvantages of multilevel diode-clamped converters are as follows [15] [16] [18]:

Advantages

- Since all phases share a common DC bus, the capacitance requirements are minimised.
- Back-to-back topology is practical for an adjustable speed drive.
- Voltage across the switch is only half of the DC-link voltage
- Group pre-charging of the capacitors.
- Efficiency is high for fundamental frequency switching.
- Voltage harmonics is centred on twice the switching frequency

Disadvantages

- The intermediate DC levels tend to overcharge or undercharge without precise control, hence, the flow of real power is difficult.
- The required number of clamping diodes is directly related to the number of levels. This makes designing additional levels challenging.

The multiple MLI topologies studied can be summarised as follows. A count of passive components has been compared for each unique topology, alongside the applications each is most popularly used for. Voltage balancing capability of each topology is also compared as that determines if an MLI would need an additional voltage-balancing circuit or not, and that ties into the size of the footprint of the inverter, as well as its cost-effectiveness and packaging.

| S.No. | Topology | Diode Clamped | Flying Capacitor | Cascaded |
|---|---|---|---|---|
| 1 | Power semi conductor switches | 2(m-1) | 2(m-1) | 2(m-1) |
| 2 | Clamping diodes per phase | (m-1)(m-2) | 0 | 0 |
| 3 | DC bus capacitors | (m-1) | (m-1) | (m-1)/2 |
| 4 | Balancing capacitors per phase | 0 | (m-1)(m-2)/2 | 0 |
| 5 | Voltage unbalancing | Average | High | very small |
| 6 | Applications | Motor drive system, STATCOM | Motor drive system, STATCOM | Motor drive system, PV, fuel cells, battery system |

**Figure 2.4:** MLI comparison summary

Several modulation techniques have also been developed for MLIs. The methods such as Sinusoidal Pulse Width Modulation (SPWM), Selective Harmonic Pulse Width Modulation (SHE-PWM), and Space Vector Modulation (SVM), and others make use of the strengths offered by MLIs to extract the best and optimal performance from the system. These have been discussed in-depth in Chapter 5.

# 3
# Gate Drivers

## 3.1 Importance of gate drivers

The gate driver circuit in a Multilevel Inverter is a specialised and crucial component that has a significant impact on the overall performance of the inverter. Its primary responsibility is to facilitate fast and precise switching of MOSFETs, which leads to reduced switching losses. A well-designed gate driver ensures that MOSFETs turn on and off at the appropriate times [23]. This action prevents voltage overshoots that might otherwise lead to device failure.

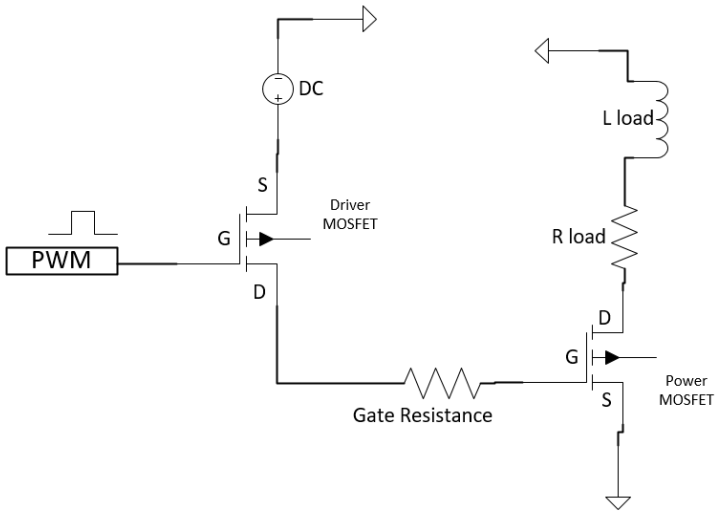



**Figure 3.1:** Basic gate driver circuit

Furthermore, the gate driver plays a vital role in achieving voltage balance across all the MOSFETs in the inverter. This balance is essential to avoid over-voltage conditions. Ensuring that each voltage level is properly maintained prevents any imbalance that could affect the system's stability and efficiency.

Multilevel Inverters often utilise various modulation techniques such as Pulse Width Modulation (PWM) and space vector PWM [12]. In this context, the gate driver's role becomes even more critical. It is responsible for accurately implementing these modulation techniques and precisely synchronising the switching of multiple power

devices. This synchronisation is vital to achieve the desired output waveform and to maintain proper control over the inverter's performance.

In conclusion, the gate driver is an indispensable element in modern power electronic systems. It ensures efficient and reliable operation by enabling fast and precise MOSFET switching, maintaining voltage balance, and implementing complex modulation techniques in Multilevel Inverters.

## 3.2 Types of Gate Drivers

Gate driver categories:-

- Gate drivers can be categorised as either hard-switching or soft-switching, each having distinct characteristics for managing power device switching. Hard-switching drivers offer simplicity and are well-suited for slow switching rates. This helps mitigate switching losses and electromagnetic interference (EMI). However, they can result in higher losses and interference.

  Conversely, soft-switching drivers employ intricate techniques such as zero-voltage and zero-current switching. These techniques offer the advantage of zero losses and minimal EMI. They also allow for achieving high switching slew rates. However, their design complexity is greater compared to hard-switching drivers.

  The choice between these two types of drivers depends on the specific application needs. Hard-switching drivers are preferable for situations with slow switching rates, prioritising simplicity. On the other hand, soft-switching drivers are suitable for situations where reducing losses and EMI is a priority, even if it means dealing with greater intricacy in design.

- Variable slew rate gate drivers provide the capability to adjust the rise and fall times of the gate voltage during switching [25],[37]. This adjustment empowers designers to find a balance between switching losses and electromagnetic interference (EMI).

  In contrast, adaptive slew rate gate drivers take it a step further. They automatically modify the gate voltage slew rate based on prevailing conditions. This adaptive approach enhances efficiency and minimises EMI by continually optimising the switching behaviour according to real-time requirements.

  An innovative approach involves the use of multilevel slew rate gate drivers, which introduce a novel control technique. In this technique, the driver MOSFET is precisely triggered just before turn-on and turn-off events. This precise timing facilitates the injection of additional current. The purpose of this extra current injection is to effectively mitigate overshooting issues caused by

fast-switching transients. This mitigation contributes significantly to the improvement of the overall performance of the system.

The proposed gate driver is a variable slew rate gate driver, by accurately controlling the rise and fall time of driver MOSFETs through pulse width modulation, to reduce the switching losses and EMI. The unbalanced loss distribution in NPC MLI is utilised to design a unique gate driver with individual slew-rates for each switching device to make the loss distribution more optimal. The multilevel slew rate control is also tested for the designed variable slew¨rate gate driver.

### 3.2.1 Drivers without slew rate

The below figure shows a simplified gate driver without slew rate control through which we can only control switching actions.

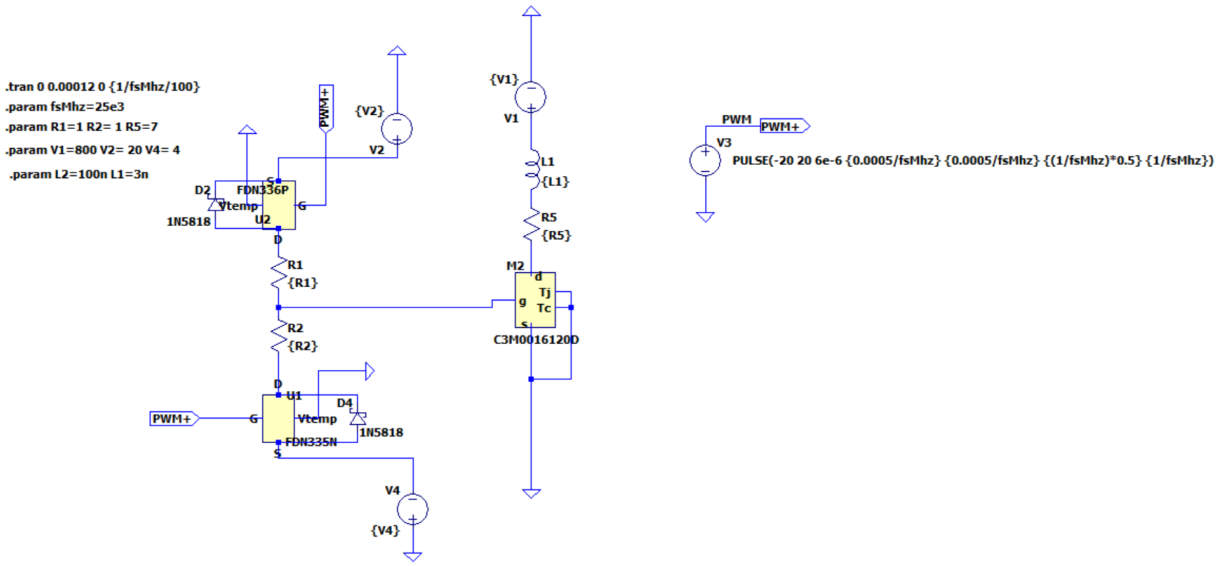



**Figure 3.2:** Driver without slew rate control

A single resistance is used to control the power MOSFET. The two driver MOSFETs, each handle the turn-on and turn-off phases of the power MOSFET through PWM modulation. The P-type driver MOSFET controls the turn-on and the N-type driver MOSFET controls turn-off side of power MOSFET[23]. The parallel combination of R1 and R2 provides a constant gate resistance, resulting in a consistent slew rate. However, this slew rate cannot be dynamically controlled.

### 3.2.2 Driver with slew-rate

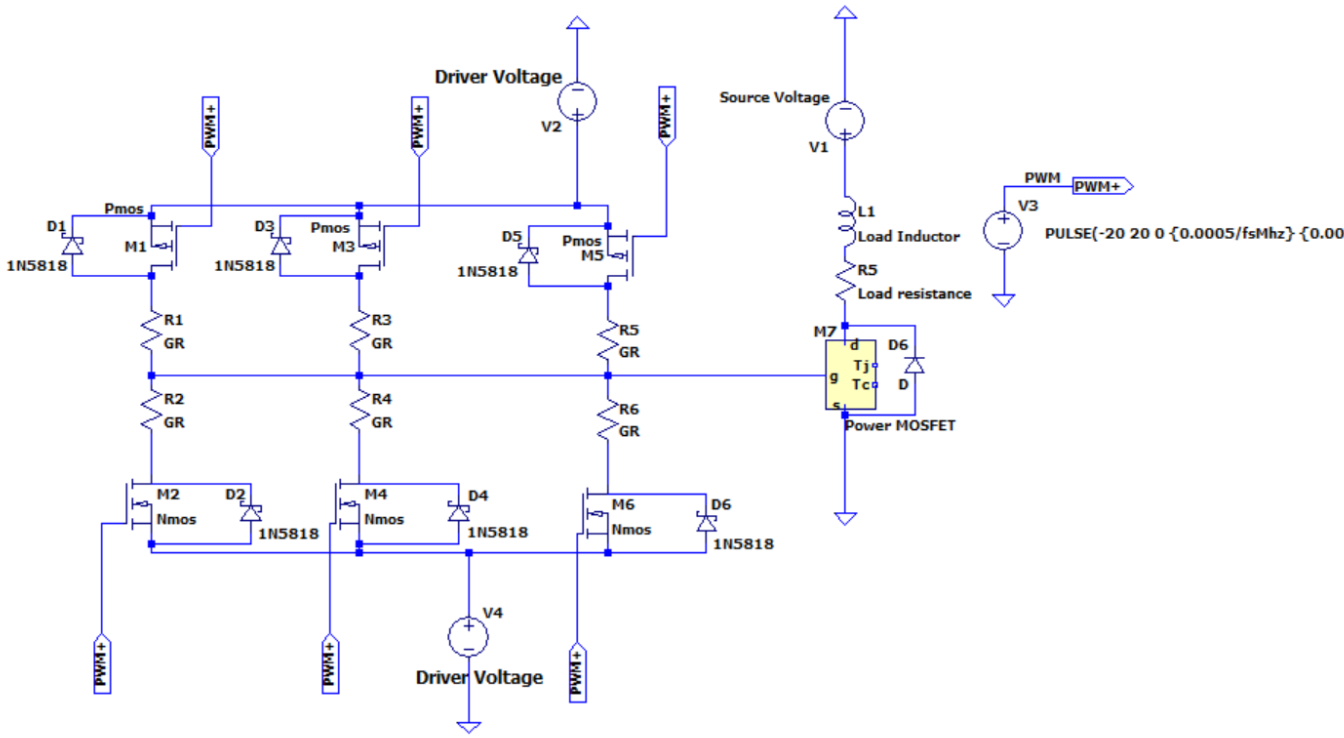



**Figure 3.3:** Driver with slew rate control

Figure 3.3 introduces a novel driver featuring slew-rate control, similar to the operational methodology in Figure 3.2. The design involves considering the driver MOSFETs connected in parallel. The resistances R1 and R2 provide a single gate resistance to control the current [24], [26]. Considering it as a single bridge, effectively integrating three bridges within the gate driver structure. This architectural arrangement empowers each bridge to establish unique gate resistance settings, varying the current at different levels.

This configuration's intrinsic advantage lies in the independent control of each bridge, affording an elevated level of control. This, in turn, facilitates precise modulation of current during power MOSFET turn-on and turn-off phases, tailored to accommodate specific slew-rate preferences and address electromagnetic interference (EMI) considerations.

## 3.3 Proposed active gate driver with slew-rate

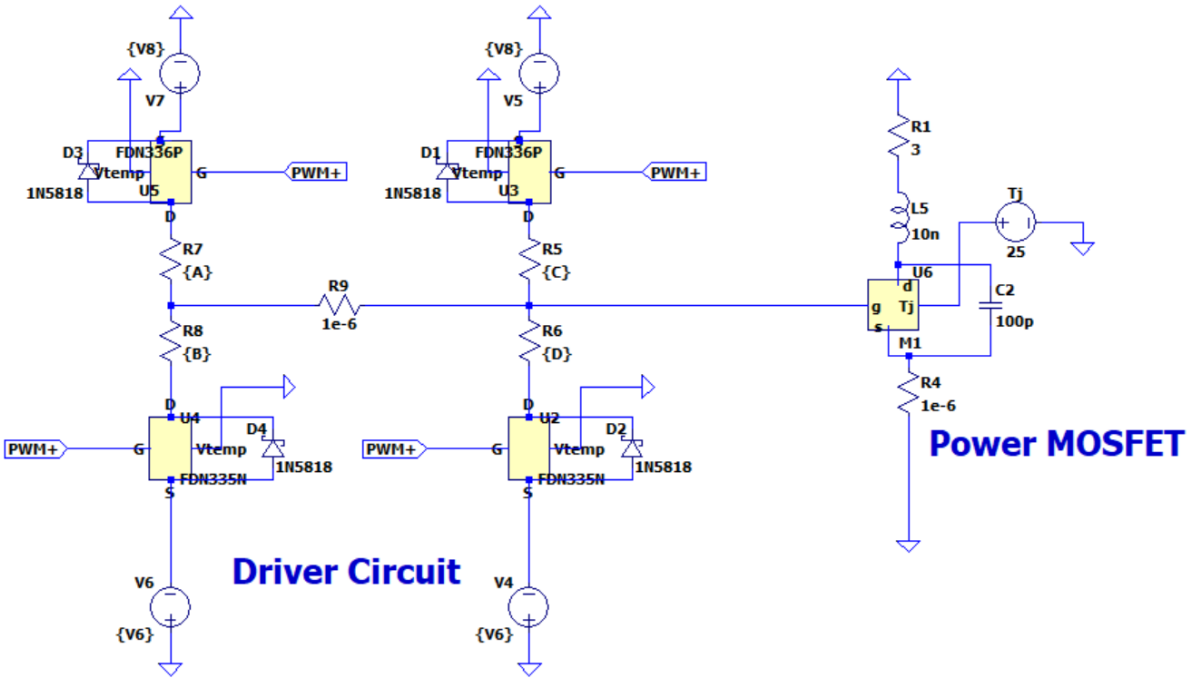



**Figure 3.4:** Driver with slew rate control

- FDN336P - PMOS
- FDN335N - NMOS
- M1 - Power MOSFET
- fs - 25k Hz, temperature - 25 deg

Two bridges are present. Each bridge consists of a P-type MOSFET that regulates the current through R7 [25]. Additionally, an N-type MOSFET is utilized to control the current through resistance R5 in the 1st bridge. The same method is used to control the current in the 2nd bridge through resistances R5 and R6[37].

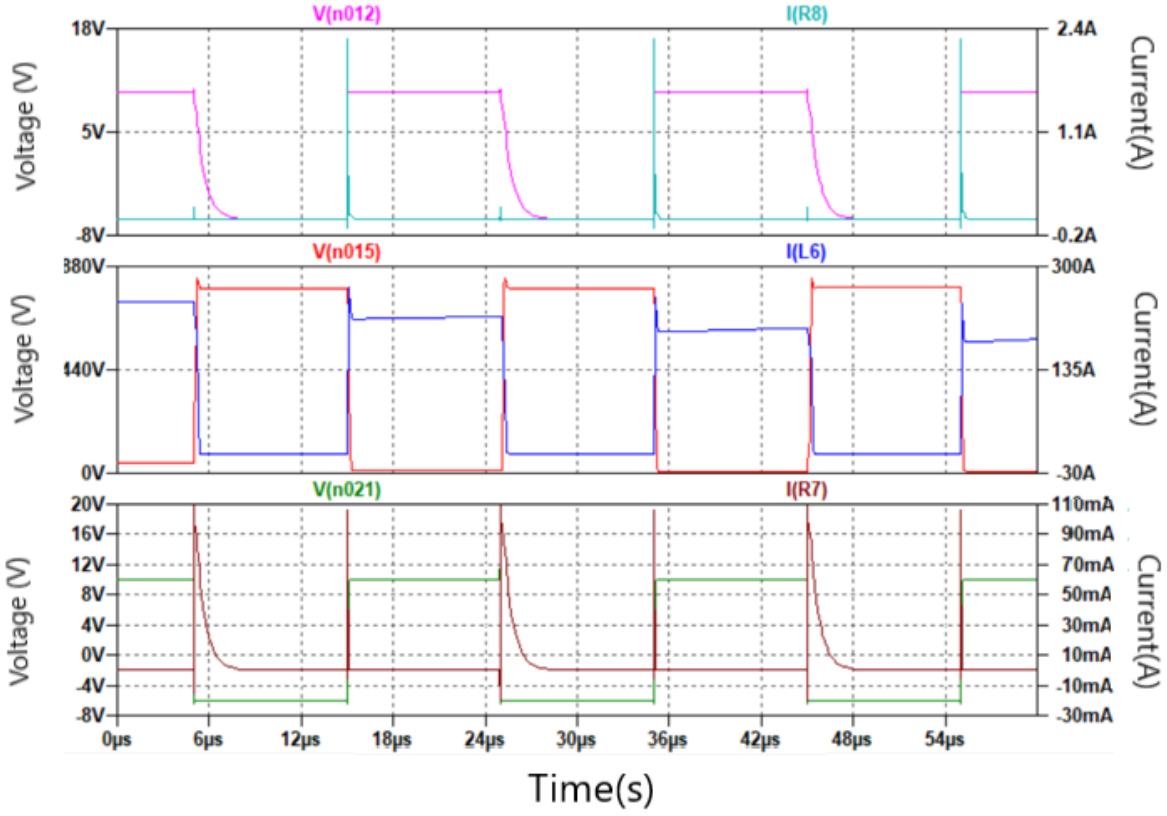



**Figure 3.5:** Driver MOSFET Characteristics

- V(n012) - PMOS Voltage
- I(R8) - PMOS Current
- V(n015) - Power MOSFET Voltage
- I(L6) - Power MOSFET Current
- V(n021) - NMOS voltage
- I(R7) - NMOS Current

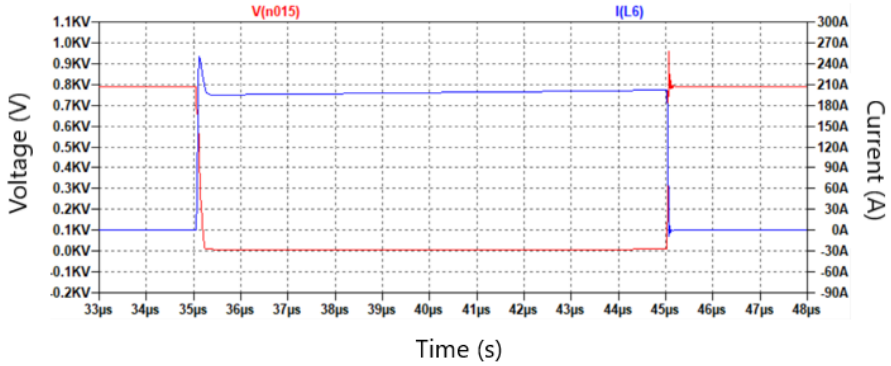



**Figure 3.6:** Power MOSFET Characteristics controlled by active gate driver

Figure 3.6 illustrates power MOSFET characteristics, which are governed by the gate resistance of the driver MOSFET [24]. The figure displays voltage and current

for one complete cycle. From 34$\mu$s to 36$\mu$s, the turn-off phase is evident as the MOSFET stops conducting, causing the current to decrease to zero. Then, between 44$\mu$s and 46$\mu$s, the turn-on phase is shown. During this phase, the switches begin to conduct again, leading to an increase in current.

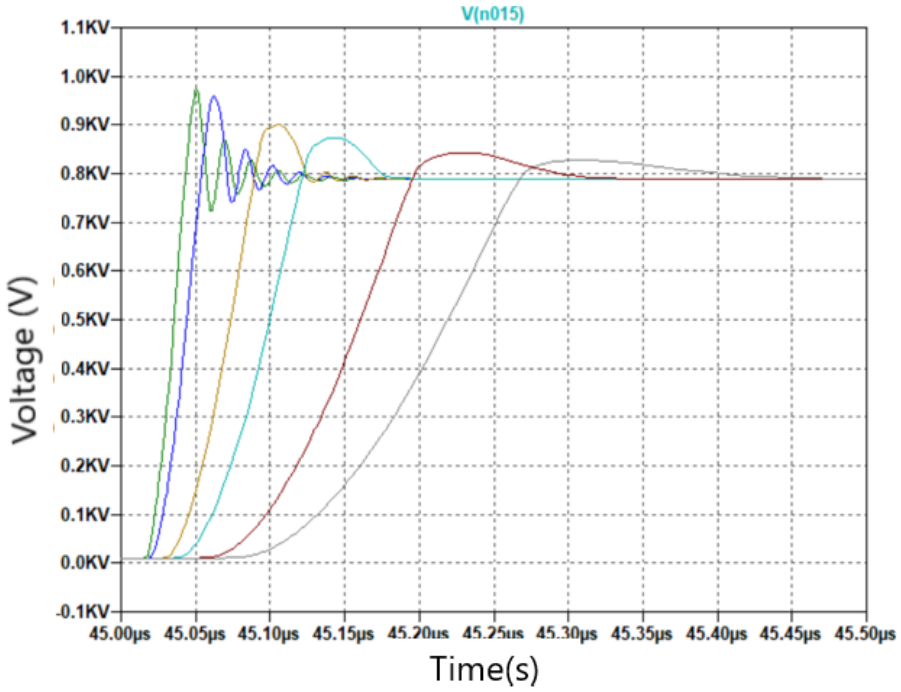



**Figure 3.7:** power MOSFET voltage at different resistances during turn-off

In Figure 3.7, the turn-off characteristics of the power MOSFET are displayed. The graph illustrates turn-off voltage at various gate resistances, ranging from 5 Ω (green) to 100 Ω (violet) [42], [41]. It's noticeable that with lower gate resistance, the ringing and peak voltage are higher. To minimise ringing, a higher gate resistance is needed, but this comes at the expense of reducing the MOSFET slew rate [28].

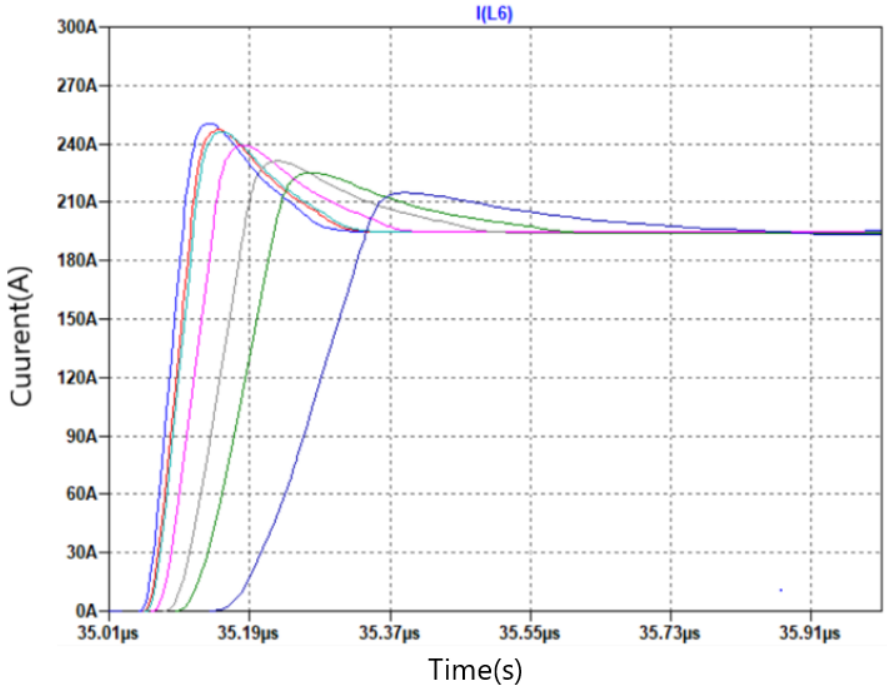



**Figure 3.8:** power MOSFET Current at different resistances during turn-on

Figure 3.8 displays the turn-on characteristics of the power MOSFET. The graph illustrates turn-on current for various gate resistances, ranging from 0.2 Ω (violet) to 15 Ω (blue). Notably, lower gate resistance leads to ringing and high peak current [26], [43]. To alleviate ringing, a higher gate resistance is necessary, although this diminishes the MOSFET slew rate. Given that turn-on involves overshoots related to voltage, low gate resistance values are employed to uphold a high slew rate.

### 3.3.1 Selection of resistance values

The choice of resistances stems from extensive test simulations, evaluating the impact on ringing and peak voltage through diverse parametric studies with varying resistance values. At 100 Ω , the voltage matches the power MOSFET's nominal voltage. However, the peak slew rate is highest at 5 Ω . This is because higher resistance leads to slower slew rates, ultimately impacting efficiency negatively.

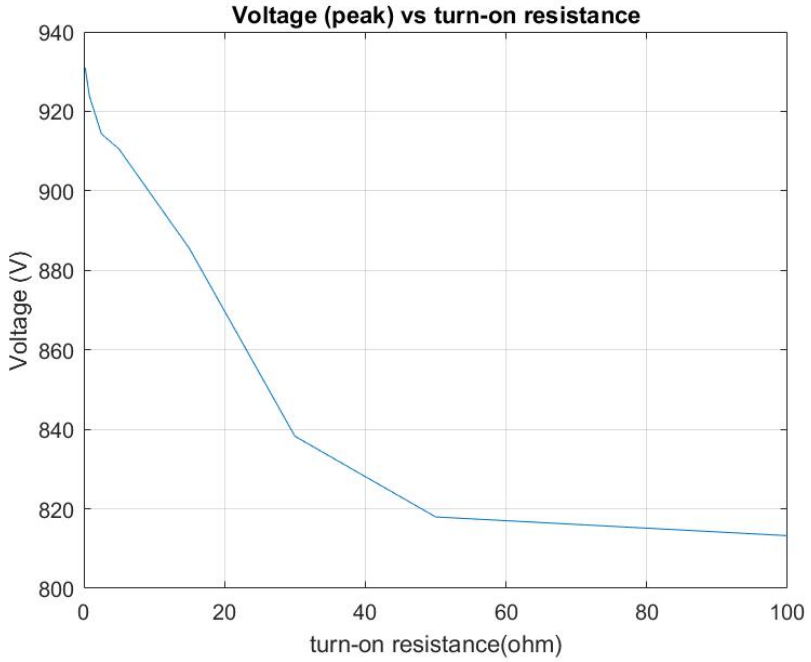



**Figure 3.9:** Peak voltage Vs Resistance

Figure 3.9 is plotted for the turn-off side of power MOSFET which needs to be reduced, as the overshoot caused due to EMI is the turn-off side [28].

### 3.3.2 MOSFET behaviour and characteristics

The MOSFET's behaviour and its switching characteristics are analysed by varying the gate resistance across a wide range until the voltage overshoot diminishes to the level required for powering the power MOSFET. The operation of the gate driver is determined by the amount of current injected into the driver. The slew-rate undergoes changes depending on the gate resistance of the power MOSFET.

**Table 3.1:** MOSFET parameters

| Power MOSFET turn-on switching characteristics | | |
|---|---|---|
| Resistance combination (Ω) | Turn on slew-rate (kv/$\mu$s) | Turn-off slew-rate (kv/$\mu$s) |
| 0.2 | 4.48611 | 3.59515 |
| 0.8 | 4.19615 | 3.59515 |
| 1 | 3.92194 | 3.59515 |
| 2.5 | 3.77355 | 3.59515 |
| 5 | 3.35078 | 3.59515 |
| 10 | 2.65078 | 3.59515 |
| 15 | 2.07154 | 3.59515 |

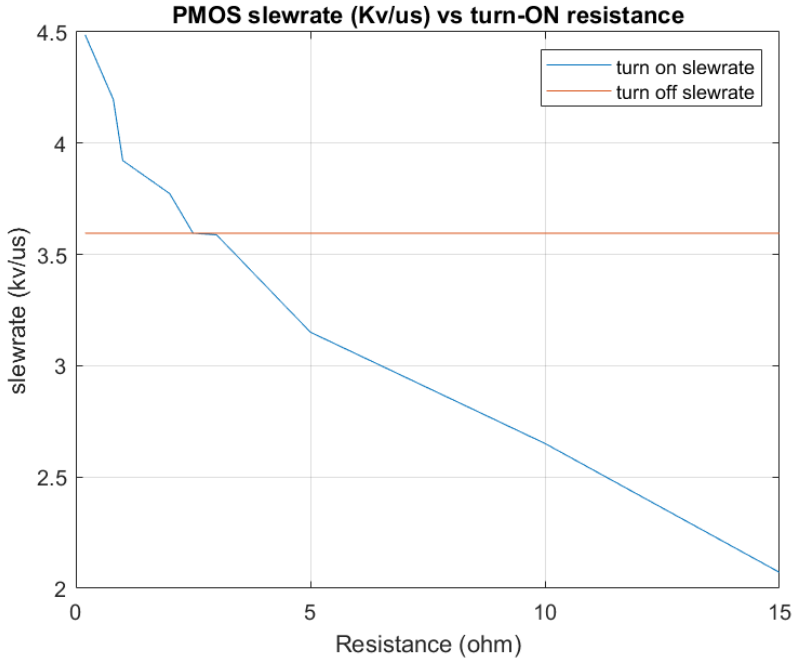



**Figure 3.10:** turn-on Slew-rate Vs Resistance

In Figure 3.10, the graph illustrates the variation in slew rate concerning the gate resistance. Since the overshoot occurs during the turn-off phase of the power MOSFET, which is governed by the N-type driver MOSFET [24]. the P-type MOSFET in the driver circuit is not controlled for managing the ringing resulting from inductive loads at turn-on side. Instead, it is used to regulate the slew rate that minimises overall losses.

**Table 3.2:** Power MOSFET parameters

| Power MOSFET turn-off switching characteristics | | |
|---|---|---|
| Resistance combination (Ω) | turn-off slew-rate (kv/$\mu$s) | turn-on slew-rate (kv/$\mu$s) |
| 0.2 | 39.312 | 14.4191 |
| 0.8 | 35.7269 | 14.4191 |
| 2.5 | 28.6549 | 14.4191 |
| 5 | 23.1995 | 14.4191 |
| 10 | 14.4191 | 14.4191 |
| 30 | 6.66498 | 14.4191 |
| 50 | 3.18498 | 14.4191 |
| 100 | 1.15437 | 14.4191 |

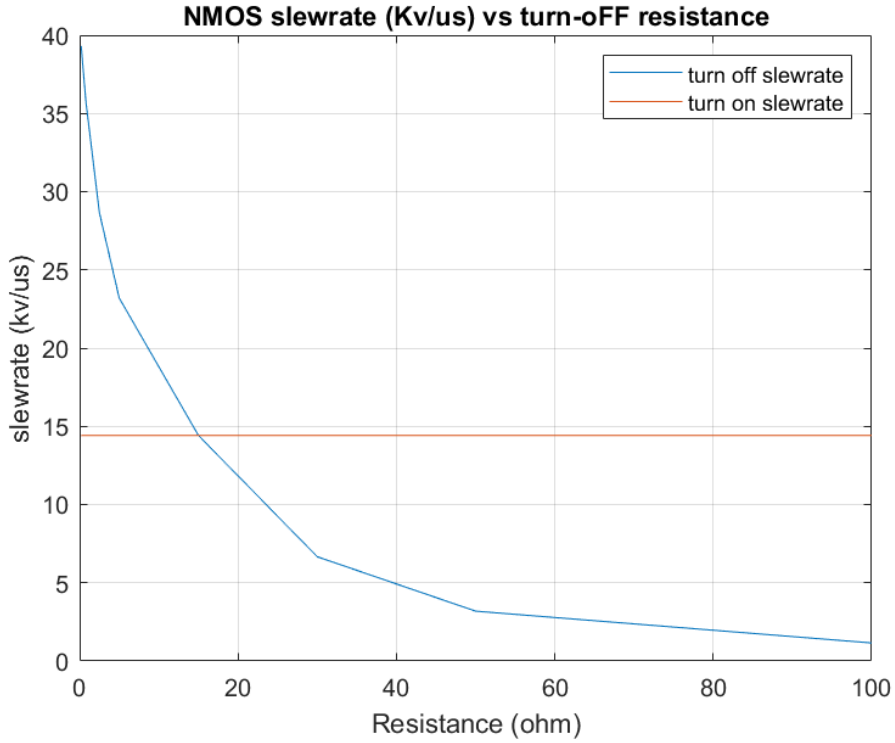



**Figure 3.11:** turn-off Slew-rate Vs Resistance

In Figure 3.11 above, a clear pattern emerges: as gate resistance rises, there is a consistent decrease in slew rate. This trend highlights the fundamental relation between slew rate and gate resistance. Increasing resistance offers a potential solution to mitigate the high-voltage ringing caused due to inductive loads. However, this approach comes at the cost of reduced switching speed and slew rate, subsequently amplifying overall switch losses [26], [28].

## 3.4 Powerloss evaluation method for power MOSFET

Understanding and managing power losses in MOSFETs are critical for enhancing the efficiency and dependability of power electronic systems. These losses can be primarily classified into two distinct categories: switching losses and conduction losses.

- **Switching Losses**
  These emerge during transitions between the on and off states of the MOSFET. When turning on, supplying the gate charge causes charging losses. Conversely, turning it off requires removing the gate charge, leading to discharging losses. Furthermore, an overlap period occurs where voltage and current are both nonzero, contributing to 'shoot-through' losses.

Switching losses hinge on factors like the device's switching speed, gate drive characteristics and load conditions.

- **Conduction Losses**
  These materialise when the MOSFET operates in its conducting state, specifically when it is turned on and conducting current from the drain to the source. These losses predominantly stem from the finite on-state resistance ($R_{ds,on}$) of the MOSFET and the current magnitude flowing through it. Elevated conduction losses result in heightened device heating, potentially impacting the overall system efficiency and temperature stability [44].

### 3.4.1 Double Pulse Test

The double pulse test serves as an experimental technique employed to characterise the switching behaviour of power electronics devices, including MOSFETs. This method entails applying two closely spaced electrical pulses to the device under examination and subsequently measuring the resultant voltage and current waveform.

The initial pulse, referred to as the 'pre-pulse' is usually of lower amplitude. It serves to partially activate the device, establishing a conduction pathway. The subsequent pulse, known as the 'main-pulse' possesses a higher amplitude, ensuring complete activation of the device, thereby enabling the flow of current.

By analysing the voltage and current waveform produced through the double pulse test, valuable parameters of the device become discernible. These encompass critical aspects like turn-on and turn-off times, forward voltage drop, and reverse recovery time. Such parameters hold immense significance when it comes to designing and optimising power electronic systems, particularly for applications involving motor drives, renewable energy setups, and power supplies.

To better understand MOSFET behaviour, a double pulse test was simulated using LTSPICE, a widely-used circuit simulation software. This simulation provides deeper insights into how these devices perform during quick switching situations. It comprehensively helps grasp their operational dynamics, contributing to the enhancement of related applications.

Double pulse test-based switching characterisation of SiC MOSFET is hence carried out.

#### 3.4.1.1 Double pulse test setup

Figure 3.12 presents the double pulse test configuration devised to ascertain vital MOSFET characteristics crucial for gate driver design [29]. In this setup, parameters like $L_{dc}/L_{cable}$ and $L_{dcr}/L_{stray}$ symbolize the DC bus inductance. This assumes the presence of an 800V battery as the primary power source. Furthermore, Lc and

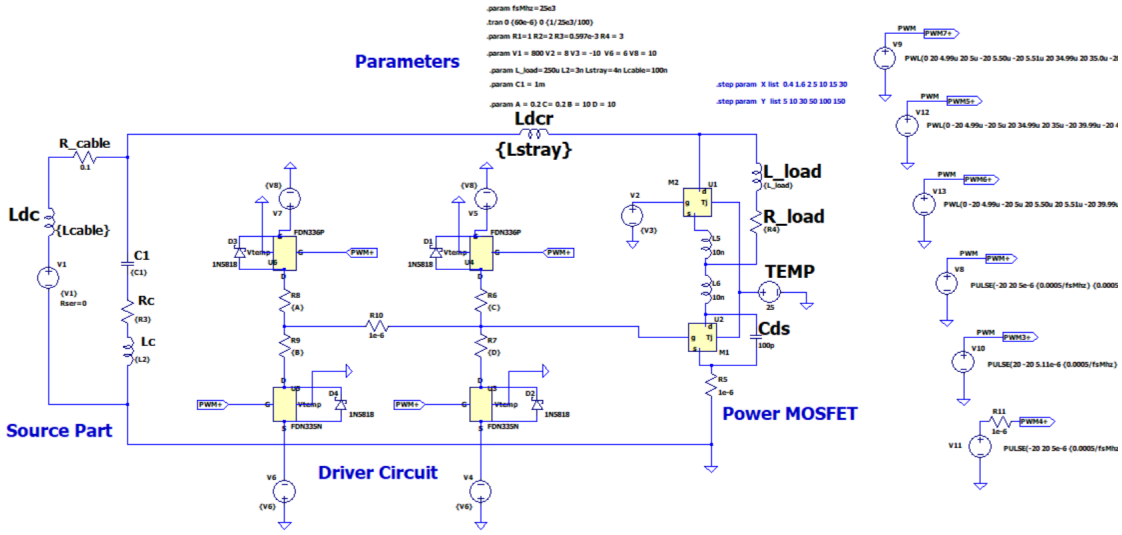



**Figure 3.12:** Double pulse test set-up in LTSPICE

Rc denote the equivalent series inductance (ESL) and equivalent series resistance (ESR), respectively, of the DC link capacitor C1.

Adding to this, L5 and L6 represent the leakage inductance inherent to the MOSFET. In this schematic, there are two MOSFETs – M1, serving as the main power MOSFET under study, and M2, utilised for its body diode to facilitate reverse recovery current management. The capacitance $C_{ds}$ signifies the drain-to-source capacitance [30], [31].

Importantly, since the power MOSFET inherently integrates a body diode, the parallel inclusion of an extra diode is unnecessary. This comprehensive design encapsulates various components that contribute to the meticulous analysis of MOSFET characteristics, essential for the refinement of gate driver design.

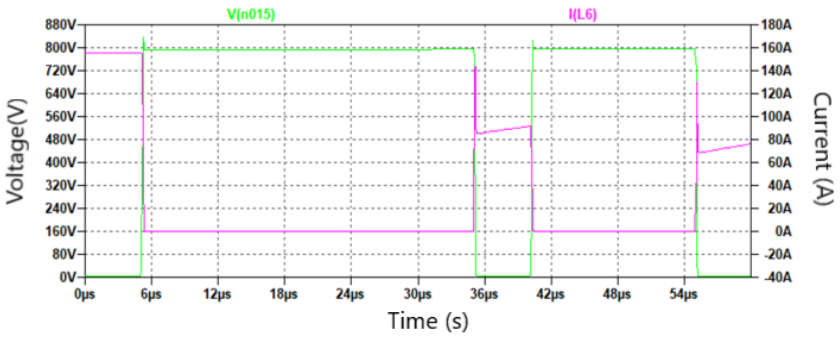



**Figure 3.13:** Double pulse test switching characteristics of power MOSFET

As previously stated, the pre-pulse is initiated at 5.5$\mu$ss, and the second pulse follows, starting from 36$\mu$ss to 42$\mu$ss. Notably, a substantial time gap exists between

the initiation of the first and second pulses. This deliberate delay serves the purpose of charging the load inductor. The second pulse holds significance as it is during this phase that the characteristics of the power MOSFET undergo analysis.

### 3.4.2 Loss distribution in power MOSFET

Switching Loss calculations have been conducted for an individual power MOSFET within the inverter setup. These losses are subsequently graphed with varying resistance values of the driver MOSFETs. These changes in the driver MOSFET's resistance directly impact the gate resistance of the power MOSFET, and hence the switching losses, and are pivotal in understanding the overall loss dynamics [33], [34].

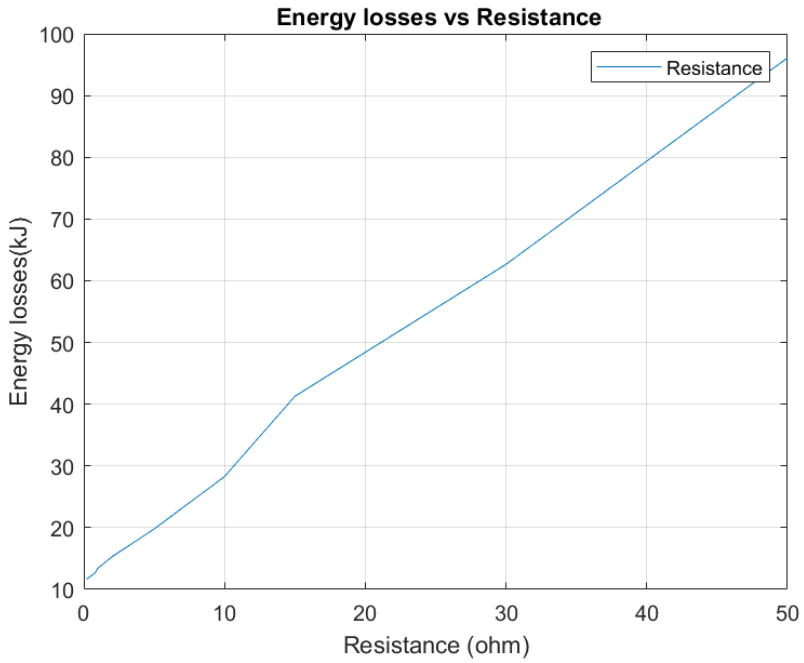



**Figure 3.14:** Turn-on energy losses(kJ) Vs turn-off resistance

Figure 3.14 shows losses at turn-on due to gate resistance. Since there were no EMI during the turn-on state of power MOSFET. A lower value of gate resistances is taken to maintain a high slew-rate, thereby reducing the losses caused due to the switching state transition of the power MOSFET [32].

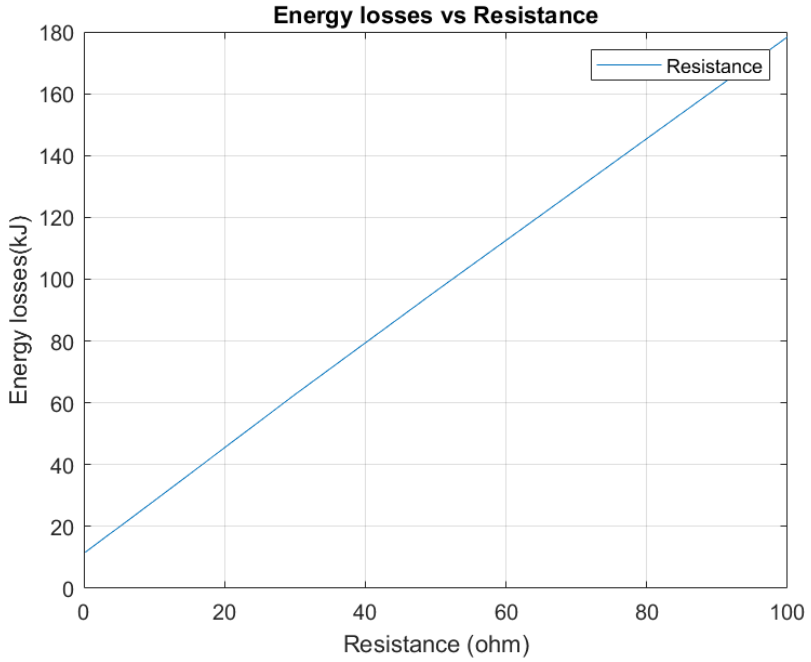



**Figure 3.15:** Turn-off energy losses(kJ) Vs turn-off resistance

Figure 3.15 shows losses at turn-off due to different gate resistances. At the turn-off side of power MOSFET, where the high voltage ringing is visualised and to reduce it, a higher gate resistance value is needed. Since at 100Ω, the peak voltage at turn-off is equal to the required nominal voltage of 800V.

The energy is plotted in KJ instead of Watts because the simulation set-up is for a double pulse test through which we can determine the exact behaviour of power, but the PWM signal is not used here for a double pulse test where there is no frequency interference, we can only determine energy values in kilo - joules (KJ).

## 3.5 FFT analysis for power MOSFET

Frequency domain analysis has been employed to examine the non-linear behaviour of the power MOSFET across diverse frequencies. Through Fast Fourier Transform (FFT) analysis, the slew-rate can be approximated and verified. Theoretically, the switching frequency should be ten times smaller than the sampling frequency; however, in our case, we conduct FFT analysis up to 100 times, thus encompassing a frequency range from 250 MHz to 3 GHz [38].

To comprehensively assess the impact of each driver MOSFET on the power MOSFET, a series of simulations has been conducted. These simulations explore the behaviour of each driver MOSFET within the frequency domain. This extensive analysis provides a comprehensive understanding of their performance across a wide frequency spectrum.

### 3.5.1 FFT analysis of Driver Mosfet

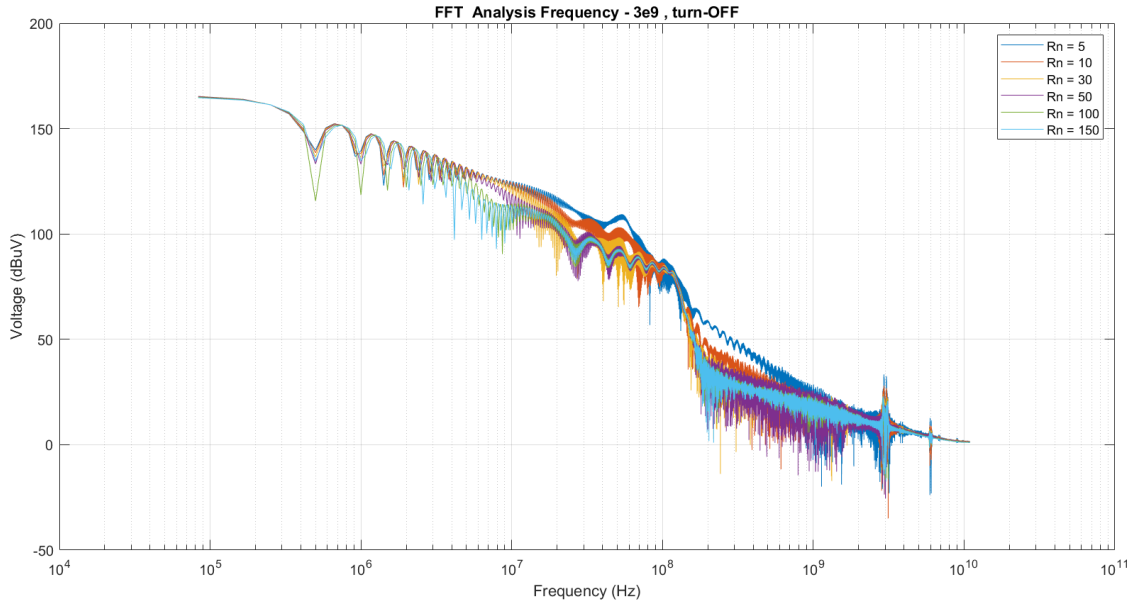



**Figure 3.16:** FFT analysis voltage at turn-off Vs Resistance

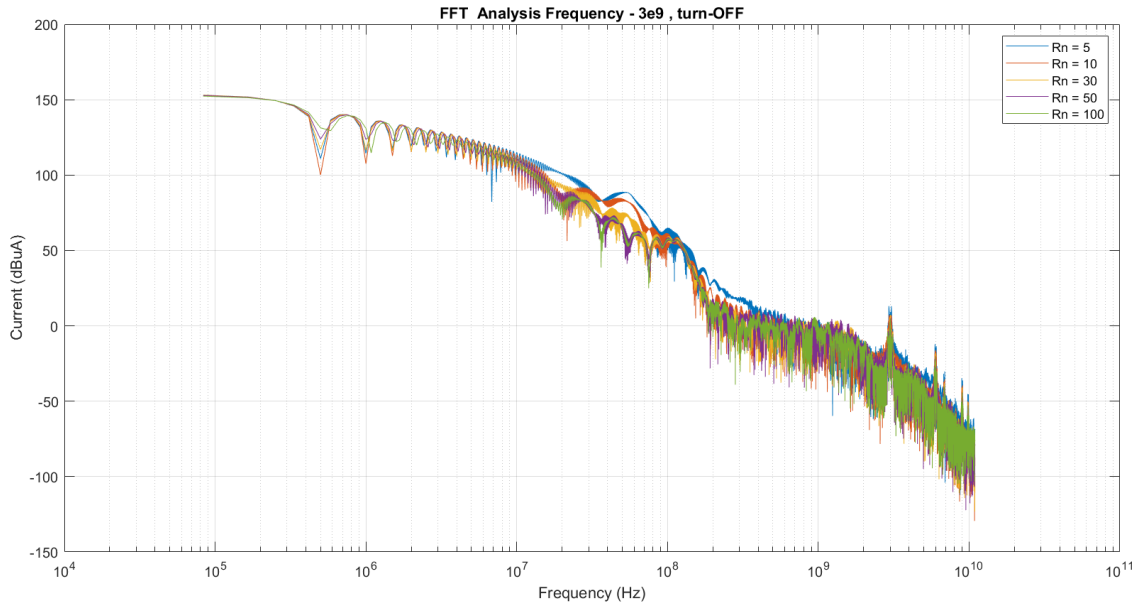



**Figure 3.17:** FFT analysis Current at turn-off Vs Resistance

Figure 3.15 and Figure 3.16 present frequency-vs-voltage and frequency-vs-current characteristics, respectively, during the turn-off phase of the power MOSFET. No-

tably, as resistance increases, the slew rate experiences a reduction. Given that the switching frequency stands around 25 kHz, with an observed sampling frequency of 3 GHz, the significant slew rate behaviour can be discerned at 300 MHz. This frequency range allows for a more insightful analysis of the observed characteristics.

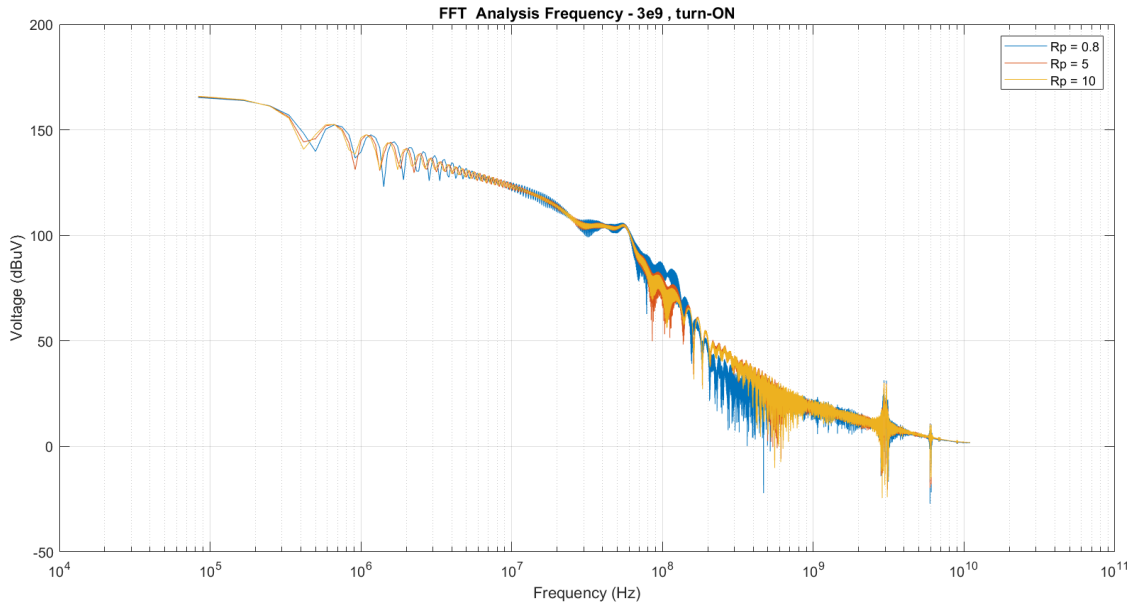



**Figure 3.18:** FFT analysis voltage at turn-on Vs Resistance

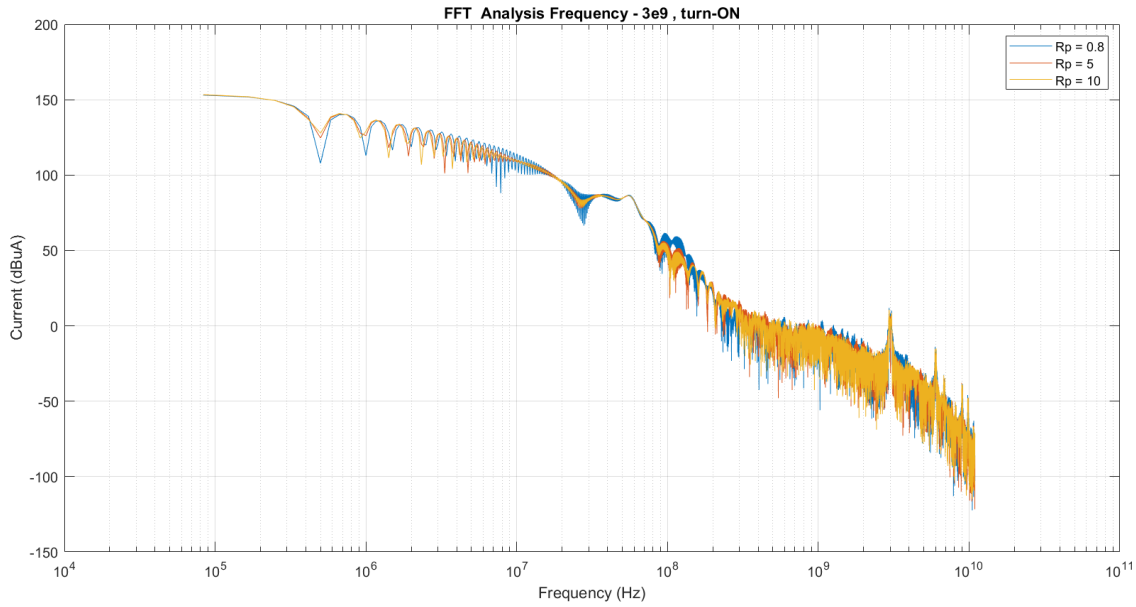



**Figure 3.19:** FFT analysis Current at turn-on Vs Resistance

Figure 3.17 and Figure 3.18 illustrate the frequency-vs-voltage and frequency-vs-

current profiles, respectively, during the turn-on phase of the power MOSFET. It is evident that the slew rate decreases with higher resistance values. Given a switching frequency of approximately 25 kHz and an observed sampling frequency of 3 GHz, the nuanced slew-rate behaviour becomes discernible around 300 MHz. This specific frequency range offers an enhanced understanding of the observed characteristics.

The slew rate denotes the rate at which the output voltage changes during the switching process. In the frequency domain, this parameter can be estimated by identifying the highest frequency component. For instance, during turn-on, the maximum voltage amplitude registers at 150 dBuV, while on the turn-off side, this peak amplitude reaches 170 dBuV. Notably, a higher resistance combined with elevated frequency results in a slower slew rate, while the opposite, lower resistance and frequency, leads to a higher slew rate.

To achieve lower total harmonic distortion (THD), a faster slew rate is attainable at lower resistance and frequency configurations. To assess this, various resistance values are sampled at a 3 GHz frequency, based on the standards ISO 16750-2 30 Mhz, is the maximum frequency EMI can be visualised. This frequency domain analysis is particularly instrumental in fine-tuning the modulation index. As a recommendation drawn from these frequency-based insights, operating the inverter at a higher frequency is advised, considering the cumulative findings from the aforementioned frequency observations.

## 3.6 Multilevel Slew-rate control of gate driver

### 3.6.1 Single level pulse generation for gate driver control

The gate driver is controlled by PWM technique, the generated pulse triggers the driver MOSFETs to control the gate resistance of power MOSFET, the gate driver is designed as 2 bridges with each is controlled by a PMOS and NMOS, when the voltage is negative it triggers the PMOS and when the pulse is positive it triggers the NMOS [39].

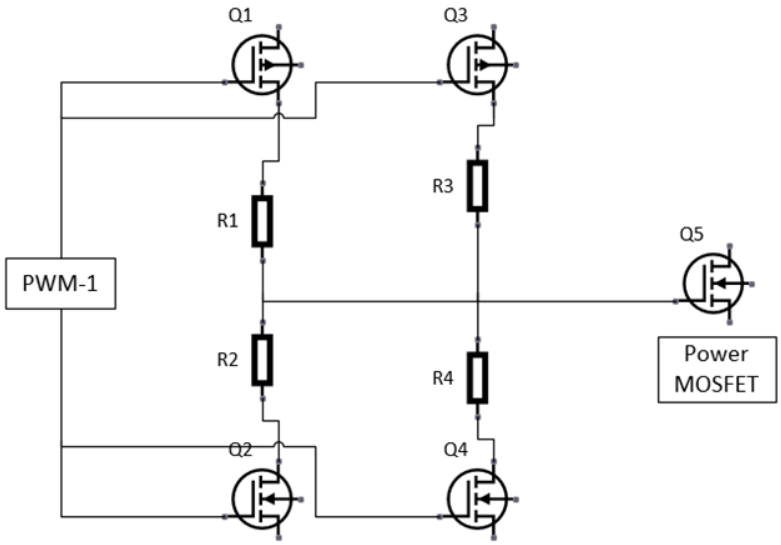



**Figure 3.20:** Driver with advanced gate pulses

In the figure 3.19 Q1 & Q3 are PMOS triggered at -negative pulse voltage, Q2 & Q4 are NMOS triggered at positive pulse voltage, Q5 represents power MOSFETS.

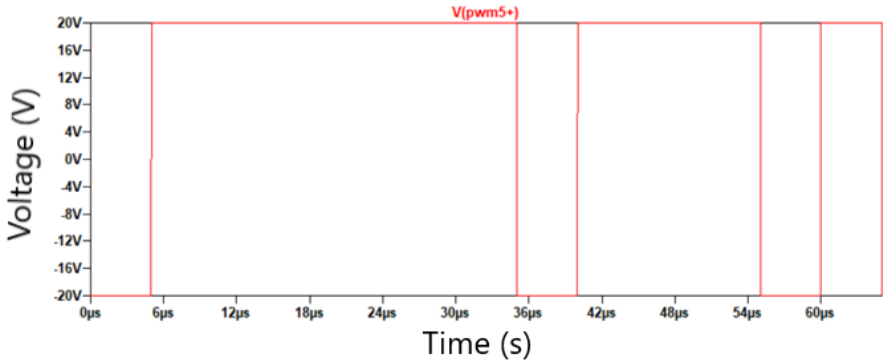



**Figure 3.21:** PWM pulses for different gate bridges

### 3.6.2 Multilevel gate pulse generation

The multi level gate pulse generation designed by independently controlling the 2nd bridge, the driver MOSFETs are triggered by 2 different PWM pulses in the 2nd bridge, the idea is to inject extra current exactly during turn-on and turn-off of power MOSFET thereby reducing the switching stresses and reducing the switching losses[39].

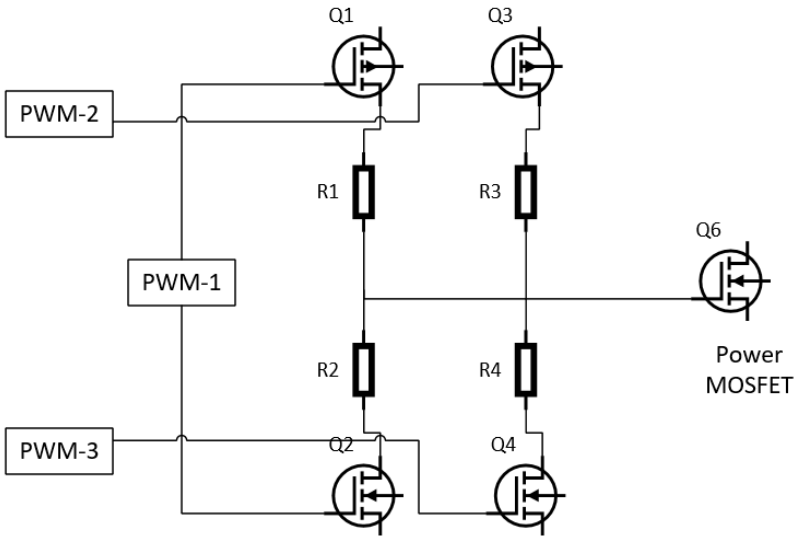



**Figure 3.22:** Driver with advanced gate pulses

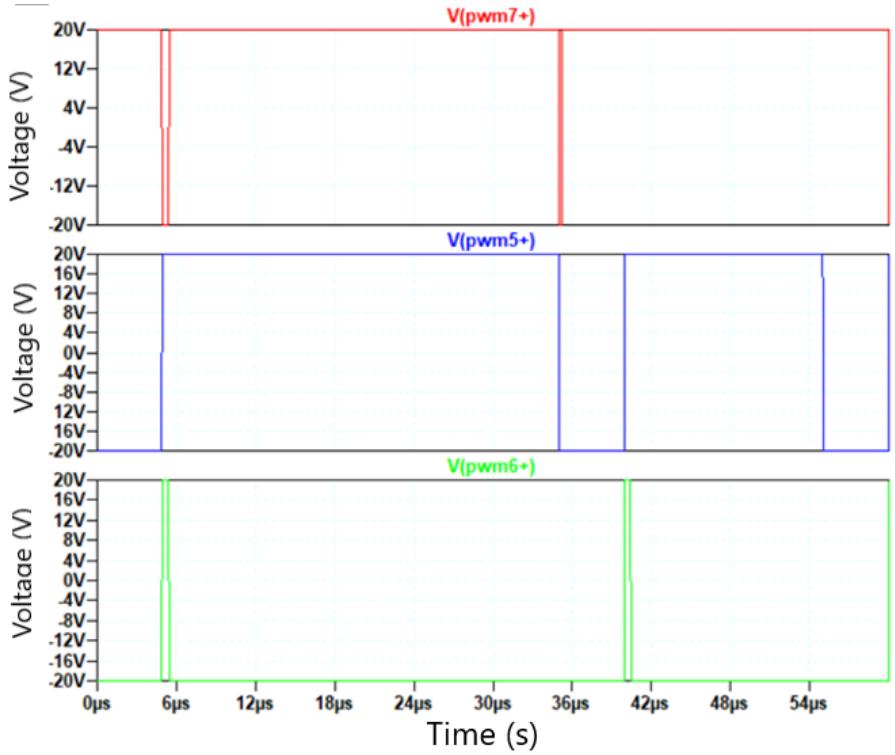



**Figure 3.23:** Single PWM pulse gate generation

The figure.3.23 the multi-level pulse generation, V(PWM5+) is original PWM pulse generated for the 1st bridge, the V(PWM6+) & V(PWM7+) are the 2 different gate pulses injected exactly during turn-on and Turn-off of the advanced control of gate pulses and Driver MOSFET behaviour is observed :

- the Voltage V(PWM5+) is the gate pulse for the 1st bridge

- the voltage V(PWM6+),V(PWM7+) are pulses for 2nd bridge for accurate control of gate resistance.
- In the graph figure.3.20 from 32us to 42us V(PWM7+) controls PMOS and V(PWM6+) controls the gate resistance of NMOS.

### 3.6.3 Power MOSFETs characteristics with and without multilevel pulse generation

The purpose of multi level pulse generation is to reduce the overall power-loss, the losses are due to high ringing voltages, to reduces the ringing voltages, an extra currents is injected at turn-on and turn-off of power MOSFET by dynamically controlling the driver bridges by triggering 3 different PWM pulses [40].

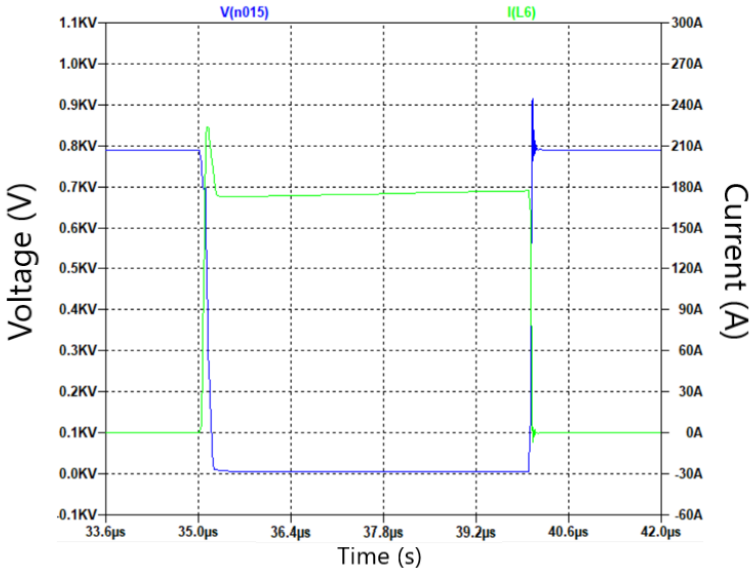



**Figure 3.24:** power MOSFET characteristics due to single level pulse generation

The figure 3.24 shows MOSFET characteristics for single pulse generation, the gate resistance is set at 10 Ω where high ringing is expected the peak voltage is at 900V at turn-off and current 210A at which is very high current at turn-on.

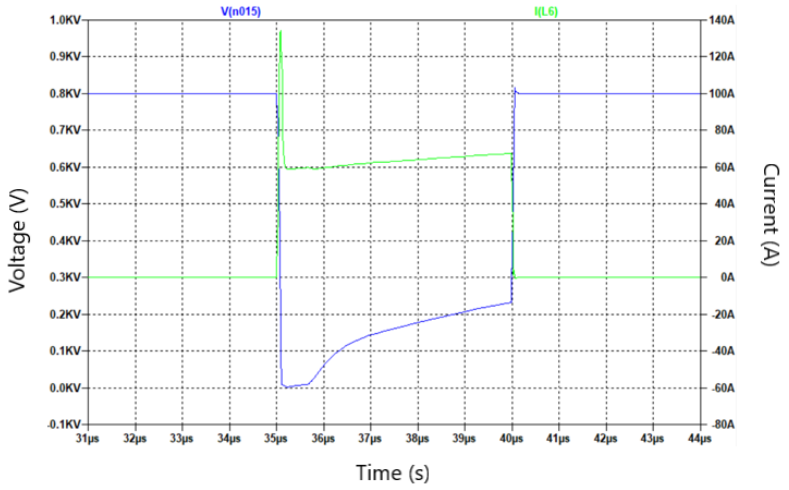



**Figure 3.25:** power MOSFET characteristics due to Multi level pulse generation

The figure 3.25 shows MOSFET characteristics for multi pulse generation, the total gate resistance is set at 10Ω where high ringing is expected but with multi level pulses the ringing voltage at turn-off is highly reduced as compared to figure 3.23, the peak voltage is at 810V at turn-off and the peak has reduced to current 140A at which is very high current at turn-on.

Based on the observation from figure 3.24 & figure 3.25 for the gate resistance at 10Ω, the peak voltage is reduced from 900V to 810V therefore the ringing is also reduced without changing the slew-rate, as well the peak current at turn-on has been reduced from 210A to 140A.

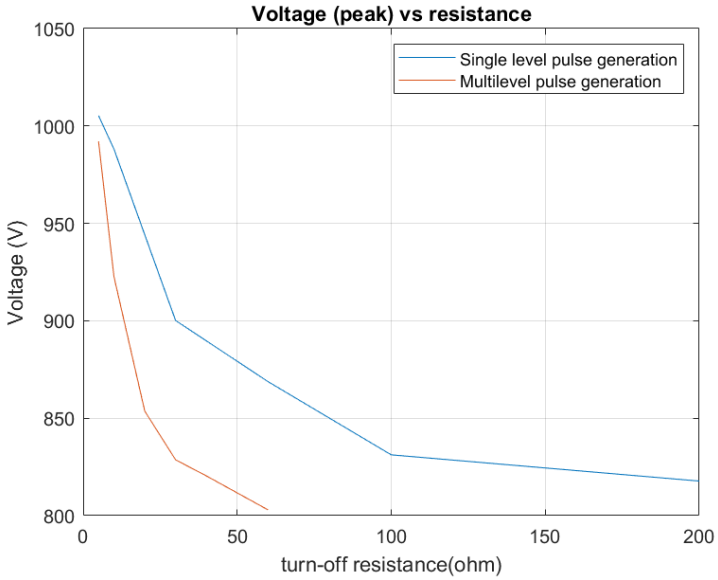



**Figure 3.26:** Comparison of peak voltage at turn-off gate resistance with single and multi level pulse modulation

The figure 3.26 shows comparison between single pulse and multilevel pulse generation at different gate resistances, the peak voltage reduces as the gate resistance increases thereby slew-rate decreases but to reach the required nominal voltage of 800V, the resistance values required to decrease the peak voltage is less when multilevel pulse generation is used, i.e. 50Ω but for single pulse generation the required resistance value is higher i.e. 150Ω, therefore we achieve better slew-rate by keeping the gate resistance value to minimum by using multilevel pulse generation.

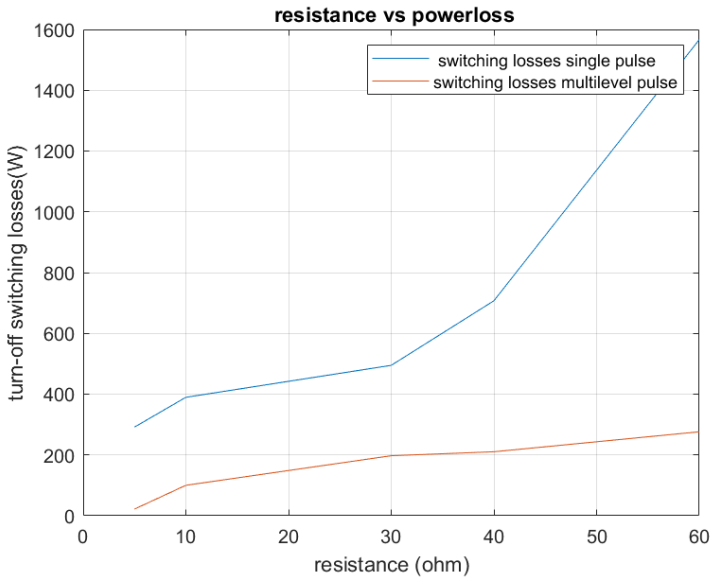



**Figure 3.27:** Comparison of switching losses at turn-off of power MOSFET at different gate resistance with single and multi level pulse modulation

The figure 3.27 shows comparison switching losses between single pulse generation and multi-level pulse generation technique, as it is observed switching losses have significantly reduced when multilevel pulse generation is used compared to single pulse generation.

# 4

# MOSFET Characteristics

This chapter addresses the modeling of switching and conduction losses, previously discussed in Chapter section 3.3. Given the involvement of two distinct software tools in the design process, LTSPICE is utilized to simulate the gate driver for a specific MOSFET within a Multilevel Inverter, while PLECS is employed for comprehensive simulation of the entire three-phase Multilevel Inverter.

Diverse modeling approaches are essential due to varying requirements. Specifically, SPICE modeling is crucial for capturing the effect of overshoot voltages at the power MOSFET's turn-on side, a prominent source of Electromagnetic Interference (EMI). In contrast, PLECS excels in defining control and modulation techniques pivotal for the multi-level Inverter's holistic modeling.

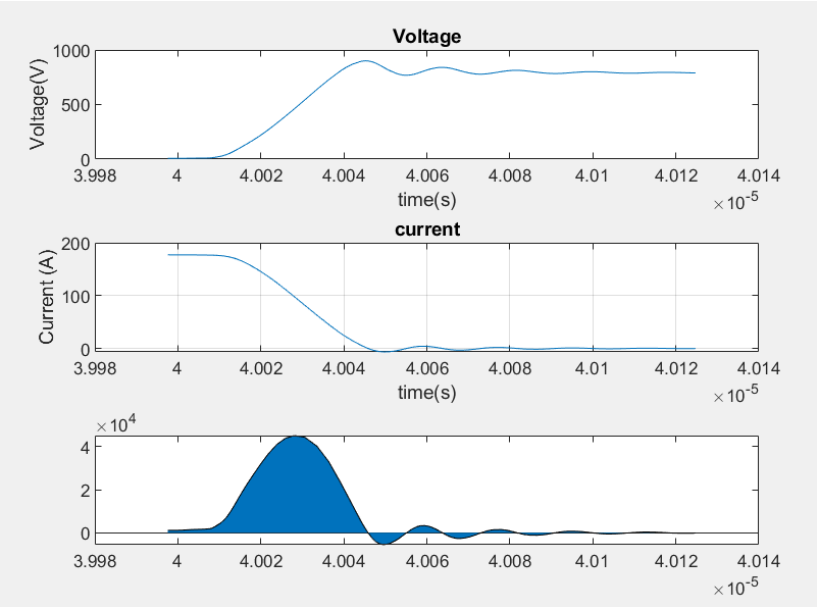
In PLECS, the power MOSFET switch models are pre-defined by the manufacturer and are independent of the overshoot voltage dynamics. Consequently, this prompts the redefinition of MOSFET characteristics in PLECS, considering overshoot voltages. The MOSFET's behavior is analyzed across different gate resistances and load conditions.

Overshoot models are categorized into three distinct cases: High overshoot, moderate overshoot, and low overshoot voltages. The extent of overshoot hinges on gate resistance adjustments, where modifications in the gate resistance induce changes in turn-on peak voltage. To assess its impact, evaluations are conducted at varying current levels and load resistances.

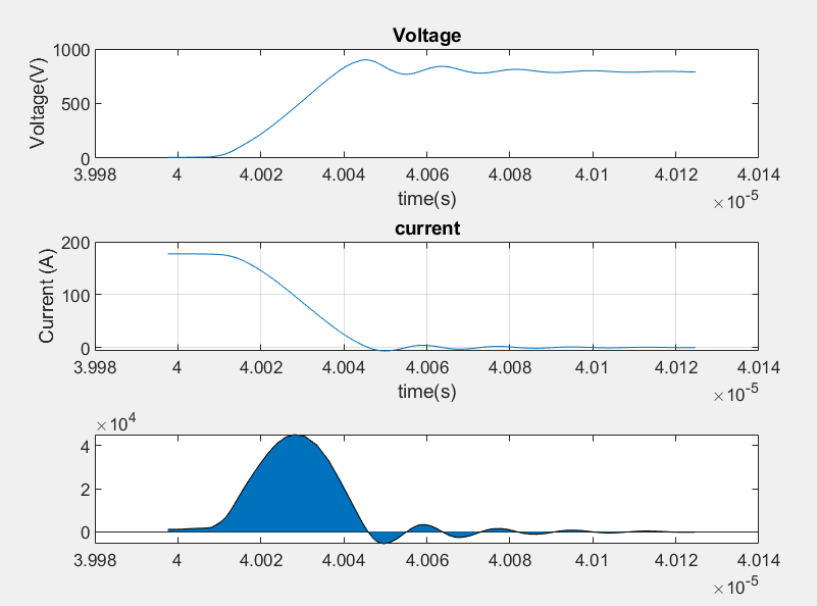
## 4.1 Test Simulation Set-up for Power MOSFET Characteristics

The characterisation of power MOSFET characteristics is achieved through Double Pulse Testing[29],[30]. figure3.11 illustrates the circuit configuration employed in LTSPICE for simulating the test and analyzing characteristics such as voltage and current. Section 3.3 elaborates on the functionality of the Double Pulse Test circuit and its operational principle.
To quantify the switching power losses originating from the power MOSFET, the product of voltage and current at the switching frequency is calculated. However, due to the utilisation of the Double Pulse Test, the need to consider the switching

frequency in loss calculation is negated. This is attributed to the user-defined nature of the PWM pulse, enabling losses to be calculated and modelled based on energy measured in milli-joules (mJ)[33].



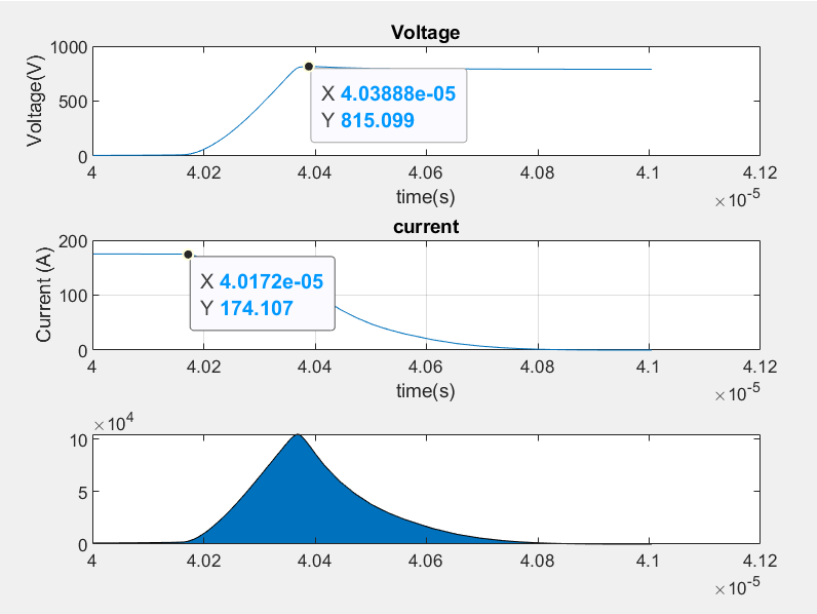

**(a)** power MOSFET turn off area under curve in joules



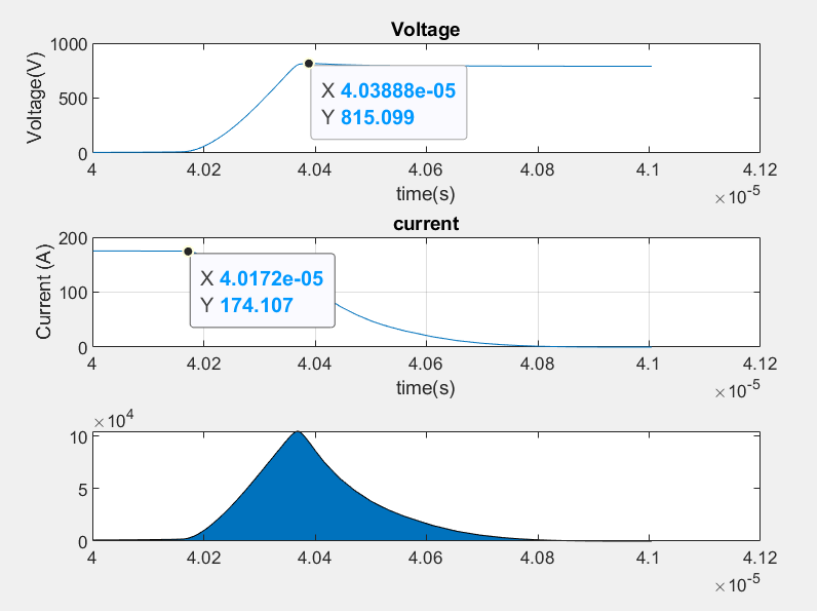

**(b)** power MOSFET turn on area under curve in joules

**Figure 4.1:** power MOSFET under maximum overshoot

Figure. 4.1 are processed data from LTSPICE, there are three plots for each turn-on and turn-on, 3rd graph shows the corresponding energy values. high overshoot voltage is observed in the turn-on region, which may cause high EMI, the gate resistance is set to 5.2 Ω, as the PMOS is set for 0.2Ω and NMOS is set to 5Ω, the resistance selection is based on the slew-rate with high switching transients.



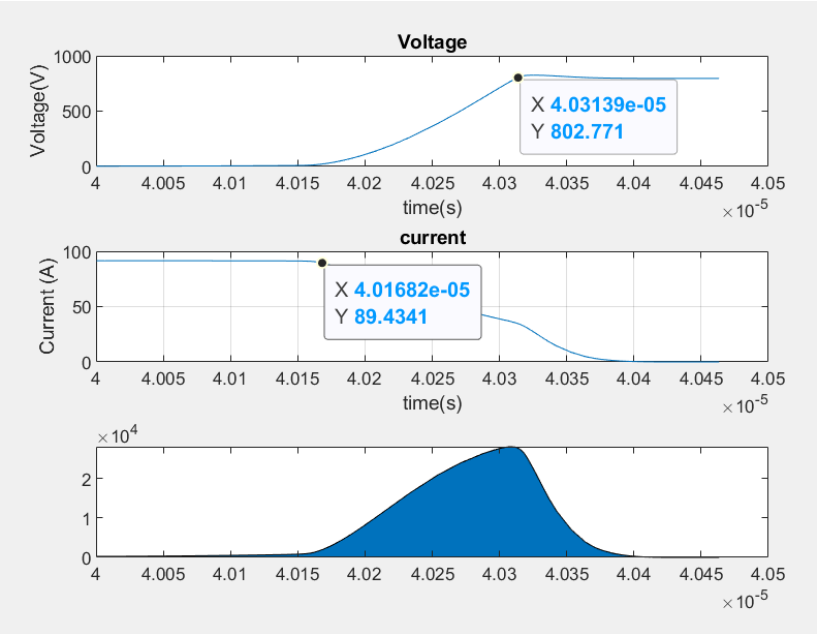

**(a)** power MOSFET turn off area under the curve in joules



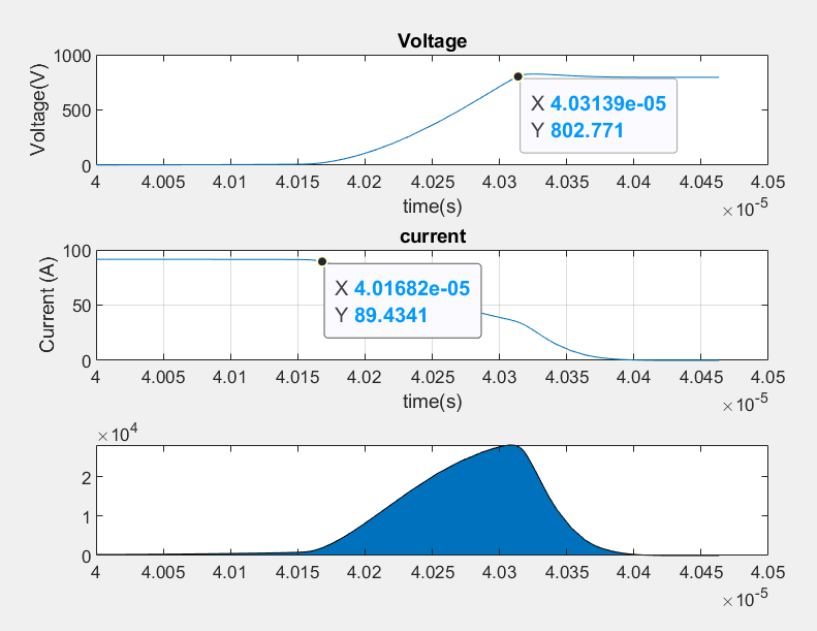

**(b)** power MOSFET turn on area under the curve in joules

**Figure 4.2:** power MOSFET under moderate overshoot

Figure 4.2 shows processed data from LTSPICE, there are three plots for each turn-on and turn-on, 3rd graph shows the corresponding energy values. It is hard to observe the high overshoot voltage since it has decreased from 920V to 815V for the moderate EMI case. The total gate resistance is set to 30Ω. the PMOS is set for 5Ω and NMOS is set to 25Ω. the resistance selection has been decreased which reduced the switching rate during tun-on of power MOSFET.




**(a)** power MOSFET turn-off the area under the curve in joules




**(b)** power MOSFET turn-on area under the curve in joules

**Figure 4.3:** power MOSFET under moderate overshoot

Figure. 4.3 processed data from LTSPICE, there are three plots for each turn-on and turn-off. The 3rd graph shows the corresponding energy values. A high voltage overshoot in the turn-on region is observed for the maximum overshoot. The gate resistance is set to 100Ω, as the PMOS is set for 10Ω and NMOS is set to 100Ω. At 100Ω there are no high overshoot voltages but the slew-rate is too slow compared to previous cases.

The smart way to handle it is not reducing the slew-rate of PMOS, but only focusing

on NMOS. This is the optimal way of getting the gate resistance when the switching losses in the inverter are less with a high slew-rate, and increasing the slew-rate where the switching losses are higher, thereby optimally controlling the switches, and reducing the losses as well as the EMI over any switches.

## 4.2 Switching Losses

This section deals with the process of modelling switching characteristics after studying the effect of overshoot voltage over the turn-on part of power MOSFET, there are 3 cases based on which 3 different models of switches are designed [33].

### 4.2.1 Maximum overshoot

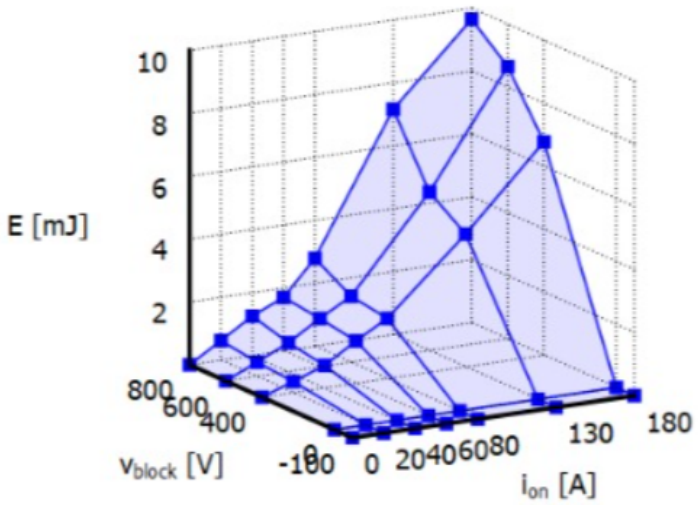



**Figure 4.4:** MOSFET characteristics maximum overshoot - turn-on

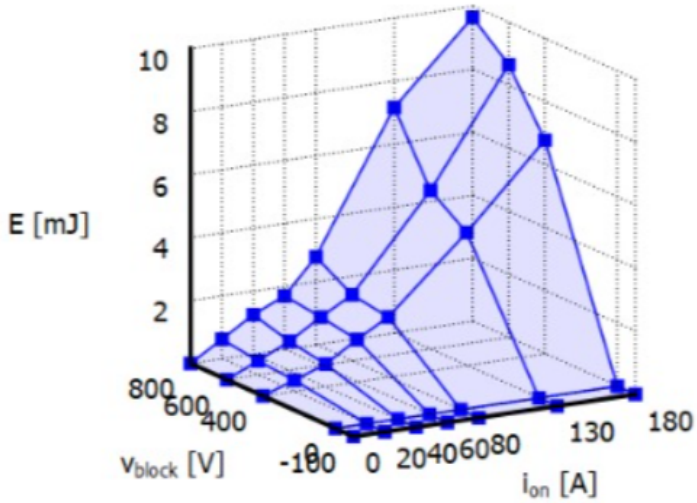



**Figure 4.5:** MOSFET characteristics Maximum overshoot - turn-off

The table above shows the corresponding values that are obtained by checking current and voltage at different loads but the gate resistance is not varied. For the case of moderate overshoot, the gate resistance is assumed to be 5Ω and 25Ω for turn-on and turn-off regions respectively. Therefore, the model has an average overshoot as well as an average slew-rate. Since the slew-rate is not very high, the efficiency decreases as compared to the maximum overshoot model.

**Table 4.1:** MOSFET Maximum overshoot model parameters for turn-on

| At 25 deg Power MOSFET characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| Current(A) | 0 | 20 | 40 | 60 | 80 | 130 | 180 |
| Voltage(V) | Energy(mJ) | | | | | | |
| -100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 400 | 0 | 2.98 | 4.48 | 6.11 | 14.81 | 36.32 | 51.62 |
| 600 | 0 | 4.96 | 7.43 | 10.21 | 17.43 | 40.63 | 61.45 |
| 800 | 0 | 10.19 | 15.29 | 20.09 | 32.82 | 46.77 | 75.44 |

**Table 4.2:** MOSFET Maximum overshoot model parameters for turn-off

| At 25 deg Power MOSFET characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| Current(A) | 0 | 20 | 40 | 60 | 80 | 130 | 180 |
| Voltage(V) | Energy(mJ) | | | | | | |
| -100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 400 | 0 | 0.35 | 0.712 | 1.343 | 1.191 | 4.22 | 6.78 |
| 600 | 0 | 0.45 | 0.92 | 1.54 | 2.1 | 5.042 | 8.66 |
| 800 | 0 | 0.62 | 1.25 | 1.7 | 2.79 | 7.16 | 9.65 |

### 4.2.2 Moderate overshoot

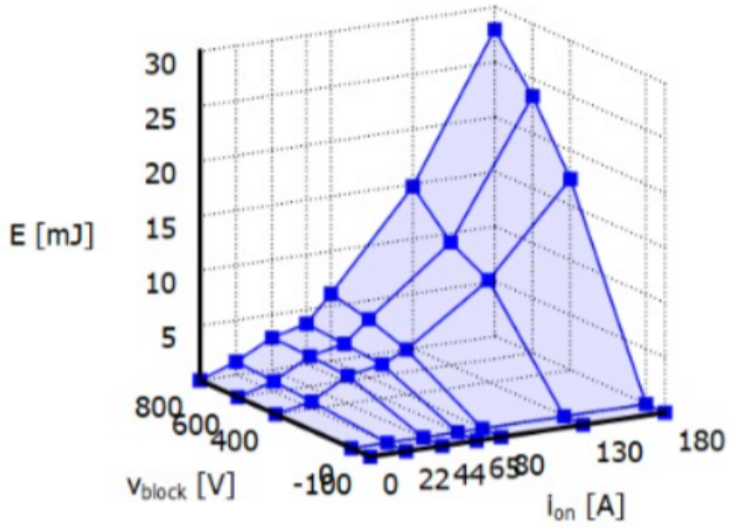



**Figure 4.6:** MOSFET characteristics Moderate EMI - turn on

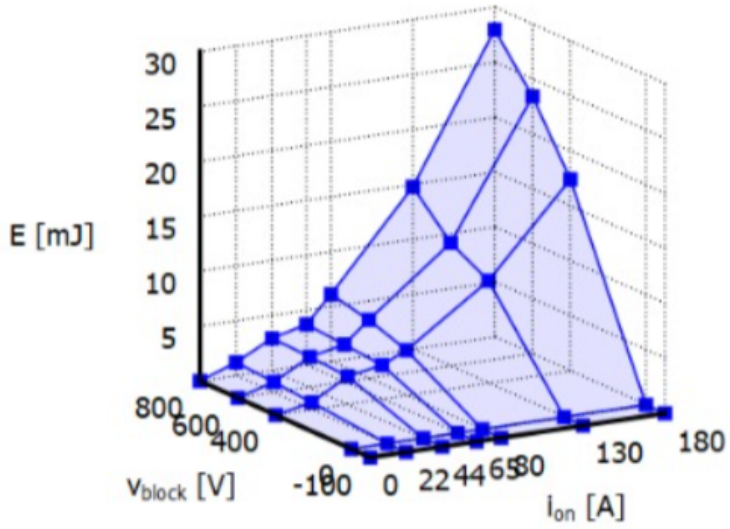



**Figure 4.7:** MOSFET characteristics Moderate EMI - turn off

In the case of high overshoot, the gate resistance is assumed to be 0.2Ω and 5Ω for turn-on and turn-off regions respectively, therefore the slew-rate is maximum. This model is expected to have a high efficiency compared to the other 2 models.

**Table 4.3:** MOSFET Moderate overshoot model parameters for turn-on

| At 25 deg Power MOSFET characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| Current(A) | 0 | 20 | 40 | 60 | 80 | 130 | 180 |
| Voltage(V) | Energy(mJ) | | | | | | |
| -100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 400 | 0 | 1.254 | 2.334 | 5.719 | 11.212 | 19.489 | 38.453 |
| 600 | 0 | 2.43 | 3.611 | 6.357 | 13.222 | 23.522 | 46.03 |
| 800 | 0 | 2.905 | 4.604 | 8.217 | 15.287 | 26.325 | 51.627 |

**Table 4.4:** MOSFET Moderate overshoot model parameters for turn-off

| At 25 deg Power MOSFET characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| Current(A) | 0 | 20 | 40 | 60 | 80 | 130 | 180 |
| Voltage(V) | Energy(mJ) | | | | | | |
| -100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 400 | 0 | 0.653 | 2.534 | 3.094 | 4.133 | 9.328 | 17.433 |
| 600 | 0 | 0.962 | 2.764 | 3.414 | 5.328 | 11.221 | 23.436 |
| 800 | 0 | 1.204 | 2.905 | 3.705 | 6.109 | 14.743 | 27.974 |

### 4.2.3 No Overshoot

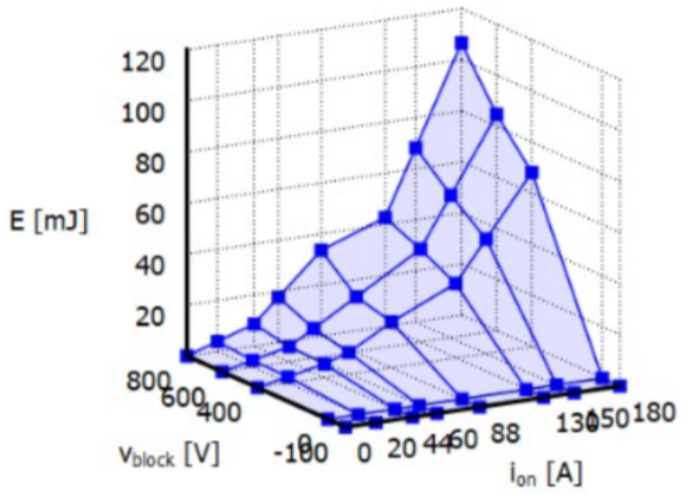



**Figure 4.8:** MOSFET characteristics NO overshoot-turn on

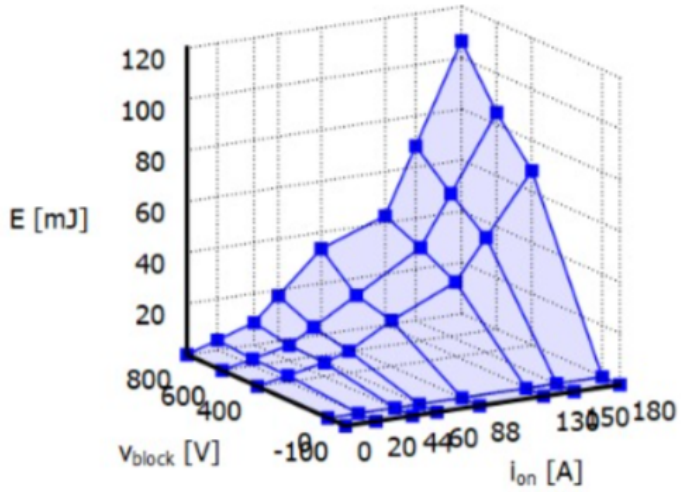



**Figure 4.9:** MOSFET characteristics NO overshoot-turn off

In this case of no overshoot, the gate resistance is assumed to be 10Ω and 100Ω for turn-on and turn-off regions respectively, therefore the slew-rate is low. This model is expected to have very low efficiency compared to the other 2 models, but since this model has no overshoot, it solves our first problem of reducing the overshoot.

**Table 4.5:** Power MOSFET No EMI model parameters for turn-on

| At 25 deg Power MOSFET characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| Current(A) | 0 | 20 | 40 | 60 | 80 | 130 | 180 |
| Voltage(V) | Energy(mJ) | | | | | | |
| -100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 400 | 0 | 7.756 | 15.505 | 25.34 | 48.5654 | 84.01 | 190.344 |
| 600 | 0 | 8.036 | 16.079 | 29.247 | 53.928 | 90.028 | 198.324 |
| 800 | 0 | 12.493 | 24.99 | 35.808 | 61.314 | 96.677 | 202.768 |

**Table 4.6:** Power MOSFET No EMI model parameters for turn-off

| At 25 deg Power MOSFET characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| Current(A) | 0 | 20 | 40 | 60 | 80 | 130 | 180 |
| Voltage(V) | Energy(mJ) | | | | | | |
| -100 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 400 | 0 | 2.422 | 5.33 | 8.391 | 17.841 | 29.166 | 68.23 |
| 600 | 0 | 2.689 | 6.916 | 11.585 | 21.505 | 36.429 | 84.775 |
| 800 | 0 | 3.909 | 8.6 | 17.682 | 33.55 | 42.65 | 106.584 |

In Table 4.1-4.6, the energy values for 0V and -100V are zero, since at 0V the switch does not conduct, at the negative voltage the body diode conducts but the MOS-

FET used in the gate driver is SIC MOSFET. the reverse recovery of SIC MOSFET has negligible losses.

## 4.3 Conduction Losses

Conduction losses occur when the switch is conducting. To obtain the conduction losses the load needs to be connected to the gate-drain. In the test setup the power MOSFET is connected in the reverse direction - the load is connected to the gate-source instead of gate-drain, to obtain the reverse conduction losses. Corresponding current values at three different source voltages i.e. 400V, 600V and 800V are noted. [44].

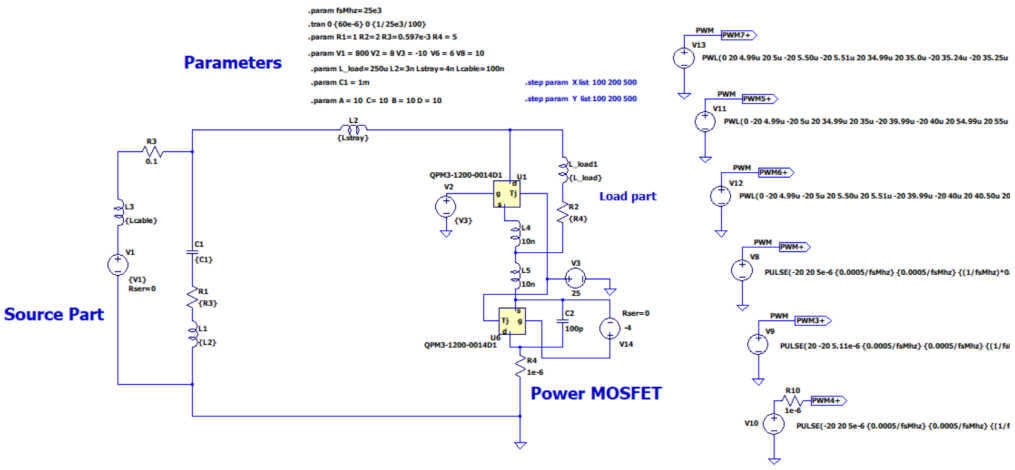



**Figure 4.10:** Conduction losses circuit set-up for the body diode (reverse conduction losses)

The conduction losses are not affected by gate driver resistance but they depend on temperature as it is expected to increase at higher temperatures. Since this study does not include simulations related to temperature, the temperature at room temperature i.e. 25 degrees is assumed.

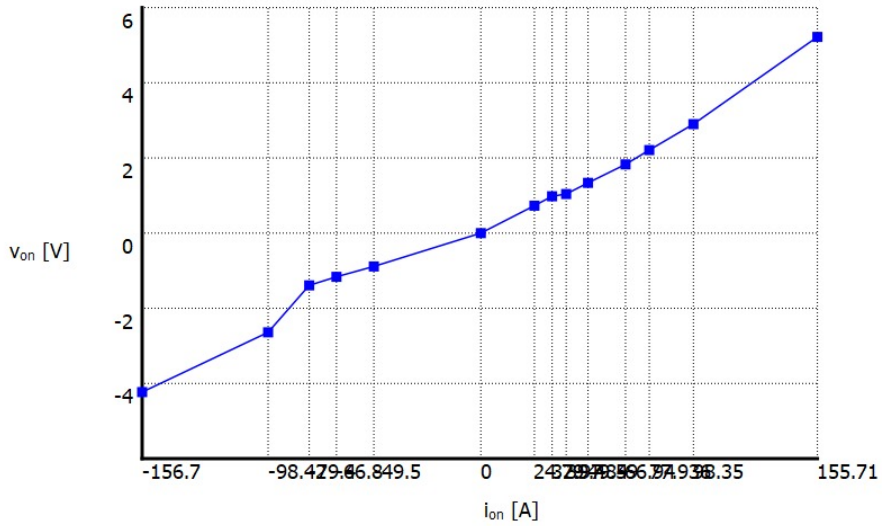



**Figure 4.11:** Conduction losses graph at 25 Degs.

**Table 4.7:** Power MOSFET Maximum overshoot model parameters for turn-on

| Power MOSFET Conduction losses at 25deg | |
|---|---|
| Voltage Drop | Current |
| -4.23 | -155.6 |
| -2.64 | -98.42 |
| -1.39 | -79.4 |
| -1.163 | -66.8 |
| -0.887 | -49.5 |
| 0 | 0 |
| 0.73 | 40.02 |
| 0.98 | 49.8 |
| 1.337 | 65.3 |
| 1.829 | 78.6 |
| 2.209 | 99.8 |
| 2.93 | 130.23 |
| 5.22 | 156.7 |

Conduction losses hold significance, even though they don't contribute to any losses when the switch is non-conducting. However, during the regenerative cycle, losses primarily arise from conduction losses. The impact of temperature is substantial on conduction losses. Figure 4.11 illustrates losses at 25 degrees Celsius, representing room temperature, given that simulation results are obtained under these conditions. This data is summarised in Table 4.7, presenting the plotted values in tabular format.

### 4.3.1 Losses due to body diode

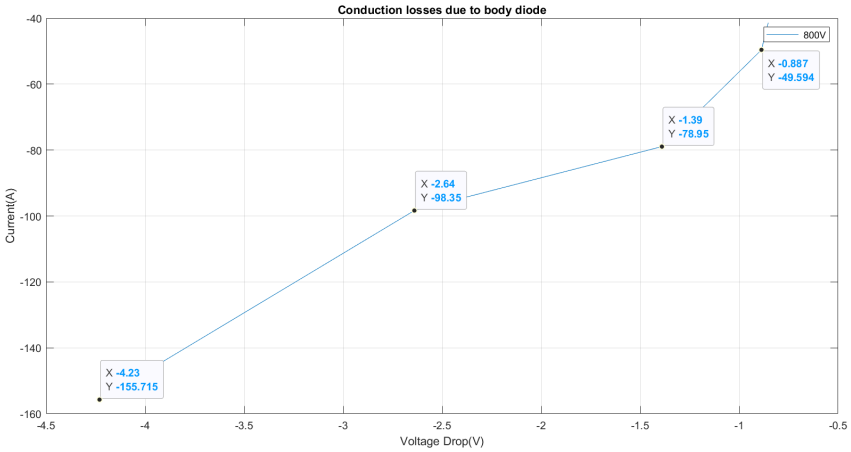



**Figure 4.12:** Body diode under negative current

Figure 4.12 depicts conduction losses arising from the diode. Conduction losses connected to the body diode in a MOSFET take place during its on-state when the diode conducts current due to reverse voltage. This phenomenon, prevalent in switching or reverse voltage scenarios, results in heightened losses compared to regular on-state conduction. The negative current, flowing in the opposing direction of normal operation, signifies the movement of electrons from drain to source [44],[45]. Simultaneously, a voltage drop emerges across the body diode, contributing to energy dissipation and losses. These losses can impede circuit efficiency and induce excessive heat, highlighting their importance in power electronics applications. Addressing this concern involves meticulous MOSFET selection, optimisation of circuit layout, and consideration of the impact on overall system performance and reliability.

# 5
# Modulators

To obtain regulated inverter output voltage, modulation entails altering the on and off duration of inverter switches under a constant input DC voltage. Pulse width modulation (PWM) is the most widely utilised method in inverters. Because of its simplicity of implementation, space vector modulation is frequently employed in inverters. There are several ways to control the inverter output voltage. An internal technique called modulation can be used to direct an inverter to produce the appropriate voltage waveform. Modulation uses fewer components than other inverter control strategies [46].

## 5.1 Common-Mode Voltage in Inverters

There is a voltage difference between the power source and the neutral point of the load when inverters convert DC to AC power. Common-mode voltage is the name given to this voltage difference in inverters [47].

### 5.1.1 Effects of Common-Mode Voltage in Inverters

Common-mode voltage can cause problems with motors, early bearing failure, unintended switchgear trip, control equipment issues, and other things. In an inverter system with common-mode impedance circuits, common-mode current can flow at any voltage level thanks to the common-mode voltage. Common-mode voltages in the inverter enhance electromagnetic interference by generating high common-mode current (EMI). Inverters powered by energy storage systems have common-mode voltages that might lead to leakage currents and improper activation of detecting components.

It is vital to apply common-mode voltage reduction strategies for the prolonged operation of machinery because common-mode voltages in inverters can result in significant damage.

### 5.1.2 Common-Mode Voltage Reduction Methods

Comparatively speaking, multilevel inverters produce less common-mode voltage than two- or three-level inverters. Consequently, one method for lowering the common-mode voltage in an inverter-based electrical system is to increase the output voltage levels by using multiple inverters. The architecture of three-phase inverters can be changed by including a fourth leg to lower the common-mode voltage.

Common-mode voltage in typical inverters is also reduced by using twin-bridge inverters [47].

Some reduction methods rely on physical circuitry. The following are examples of similar hardware circuitry-based common-mode reduction techniques:

1. Isolation transformers
2. Common-mode chokes or zero sequence impedance
3. Active and passive filters

The system's cost and size are both increased by several hardware circuit adjustments. Modifying the control strategy of inverters can help overcome the additional cost associated with hardware-based common-mode voltage reduction solutions. It has been demonstrated that space vector pulse-width modulation (SVM) and sinusoidal pulse-width modulation (SPWM) are efficient ways to lower common-mode voltages in inverters.

## 5.2 Switching Techniques

PWM inverters also get rid of lower-order harmonics and reduce the amount of THD in the output AC voltage. They reduce the need for filters as well. The following modulation types are frequently employed in inverters: [46] [48]

### 5.2.1 Sinusoidal Pulse Width Modulation

SPWM is a form of multiple pulse modulation, where each half-cycle contains several pulses. The sinusoidal function of the angular position of the pulse within a cycle is the pulse width. After comparing the triangle wave carrier and three-phase sinusoidal reference voltage signals in each of the N sections created by sinusoidal pulse width modulation, the resulting SPWM pulse sequence waves would be regarded as the driving control signals of inverter power switching devices. The basic sine wave needed for modulation is the fundamental wave of the inverter output voltage. Hence, by adjusting the amplitude and frequency of the sine wave reference signals, the output voltage of SPWM frequency inverters can be changed. The references for the three phases are per:

$$V_a^*(t) = m_a \times V_{dc} \times sin(\omega \times t) \tag{5.1}$$

$$V_b^*(t) = m_a \times V_{dc} \times sin(\omega \times t - \frac{2\pi}{3}) \tag{5.2}$$

$$V_c^*(t) = m_a \times V_{dc} \times sin(\omega \times t + \frac{2\pi}{3}) \tag{5.3}$$

Here $V_a^*(t)$, $V_b^*(t)$, and $V_c^*(t)$ are the reference voltages for three phases, $V_{dc}$ is the DC link voltage, $m_a$ is modulation index. There are two major types of SPWM techniques, Phase-Shifted PWM and Level-Shifted PWM.

#### 5.2.1.1 Level-shifted Pulse Width Modulation

The carrier signals in level-shifted multi-carrier PWM (LSPWM) are level-shifted. All of the carrier signals will be compared using the same reference signal. The reference signal's amplitude is equal to the total of the amplitudes of all the carrier signals.

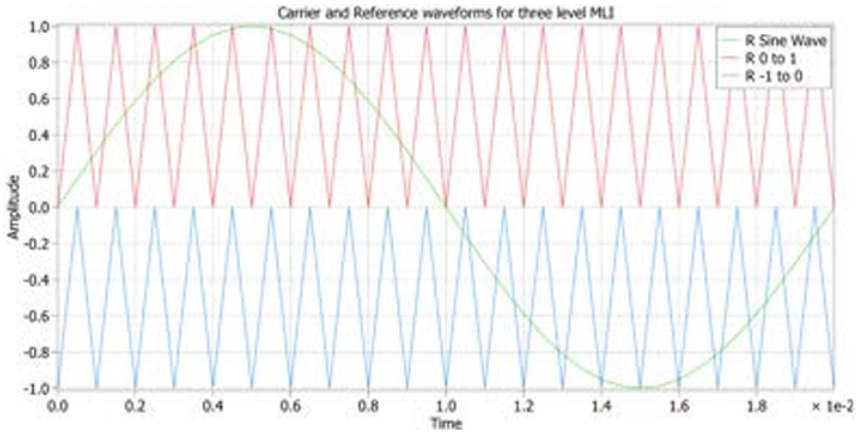



**Figure 5.1:** Space Vector diagram

#### 5.2.1.2 Phase-shifted Pulse Width Modulation

The carrier signals in phase-shifted multi-carrier PWM (PSPWM) will be phase-shifted by 360/(n-1). All of the carrier signals will be compared using the same reference signal. Both the carrier and the reference signal have the same amplitude.

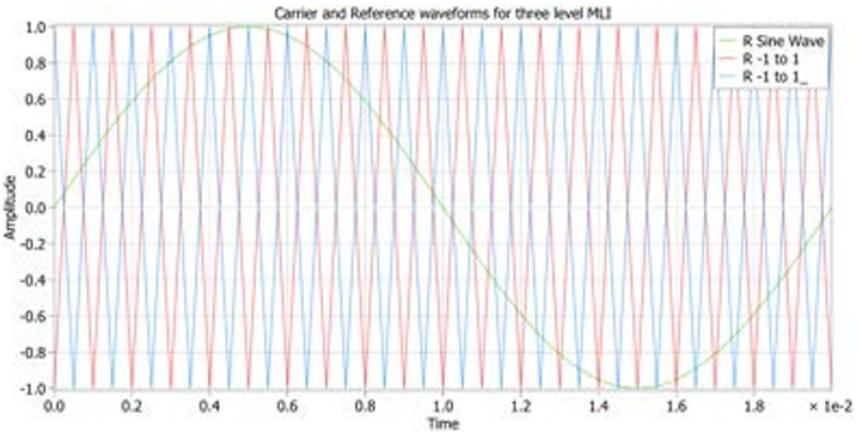



**Figure 5.2:** Space Vector diagram

### 5.2.2 Modified Sinusoidal Pulse Width Modulation

Owing to a sine wave's inherent properties, the SPWM technique's modulation index can't be varied to alter the wave's pulse width. Because of this, the MSPWM approach is presented. With this method, the first and last 60-degree intervals of each half-cycle are used to apply the carrier signal. Its harmonic feature is enhanced in this way. This method's key benefits include a larger fundamental component, fewer switching power devices, and less switching loss.

### 5.2.3 Space Vector Modulation

Due to its simplicity of use, the Space Vector Modulation (SVM) approach is frequently utilised in inverters. The use of multilevel inverters commonly involves it. With the space vector modulation technique, each cell's periodic switching only affects one device, resulting in little switch consumption. To make calculations simpler, the three-phase PWM wave is directly generated from the voltage space vector. The DC side voltage, which is 15% greater than the output voltage of a standard SPWM inverter, is the inverter's output line voltage's fundamental maximum value [46] [48].

Because the modulation employed in an inverter affects the THD content and filter requirements, it is crucial to choose a technique appropriate for the voltage requirements of the AC loads.

## 5.3 Application of SVM

SVM is a Pulse Width Modulation (PWM) technique used to control the switching states of power semiconductor devices in inverters. It represents the output voltage of the inverter as a combination of two or more voltage vectors in a complex plane, forming a space vector. By adjusting the amplitude and angle of the space vector, the inverter can produce different voltage levels and frequencies to create the desired output waveform [49].

It is particularly well-suited for Neutral-Point-Clamped (NPC) Multi-Level Inverters. The main objective of SVM is to control the output voltage of the inverter to achieve a desired output waveform with reduced harmonic distortion and better efficiency. SVM is widely used in NPC Multi-Level Inverters due to its ability to generate low-distortion output voltage waveforms. By selecting appropriate voltage vectors, SVM ensures balanced and optimized voltage levels across the output phases, minimizing harmonic content in the output voltage. The modulation index determines the number of voltage levels in the output waveform, and SVM helps control this index to achieve the desired output voltage level.

### 5.3.1 Operating Principle

The 3-level space-vector modulator generates a voltage vector on the AC terminals of an NPC 3-phase inverter according to a reference signal provided in the stationary $\alpha\beta$ reference frame. By controlling the semiconductor gate signals, each AC terminal can be connected either to the high (+), low (-) or neutral (O) point of the DC-link. This results in 27 vectors including 12 short vectors, 6 medium vectors and 6 long vectors, as well as 3 zero vectors. Under the assumption of balanced voltages on the capacitors $Vdc+$ and $Vdc-$ the space-vector diagram is graphically depicted below [50] [51] [52].

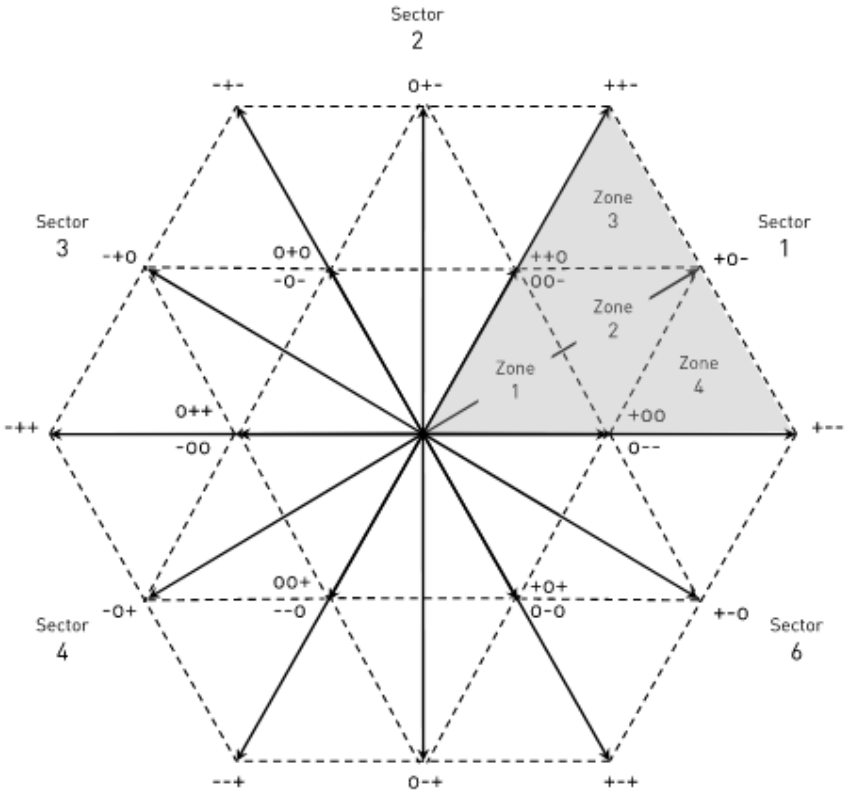



**Figure 5.3:** Space Vector diagram

As noted, the SVM diagram for a 3-phase inverter can be divided into six sectors. Each of these sectors consists of $(n-1)^2$ triangles. Each vertex of the triangles represents a switching state, and the reference vector can be located in any of the triangles of any sector. There are $n^3$ switching states in an n-level inverter, and a switching vector can represent one or more of these states depending on its location. The SVM is performed by suitably selecting the switching states of the triangle for the respective on-times. This approach is called the "Nearest Three Vector" (NTV) approach. These switching states decide the performance of the inverter. This space vector diagram has 19 voltage vectors, six sectors, four triangles per sector, and 27 switching states.

$\theta_n$ is calculated as per the given equation:

$$\theta_n = 2\pi f_{sw} t \tag{5.4}$$

Where $f_{sw}$ is the switching frequency and $t$ is the on-time. If the $\theta_n$ is between-

- 0° and 60°, $V_{ref}$ is in sector 1.
- 60° and 120°, $V_{ref}$ is in sector 2.
- 120° and 180°, $V_{ref}$ is in sector 3.
- 180° and 240°, $V_{ref}$ is in sector 4.
- 240° and 300°, $V_{ref}$ is in sector 5.
- 300° and 360°, $V_{ref}$ is in sector 6.

Depending on the magnitude and the direction of the voltage vector, the reference vector can be present in any of the sectors as defined above.

The 19 voltage vectors represented in the SVM diagram can be categorised as follows-

- Zero Voltage Vectors (ZVV): 1 (3 redundant states where V=0)
- Small Voltage Vectors (SVV): 6
- Medium Voltage Vectors (MVV): 6
- Large Voltage Vectors (LVV): 6

Each triangle in each sector is congruous and identical [53]. The two edges of each triangle connected to the centre of the hexagon form an LVV, while the median dropped from the intersection of these edges to the middle of the opposite edge forms an MVV. The SVVs are along the same direction as an LVV, but each SVV is exactly half the magnitude of the LVV it is directed along. Since the hexagon is symmetric along all axes, and the sectors and triangles are all identical, it can be surmised that each LVV is of equal magnitude. Similarly, each MVV has an equal magnitude, and so does every SVV. The redundant ZVVs are found at the centre of the hexagon.

Switching signals for Sector 1 are as follows:

- Region 1: - - -/ O - -/ O O -/ O O O/ + O O/ + + O/ + + +
- Region 2: O - -/ O O -/ + O -/ + O O/ + + O
- Region 3: O O -/ + O -/ + + -/ + + O
- Region 4: O - -/ + - -/ + O -/ + O O

Similarly, switching signals for other sectors can also be listed [54]. Hence, the switching transitions can also be identified using this list, to get a quantitative analysis of switching losses in each switch in each phase-leg in the inverter.

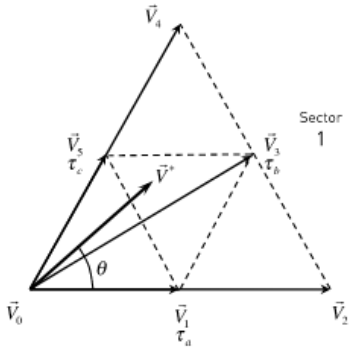



**Figure 5.4:** Space Vector diagram for sector 1

As noted, the hexagon area can be divided into six sectors (1 to 6), each with four triangular zones (1 to 4). For example, consider the reference voltage $\overrightarrow{V}$ located in zone 2 of sector 1. To generate the reference voltage $\overrightarrow{V}^*$ on the ac terminals, the adjacent vectors $\overrightarrow{V}_1, \overrightarrow{V}_3$ and $\overrightarrow{V}_5$ are selected and weighted by time [55]. The on-time of each vector concerning the switching period is calculated as:

$$\tau_a = 1 - k * \sin(\theta) \tag{5.5}$$

$$\tau_b = 2k * \sin(\frac{\pi}{3} + \theta) - 1 \tag{5.6}$$

$$\tau_c = 1 - 2k * \sin(\frac{\pi}{3} - \theta) \tag{5.7}$$

This block implements a symmetrical sequence to achieve minimum total harmonic distortion (THD) [55]. The short vectors have redundant switch states, e.g. $\overrightarrow{V}_1$ can be either generated by the combination (+ O O) or (O - -). In order to keep the DC-link voltages balanced, both switch states must be applied for the same duration during one switching period. The resulting switch pattern is illustrated below:

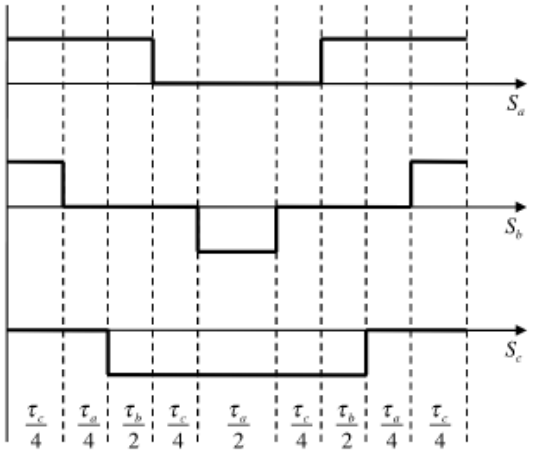


**Figure 5.5:** Switching pulses for all three phases

### 5.3.2 Dwell Time

After the reference voltage is located, the closest three vector positions are known, for any n-level MLI, it makes use of an algorithm based on the Volt-second balancing principle to determine the dwell time for the respective switches. This principle implies the product of the reference voltage vector and the sampling period Ts is equal to the sum of the nearest three voltage vectors multiplied by the time interval of the corresponding vectors [56].

Figure 5.2 shows that $\overrightarrow{V}_{ref}$ is in region 2 of sector 1. The nearest three voltage vectors are $\overrightarrow{V}_1$, $\overrightarrow{V}_3$, and $\overrightarrow{V}_5$. Using the volt-second balancing principle the dwell times are calculated using:

$$\overrightarrow{V}_{ref}T_s = V_1T_a + V_2T_b + V_3T_c \tag{5.8}$$

$$T_s = T_a + T_b + T_c \tag{5.9}$$

where Ts is the sampling time for one period, $T_a$, $T_b$, and $T_c$ are the dwell times at voltage vectors $\overrightarrow{V}_1$, $\overrightarrow{V}_3$, and $\overrightarrow{V}_5$.

Now, based on the region and the switching states, the switching sequence is generated and this can be done in several ways since there are multiple redundant states for each inverter topology. The switching sequence is determined in such a way that the switching loss and the THD are minimized. The requirement to achieve this strategy is to have

- only two switches in the same inverter phase leg are involved in the transition from one switching state to the next state i.e.; one being switched on and the other being switched off.
- minimum number of switching (zero if possible) when the reference voltage vector moves from one sector (or region) to the next.
- minimal neutral point voltage deviation depending on the inverter topology.

### 5.3.3 Voltage Determination

Assuming the three-phase system is balanced, the voltages in the alpha and the beta frames are given as,

$$V_\alpha = \frac{2}{3}(V_a - \frac{1}{2}V_b - \frac{1}{2}V_c) \tag{5.10}$$

$$V_\beta = \frac{2}{3}(\frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c) \tag{5.11}$$

$$V_{ref} = V_\alpha + jV_\beta \tag{5.12}$$

where $V_\alpha$ is the alpha component of the reference voltage in the alpha-beta frame, $V_\beta$ is the beta component of the reference voltage, $V_a$ is the phase A to neutral voltage, $V_b$ is the B phase voltage, $V_c$ is the C phase voltage and $V_{ref}$ is the reference voltage [57].

### 5.3.4 State Transitions

The table here depicts the state of each switch for every voltage level in the 3-level MLI. As we can see, for a positive voltage we need switches 1 and 2 in the ON condition, and switches 3 and 4 in the OFF condition. For a negative voltage, we need switches 3 and 4 in ON condition and switches 1 and 2 in OFF condition. For generating a zero voltage state in the inverter, we need switches 2 and 3 in ON condition, while switches 1 and 4 are OFF.

| | sw1 | sw2 | sw3 | sw4 |
|---|---|---|---|---|
| **P** | ON | ON | OFF | OFF |
| **O** | OFF | ON | ON | OFF |
| **N** | OFF | OFF | ON | ON |

**Figure 5.6:** Switch state for each voltage level

Here, the P state relates to the positive (+) state, while N relates to the negative state (-), and the O state relates to the neutral (O) state - all that have been defined at the beginning of this section, in the operating principles of SVM. During the operation of the 3-level NPC Multi-level Inverter, the switching losses accumulated during the operation can be assessed accurately based on the switching state of each switch. Tracing the switching state of each switch aids in mapping the switching transitions made by each switch. The switching losses happen really because of the switching transitions between the several possible states attainable, and not due to the switch being in a particular state. The higher the number of transitions, the higher will be the switching loss for an individual switching device.

Ideally, for an inverter the loss distribution would be equally spread over all the participating switches, over a whole, or a multiple of a whole switching period. However, the NPC Multi-level Inverters pose a challenge, in that the loss distribution is not equally shared by all the switches in a phase. Depending on the operating mode and modulation index of the modulator, the load current magnitude and direction, and the load power factor (PF), the distribution of the loss changes. It could be concentrated more in the switches in the middle - sw2 and sw3, and less in the switches on the extreme ends of the phase leg - sw1 and sw4. It could also be vice-versa, being more concentrated in the switches on the extreme ends, and less in the switches in the middle. More has been discussed about which operating mode promotes which loss distribution in the following chapter.

The table below outlines the switches which undergo a transition in their condition when there is a change in the voltage level in the inverter. This helps trace the switching losses and observe how many transitions each switch goes through.

| | sw1 | sw2 | sw3 | sw4 |
|---|---|---|---|---|
| P-O | off | - | on | - |
| O-N | - | off | - | on |
| O-P | on | - | off | - |
| N-O | - | on | - | off |

**Figure 5.7:** Switch states for each transition

This table has been derived using the switch state table in Figure 5.4 above. The state transitions that have been identified are - positive to neutral (P-O), neutral to positive (O-P), neutral to negative (O-N), and negative to neutral(N-O). In SVM, and in 3-phase NPC Multi-level Inverters, the state transitions happen smoothly, one state at a time. The states do not directly jump to another state which is 2 transitions away. If they do, that would be a dysfunction of the modulator and result in an inefficient operation of the inverter.

For a complete sector in the SVM diagram, the switch transitions have been broken down as below. Here we can note the complete list of transitions undergone by all the switches throughout all the phases when the inverter switches between the 3 levels available in a 3-level NPC MLI.

| | | | | | | | A | | | | B | | | | C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A | B | C | ON-OFF transitions | OFF-ON transitions | sw1 | sw2 | sw3 | sw4 | sw1 | sw2 | sw3 | sw4 | sw1 | sw2 | sw3 | sw4 |
| SECTOR 1 (0-60) | region 1/0_4_0 | P | P | O | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| | | P | O | O | 1 | 1 | | | | | off | - | on | - | | | | |
| | | O | O | O | 1 | 1 | off | - | on | - | | | | | | | | |
| | | O | O | N | 1 | 1 | | | | | | | | | - | off | - | on |
| | | O | N | N | 1 | 1 | | | | | - | off | - | on | | | | |
| | | O | O | N | 1 | 1 | | | | | - | on | - | off | | | | |
| | | O | O | O | 1 | 1 | | | | | | | | | - | on | - | off |
| | | P | O | O | 1 | 1 | on | - | off | - | | | | | | | | |
| | | P | P | O | 1 | 1 | | | | | on | - | off | - | | | | |
| | Number of Transitions | | | | 8 | 8 | | | | | | | | | | | | |
| | region 2/0_4_0 | P | P | O | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| | | P | O | O | 1 | 1 | | | | | off | - | on | - | | | | |
| | | P | O | N | 1 | 1 | | | | | | | | | - | off | - | on |
| | | O | O | N | 1 | 1 | off | - | on | - | | | | | | | | |
| | | O | N | N | 1 | 1 | | | | | - | off | - | on | | | | |
| | | O | O | N | 1 | 1 | | | | | - | on | - | off | | | | |
| | | P | O | N | 1 | 1 | on | - | off | - | | | | | | | | |
| | | P | O | O | 1 | 1 | | | | | | | | | - | on | - | off |
| | | P | P | O | 1 | 1 | | | | | on | - | off | - | | | | |
| | Number of Transitions | | | | 8 | 8 | | | | | | | | | | | | |
| | region 3 0_3_0/dis-OOO (state 4) | P | P | O | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| | | P | P | N | 1 | 1 | | | | | | | | | - | off | - | on |
| | | P | O | N | 1 | 1 | | | | | off | - | on | - | | | | |
| | | O | O | N | 1 | 1 | off | - | on | - | | | | | | | | |
| | | P | O | N | 1 | 1 | on | - | off | - | | | | | | | | |
| | | P | P | N | 1 | 1 | | | | | on | - | off | - | | | | |
| | | P | P | O | 1 | 1 | | | | | | | | | - | on | - | off |
| | Number of Transitions | | | | 6 | 6 | | | | | | | | | | | | |
| | region 4 0_3_0/dis-NNN (state 4) | P | O | O | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| | | P | O | N | 1 | 1 | | | | | | | | | - | off | - | on |
| | | P | N | N | 1 | 1 | | | | | - | off | - | on | | | | |
| | | O | N | N | 1 | 1 | off | - | on | - | | | | | | | | |
| | | P | N | N | 1 | 1 | on | - | off | - | | | | | | | | |
| | | P | O | N | 1 | 1 | | | | | - | on | - | off | | | | |
| | | P | O | O | 1 | 1 | | | | | | | | | - | on | - | off |
| | Number of Transitions | | | | 6 | 6 | | | | | | | | | | | | |

**Figure 5.8:** Detailed breakup of state transitions in sector 1

### 5.3.5 Advantages

In summary, SVM is a highly versatile modulation technique which is very easily implemented in MLI topologies [57] [58]. As compared to other techniques like SPWM, we see the following benefits-

- Lower Total Harmonic Distortion (THD) in the output voltage, leading to improved motor performance in motor drives and reduced electromagnetic interference in power systems.
- Better utilization of DC bus voltage and reduced voltage stress on semiconductor devices, contributing to increased system reliability and efficiency.
- 15% higher voltage obtained, when compared to SPWM.
- Simplified control algorithms compared to other PWM techniques, making it more practical and easier to implement in real-time control systems.
- SVM inherently reduces the common-mode voltage, which can help mitigate issues related to electromagnetic interference (EMI) and motor bearing currents. This is particularly important in applications where EMI compliance is critical.
- SVM often results in reduced switching losses compared to Sine PWM, especially at high modulation indices. The optimized switching sequences in SVM reduce the number of transitions between switching states, minimizing losses in the power electronics components.
- SVM simplifies the implementation of overmodulation techniques, which allow the inverter to operate beyond the traditional $\pm 1$ modulation index. This can be beneficial for applications requiring high torque at low speeds, such as electric vehicle propulsion or wind turbine control.
- In motor drive applications, SVM can lead to lower audible noise due to its improved waveform quality and reduced harmonic content.

# 6
# Loss Distribution

As is true with every power device that operates, the inverters also experience losses during operation. Efforts are made to reduce these losses to as little a value as possible. Optimal losses can be obtained using several methods, like studying modulation and triggering the switches when the voltage and the current are approaching a low value or even zero. Soft-switching methods, advanced modulation techniques, and modern inverter topologies are all steps in the same direction- to make the operation of an inverter as lossless and maximally efficient as possible [59] [60].

Below losses associated with an inverter are studied in detail, and then the distribution of the said losses is studied among the various switches in a 3-phase 3-level NPC MLI utilising SVM for its operation.

## 6.1 Losses in Multi-level Inverters

Different factors contribute to losses in a three-phase inverter. The majority of the losses is due to the power semiconductor device, the MOSFET [61]. There are two types of losses which happen in the MOSFET and can be represented as:

$$P_{tot} = P_{sw} + P_{cond} \tag{6.1}$$

where $P_{tot}$ is the total power loss, $P_{sw}$ is the switching loss and $P_{cond}$ is the conduction loss happening in the MOSFET [59]. As there are other components present in the inverter, they will have equivalent resistances and contribute towards losses in the inverter. This is called Ohmic losses and is represented by:

$$P_{ohm} = I_{rms}^2 R \tag{6.2}$$

where $P_{ohm}$ is the ohmic losses, $I_{rms}$ is the RMS value of current flowing through the component during conduction and $R$ is the value of resistance of the corresponding components.

### 6.1.1 Conduction Losses

Conduction losses happen due to the presence of internal resistances and forward voltage drops present in a power semiconductor device [62] [63]. The conduction losses for any device can be represented using:

$$P_{cond} = V_{pn} I_{cond_{avg}} + R_{cond} I_{cond_{rms}}^2 \tag{6.3}$$

here $P_{cond}$ is the conduction loss, $I_{cond}$ is the instantaneous current flowing through the device, $V_{pn}$ is the forward voltage drop in the device, $R_{cond}$ is the resistance of the device during conduction, $I_{cond_{avg}}$ is average conduction current flowing through the device, $I_{cond_{rms}}$ is the RMS value of current flowing the device [59] [60]. The MOSFET being a unipolar device, there is no constant voltage drop ($V_{pn} = 0$). Hence the conduction losses for a MOSFET can be written as

$$P_{MOSFET} = R_{DS_{on}} I^2_{FET_{rms}} \tag{6.4}$$

where $P_{MOSFET}$ is the conduction losses in a MOSFET, $R_{DS_{on}}$ is the resistance of MOSFET, $I_{FET_{rms}}$ is the RMS value of current flowing through the MOSFET. As the diode has both the internal resistance and forward voltage drop, the conduction losses for the diode shall be as per the full equation defined above [59] [60].

### 6.1.2 Switching Losses

Switching loss occurs when the MOSFET is turned on or turned off as this cannot happen instantaneously. There is always a turn-on and turn-off time for the switches which causes power dissipation. During turn-off, the switch has a voltage which is equal to the source voltage and during turn-on, the voltage becomes zero and at the same time, the current also starts flowing through the switch [62] [63]. Since there is both voltage and current at this time, there will also be power loss which is called switching loss which can be estimated with the:

$$P_{sw} = f_{sw} E_{sw} \left( \frac{1}{\pi} \frac{\hat{I_{out}}}{I_{ref}} \right)^{K_i} \left( \frac{V_{DS}}{V_{ref}} \right)^{K_v} \tag{6.5}$$

where $P_{sw}$ is the total switching loss, $f_{sw}$ is the carrier frequency used for pulse width modulation, $E_{sw}$ represents either the turn on and turn off losses for one time period in a MOSFET or the reverse recovery losses in a diode, $\hat{I_{out}}$ is the peak value of current flowing through the switch, $I_{ref}$ and $V_{ref}$ are the values taken from the test condition of corresponding $E_{sw}$, $V_{DS}$ is the voltage applied across the switch, $K_i$ and $K_v$ are constants for current and voltage depending on the $E_{sw}$. The switching losses are also dependent on MOSFET's junction temperature [59] [60].

## 6.2 Loss distribution as per operating conditions

Three models have been developed - high ringing, moderate ringing, and low ringing. Ringing is the effect observed when there is EMI present in the waveforms.

High ringing means high EMI and has a high slew rate; the higher the slew rate, the lower the switching losses. The simulation is run for a variation of 3 parameters being varied over low, medium and high. The load current, load power factor(PF), and the modulation index of the modulator are varied. In total 27 cases have been run following the factorial Design of Experiment method.

Modulation index: 0.2 | 0.5 | 0.95
Load current: 79.95/2 | 79.95 | 79.95 × 2
Load PF: -90 | 0 | +90

The following cases have also been run for regenerative braking mode, where the current flows in reverse from the inverter to the battery, and the load current has been taken as -79.95/2, -79.95, and $-79.95 \times 2$. All the remaining parameters have been kept the same as in the motor mode.

The mixed model refers to the simulation where the switches with a high concentration of losses were given the high-ringing model, and the switches with a low concentration of losses were given the low-ringing model. What this does is that it helps with the balancing of the losses to an extent without affecting efficiency majorly. We see in the mixed model plots when compared to moderate ringing plots, that the high-concentration switches (switch 1 and switch 4) have seen a reduction in losses, while an increase has been seen in the low-loss concentration switches (switch 2 and switch 3), while maintaining the overall loss levels, hence maintaining the efficiency.

The graphs below show the typical loss distribution behaviour noted in NPC inverters. This is one of the few caveats of the NPC topology, and through this experiment, an attempt to make up for it has been made. Interestingly, the conduction losses have the same profile through various operating conditions. This can be attributed to the fact that the conduction losses are directly dependent on the temperature values, and in this analysis, only one temperature value has been assumed. The whole analysis has been conducted assuming an ambient temperature of 25 degrees Celsius. The switching losses, however, vary significantly depending on the operating condition and the operating parameters.

The conduction losses were more concentrated in the switches in the middle. The magnitude on average is 195.2W - across switch 2 and switch 3 across all phase-legs. In switches 1 and 4 across all phase-legs, the magnitude of conduction losses has been noted to be slightly less at around 191.5W. The difference is not as large as in the case of switching losses.

### 6.2.1 Motor mode Model with High Ringing

In this case, the modulation index is maintained at 0.95, load current at 159.9 A, and load PF at 0 degrees, a purely resistive load. All the switches have the same gate driver model - with high ringing or low switching losses. This has been done to observe the effect of this gate driver on the loss distribution in the NPC MLI.

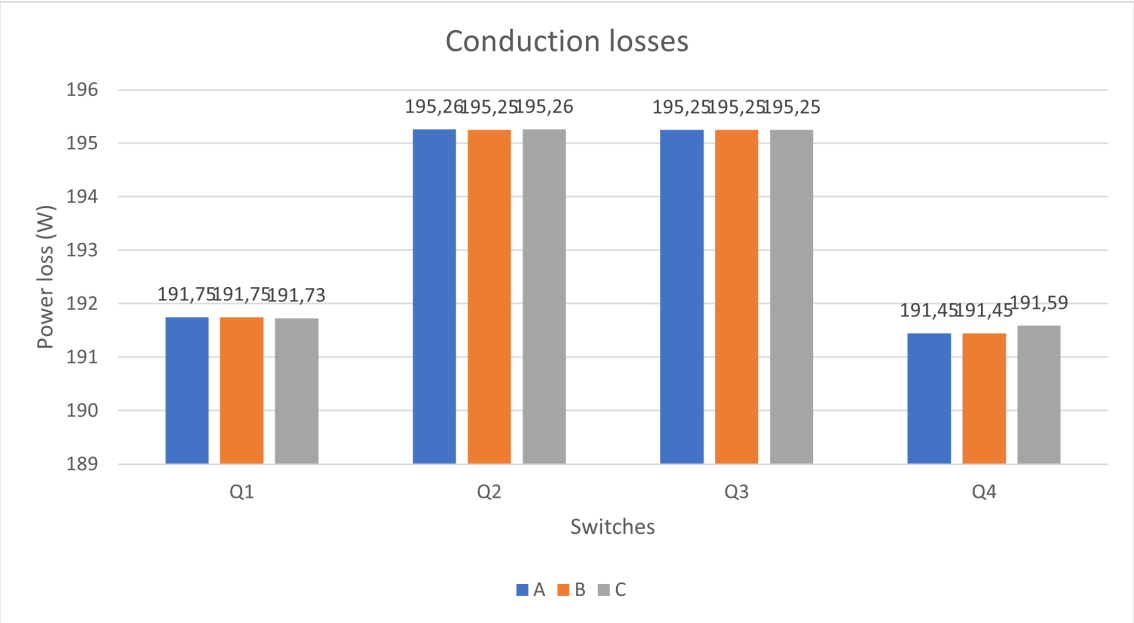



**Figure 6.1:** Conduction losses with high ringing model

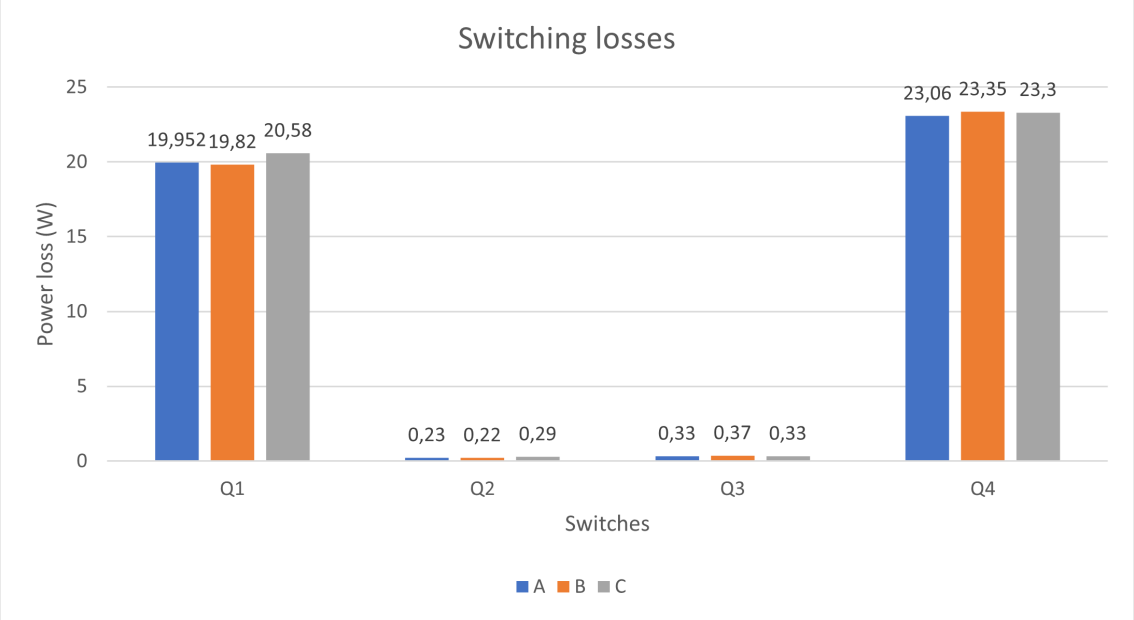



**Figure 6.2:** Switching losses with high ringing model

In Figure 6.2, we can see that the losses are concentrated in the switches in the extreme in each phase-leg, in switches 1 and 4. While the losses in switches 2 and 3 are relatively small.

Switch 1 across all 3 phase-legs sees a rough power loss of 20W, while switch 4 across all 3 phase-legs sees a power loss of about 23.2W. In comparison, the switches in the middle, switch 2 and switch 3, see largely reduced magnitude of losses - approximately 0.29W, in both of them, across all the phase-legs.

### 6.2.2 Motor mode Model with Moderate Ringing

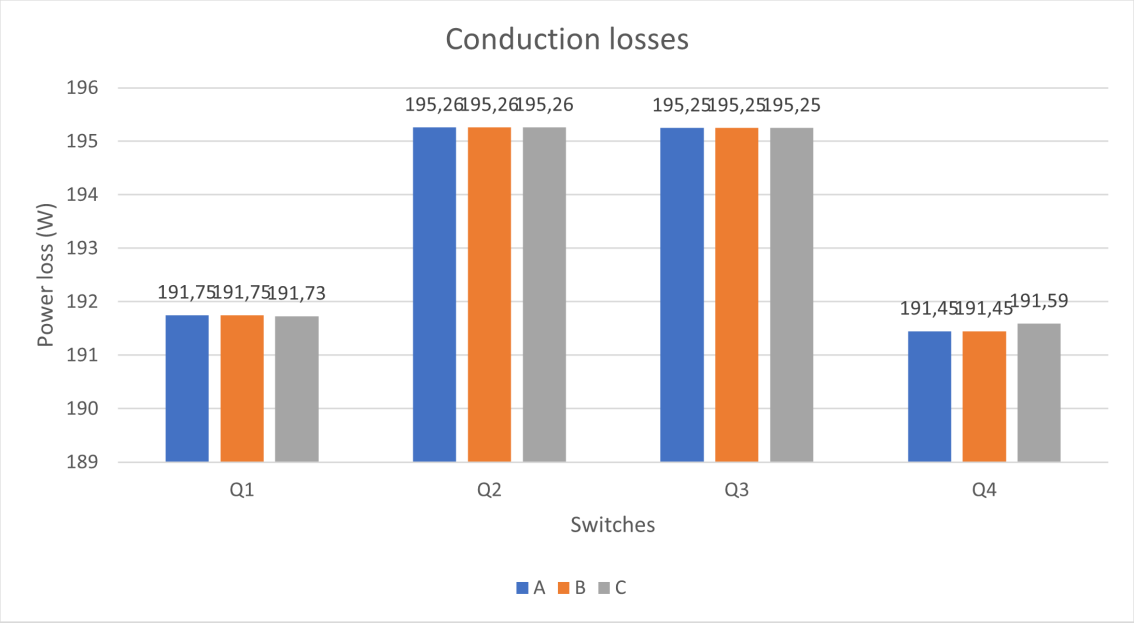



**Figure 6.3:** Conduction losses with moderate ringing model

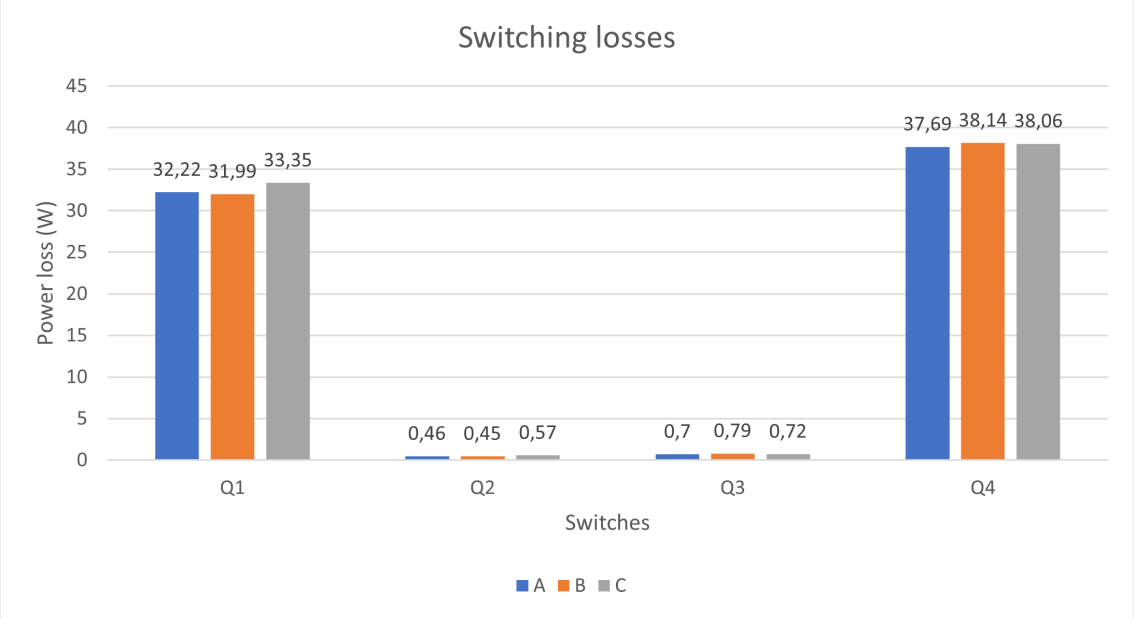



**Figure 6.4:** Switching losses with moderate ringing model

In Figure 6.4, we can see that the losses are concentrated in the switches in the extreme in each phase-leg, in switches 1 and 4. While the losses in switches 2 and 3 are relatively small.

Switch 1 across all 3 phase-legs sees a rough power loss of 20W, while switch 4 across all 3 phase-legs sees a power loss of about 23.2W. In comparison, the switches

in the middle, switch 2 and switch 3, see largely reduced magnitude of losses - approximately 0.5W and 0.75W in both respectively across all the phase-legs.

### 6.2.3 Motor mode Model with Custom Gate Drivers for each switch-type

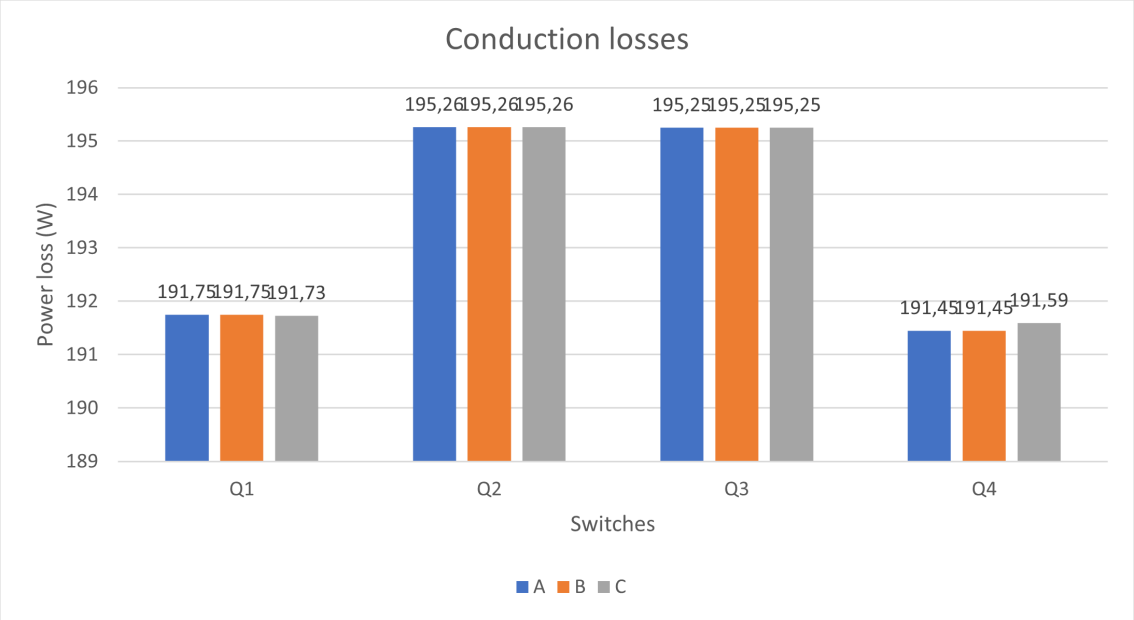



**Figure 6.5:** Conduction losses with mixed ringing model

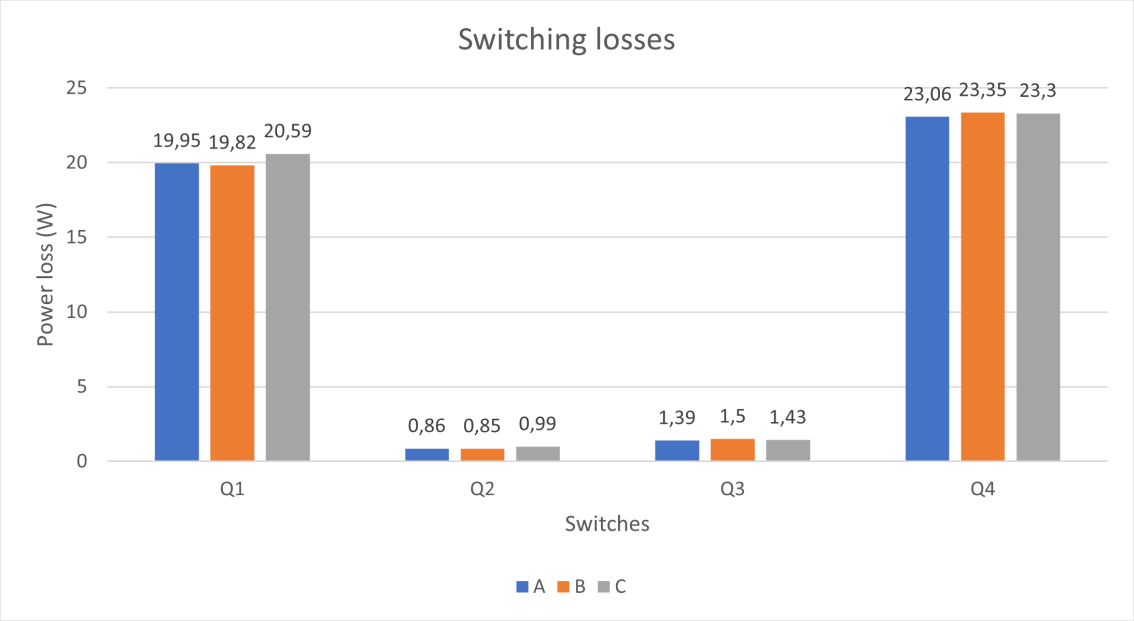



**Figure 6.6:** Switching losses with mixed ringing model

In Figure 6.6, we can see that the losses are still mostly concentrated in the switches in the extreme in each phase-leg, in switches 1 and 4. However, the magnitude has reduced as compared to the moderate ringing model. While the losses in switches 2 and 3 are relatively small but have increased in relation to the moderate ringing case. Hence, it is more balanced than before.

Switch 1 across all 3 phase-legs sees a rough power loss of 20W, while switch 4 across all 3 phase-legs sees a power loss of about 23.2W. In comparison, the switches in the middle, switch 2 and switch 3, see largely reduced magnitude of losses - approximately 0.9W and 1.45W in both respectively across all the phase-legs.

### 6.2.4 Regen mode Model with High Ringing

We can note an opposite behaviour for the regenerative braking case compared to the motoring mode. The switches with a high loss concentration and switches with a low loss concentration have swapped places - now switches 1 and 4 have significantly lower switching losses and conduction losses than switches 2 and 3. The mixed model there is applied accordingly. Balancing of losses is observed in this case as well.

The conduction losses were more concentrated in the switches in the middle. The magnitude on average is 160W - across switch 2 and switch 3 across all phase-legs. In switches 1 and 4 across all phase-legs, the magnitude of conduction losses has been noted to be slightly less at around 146W. The difference is not as large as in the case of switching losses. This profile of conduction losses stays constant for the regenerative braking mode through the changing operating parameters.

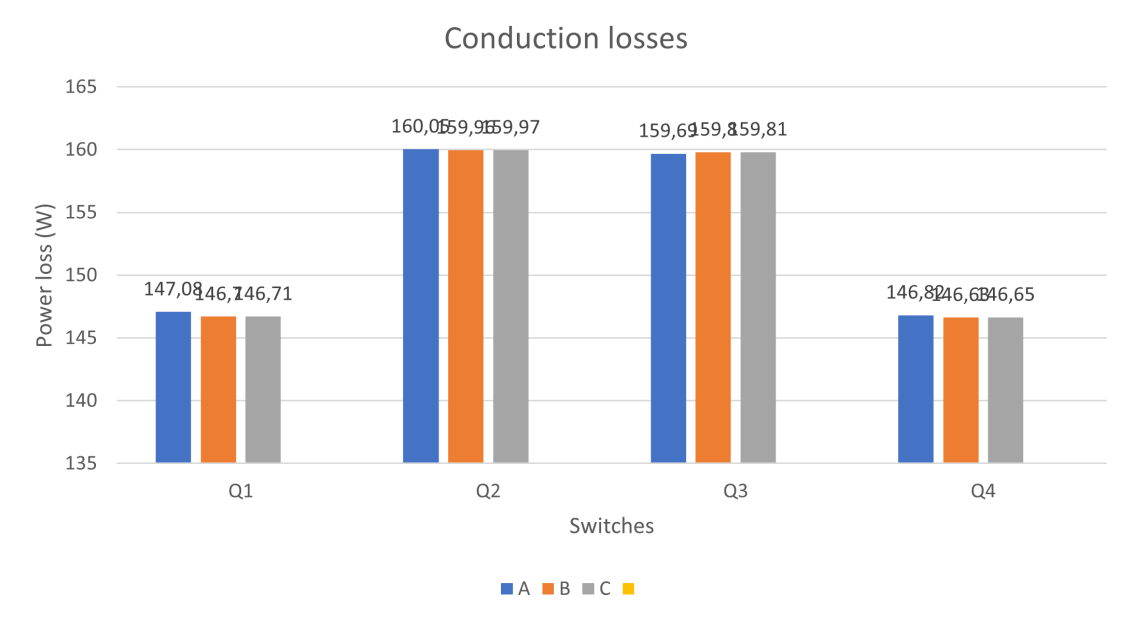



**Figure 6.7:** Conduction losses in regen with high ringing model

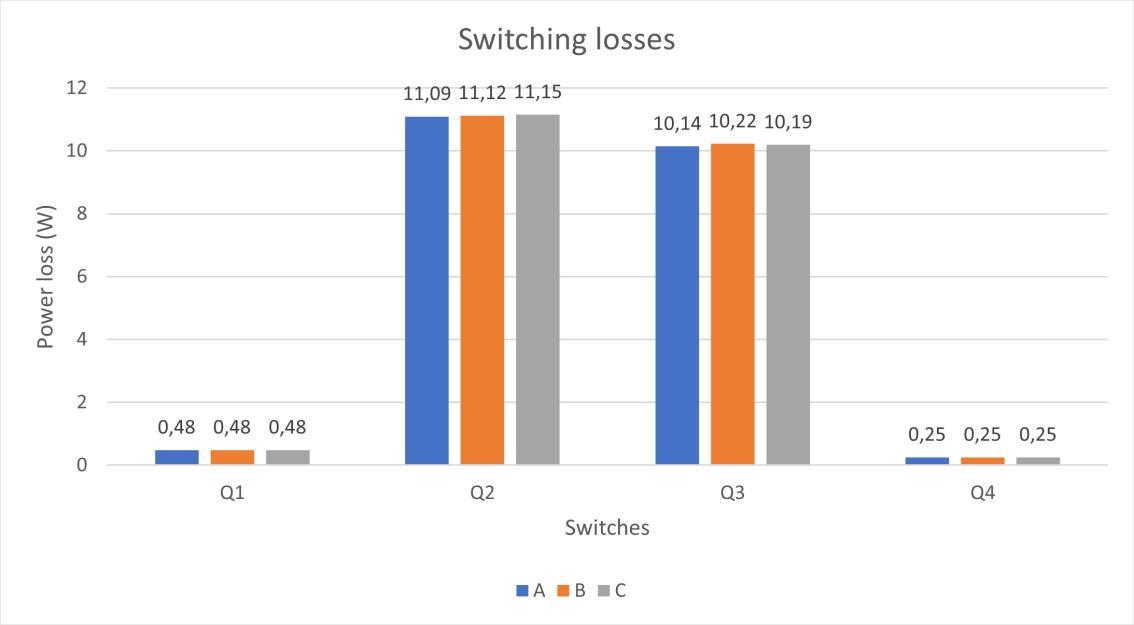



**Figure 6.8:** Switching losses in regen with high ringing model

In Figure 6.8, we can see that the losses are less concentrated in the switches in the extreme in each phase-leg, in switches 1 and 4. While the losses in switches 2 and 3 are relatively large.

Switch 2 across all 3 phase-legs sees a rough power loss of 11.12W, while switch 3 across all 3 phase-legs sees a power loss of about 10.18W. In comparison, the switches in the extreme, switch 1 and switch 4, see largely reduced magnitude of losses - approximately 0.36W, in both of them, across all the phase-legs.

### 6.2.5 Regen mode Model with Moderate Ringing

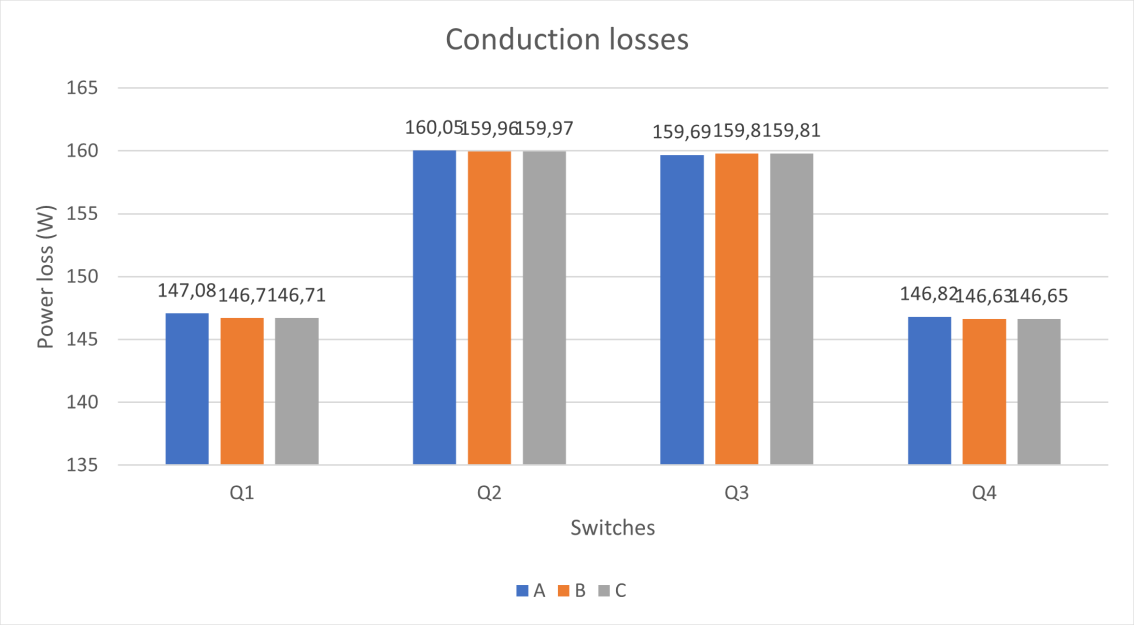



**Figure 6.9:** Conduction losses in regen with moderate ringing model

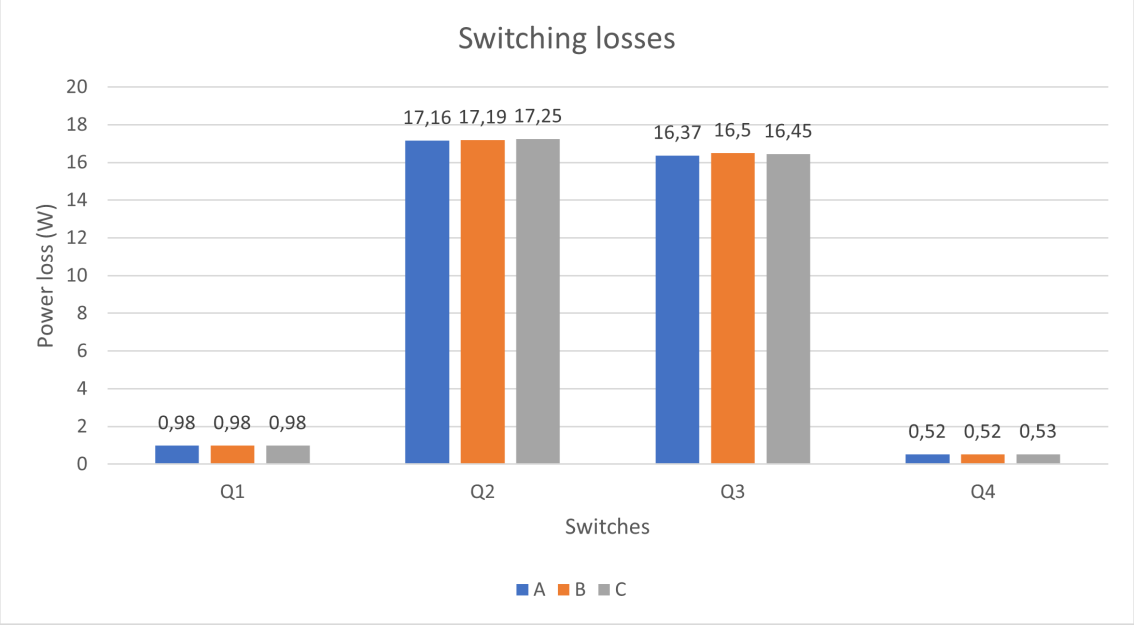



**Figure 6.10:** Switching losses in regen with moderate ringing model

In Figure 6.10, we can see that the losses are less concentrated in the switches in the extreme in each phase-leg, in switches 1 and 4. While the losses in switches 2 and 3 are relatively large.

Switch 2 across all 3 phase-legs sees a rough power loss of 17.2W, while switch 3 across all 3 phase-legs sees a power loss of about 16.44W. In comparison, the switches in the extreme, switch 1 and switch 4, see largely reduced magnitude of losses - approximately 0.75W, in both of them, across all the phase-legs.

### 6.2.6 Regen mode Model with Custom Gate Driver for each switch-type

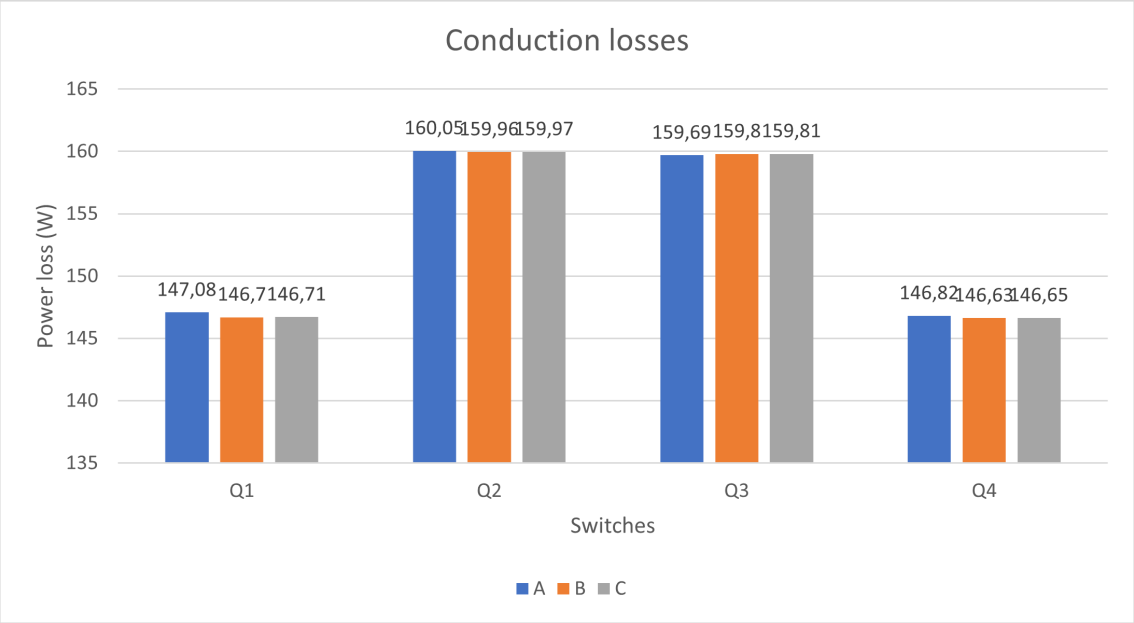



**Figure 6.11:** Conduction losses in regen with mixed ringing model

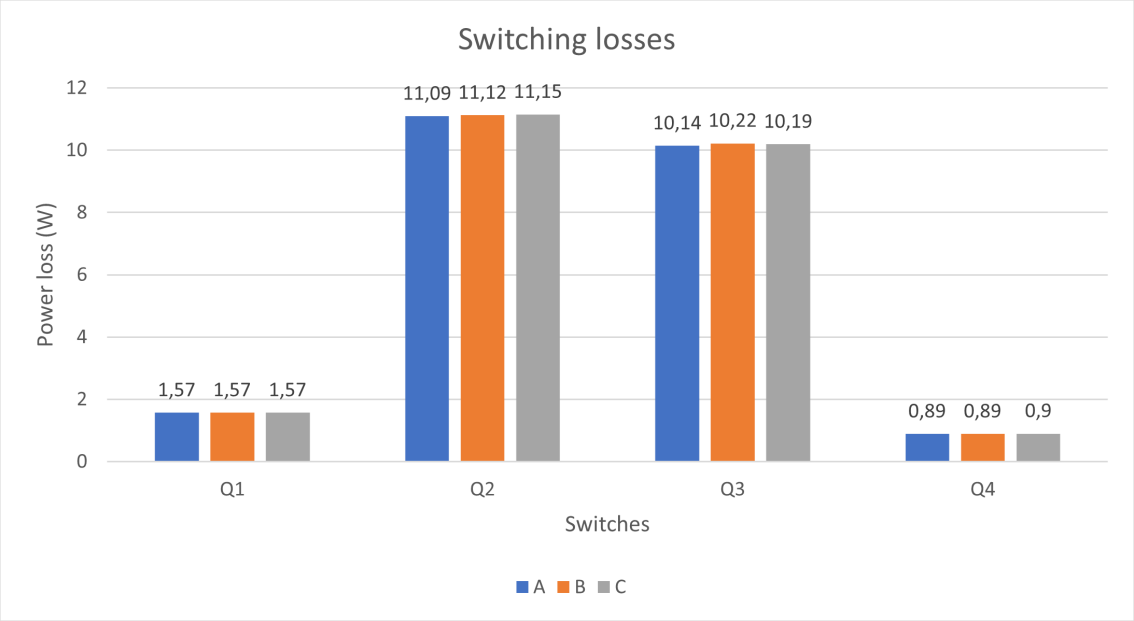



**Figure 6.12:** Switching losses in regen with mixed ringing model

In Figure 6.12, we can see that the losses are less concentrated in the switches in the extreme in each phase-leg, in switches 1 and 4. While the losses in switches 2 and 3 are relatively large.

Switch 2 across all 3 phase-legs sees a rough power loss of 11.12W, while switch 3 across all 3 phase-legs sees a power loss of about 10.19W. In comparison, the switches in the extreme, switch 1 and switch 4, see largely reduced magnitude of losses - approximately 1.23W, in both of them, across all the phase-legs.

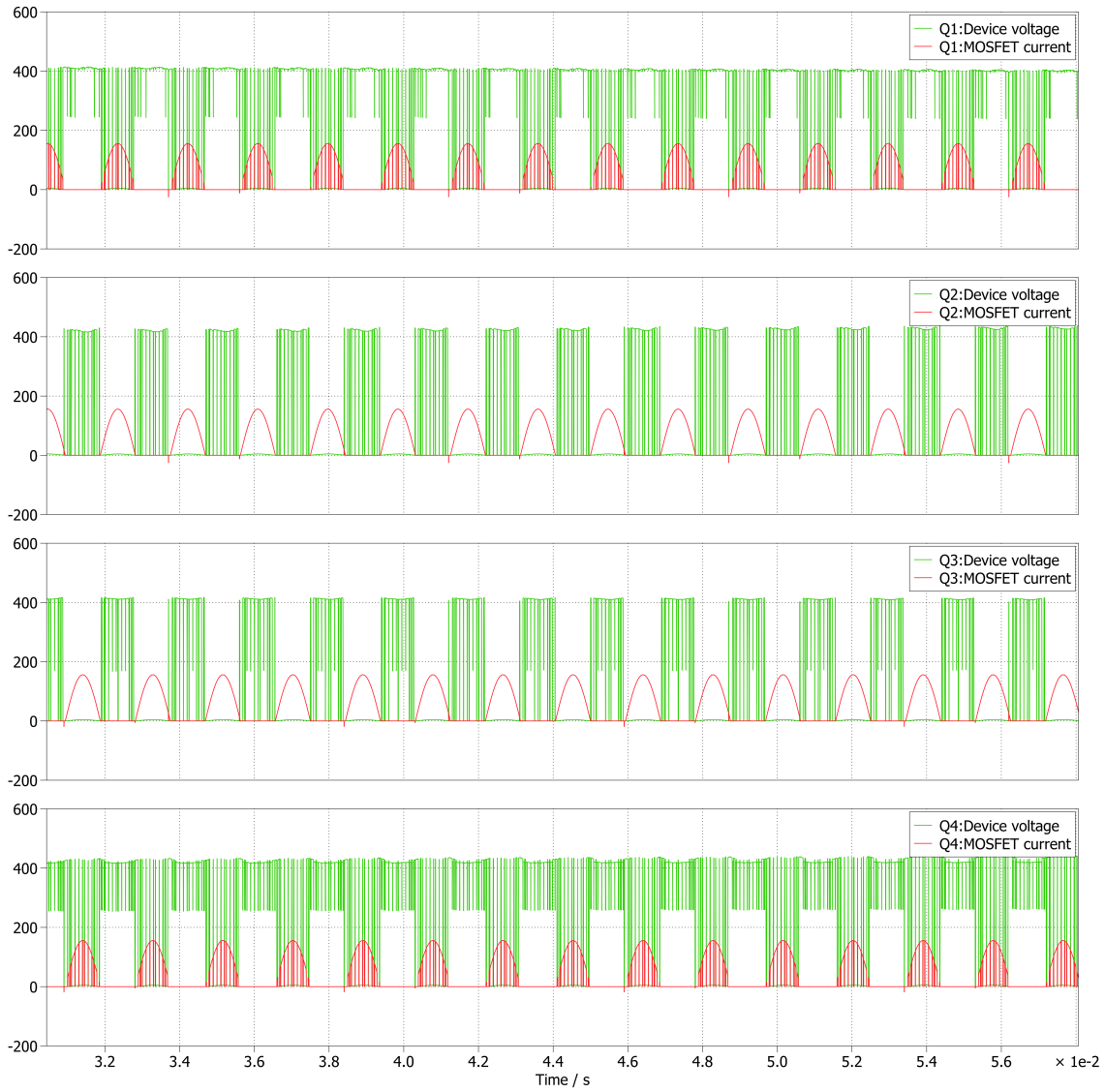



**Figure 6.13:** Voltage and current switching transients for switches in a phase.

In Figure 6.13, the switch current and switch voltage waveforms can be observed. Interestingly, the waveforms corresponding with switch 1 and switch 4 are overlapping, thus giving rise to power loss, which mathematically is a product of the voltage across a device and the current through the device. At the same time, we can also note that the waveforms corresponding to switch 2 and switch 3 are not overlapping

completely but only briefly - when the current pulse rises and the voltage pulse wanes off, and then again when the current pulse wanes off and the voltage pulse starts to rise. This result has been obtained for the motor mode operations, but the same principle also stands true for the regenerative braking operation mode. The only difference would be that switch 1 and switch 4 would see non-overlapping waveforms, and switch 2 and switch 3 would undergo overlapping voltage and current waveforms.

# 7
# Conclusion

In summary, the development of a gate driver circuit with variable slew rates tailored to different switches has been a pivotal achievement in our quest for optimized system performance. This approach effectively strikes a balance between reducing switching losses, enhancing overall efficiency, and minimizing conduction losses. Additionally, it has significantly contributed to mitigating electromagnetic interference (EMI), a critical consideration in ensuring electromagnetic compatibility.

By implementing gate driver control techniques, we've not only achieved precise and efficient switching but have also bolstered the overall robustness of our system. Furthermore, our in-depth study of EMI using FFT analysis within the frequency domain has played a crucial role in our efforts. This analytical approach has allowed us to identify and comprehend the specific frequency components contributing to interference, which ultimately lead to elevating the inverter performance.

Moreover, the use of a PLECS model for analyzing a 3-level inverter, controlled by the SVPWM (Space Vector Pulse Width Modulation) method, has enabled us to calculate and verify the accurate power losses within the inverter. This comprehensive approach ensures that we have a thorough understanding of the system's performance characteristics, providing invaluable insights for further enhancements.

In conclusion, these efforts underscore the importance of comprehensive approaches in Inverter design, enabling us to achieve a solution that optimizes performance, reliability, and electromagnetic compatibility by adjusting the slew-rate and controlling the gate driver and targeting the MOSFETs and arranging the MOSFETs to produce high overall efficiency with reduced EMI.

# Bibliography


[1] Dhanasekar R; Vijayaraja L; Kaushik V N; Prasanth S; Poornesh C K; Ragunathan A "An Overview of EV Batteries and Study Analysis on Charging Methodology" 2022 International Conference on Computer Communication and Informatics (ICCCI), 31 March 2022.

[2] Chithra M "An Overview of the Importance of Power Electronic Converters in Electric Vehicle Technologies" 2023 9th International Conference on Advanced Computing and Communication Systems (ICACCS), 05 May 2023.

[3] Zhi Cao; Amin Mahmoudi; Solmaz Kahourzade; Wen L. Soong "An Overview of Electric Motors for Electric Vehicles" 2021 31st Australasian Universities Power Engineering Conference (AUPEC), 16 November 2021.

[4] S. Weber, S. Guttowski, E. Hoene, W. John and H. Reichl, "EMI coupling from automotive traction systems," 2003 IEEE International Symposium on Electromagnetic Compatibility, 2003. EMC '03., Istanbul, Turkey, 2003, pp. 591-594 Vol.1, doi: 10.1109/ICSMC2.2003.1428328.

[5] B. Archambeault, S. Connor, M. S. Halligan, J. L. Drewniak, A. E. Ruehli "Electromagnetic Radiation Resulting From PCB/High-Density Connector Interfaces" IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 55, NO. 4, AUGUST 2013.

[6] https://www.testups.com/automotive-emc-standards-regulations/

[7] C. R. Paul "Introduction to Electromagnetic Compatibility" 2nd ed. Hoboken, NJ, USA: Wiley, 2006.

[8] F.B. Libano; R.A.M. Braga; L.N. de Souza "Introduction to electromagnetic compatibility in inverted-fed induction motor drives" 10th International Conference on Harmonics and Quality of Power. Proceedings (Cat. No.02EX630) 18 August 2003.

[9] L. B. Gravelle and P. F. Wilson "EMI/EMC in Printed Circuit Boards: A Literature Review" IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 34, NO. 2, MAY 1992.

[10] S. A. Azmi, K. H. Ahmed, S. J. Finney and B. W. Williams, "Comparative analysis between voltage and current source inverters in grid-connected application," IET Conference on Renewable Power Generation (RPG 2011), Edinburgh, 2011, pp. 1-6, doi: 10.1049/cp.2011.0138.

[11] N. Mohan, T. Undeland, W. Robbins, "Power Electronics – converters, applications and design", John Wileys & Sons inc., 2003

[12] H. Opsahl, "Design and Testing of Voltage Source Inverter and Motor Control System for Electric Vehicle," no. July, 2015.

[13] K.J. Egbe, B.R. Murali, "Modelling, Simulation and Investigation of Losses and Ripple in Traction Inverters", August 2021.

[14] M.K. Seshadri, V. Kanipakam, "Analysis of Multi-level Inverters for Electric Vehicle Application", October 2022.

[15] Surin Khomfoi Ph.D; Leon M. Tolbert Ph.D., P.E., "Multilevel Power Converters", Power Electronics Handbook (Third Edition), Butterworth-Heinemann, 2011, Pages 455-486, ISBN 9780123820365, https://doi.org/10.1016/B978-0-12-382036-5.00017-3.

[16] J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel Inverters: Survey of Topologies, Controls, and Applications," IEEE Transactions on Industry Applications, vol. 49, no. 4, Aug. 2002, pp. 724-738.

[17] J. S. Lai and F. Z. Peng, "Multilevel Converters-A new Breed of Power Converters," IEEE Trans. Ind. Applicat., vol.32,pp. 509-517, May/June 1996.

[18] A. Krishna R and L. P. Suresh, "A brief review on multi level inverter topologies," 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), Nagercoil, India, 2016, pp. 1-6, doi: 10.1109/ICCPCT.2016.7530373

[19] L. M. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel Converters for Large Electric drives," IEEE Trans. Ind. Applicat.,vol.35,pp. 36-44, Jan./Feb. 1999.

[20] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kw single-phase seven level flying capacitor multilevel inverter with an active energy buffer," IEEE Transactions on Power Electronics, vol. 32, no. 11, pp. 8570–8581, 2017.

[21] Dnyaneshwar D. Khairnar, V. M. Deshmukh. Review Study on Topologies of Multilevel Inverters. INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH DEVELOPMENT Vol 3 Issue 5, 19-24.

[22] Mailah Nashiren, Bashi S.M., Aris Ishak, Mariu N. (2009). Neutral-Point-Clamped Multilevel Inverter Using Space Vector Modulation. European Journal of Scientific Research. 28(1) 82-91.

[23] R. Manikandan, P. Selvakumar, N. Thillaikarasi "Simple Gate Driver Circuit for Higher Level Inverters" 2023 9th International Conference on Electrical Energy Systems (ICEES).

[24] Nadir Idir, Robert Bausière,and Jean Jacques Franchaud "Active Gate Voltage Control of Turn-on di=dt and Turn-off dv=dt in Insulated Gate Transistors" IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 21, NO. 4, JULY 2006.

[25] Alejandro Paredes Camacho, Vicent Sala, Hamidreza Ghorban, Jose Luis Romeral Martinez "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory" IEEE Transactions on Industrial Electronics Volume: 64, Issue: 11, November 2017.

[26] N. Idir, R. Bausiere, and J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," Power Electronics, IEEE Transactions on, vol. 21, no. 4, pp. 849–855, 2006.

[27] A. AlHoussein, H. Alawieh, Z. Riah and Y. Azzouz, "A New Modeling Approach for Predicting the Static and Dynamic Behavior of SiC Power MOSFETs," 2018

International Symposium on Electromagnetic Compatibility (EMC EUROPE), Amsterdam, Netherlands.

[28] T. Shimomura, T. Ikari, A. Okubo, R. Yamada, K. Numakura and T. Hayashi, "High speed dV/dt control technology for SiC power module for EV/HEV inverters," 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 2017

[29] S. S. Ahmad, G. Narayanan "Double pulse test based switching characterization of SiC MOSFET" 2017 National Power Electronics Conference (NPEC).

[30] Bendik Nybakk Torsæte, "Evaluation of Switching Characteristics, Switching Losses and Snubber Design for a Full SiC Half-Bridge Power Module" thesis - Norwegian university of science and technology.

[31] Jan Gottschlich and Rik W. De Doncker "A Programmable Gate Driver for Power Semiconductor Switching Loss Characterization" IEEE PEDS 2015.

[32] N. Oswald, P. Anthony, N. McNeill, and B. Stark,"An experimental investigation of the tradeoff between switching losses and emi generation with hard switched all-si, si-sic, and all-sic device combinations" Power Electronics, IEEE Transactions on, vol. 29,no. 5, pp. 2393–2407, 2014.

[33] Ashutosh Kumar, Ravi Raushan and R.K. Mandal And Pratyushgauri, "Design And Analysis Of The Gate Driver Circuit For Power Semiconductor Switches", International Conference On Emerging Forntiers In Electrical And Electronic Technology (ICEFEET), pp. 10-11, July 2020.

[34] Jun-Hyuk Choi, Yong-Su Noh, Jin-Hong Kim, "Development of Active Gate Driver to Reduce Switching Loss for Inverter System",2019 the 7th International Conference on Smart Energy Grid Engineering.

[35] KULKARNI, Sumeet, Prakash 80807 München (DE), EUROPEAN PATENT SPECIFICATION, Priority: 07.06.2013 US 201361832626 P27.11.2013 US 201314092689, Texas Instruments Incorporated Dallas, TX 75265-5474 (US)

[36] Chin-Yang Chen, Hsinchu City (TW), United States Patent Application Publication, "GATE DRIVER FOR SWITCHING POWER MOSFET", Pub. No.: US 2009/0237126A1 Pub. Date: Sep. 24, 2009.

[37] Noge, Yuichi and Shoyama, Masahito,"High Bandwidth Active Gate Driver for Simultaneous Reduction of Switching Surge and Switching Loss of SiC-MOSFET",2022 International Power Electronics Conference.

[38] A. Alhoussein, H. Alawieh, R. Zouheir and Y. Azzouz, "Optimising a New SiC MOSET Model's Parameters Using FFT Analysis," 2019 IEEE 13th International Conference on Power Electronics and Drive Systems (PEDS), Toulouse, France, 2019.

[39] D. Han et al., "An Integrated Multi-level Active Gate Driver for SiC Power Modules," 2022 IEEE Transportation Electrification Conference Expo (ITEC), Anaheim, CA, USA, 2022.

[40] Y. Wei, L. Du, X. Du and A. Mantooth, "Multi-level Active Gate Driver for SiC MOSFETs with Paralleling Operation," 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), Cartagena, Colombia, 2021

[41] M. Vilathgamuwa, J. Deng and K. J. Tseng, "EMI suppression with switching frequency modulated DC-DC converters," in IEEE Industry Application.

[42] D. Zhuolin, Z. Dong, F. Tao and W. Xuhui, "Prediction of conducted EMI in three phase inverters by simulation method," 2017 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific), Harbin, China, 2017.

[43] Z. Li, R. W. Maier, M. -M. Bakran, F. -J. Niedernostheide and D. Domes, "A Simulation Model for SiC MOSFET Switching Transients Controlled by an Adaptive Gate Driver with the Capability of Reducing Switching Losses and EMI across the Full Operating Range," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022.

[44] A. Acquaviva and T. Thiringer, "Energy efficiency of a SiC MOSFET propulsion inverter accounting for the MOSFET's reverse conduction and the blanking time," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, Poland, 2017,

[45] J. W. Kolar, H. Ertl and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting, Seattle, WA, USA, 1990.

[46] Bharatiraja, C. Padmanaban, Sanjeevikumar Blaabjerg, F.. (2018). Investigation and Comparative Analysis of Advanced PWM Techniques for Three-Phase Three-Level NPC-MLI Drives. Electric Power Components and Systems. 10.1080/15325008.2018.1445142.

[47] F. Chen, W. Qiao, H. Wang and L. Qu, "A Simple Zero-Sequence Voltage Injection Method for Carrier-Based Pulsewidth Modulation of the Three-Level NPC Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 4, pp. 4687-4699, Aug. 2021, doi: 10.1109/JESTPE.2020.3012726.

[48] V. Ramu, P. Satish Kumar, G.N. Srinivas, "LSPWM, PSPWM and NLCPWM on multilevel inverters with reduced number of switches", Materials Today: Proceedings 54 (2022) 710–727, https://doi.org/10.1016/j.matpr.2021.10.4102214-7853/ 2021 Elsevier.

[49] V. Jayakumar, B. Chokkalingam and J. L. Munda, "A Comprehensive Review on Space Vector Modulation Techniques for Neutral Point Clamped Multi-Level Inverters" in IEEE Access, vol. 9, pp. 112104-112144, 2021, doi: 10.1109/ACCESS.2021.3100346.

[50] Bengi Tolunay, "Space Vector Pulse Width Modulation for Three-Level Converters - a LabVIEW Implementation", Uppsala Universitet, February 2012.

[51] D. Dujic, G. Grandi, M. Jones and E. Levi, "A Space Vector PWM Scheme for Multifrequency Output Voltage Generation With Multiphase Voltage-Source Inverters," in IEEE Transactions on Industrial Electronics, vol. 55, no. 5, pp. 1943-1955, May 2008, doi: 10.1109/TIE.2008.918468.

[52] A. K. Gupta and A. M. Khambadkone, "A Space Vector PWM Scheme for Multilevel Inverters Based on Two-Level Space Vector PWM," in IEEE Transactions on Industrial Electronics, vol. 53, no. 5, pp. 1631-1639, Oct. 2006, doi: 10.1109/TIE.2006.881989.

[53] X. Lin, S. Gao, J. Li, H. Lei and Y. Kang, "A new control strategy to balance neutral-point voltage in three-level NPC inverter," 8th International Conference

on Power Electronics - ECCE Asia, Jeju, Korea (South), 2011, pp. 2593-2597, doi: 10.1109/ICPE.2011.5944742.

[54] Keqing Qu, Xi Jin, Yuehong Xing, Zuojin Ding and W. Chen, "A SVPWM control strategy for NPC three-level inverter," 2011 IEEE Power Engineering and Automation Conference, Wuhan, China, 2011, pp. 256-259, doi: 10.1109/PEAM.2011.6134849.

[55] M. Trabelsi, L. Ben-Brahim, T. Yokoyama, A. Kawamura, R. Kurosawa and T. Yoshino, "An improved SVPWM method for multilevel inverters," 2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC), Novi Sad, Serbia, 2012, pp. LS5c.1-1-LS5c.1-7, doi: 10.1109/EPEPEMC.2012.6397476.

[56] A. Panda, G. Dyanamina and R. K. Singh, "MATLAB Simulation of Space Vector Pulse Width Modulation for 3-level NPC Inverter and 2-level Inverter," 2021 International Conference on Sustainable Energy and Future Electric Transportation (SEFET), Hyderabad, India, 2021, pp. 1-5, doi: 10.1109/SeFet48154.2021.9375668

[57] Soumya S, Dr. B. V. Sumangala, "Application Of Space Vector Modulation Technique For Three Level Neutral Point Clamped Inverters", International Journal of Engineering Research  Technology (IJERT) ISSN: 2278-0181 www.ijert.org Vol. 2 Issue 6, June - 2013

[58] G. Mademlis, Y. Liu, N. Sharma and X. Huang, "Circulating Current Reduction in Common DC-Link Power-HIL for Drives using SVM with Zero-Sequence Compensation," IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, Singapore, 2020, pp. 4673-4678, doi: 10.1109/IECON43393.2020.9254744

[59] Jonathan Dodge, "3L-ANPC vs. 3L-NPC Inverters" APPLICATION NOTE UnitedSiC_AN0023 – February 2020, Unites SiC

[60] Laszlo Balogh, "Fundamentals of MOSFET and IGBT Gate Driver Circuits", Application Report SLUA618A–March 2017–Revised October 2018

[61] J. Zhou, S. -c. Shie and P. -t. Cheng, "A Loss Redistribution Technique for the Power Devices in the NPC Converter by PWM Zero-Sequence Injection," in IEEE Transactions on Power Electronics, vol. 36, no. 6, pp. 7049-7059, June 2021, doi: 10.1109/TPEL.2020.3035189

[62] M. H. Ahmed, M. Wang, M. A. S. Hassan and I. Ullah, "Power Loss Model and Efficiency Analysis of Three-Phase Inverter Based on SiC MOSFETs for PV Applications," in IEEE Access, vol. 7, pp. 75768-75781, 2019, doi: 10.1109/ACCESS.2019.2922741.

[63] S. Bhattacharya, "Three-Level Discontinuous PWM for Loss and Thermal Redistribution of T-NPC Inverter at Low Modulation Index," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 1, no. 2, pp. 143-151, Oct. 2020, doi: 10.1109/JESTIE.2020.3014821.

[64] Gustaver, M. (2020) A Chalmers University of Technology Master's thesis template for LaTeX. Unpublished.

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