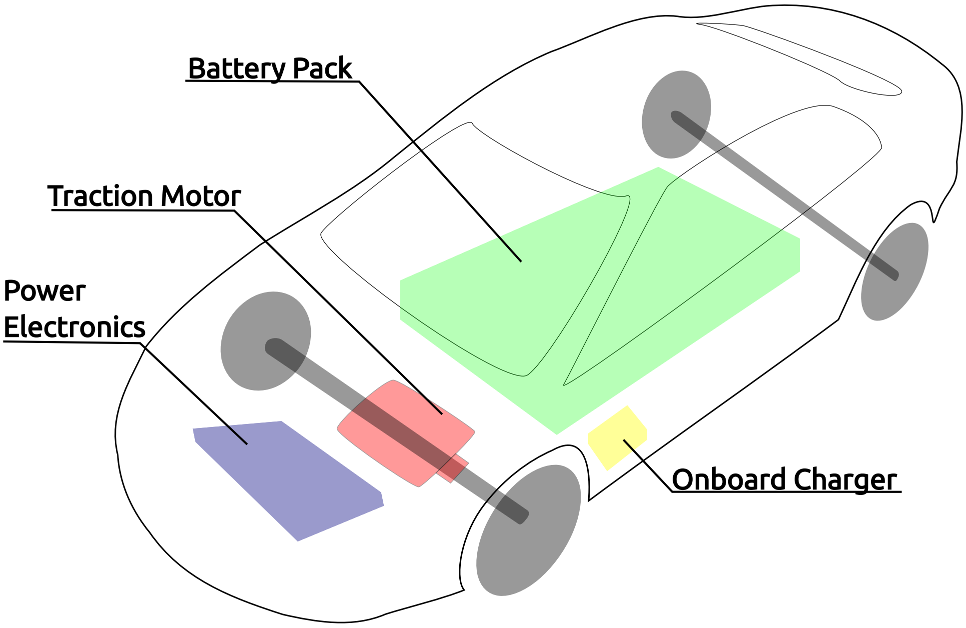

Condition Monitoring of DC-Link Capacitor in Traction Inverters

Master's thesis in Systems, Control and Mechatronics

Kushal Kumar Chengavi Udaya Kumar

DEPARTMENT OF ELECTRICAL ENGINEERING
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2025
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MASTER’S THESIS 2025

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KUSHAL KUMAR CHENGAVI UDAYA KUMAR

Supervisors: Dr. Nimananda Sharma & Dr. Artem Rodionov, Department of Electrical Engineering
Examiner: Prof. Yujing Liu, Department of Electrical Engineering

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Department of Electrical Enginnering
Division of Systems and Control
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: Key components of battery electric vehicle.

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Abstract

With the increasing use of battery electric vehicles (BEVs) in the road transport sector for driving the decarbonization of industry poses additional challenge for reliability. The DC-link capacitor which links the power source, typically a battery, with the load - an electric machine, performs a critical function of reducing the voltage and current ripple induced mainly by the switching action of IGBTs in inverter module. Metallized polypropylene film (MPPF) capacitor are used in traction application which carries out its operation by providing an instaneous power by acting as a reservoir and limiting the charge and discharge cycle stress on the main power source. This continuous usage induces high stress mainly due to over voltage or surge current eventually leading to wearout of dielectric medium. These factors make capacitors the weakest link in the drive system which alone contributes to about 30% of all the failures.

Reliability of these components is thus crucial for safe operation of the drive system. Condition monitoring (CM) helps to address these challenges by providing a means of continuous monitoring of some of the health indicators like capacitance, equivalent series resistance (ESR) and dissipation factor (DF). As MPPF capacitors have relatively small ESR and DF values, the thesis will be focused on only utilizing capacitance as the estimation parameter. Although many literature study have proposed the offline monitoring technique, it requries a direct access of capacitor terminals which in traction application demands the converter module to be dismantled. As this is a major inconvenience, only online CM methods are considered for the comprehensive study in this thesis. The DC-link capacitor has a wide range of application ranging from adjustable speed drives (ASD) to DC/DC convereters and power factor correction (PFC), photovoltaic (PV) grid. As most of the methods presented in literature depend on certain specific parameter or hardware present in the topology, only ASD systems were examined as the topology closely relates to that of traction EVs.

Whilst many of the approaches proposed in ASD system are online, they still rely on additional hardware like capacitor current sensor or measurement circuit to accurately estimate the health of the capacitor. Applying these techniques directly to traction application will induce additional stray inductance and cost overhead. Two methods were found suitable, one of which is completely online that leverages the zero state working of inverters and estimate the capacitance by change in voltage to current accumulated during which the capacitor is charged. The current is the same as the battery current and can be accurately measured with an existing sensor. Another method is a quasi-online approach is implemented when the motor is stationary and the capacitor is already charged upto some level. A unipolar pulse width modulation strategy is utilized to partially discharge the capacitor through any of the two stator windings and capacitance is estimated by measuring the change in DC-link voltage and current discharged through windings. Both the methods were modelled and evaulated in PLECS/Simulink environment and results found that the discharge method was more accurate at $< 0.05\%$ error in estimation than its counterpart at $< 0.4\%$.

Keywords: BEVs, Traction inverter, MPPF capacitor, Condition monitoring, DC-link.

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Kushal Kumar Chengavi Udaya Kumar, Göteborg, February 2025

List of Acronyms

AC Alternating Current.
AEC Aluminium Electrolytic Capacitor.
ASD Adjustable Speed Drives.

$BaTiO_3$ Barium Titanate.
BEVs Battery Electric Vehicles.

$CaZrO_3$ Calcium Zirconate.
CM Condition Monitoring.
CO_2 Carbon Dioxide.
CSI Current Source Inverters.

DC Direct Current.
DFIG Doubly Fed Induction Generator.

ESL Equivalent Series Inductance.
ESR Equivalent Series Resistance.

FFT Fast Fourier Transform.
FOC Field Oriented Control.

IGBT Insulated Gate Bipolar Junction Transistor.
ILS Iterative Least Square.

LMS Least Mean Square.

MCU Micro Control Unit.
MLCC Multi-layer Ceramic Capacitor.
MNR Multivariate Non-linear Regression.
MOSFET Metal Oxide Semiconductor Field Effect Transistor.
MPPF Metalized Poly-Propylene Film.

PAA Parameter Adaptation Algorithm.
PC Polycarbonate.
PCB Printed Circuit Board.
PET Polyester.
PFC Power Factor Correction.
PLECS Piece-wise Linear Electrical Circuit Simulation.
PMSM Permanent Magnet Synchronous Motor.

PP Polypropylene.
PS Polystyrene.
PTFE Polyfluorotetraethylene.
PV Photo-Voltaic.
PWM Pulse Width Modulation.

RLS Recursive Least Squares.
RMS Root Mean Square.
RUL Remaining Useful Life.

SDG Sustainable Development Goals.
SNR Signal to Noise Ratio.
SPWM Sinusoidal Pulse Width Modulation.
SVPWM Space Vector Pulse Width Modulation.

THD Total Harmonic Distortion.
TiO$_2$ Titanium dioxide.

VEN Variable Electrical Network.
VFD Variable Frequency Drives.
VSI Voltage Source Inverters.

Nomenclature

Below is the nomenclature of indices, sets, parameters, and variables that have been used throughout this thesis.

Indices

a, b, c	Line phase parameters
i, j	Indices for distribution network buses
t	Index for time step

Variables

V_{a}	Line voltage of phase a with neutral
V_{b}	Line voltage of phase b with neutral
V_{c}	Line voltage of phase c with neutral
V_{ab}	Line to line voltage between phase a & b
V_{bc}	Line to line voltage between phase b & c
V_{ca}	Line to line voltage between phase c & a
V_{ref}	Reference voltage
U_{bat}	DC-link voltage available across battery terminal
U_{dc}	DC-link voltage applied to the capacitor
i_{as}	Line current of phase a
i_{bs}	Line current of phase b
i_{cs}	Line current of phase c
i_{α}	Line current of α axis
i_{β}	Line current of β axis
i_{d}	Line current of direct (d) axis

i_q	Line current of quadrature (q) axis
i_bat	Current drawn from battery
i_inv	Current drawn from inverter
i_cap	Current drawn from capacitor
i_RMS	Root mean square value of current
C_dc	Capacitance of DC-link capacitor
θ_d	Rotation angle of d-axis

Parameters

C	Capacitance in Farad
ϵ_o	absolute permittivity of dielectric
A	Effective area of overlap between plates
d	Distance between plates in meters
Q	Total charge in coulombs
R_ESR	Equivalent series resistance of capacitor
L_ESL	Equivalent series inductance of capacitor
ω	Angular frequency
f	Frequency
T	Temperature in $^\circ C$
R_θ	Thermal resistance
t_on	Turn-on time of IGBT
t_off	Turn-off time of IGBT
$S_1, S_2, S_3, S_4, S_5, S_6$	Inverter switches
α,β	Axes of clarke transformation
P_T	Total power loss through IGBT
P_ON	Turn-on power loss from IGBT
P_OFF	Turn-off power loss from IGBT
P_SW	Switching power loss from IGBT
P_CON	Conduction power loss from IGBT

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1

Introduction

1.1 Background

Fossil fuel based emissions are major cause for climate change around the world. This results in increase of harmful particles in the atmosphere and significant increase in atmospheric temperature [1]. It can be seen from the below Fig. 1.1 that road transport sector has a higher share in carbon dioxide (CO_2) emissions than other means of transport [2]. Inline with goal 13 of United Nations sustainable development goals (SDG) for 2030, the shift towards electrification helps to tackle this issue as an alternative to meet the energy demands of society. Battery electric vehicles (BEVs) play a pivotal role in helping transition towards clean energy systems by reducing the emission footprint and dependance on non-renewable energy systems [3].

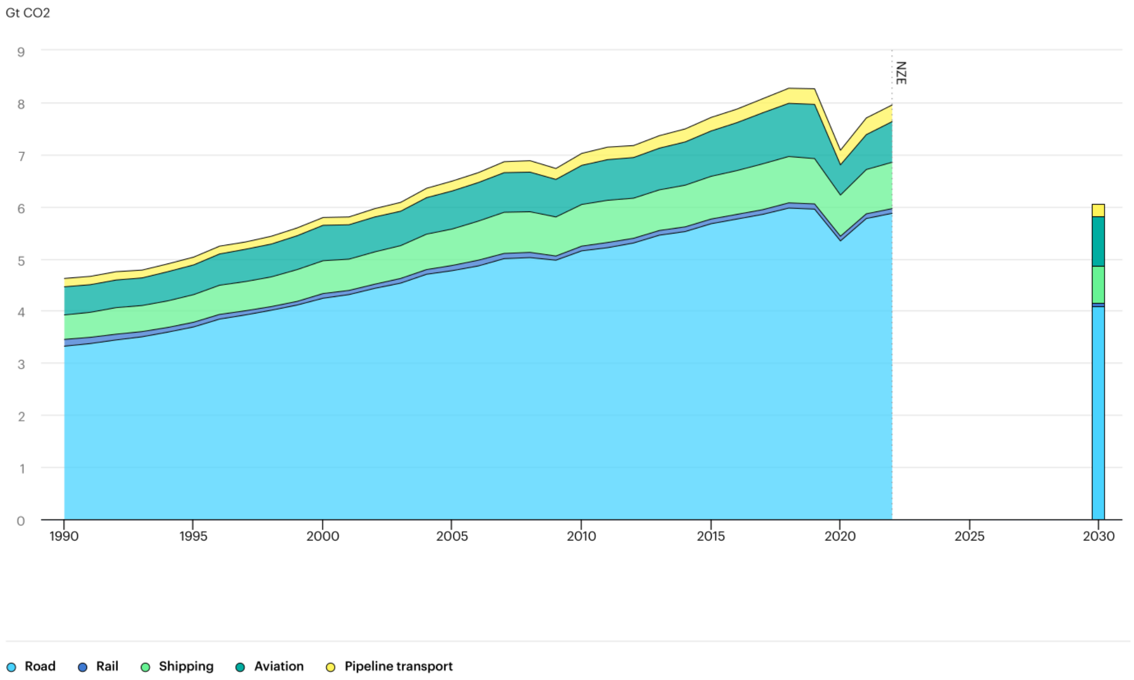

Figure 1.1: Global CO_2 emissions from transport by sub-sector in the net zero scenario, 2000-2030[2]

A typical BEV is shown in Fig. 1.2 which consists of many safety critical components namely battery pack, electric motor, on-board charger and electronics. Traction battery helps in storage of electrical energy as chemical energy which can be charged and discharged. The charging of a battery is carried out with the help of an external electrical source using an on-board charger. The inverter helps in converting the direct current (DC) power from the battery into a 3-phase alternating current (AC) power to drive the electric motor. A thermal system helps to monitor and regulate the temperature of all critical components during operation.

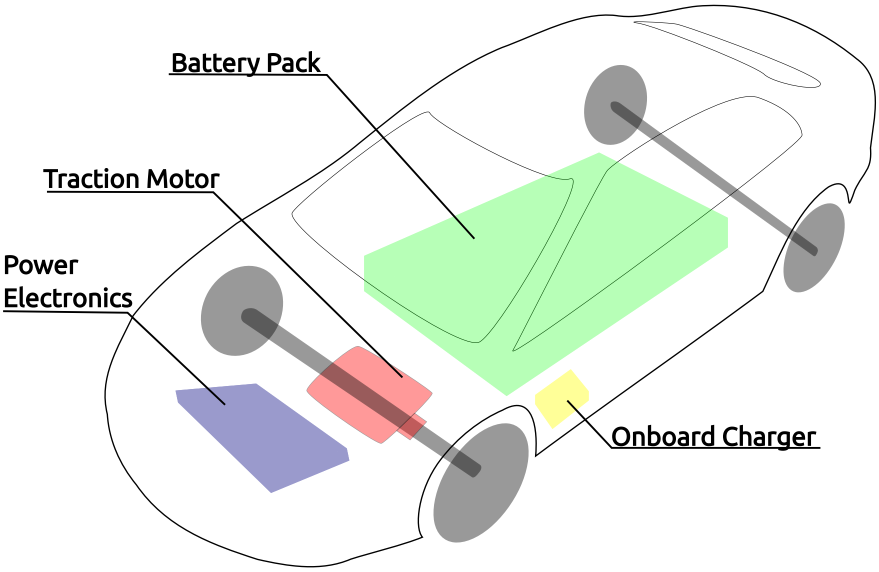

Figure 1.2: Key components of battery electric vehicle

1.1.1 Inverter technology

An inverter is a power converter device which helps in converting and controlling electrical power by utilizing power switches such as insulated gate bipolar transistor (IGBT) or metal oxide semiconductor field effect transistor (MOSFET). A typical inverter module is shown in Fig. 1.3 which includes a printed circuit board (PCB) to control the gate signals for the power switches by processing the signals from sensors and powertrain logic. A large bus bar helps in interconnecting all the subcomponents with the external cable interface. The power module (semiconductor switches and diode) arranged in specific transistor bridge configuration directs the voltage and inturn control the power transmitted. A heat sink is also present to cool the heat generated by the switching action mainly from the power module. Inverters can be broadly classified into two types as voltage source inverters (VSI) and current source inverters (CSI) based on the type of source available as input. As the name implies VSI converts a constant voltage source into AC and CSI converts the power from a constant current source. Since in traction application, a battery is used which provides a constant voltage across the terminal, VSI system is used as the power converting device.

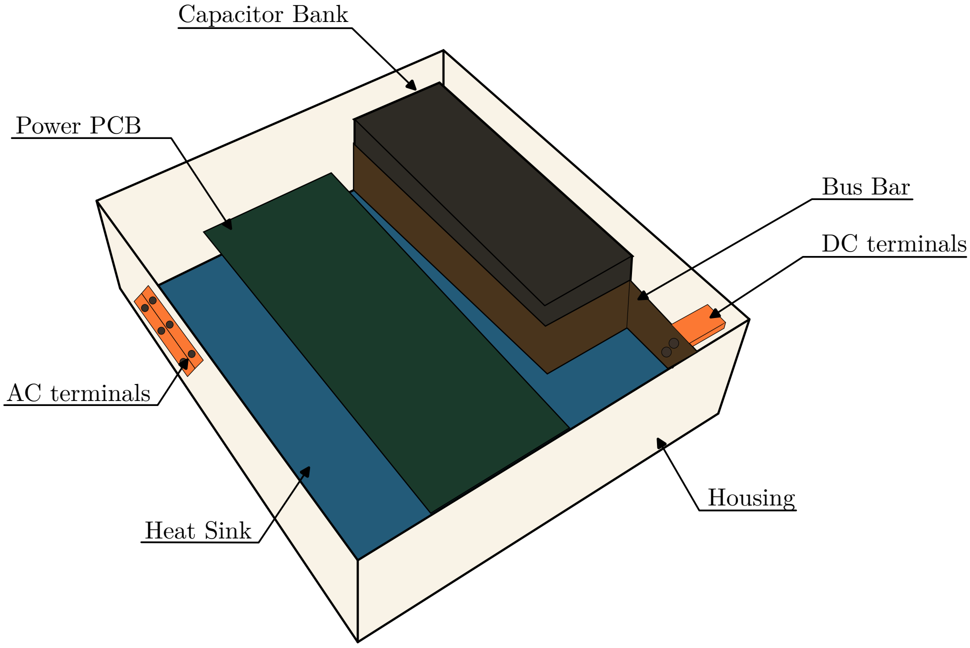

Figure 1.3: Key components of a traction inverter

Based on the voltage levels used to generate the desired output, inverters can be classified as two, three, five and so on. The increase in levels decreases the voltage handled by each switch and rate of voltage change ($\frac{dV}{dt}$) thus lowering the total hormonic distortion (THD) caused by switching action. However higher levels of an inverter increases the complexity of the system [4]. A basic two level inverter divides the applied voltage (U_{dc}) into two voltage levels $+\frac{U_{\mathrm{dc}}}{2}$ and $-\frac{U_{\mathrm{dc}}}{2}$ as shown in the Fig. 1.4.

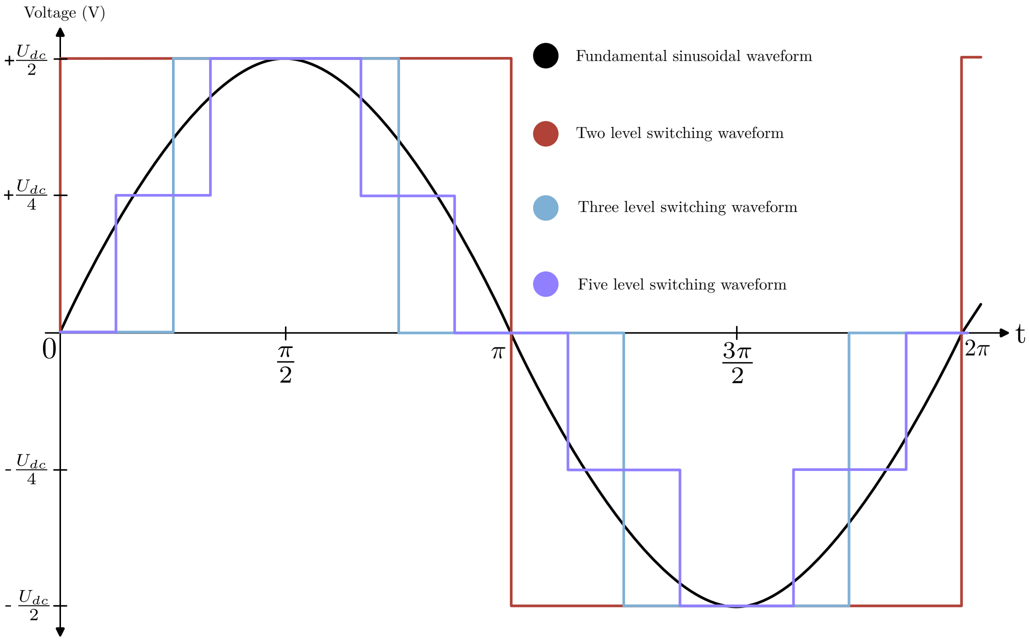

Figure 1.4: Basic multilevel inverter output waveforms

In order to achieve these voltage levels, the power switches have to be arranged in certain configuration. Although many different possibilities exist, a simple arrangement is a H-bridge configuration shown in Fig. 1.5. Each of the leg consisting of two switches which are connected to each phase of the motor stator windings. All the three phase legs are then connected to the battery via a capacitor as the DC-link.

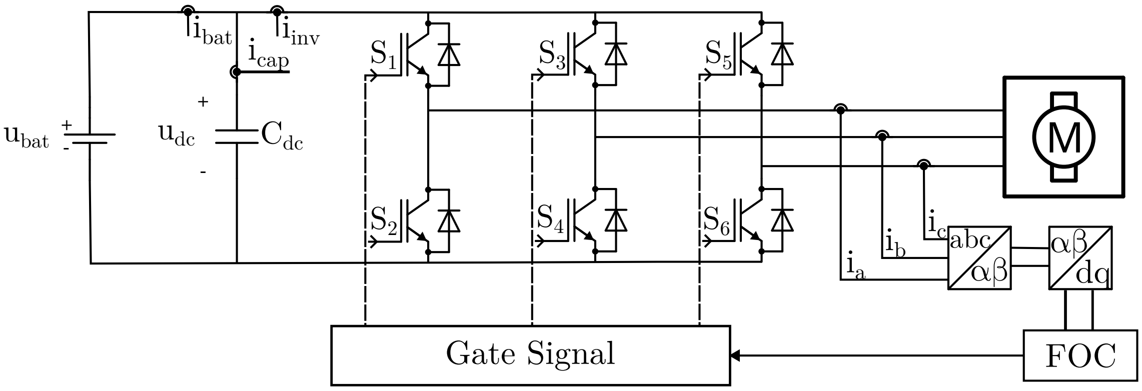

Figure 1.5: Two level inverter topology

Ideally, the switches should turn ON and OFF instantaneously. However, due to many factors such as delay and parasitic capacitance, the actual waveform is altered. Fig. 1.6 shows the comparision between ideal and non-ideal switching waveform of IGBTs [5]. t_{on} and t_{off} represents the turn ON and turn OFF delay times for the IGBT. The delay is mainly caused by the transport of signal from the controller to the switch. These factors can be compensated by introducing a dead time in between the switching operation to safeguard the switches from short circuit. It is worth noting that the ON/OFF characterstics is significantly affected by operating temperature of the power module.

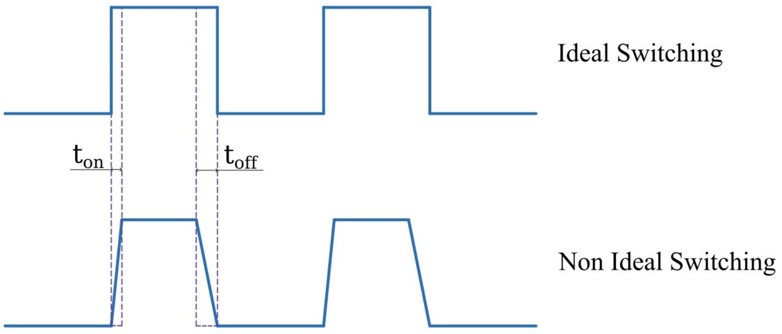

Figure 1.6: Switching waveform of IGBT

The power loss of inverter module can be attributed mainly to losses from IGBTs and anti-parallel diodes. The switching action is responsible for power loss in IGBTs which can be further broken down into conduction and turn ON/OFF loss [6]. Conduction loss is resulted due to the resistance to flow of current and the power factor at the time of operation. Also the type of modulation used for the control of switches can influence the power loss of the module.

$$P_{\mathrm{T}} = P_{\mathrm{con}} + P_{\mathrm{SW}} = P_{\mathrm{con}} + P_{\mathrm{ON}} + P_{\mathrm{OFF}} \tag{1.1}$$

1.1.2 Modulation technique

Serveral modulation techniques can be utilized to improve the resolution of output. One such modulation method is the pulse width modulation (PWM) where the duty cycle (width) of the pulse is varied to match with the average value of the waveform in that particular switching period. Thus achieving the desired sinusoidal output waveform.

A triangular wave is taken as carrier and compared against the reference signal. Whenever the reference signal is greater than the carrier wave, the gate signal for the switch will be high. By choosing the frequency of carrier wave to be much higher than the reference signal, precise control of voltage and inturn the current and power can be obtained.

A sinusoidal pulse width modulation (SPWM) is one such modulation strategy usually used for single phase inverters where, a sine wave is used as the reference signal to generate and control the output. As it is evident from Fig. 1.7, in a single switching period of the carrier wave, the average value of pulse is directly proportional to the voltage of reference signal in that period. By increasing the carrier frequency, the voltage generated from the PWM converges to the actual reference voltage.

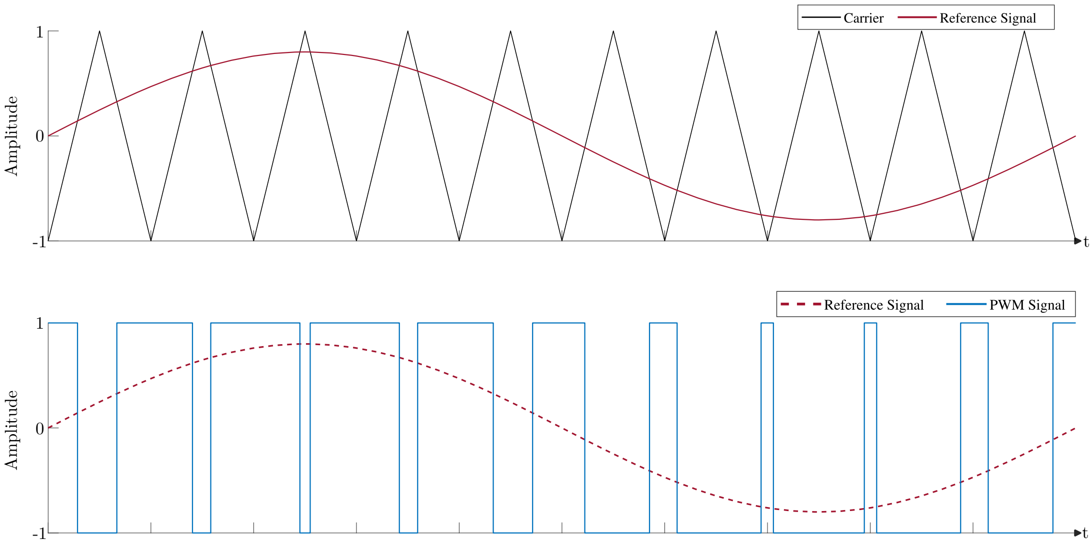

Figure 1.7: Sinusoidal pulse width modulation

In case of controlling a three phase AC motor, a much more robust approach is required as the lines can be easily shorted if two switches of the same leg are required to be turned ON at the same time. Space vector pulse width modulation (SVPWM) solves this issue by incorporating a complimentary switching sequence for the switches in the same leg. Thus, it is possible to generate eight different ($2^3 = 8$) states by the combination of different switching action as shown in Table 1.1. Out of the eight states, two states ({000} and {111}) correspond to zero states as the output voltage is zero. The remaining six active states can then be varied in combination to produce a desired waveform.

Table 1.1: States of space vector modulation

State Vectors	$\mathbf{S_1}$	$\mathbf{S_3}$	$\mathbf{S_5}$	$\mathbf{V_{ab}}$	$\mathbf{V_{bc}}$	$\mathbf{V_{ca}}$
{000}	OFF	OFF	OFF	0	0	0
{100}	ON	OFF	OFF	$+\frac{U_{dc}}{2}$	0	$-\frac{U_{dc}}{2}$
{110}	ON	ON	OFF	0	$+\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$
{010}	OFF	ON	OFF	$-\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	0
{011}	OFF	ON	ON	$-\frac{U_{dc}}{2}$	0	$+\frac{U_{dc}}{2}$
{001}	OFF	OFF	ON	0	$-\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$
{101}	ON	OFF	ON	$+\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	0
{111}	ON	ON	ON	0	0	0

The six active states can also be represented using a hexagon as shown in the Fig. 1.8. The states are arranged such as to obtain only one state change from its adjacent state. Thus, any rotating vector can be resolved with the two active vectors made by the state vectors in the corresponding sector. The zero states are also used to adjust the magnitude of resultant voltage.

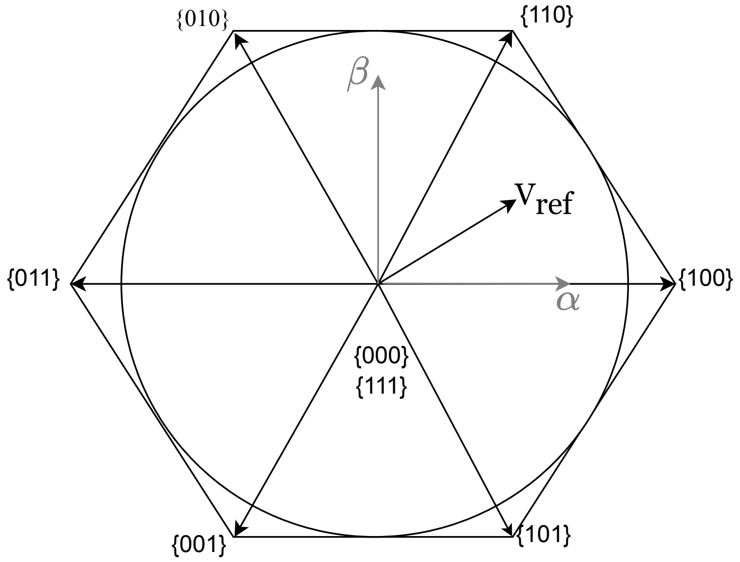

Figure 1.8: Active states arranged in space vector configuration

Permanent magnet synchronous motor (PMSM) is generally chosen as the drive for traction application. The main challenge in this type of motor is to excite the motor which maximize the torque output with minimum current possible as it would directly impact battery capacity sizing and inturn the range of vehicle. Many literature studies have been done and concluded that maximum torque is achieved when the rotor (magnetic pole) is excited with flux orthogonal to the magnetic field produced by the rotor [7]. Field oriented control (FOC) tries to address this by implementing a strategy to control the current in order to maximizing the torque output.

The output waveforms of the phase current are varying as the motor rotates. Having a varying reference for the control will be difficult for the system to track. Thus two new coordinate transformations (clarke and park) are utilized to simplify the implementation.

The clarke transformation uses two frames (α and β), which are orthogonally placed to each other. One of the coordinate axis is usually coincided with one phase of system. The coordinate frames are stationary with respect to the stationary housing of the motor. Each of the phase current parameters are transformed into the two axes by following the equation:

$$i_\alpha = \frac{3}{2} i_\mathrm{a} \tag{1.2}$$

$$i_\beta = \frac{\sqrt{3}}{2} i_\mathrm{b} - \frac{\sqrt{3}}{2} i_\mathrm{c} \tag{1.3}$$

The park transformation uses the previously obtained α and β references and transforms into a rotating coordinate frame i.e., direct (d) and quadrature (q) frame which are again orthogonal to each other. The d axis is chosen to be along the direction of magnetic pole of rotor and thus rotates along with it as the motor is actuated. The transformation can be achieved by the following equations:

$$i_{\mathrm{d}} = -i_{\alpha} \cdot sin(\theta_{\mathrm{d}}) + i_{\beta} \cdot cos(\theta_{\mathrm{d}}) \tag{1.4}$$

$$i_{\mathrm{q}} = i_{\alpha} \cdot cos(\theta_{\mathrm{d}}) + i_{\beta} \cdot sin(\theta_{\mathrm{d}}) \tag{1.5}$$

Thus, the current obtained after doing both clarke and park transformation is a constant value and easily trackable using a controller. This method also helps in lowering the control parameters from three to two at the expense of phase information getting lost during the transformation of the current.

1.1.3 Failures

Many components of a power converter module are subjected to constant stresses like temperature cycling, moisture and vibrations. These factors causes them to wear and aids in deterioration of their performance over time and eventually reach the end of their designed lifetime. The power module dissipate the maximum amount of heat generated by the switching action of semiconductor switches [8]. This results in fatigue of the connections like the bond wire and thermal paste. Vibrations can also cause stress on the solder joints of components in PCB which eventually results in poor contacts. A DC-link capacitor bridges the connection between the battery and the power module and act as an auxillary energy storage system which helps in absorbing the ripple in voltage due to the switching action of transistors. This makes the component vulnerable to transients in the system and stresses the component further. A pie chart shown in Fig. 1.9 depicts the distribution of root cause of failures in the components of a power system. It is evident that capacitors occupy a significant portion than any other component [9].

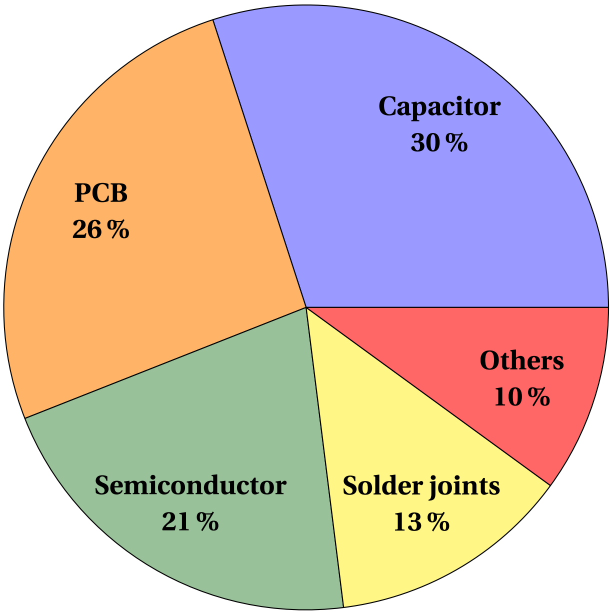

Figure 1.9: Failure root cause distribution[9]

Typically metalized poly-propylene film (MPPF) capacitors are used in traction inverter application due to the ability of self-healing property. These capacitors have a poly-propylene film as the dielectric medium with a thin layer of metal deposited inbetween the layers which function as electrodes. Many factors can influence the presence of minor flaws in the dielectric which becomes sensitive to the applied voltage. Whenever a surge in input voltage occur, these defects causes a minor breakdown leading to arc formation. The surrounding healthy dielectric medium restricts the propogation of the produced arc and thus self-healing the capacitor. But as the frequency of these minor breakdown increases, reduces the effective surface area and thereby decreasing the capacitance [10].

Traditionally, the failure of the capacitors is noticed only when a catastrophic failure happens affecting the function of entire system or by carrying out a periodic maintenance activity where we test the capacitor manually by taking it out and replace if needed. This approach is very inconvenient and can be laborious.

Hence a novel approach to detect these failures at an earlier stage is cruical for reliable and safe operation of the system. Condition monitoring (CM) of DC-link capacitors tries to address this issue by monitoring of key parameters and detecting a faulty condition earlier and help in notifying to perform a predictive maintenance activity.

1.2 Aim

The aim of this thesis is to provide a comprehensive and robust method for achieving an accurate monitoring of DC-link capacitors equipped in traction inverters. Accurate detection and prognosis of capacitor health is crucial in order to distinguish between a healthy state and a failed state. Since the inverters spans a wide variety of application areas, the proposed method should be modular enough to accomodate for small changes in the topology. Analaysis of different parmater changes onto the estimation accuracy to determine an optimal condition for monitoring the health.

1.3 Scope and Limitations

The scope of the proposed schemes are intended for online-monitoring of one critical parameter of capacitor (i.e., capacitance) and not the equivalent series resistance (ESR) as the typical values of ESR for MPPF capacitors are too low [11]. This means the capacitor is not taken out of the system. Also the proposed methodology only use the existing voltage and current sensors typically present in a BEV with no additional hardware or sensors required.

The scope is also limited to monitor the healthy working of a capacitor and not to estimate the remaining useful life (RUL) of the capacitor. Hence the proposed methods are applicable to systems where the component is assumed to be in a healthy working state and gradually deteriorates under normal working operation of the system.

2

Capacitors

2.1 Construction

A capacitor is a passive electrical component which helps in storage of electrical energy for a very short duration and supply back the stored energy almost instantaneously. The capacitors consists of one or many electrodes separated by an insulating material which act as a dielectric as shown in Fig. 2.1. Whenever an external voltage source is applied across its electrodes, polarization of the insulating material occur and forms a stream of dielectric particles which aligns along the external electrical field lines. As the charged particles are immobile in an insulator, cause a ripple effect and attract the charges of opposite polarity along the electrode plate as long as the external voltage source is active. This net storage of charge act as a small reservoir of electrical energy and in the absence of the source discharge its stored charges across the circuit and compensating for a small flow of current.

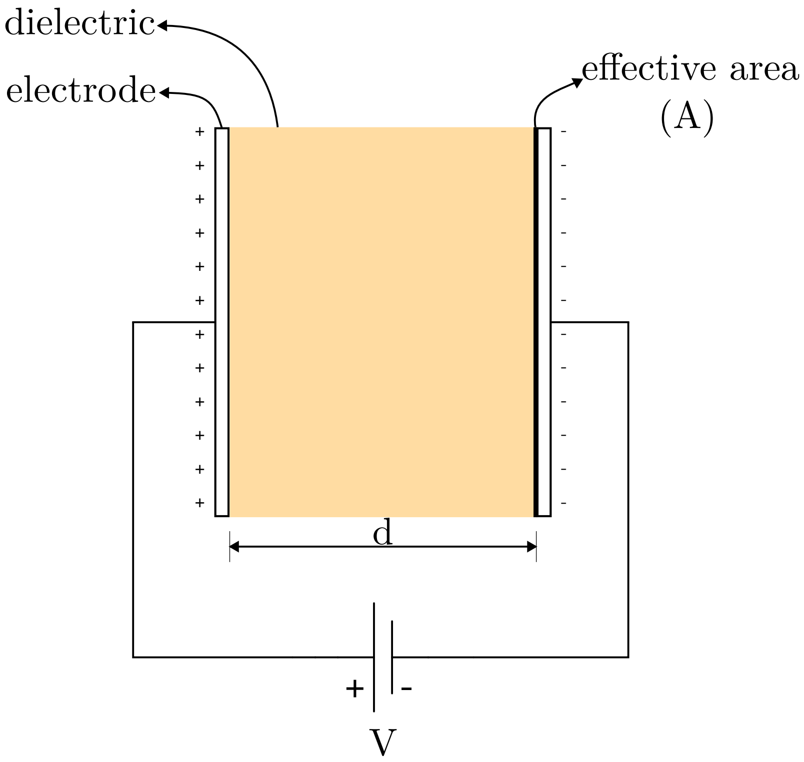

Figure 2.1: Construction of a simple single layer parallel plate capacitor

From the definition, capacitance is defined as the ratio of amount of charge held across its plates to the voltage difference applied across its terminal. Considering Q as the amount of charge held in coulumbs and V as the voltage potential, mathematically it can be represented as per Eq. 2.1.

$$Q = CV \tag{2.1}$$

Based on the geometric features as the capacitance is directly proportional to the effective area of plates and inversely proportional to the distance between the electrodes, another equation can be formulated as Eq. 2.2. Here ϵ represents the absolute permittivity of dielectric material. A being the surface area available for charges to accumulate and d is the distance between the plates as illustrated in Fig.2.1.

$$C = \frac{\epsilon A}{d} \tag{2.2}$$

2.2 Modelling

An ideal capacitor is desired to consist of only the capacitance (C). However, in real world, there may be additional parameters present such as internal resistance or inductance induced due to the imperfections in the construction and other environmental factors. Electrically, these parameters can be modelled as a series of additional components such as C, ESR and equivalent series inductance (ESL) as shown in Fig. 2.2.

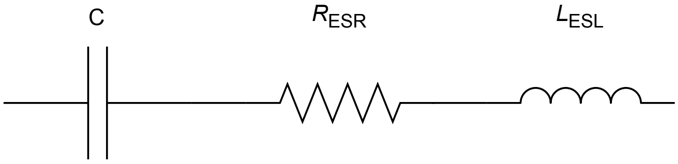

Figure 2.2: Simplified equivalent model of non-ideal capacitor

Each of the component parameter has different characteristic effect on the system. These effects can be better understood by the impedence analysis based on the frequency of operation. The first section which consists of lower frequencies($< \omega_1$), the impedance of the capacitor is mainly dominated by its capacitance. In the second region (between $> \omega_1$ and $< \omega_2$), ESR becomes prominent and in the last section($> \omega_2$), ESL is dominant. Fig.2.3 shows the impedence characterstic of a capacitor.

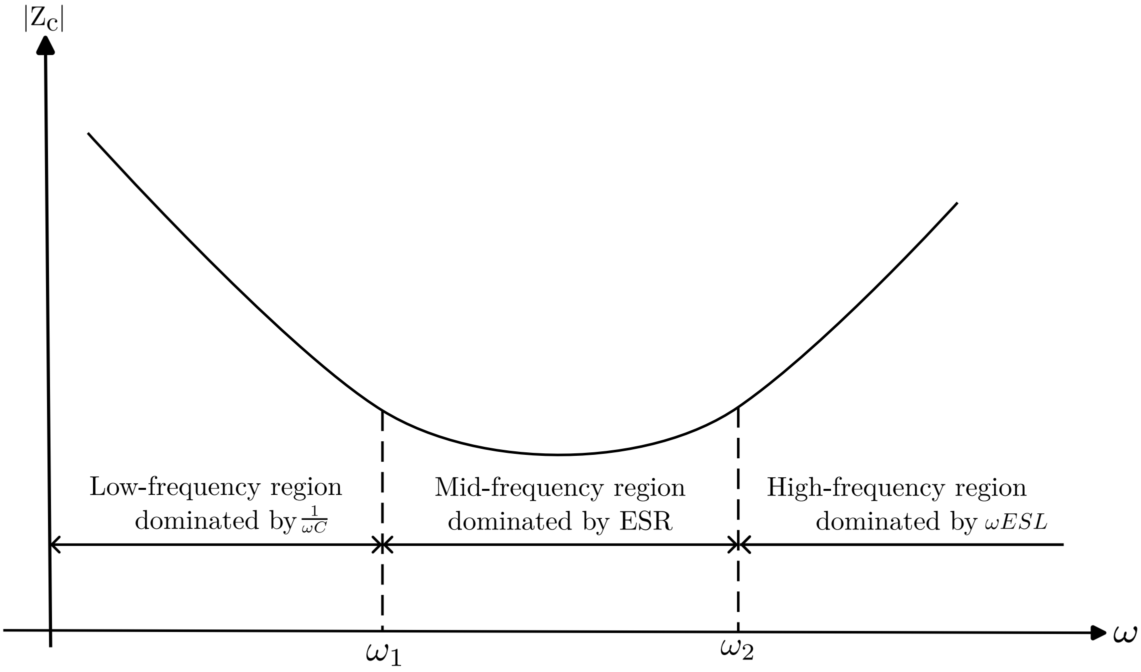

Figure 2.3: Impedance characterstics of a capacitor

Typically the impedance values are characterstic of the dielectric material and the technology used for construction of the capacitor. Table 2.1 shows the comparision between different types. The aluminium electrolytic capacitor (AEC) chosen for comparision is of $470\mu F$ and rated at $450V$ [12]. MPPF Capacitor has a capacitance of $480\mu F$ and a voltage rating of $450V$ [13]. A $480\mu F$ multilayer ceramic capacitor (MLCC) rated at $25V$ [14] is chosen. As it is evident from the table, each capacitor type has its characterstic resonant frequencies at different ranges and thus better suited for certain applications.

Table 2.1: Typical resonant frequency values

Type of Capacitor	f_1	f_2
AEC	10kHz	100kHz
MPPF	88kHz	99kHz
MLCC	225kHz	300kHz

2.3 Capacitor technologies

Capacitors are mainly classified based on the type of insulation(dielectric) used such as ceramic, film and electrolytic.

2.3.1 Electrolytic capacitors

Electrolytic capacitors consists of two metal foils stacked between a soaked paper film as shown in Fig. 2.4. One of the metal foils is anodized which forms the oxide layer and acts as the insulating dielectric layer for holding the electric charges. The soaked paper acts as a barrier for the metal foils but is porous for the transfer of charges through the electrolyte. The stacked layers are then rolled up in a cylindrical manner with the leads of terminal connecting each metal foil. The anodization process makes these capacitors inherently polarized. Due to the presence of liquid electrolyte as the dielectric medium, the effective surface area can be further enhanced by etching the anode surface and achieve higher capacitance and density values.

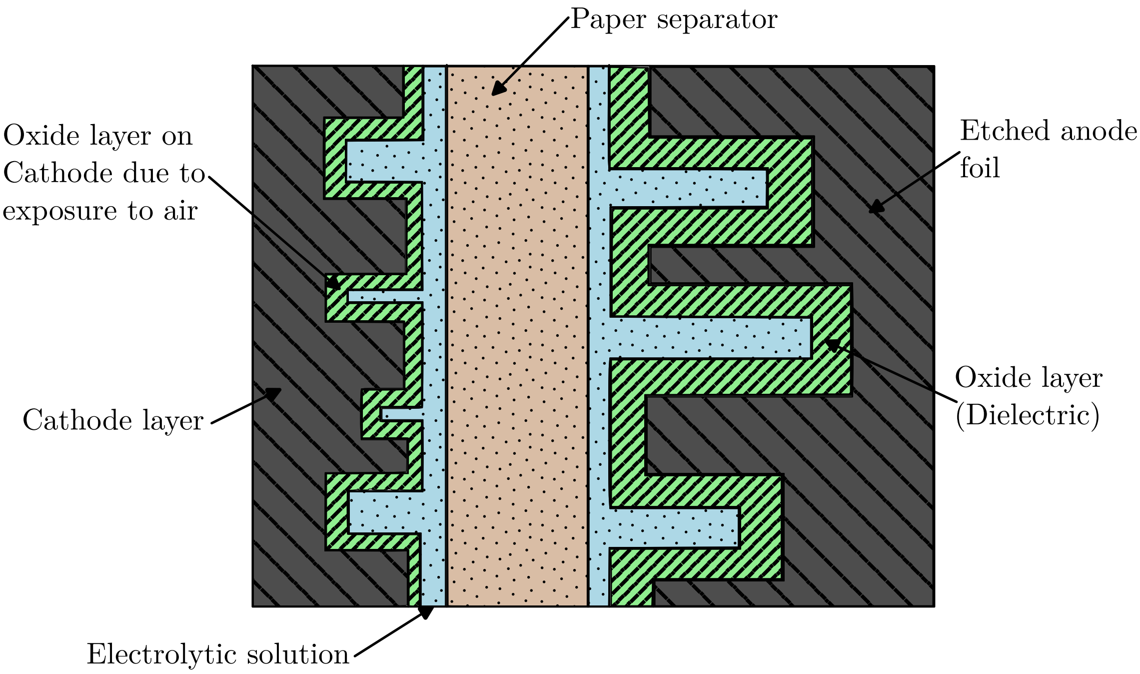

Figure 2.4: Cross-section of aluminium electrolytic capacitor

Only certain special metals designated as ’valve metals’ can be used as anode for electrolytic capacitors. The characteristic of these metals is the ability to allow current in one direction only. The commonly used anodic metals include aluminium, tantalum and niobium. Due to the oxidation of anodic layer, the respective oxides form the dielectric of the capacitor. Based on the compatibility with the anode material suitable electrolyte is used which can further be classified based on the state of electrolyte being a liquid or solid. Usually manganese dioxide is preferred as a solid electrolyte for all three types of anodic material.

Even though these capacitors have a higher capacitance value, the limiting factor for these capacitors are usually the root mean square (RMS) current. Although ideally the capacitor can have an infinite current rating, due to the presence of parasitic elements like ESR limits the amount of current as some of the power is lost as heat. This additional heat helps to increase the rate of electrolyte evaporation and have a higher probability of thermal runaway. ESR is an undesirable property of all capacitors which affect the performance of capacitors over time as the additional heat accelerate the chemical reactions that degenerate the dielectric. ESR in electrolytic capacitors are usually influenced by the electrolytic resistance, internal resistance between contact leads and inherant in the construction of the capacitor. All of these adds to the resistance of the current flow happening inside of the capacitor. Despite the fact that ESR from electrolytic resistance is based on the electrical conductivity of material used and cannot be changed but the ESR from other aspects such as size of current collector, terminals and leads can be easily optimized for better performance. Typically the value of ESR ranges between 0.1Ω and $2\ \Omega$ for a standard electrolytic capacitor. Low ESR type of electrolytic capacitors have the value in the range of 0.01Ω to 0.05Ω. Also due to the cylindric type of construction, these capacitors have a lot of self inductance which can range from 10 nH to 1μH. This is one of the reason for having a lower resonant frequency.

Having relatively higher ESR values, they dissipate lot of energy as heat. The relationship between these parameters is deciphered using equation 2.3. It is evident that the temperature rise is directly proportional to ESR and square of the RMS current conducted through the capacitor. Thus even a small increase in RMS current can result in a very large increase in temperature over time. The square of (i_{RMS}) is which is limited by the Eq. 2.3 the dielectric can eventually be vaporized causing very short lifetimes and even catastrophic failures

$$i_{\mathrm{RMS}} = \sqrt{\frac{\Delta T}{\beta \cdot R_{\mathrm{ESR}}}} \tag{2.3}$$

where,

i_{RMS} is the rated RMS value of current (in Ampere)

R_θ is the thermal resistance($^\circ C$/W)

ΔT is the rise in temperature due to internal heating($^\circ C$)

R_{ESR} is the ESR value of capacitor(Ω)

2.3.2 Ceramic capacitors

Ceramic capacitors are characterized with the use of powdered and sintered ceramic material as the dielectric medium. These are usually constructed by two or more layers of alternating ceramic and electrode to increase the capacitance and achieve greater degree of miniaturization as shown in Fig. 2.5. Because of the construction, most of the capacitors of this type are rated for higher voltage and capacitance values. Although most of the general purpose ceramic capacitors show sensitivity to temperature and frequency of operation.

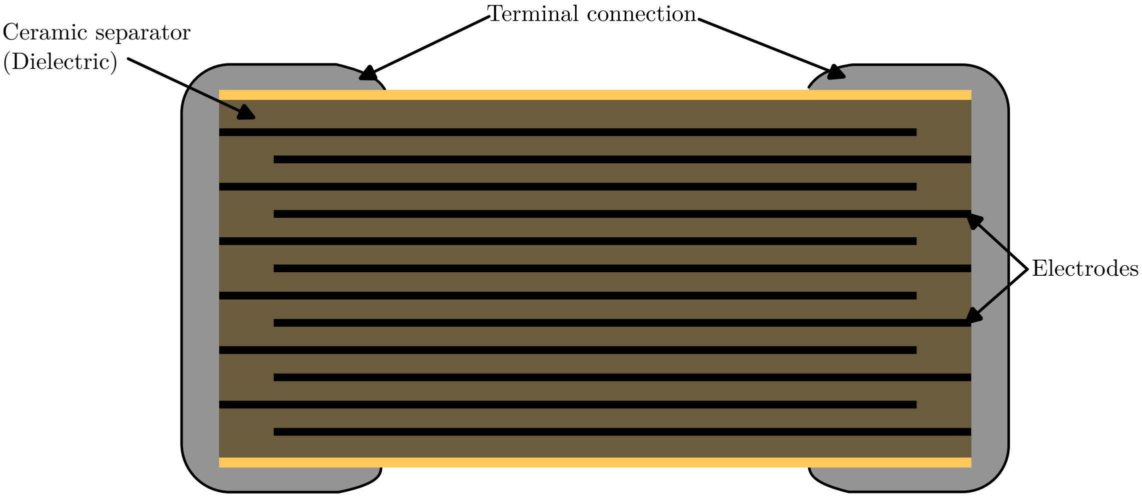

Figure 2.5: Cross-section of multilayer ceramic capacitor

Only few oxides like barium titanate ($BaTiO_3$), titanium dioxide (TiO_2) and calcium zirconate ($CaZrO_3$) forms the base material for the dielectric in case of cermaic capacitors. Pure $BaTiO_3$ has a very sensitive temperature dependance and non-linear behaviour when used as a dielectric. The combination of additives like zinc, zirconium, magnesium, cobalt and strontium for TiO_2 and aluminium silicate, aluminium oxide and magnesium silicate for $BaTiO_3$ improves the characterstics of the capacitor with required performance. These additives mainly induce higher electrical permittivity(ϵ_0) aiding for increase in their capacitance value. The major drawback of these capacitor lies in achieving an accurate value of capacitance. Hence these capacitors usually have very large tolerances. Another downside is the unintended oscillations that causes the component to vibrate continuously with a hissing sound due to piezoelectric characterstics of ceramic. The brittle nature of the dielectric also makes it susceptible to breakage under mechanical stress.

The typical voltage rating of a ceramic capacitor can range from 50V to 3000V. Few high power ceramic capacitors can withstand a high voltage of upto 100kV. But as the relative permittivity of the ceramics are quite low, these type of capacitors offer lower capacitance than their counterparts. Inspite of the fact of increasing the volumetric efficiency by stacking multiple layers, usually come with the downside of reduced voltage rating. Much of the losses incurred by these capacitors can be attributed to frequency dependent ohmic dielectric losses and can vary significantly with aging.

2.3.3 Film capacitors

Film capacitors are usually non polarized and consists of thin plastic films coated with a metal on one side in a vacuum environment. The combined layer is then rolled so as to obtain an alternating layer of metal plates which function as the terminals and the film forms the dielectric as shown in Fig. 2.6. The possibility to draw thin plastic films and to deposit a thin coating makes film capacitors achieve high volumetric density. Also the possibility of partial metallization allows for higher voltage rating without increasing the size. The ends of the film are sprayed to facilitate for terminal connection. The possibility of having electrodes with large surface area inherently lowers the resistance offered for charge mobility and helps in lowering the ESR. The close proximity of end terminals with all the electrode layers allows the capacitor to have relatively low ESL values.

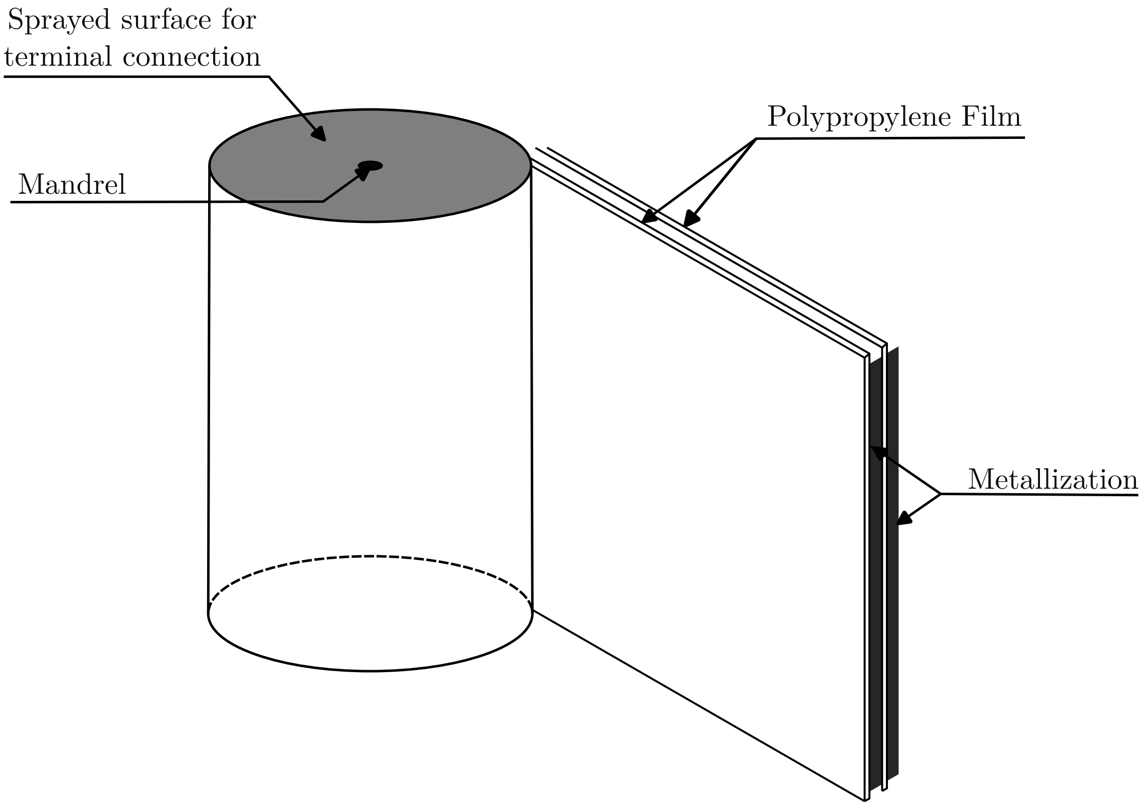

Figure 2.6: Detailed view of MPPF capacitor

Various materials can be used as the dielectric for the film capacitors such as polyester (PET), polypropylene (PP), polycarbonate (PC), polystyrene (PS) and polyfluorotetraethylene (PTFE). These materials have very high dielectric strength ranging from 25 kV/mm for PET to 150 kV/mm for PTFE. PP is the commonly used as the dielectric which has its breakdown voltage in the range of 40 to 50 kV/mm. Although PET is a cost effective option, it has very weak temperature tolerance and stability. PP offers stable performance even at high temperatures but is quite expensive than PET. The applications of PTFE are more suitable for high end applications beacuse of its excellent dielectric strength but is less commonly used for general purpose applications because of the cost.

One of the characterstic feature of these capacitors is the ability of self healing. Whenever a breakdown occurs due to point defects present in plastic film during manufacturing, high density current passes through the film for a short time and results in an arc around the region. This arc then vapourizes the metal coating and thus preventing the further run over into other healthy regions of the capacitor as depicted in the Fig. 2.7. The affected area is considerably low (~ $50nm$) and the phenomenon also happens fairly quick ($\sim 10\mu s$) which doesnt affect the normal operation of capacitor [15].

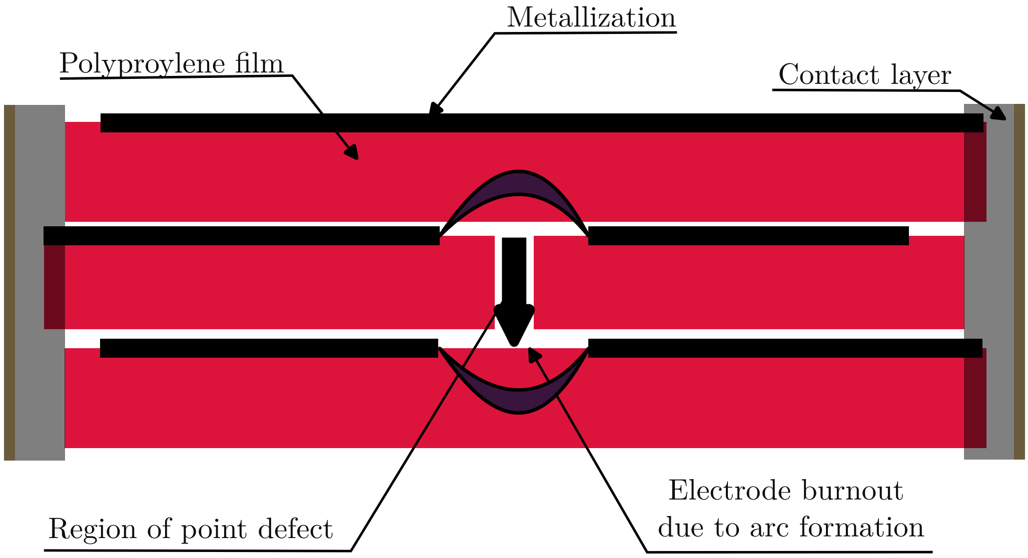

Figure 2.7: Cross sectional view of self healing in MPPF capacitors

Another distinctive feature of film capacitors is their ability to withstand a wide range of temperature variation. These capacitors offers excellent stability even temperatures as high as $125°C$ for PC and PTFE. Although PET materials exhibit a capacitance drift at higher temeprature, these can be minimised and some alterations can be made for them to have a temperature tolerance upto $85°C$ or $105°C$. PP offers the best performance even at a temperature variation from -40$°C$ to +125$°C$.

Despite having very good performance in electrical parameters, the major downside of these capacitors is their lower capacitance value. Usually the capacitance for these type of capacitors varies from 1 nF to $100\mu F$. Also these capacitors take up more space for the same capacitance value compared to ceramic or electrolytic capacitors.

2.3.4 Applications

As electrolytic capacitors are simple in construction and inexpensive, they are used in numerous applications ranging from filtering to bypassing and decoupling. Also due to their high energy density, they are extensively used in applications where a large amount of charge is needed in a very short duration like conventional motor drive applications [16], spot welding, flashtube ignition, airbag, backup power systems for microcontrollers and camera flash circuit [17]. For the voltage regulators, they help in maintaning a stable output voltage by supressing the ripple induced by load variations. Due to their ability to filter certain frequency signals, they are utilized in audio amplifiers. Most often these applications demand a voltage rating ranging from tens of volts to several hundred volts. Some capacitors with a high capacitance value of 1F to 5000F are used as supercapacitors in backup power grids and energy storage applications. These applications can be classified based on the voltage rating as low voltage applications for applications operating from 1.5 V to 50V such as portable electronic devices. Some consumer devices having a voltage rating of 50V to 250V can be classified as medium voltage and the capacitors utilized in industrial systems and power grids will have a rating higher than 250V, making them high voltage applications. But due to their sparse current carrying capacity and brief lifespan, limit their application onto other fields.

Ceramic capacitors having overcome most of the shortcomings of electrolytic capacitors find its use in many applications like integrated circuits, memory chips and other electronic devices. However, these are also limited by higher voltage rating and brittle dielectric. Infact, the brittleness of dielectric makes it susceptible to catastophic failures under mechanical and thermal stress and thus needs to be improved before using it for safety critical systems like traction EVs.

Because of relatively high dielectric strength, these capacitors find its uses in a diverse range of applications. Several low voltage applications which typically operate in the range of 50 V to 250V utilize these type of capacitors for their low power loss. Some medium voltage applications like analog to digital converters, signal processing, sample and hold, timing and snubbers use film capacitors while operating at 250V to 630V. Many high voltage applications which function at 630V to 3kV, usually in industrial, high power and pulsed applications also prefer these capacitors due to their low parasitic elements. Some high voltage power generation and transmission systems operating at a voltage level of upto 20kV can be benefited from film capacitors. Film capacitors thus becomes an obvious choice with higher current ratings and unique self healing characteristics. Thus only MPPF capacitors are considered further for the study and analysis.

2.4 Stressors of capacitors in inverters

Many factors influence the behaviour of DC-link current in a three phase system like load imbalance, modulation technique, switching frequency and inverter configuration. These factors primarily affect and add to the stress on DC-link filter i.e., capacitor. A study of fast fourier transform (FFT) of capacitor current helps in recognizing the major components in frequency domain. Fig. 2.8 shows the analysis of capacitor current when simulated in piecewise linear electrical circuit simulation (PLECS) with parameter values of A.1. The first spike between 0 and $20kHz$ is due to the sidelobe of DC bias of the capacitor current. Although the switching frequency was chosen as $20kHz$, the fundamental component is observed at $40kHz$. Many subsequent peaks are also observed with the same period of $40kHz$ which indicate the harmonics present in the capacitor current. Key observation can be made about the exponential decay of peak amplitudes at higher frequencies.

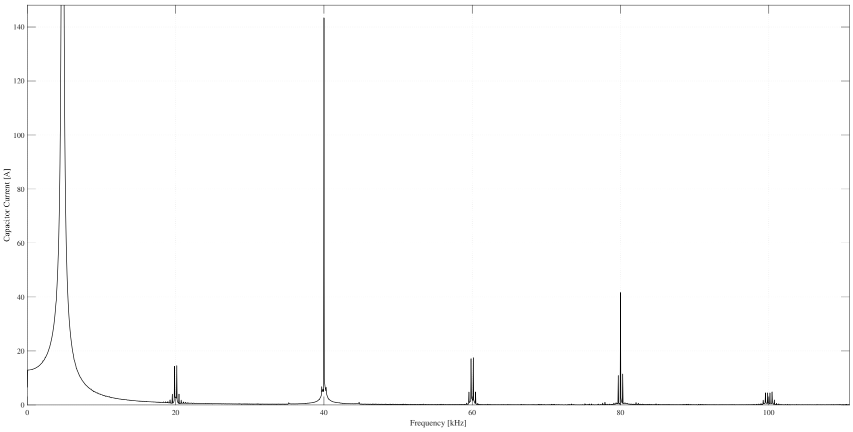

Figure 2.8: FFT of capacitor current

The variations can be better explained with the help of capacitive reactance as per Eq. 2.4. Here, f is the frequency of operation, C is the capacitance and X_c is the reactance of capacitor. At low frequencies, the reactance is low for a given capacitance value and this the capacitor current is also lower at these frequencies. An inflection point is reached known as the critical frequency after which the increase in frequency significantly lowers the reactance and thus allowing more current through the capacitor.

$$X_\mathrm{c} = \frac{1}{2\pi f C} \tag{2.4}$$

Another contour plot was obtained from a simulation made with varying power factor and modulation index as shown in Fig. 2.9. The power factor is a dimensionless term used to quantify the amount of actual work done by an electric machine. Modulation index denotes the extent of modulation of the carrier signal. Overall it can be seen that the variation of these two parameters has a non-linear effect on the RMS of capacitor current. But in general there is an increase in RMS current with an increase in modulation index. However there is an inverse trend with the power factor. Lower power factor corresponds to a higher capacitor current and increased stress on the capacitor. The increase in capacitor current at higher modulation index is due to larger voltage swings made during the switching operation. Also at low power factor, much of the reactive power is consumed by the capacitor increasing the current.

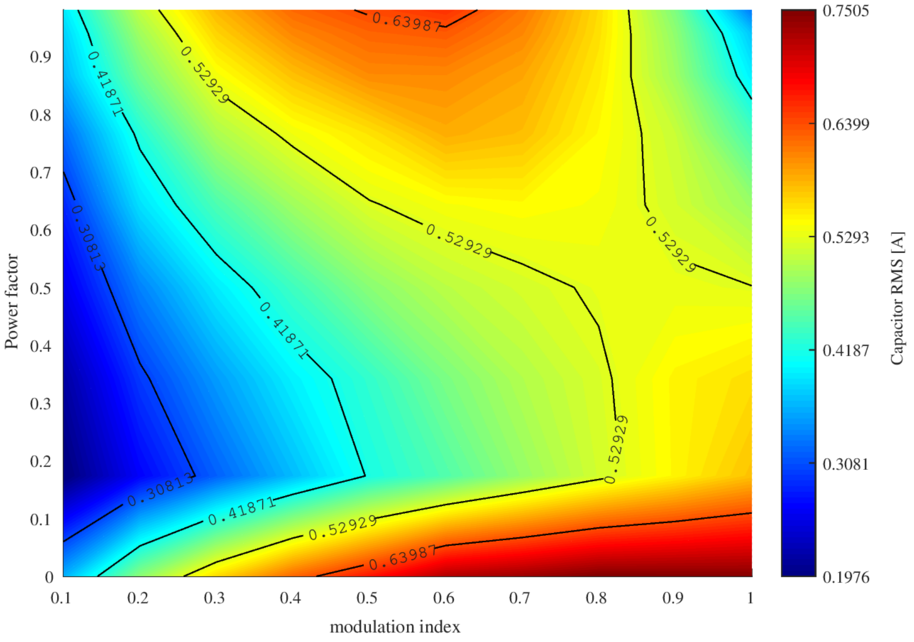

Figure 2.9: Contour plot of capacitor current

2.5 Ageing and failure mechanism

Typically the characteristics of a capacitor like C and ESR deteriorate over a period of time with usage after which requires it to be replaced. The end of life criteria is slightly different for each of the capacitor type with AEC required to be replaced when the capacitance falls below 80% of its initial value or ESR doubling. As ESR is significantly low in film and ceramic capacitors, only reduction in capacitance less than 95% and 90% from its initial value is used as the failure criteria respectively. Normally the electrical stress (voltage ripple) and thermal stress majorly contribute to the failure of capacitors. Due to the presence of inherant manufacturing defects, stresses accelerate the wearout further and ultimately leading to failure of the component.

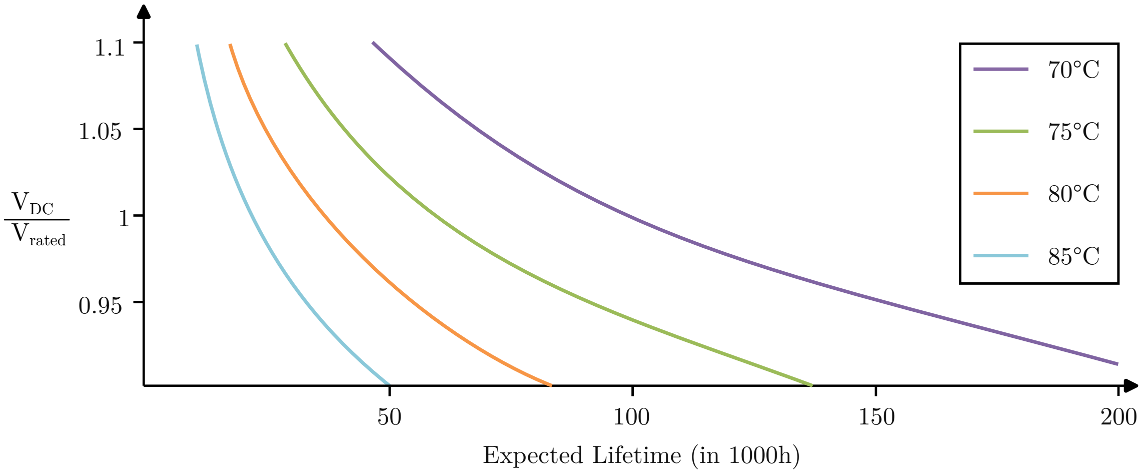

Figure 2.10: Lifetime trends of capacitor under different thermal stress

Much of the aging in a capacitor can be inculpated to temperature. Infact, a service life trend of capacitors under different hotspot temperatures from TDK Electronics [18] shown in Fig. 2.10 illustrates the consequence of heat. Theoretically, these trends follow the mathematical formulation as per equation 2.5. It can be inferred that the lifetime is nearly halved for every $10°C$ increase in temperature.

$$L = L_0 \cdot 2^{\left(\frac{T_\mathrm{r}-T}{10}\right)} \tag{2.5}$$

where,

L is the estimated useful life of capacitor in hours

L_0 is the rated life time hours of the capacitor at temperature T_r

T is the operating temperature of capacitor

3

Modelling of capacitor ageing

3.1 Overview of methods

A large number of literature has been published which address the CM of DC-link capacitors. However as DC-link capacitors have a wide range of application footprint, many of these proposed techniques often rely on the specific hardware or topology feature which might not be present in other use cases. For instance, different DC-link applications like DC/DC converters, power factor correction (PFC), adjustable speed drives (ASD), photovoltaic (PV) grid systems are discussed in [19]. The article mainly provides a comprehensive and comparative overview of different CM methods applied to various applications. As much of the methods focus on the low frequency grid component for accuractely estimating the capacitor parameters, these are unbefitting for traction inverter application. Thus, this thesis only discuss the methods presented and focussed on ASD systems.

ASD systems also known as variable frequency drives (VFD) allow for precise control of speed for different load conditions. Although the methods discussed are closely related to BEV topology, some of the schemes depend on additional current sensor or hardware for current injection and measurement circuit. Addition of these systems pose a significant cost overhead and reliability for the overall system. Also some of the methods also rely on data training and machine learning model which are not considered for review. Broadly the methods can be classified as real-online and quasi-online approaches. The real-online based methods can be implemented during normal working conditions of the drive cycle. On the contrary, quasi-online approach requires system to be in certain specific operation condition for successful implementation of the method.

3.2 Method 1

A real-online based method is presented in [20] where, the primary intended application is fault tolerant aerospace drives. The power conversion unit is connected to a three phase AC rated between 115V to 230V and operating at a frequency of 300Hz to 800Hz. The source is rectified before connecting it to the DC-link which is connected to an inverter and ultimately to the three phase load. The inverter is a two level configuration similar to Fig. 1.5 and operated between switching frequencies of 50 kHz and

200 kHz, depending on the load. All the sensors typically present in an ASD system are utilized like the DC-link voltage, current from rectifier and three phase currents connected to the load which are mainly used for the purpose of control.

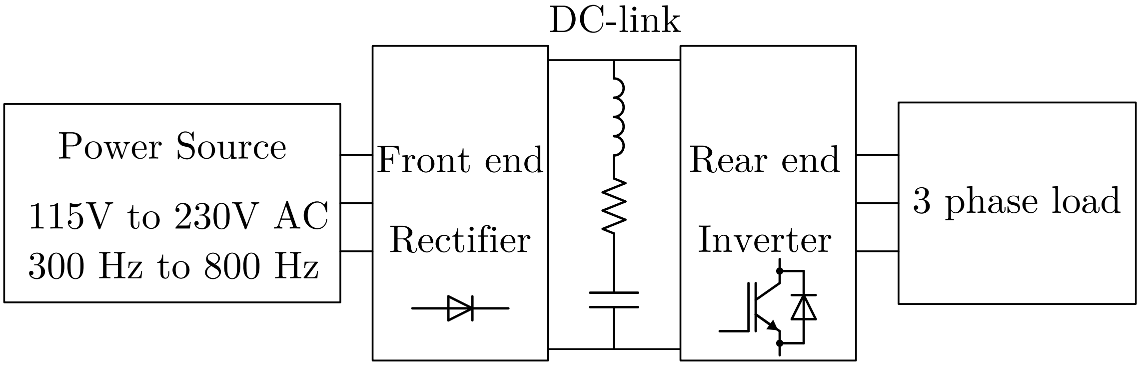

Figure 3.1: Topology of capacitor operation in [20]

The method models the capacitor as per Fig. 2.2 and obtain a mathematical model of the capacitor. As the intendent application demands for a higher switching operation of invereter switching, the effect of ESL is considered in modelling of the capacitor. This model is then utilized to derive a transfer function of the capacitor as per Eq. 3.1 in the complex frequency domain or s-domain using laplace transform. The continuous time transfer function is then discritized using bilinear tustin technique. Bilinear tustin transform is a first order approximation of the continuous transfer function. The main advantage of using this approach for discretization is the preservation of system responses like stability and minimum phase information in both time and frequency domains by prewraping the frequencies, especially near critical frequencies. The parameters are then rearranged to obtain the coefficients of z-transform variables which are a function of sampling frequency (T_s), R_ESR, C and L_ESL as shown in Eq. 3.2.

$$H(s) = \frac{u_\mathrm{dc}(s)}{i_\mathrm{cap}(s)} = \frac{1 + R_\mathrm{ESR} \cdot C \cdot s + L_\mathrm{ESL} \cdot C \cdot s^2}{C \cdot s} \tag{3.1}$$

$$H(z^{-1}) = \frac{b_0 + b_1\, z^{-1} + b_2 z^{-2}}{1 - z^{-2}} \tag{3.2}$$

where,

$$b_0 = \frac{T_\mathrm{s}^2 + 2R_\mathrm{ESR} \cdot C \cdot T_s + 4L_\mathrm{ESL} \cdot C}{2C \cdot T_\mathrm{s}}$$

$$b_1 = \frac{2T_\mathrm{s}^2 - 8L_\mathrm{ESL} \cdot C}{2C \cdot T_\mathrm{s}}$$

$$b_2 = \frac{T_\mathrm{s}^2 - 2R_\mathrm{ESR} \cdot C \cdot T_\mathrm{s} + 4L_\mathrm{ESL} \cdot C}{2C \cdot T_\mathrm{s}}$$

Utilizing the previously obtained coefficients, the system is approximated with a linear model. A linear model is used for describing the system as it is the simplest approximation wherein the system is assumed to have a unique response for each different input. Also the complex combination of responses can be broken down as the addition of simple responses for a predefined set of inputs and the output is scaled linearly for the scaled input.

$$y(t) = \varphi(t)^T\theta + v(t) \tag{3.3}$$

where $y(t)$ is the output of the system, $\varphi(t)$ is the regression vector which consists of preceding output and input values, θ is composed of coefficients that are obtained from the transfer function and $v(t)$ denotes the error encompassing of model inaccuracies and nonlinearities. This way of segregation of variables makes it easier to analyse the system responses to specific inputs and disturbances and to obtain the solutions as the mathematical equations can be solved using a microcontroller.

The linear model considered in this method is shown in Eq. 3.3. An initial guess is made for the parameter values in $\hat{\theta}$ vector and then the algorithm scans through the space for optimal coefficient values based on the available input and output data. The goal of the parameter adaptation algorithm is to reduce the error between the prediction and real. Although many algorithms can be utilized for this purpose, this method analyzed recursive least square (RLS) which is a common least square estimator for the prediction. It should be noted that the algorithm heavily relies on constant low frequency excitation of the system to accurately converge to optimal coefficient values. The estimated coefficient values are then used to calculate the capacitor parameters like R_{ESR}, C and L_{ESL} from the Eq. 3.4.

$$\begin{aligned} R_{\mathrm{ESR}} &= \frac{b_0 - b_2}{2} \\ C &= \frac{2T_{\mathrm{s}}}{b_0 + b_1 + b_2} \\ L_{\mathrm{ESL}} &= \frac{T_{\mathrm{s}}(b_0 - b_1 + b_2)}{8} \end{aligned} \tag{3.4}$$

The authors also presented the effect of different noise levels to the performance of the algorithm on an aged and healthy capacitor. Fig. 3.2 illustrates the same with Capacitor 1 being a healthy one and the rest of the capacitors aged with corresponding values. Signal to noise ratio (SNR) is a metric employed to quantify the strength of a signal compared to the noise. It is a dimensionless number defined as the ratio of powers of signal to that of noise and usually expressed in a logarithmic scale. Overall it can be seen that L_{ESL} is more sensitive to noise. A SNR of 50 was necessary to get an accurate estimation of coefficients irrespective of the health of the capacitor.

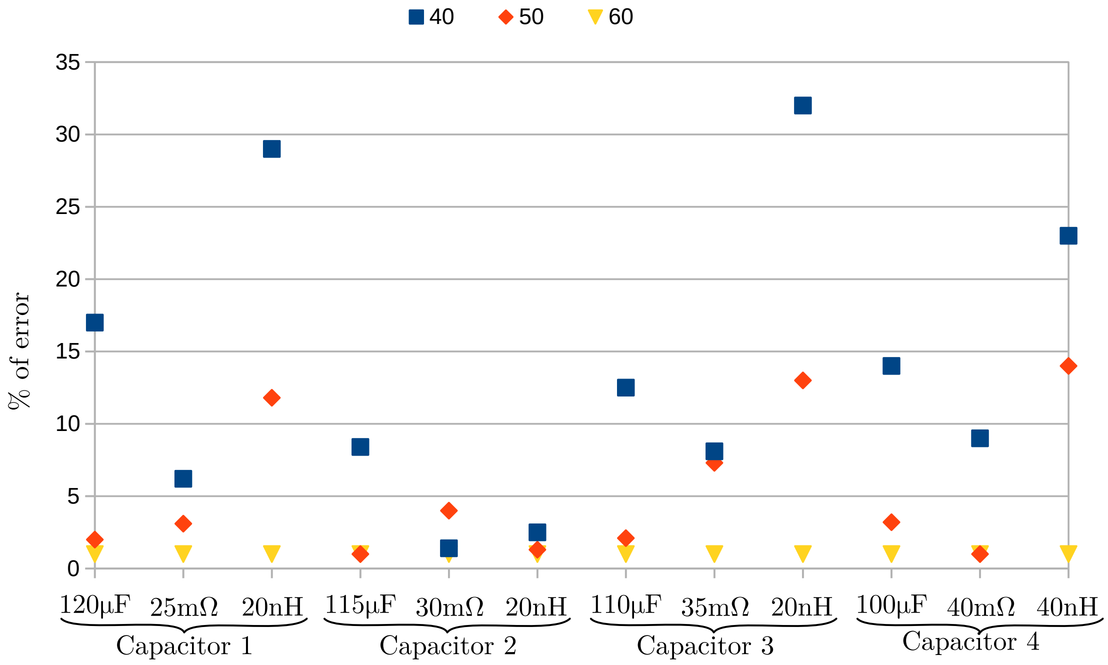

Figure 3.2: Performance of algorithm at different SNR levels

3.3 Method 2

A similar approach as [20] i.e., method 1 is used in [21] where the DC-link is employed in an AC/DC/AC converter system as shown in Fig. 3.3. A power source operating at 380V AC is rectified with the help of diodes on all three phase lines to be connected with a DC-link capacitor with parameter values of $470\mu F$ capacitance and R_{ESR} of $250m\Omega$. The higher R_{ESR} value can be attributed to the use of aluminium electrolytic capacitor as the DC-link. All the sensors of a typical ASD system are employed to have a precise control of the motor. A two level topology similar to Fig. 1.5 is used on the rear end of the power conversion unit.

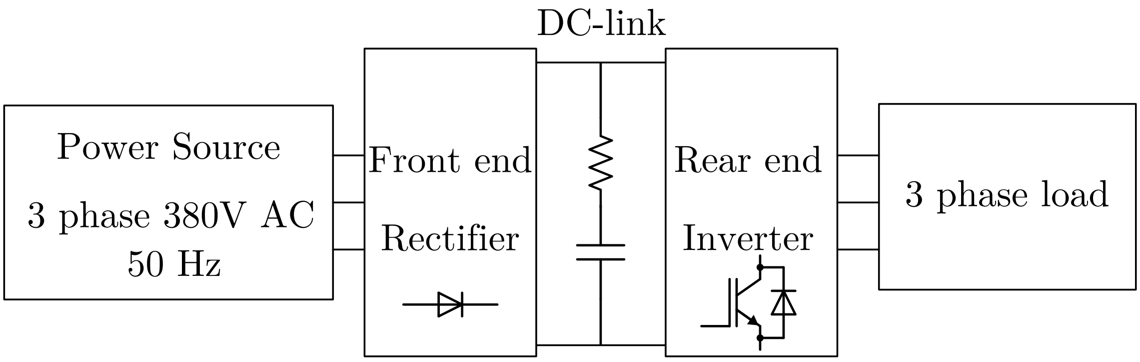

Figure 3.3: Topology of capacitor operation in [21]

Whenever the motor is stopped, a unipolar PWM with fixed duty cycle and frequency is applied to one of the switches of the inverter. The equivalent circuit can be modelled as per Fig. 3.4. The L_{line} and $D_{\text{rectifier}}$ represents the line inductance and forward bias resistance of the rectifier diode respectively. As a low switching frequency of 900 Hz was used to drive the inverter, the effect of ESL was not considered in modelling the capacitor. Since the PWM is applied only to switch S_1 in Fig. 1.5, the current flows through two of the phase lines of the motor and returns through the diode of switch S_2 represented by D_2 in Fig. 3.4. Since the motor is not moving, the stator impedance for two phase lines can be modelled as two series connected resistance and inductance with values of R_{line} and L_{line} for each phase line respectively.

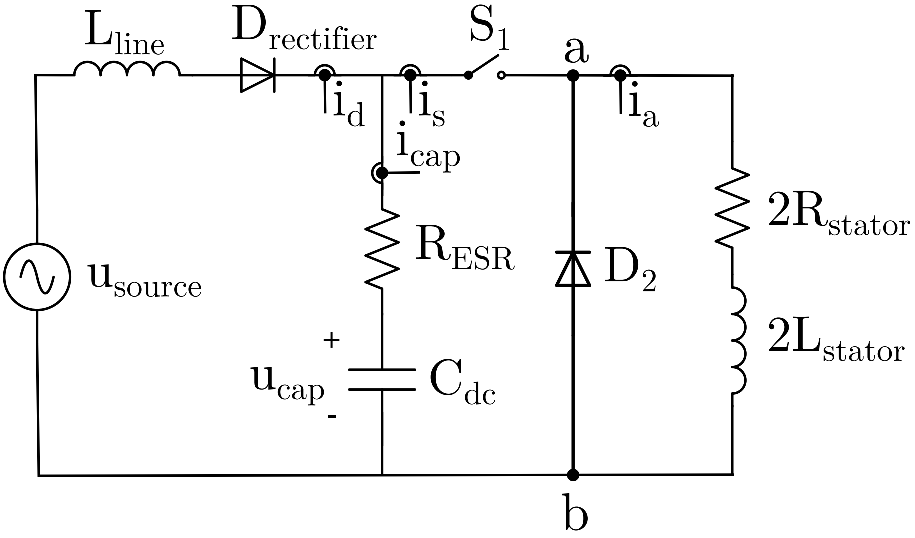

Figure 3.4: Equivalent ciruit model during estimation

The transfer function of the updated model thus follows the mathematical framework in Eq. 3.5. The model is again discretized using bilinear tustin transform to obtain a z-domain variant of the transfer function as per Eq. 3.6. The parameters are rearranged to obtain the coefficients a_0 and a_1.

$$H(s) = \frac{u_{\text{dc}}(s)}{i_{\text{cap}}(s)} = \frac{1 + R_{\text{ESR}} \cdot C \cdot s}{C \cdot s} \tag{3.5}$$

$$H(z^{-1}) = \frac{a_0 + a_1\, z^{-1}}{1 - z^{-1}} \tag{3.6}$$

where,

$$a_0 = R_{\text{ESR}} + \tfrac{T_{\text{s}}}{2C}$$

$$a_1 = \tfrac{T_{\text{s}}}{2C} - R_{\text{ESR}}$$

The coefficients are then expressed as a linear combination of the output $(y(k))$, regression vector $(\varphi(k))$ and the error $(e(k))$ as per the Eq. 3.7. The discrete time linear model helps us to introduce the capacitor current as the input and obtain the results in terms of DC-link voltage as output. The error term consists of all the model simlification or inaccuracies and other disturbances affecting the system.

$$
\begin{aligned}
y(k) &= y(k-1) + a_0 u(k) + a_1 u(k-1) + e(k) \\
&= \varphi(k)^T \theta + e(k)
\end{aligned}
\tag{3.7}
$$

A least square algorithm is chosen for parameter estimation which provides the best fit for the curve in each iteration. RLS algorithm is preferred as it can adapt to other parameter changes like temperature or load and can be computed offline with low computational overhead. As this is a recursive algorithm, the objective of the cost function is to minimize the error between the actual value and the prediction. That being said, the model has a higher chance of convergence to the actual value if it is excited with a constant duty unipolar PWM that is applied to two stator legs during the shutdown period of motor. The excitation aids the algorithm to scan the vector field and converge faster to the optimal coefficient values.

The RLS algorithm is essentially an adaptive filter where the filter coefficient ($\hat{\theta}(k)$) at any given time step k is given by the sum of filter coefficient at previous time step i.e., $k-1$ and the product of kalman gain $K(k)$ with the error residual as per the Eq. 3.8. The error residual is obtained as the difference between the desired output ($y(k)$) and the prediction of the ouput ($\varphi^T(k)\hat{\theta}(k-1)$). The kalman gain is computed by choosing an appropriate value for forgetting factor λ typically closer to 1 and the covariance matrix obtained from the previous time step ($P(k-1)$). The covariance matrix is adapted by the previous values of kalman gain, input data and λ. A higher value of covariance matrix means that the filter has more uncertainity and tries to adapt the filter coefficients to newer input values. This also influences the behaviour of kalman gain as the values are nearly proportional and the kalman gain also increases to accompany the changes in input data for an increase in covariance matrix.

$$
\begin{aligned}
&\hat{\theta}(k) = \hat{\theta}(k-1) + K(k)\left[y(k) - \varphi^T(k)\hat{\theta}(k-1)\right] \\
&K(k) = P(k-1)\varphi(k)\left[\varphi^T(k)P(k-1)\varphi(k) + \lambda\right]^{-1} \\
&P(k) = \lambda^{-1}\left[1 - K(k)\varphi^T(k)\right]P(k-1)
\end{aligned}
\tag{3.8}
$$

The previously obtained optimized coefficients are then used to calculate the health indicating parameters of a capacitor, mainly R_{ESR} and the capacitance as per the Eq. 3.9.

$$\begin{aligned} R_{\mathrm{ESR}} &= \frac{a_0 - a_1}{2} \\ C &= \frac{T_{\mathrm{s}}}{a_0 + a_1} \end{aligned} \tag{3.9}$$

A residual lifetime analysis of the capacitor was also presented in the paper which takes into account the effect of temperature on capacitor parameters like R_{ESR} and C. An exponential decrease in R_{ESR} and a linear increase in C was found with an increasing ambient temperature. Simulations were also performed to analyse the sensitivity of the algoritm to changes in duty ratio and switching frequency but the algorithm showed immunity to both of these changes. As this approach requires a special operation of the inverter, it has a drawback of being a quasi-online approach for condition monitoring.

3.4 Method 3

In [22], a discharge scheme is utilized to measure the parameteres of DC-link capacitor in an AC/DC/AC drive unit as per Fig. 3.5. The intended application consists of a three phase power source operating at $220V$ and $50Hz$. The DC-link consists of serveral capacitors C_1, C_2 and C_3 connected in series across the inverter. There is also balance resistors $R_{\mathrm{b1}}, R_{\mathrm{b2}}$ and R_{b3} which are connected in parallel with the corresponding capacitor bank to equally divide the voltage across each capacitor. The method assumes an additional component called variable electrical network (VEN) is connected across the capacitors. It has to be noted that the VEN component can be controlled with the help of a microcontroller.

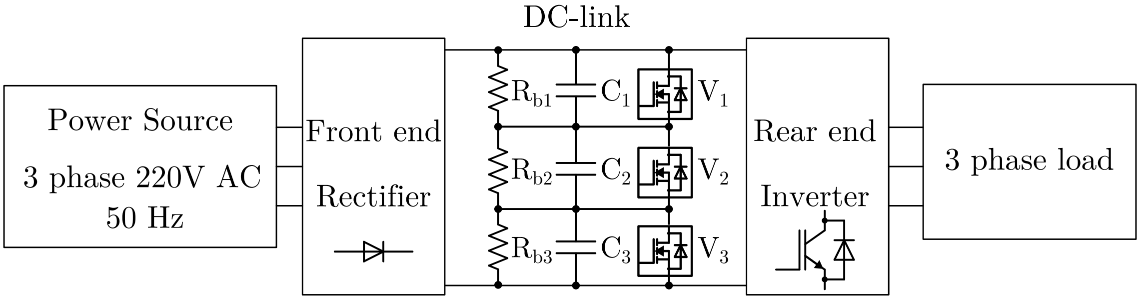

Figure 3.5: Topology of capacitor operation in [22]

A VEN network consists of two branches of switches and resistors arranged as per Fig. 3.6 with each branch intended for estimating one of the capacitor parameters i.e., either capacitance or ESR. Each branch has a semiconductor switch which can be a MOSFET or IGBT connected in series with a resistor. The actuation of switches are controlled by a micro control unit (MCU) of the machine. The value of resistor in each branch is carefully chosen so as to aid the parameter estimation. The capacitor branch consists of resistor designed for slow discharge rate. For this reason, a resistor of range

100 Ω to 1kΩ is chosen. For the ESR estimation branch, as the ESR is only in the range of tens of milliohms, wire resistance coupled with the ON resistance of the switch will be sufficient to match the magnitude of ESR. Since the resistors R_{X1} and R_{X2} can be accurately measured with LCR meter before using, accurate estimation of capacitor health is possible. The capacitor is modelled as a series connected ideal capacitor and a resistor with values of C and R_{ESR} respectively.

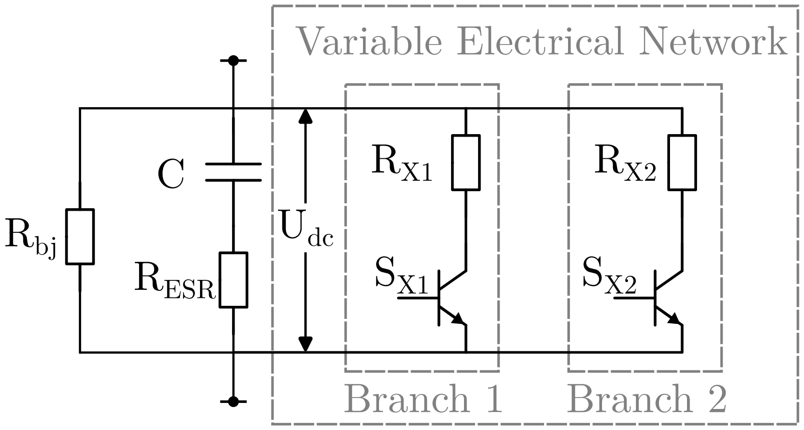

Figure 3.6: Individual VEN circuit model for capacitor monitoring

During the shutdown phase of machine, when the capacitor is isolated from both the source and the load, self discharge of the capacitor assist to reduce the DC-link voltage across its terminal as shown in Fig. 3.7. This discharge period can be modelled mathematically as a first order zero input response as per Eq. 3.10.

$$u_i(t) = V_0 e^{-t/[(R_{bj}+R_{ESR})C]} \tag{3.10}$$

where u_i is the instantaneous voltage level of the capacitor, V_0 is the initial voltage level before self discharge, R_{bj} being the resistance of the corresponding balance resistor connected across the capacitor, R_{ESR} and C are the equivalent series resistance and the capacitance of the capacitor.

A predefined voltage level V_1 is chosen for the DC-link voltage and the capacitor is discharged in a controlled manner according to discharge 1 part of Fig. 3.7. The discharge is carried by actuating one of the switch in the VEN branch particularly for capacitance estimation (branch 1). As the discharge process is done very rapidly, new equations as per 3.11 govern the process. τ_1 is the time consumed for this discharge process which can be evaluated from the Fig. 3.7.

$$\begin{aligned} u_i(t) &= V_1 e^{-t/\tau_1} \\ \tau_1 &= [(R_{bj}||R_{X1}) + R_{ESR}]C \end{aligned} \tag{3.11}$$

Towards the end of discharge 1, at time t_1 another VEN branch is activated for the estimation of ESR as shown in Fig. 3.7. It is worth noting that the branch 1 is deactivated before activating the switch in branch 2. The combined effect of all the resistors leads to an exponential decay of the DC-link voltage according to Eq. 3.12.

$$\begin{aligned} u_\mathrm{i}(t) &= V_2 e^{-t/\tau_2} \\ \tau_2 &= [(R_\mathrm{bj}||R_\mathrm{X2}) + R_\mathrm{ESR}]C \end{aligned} \tag{3.12}$$

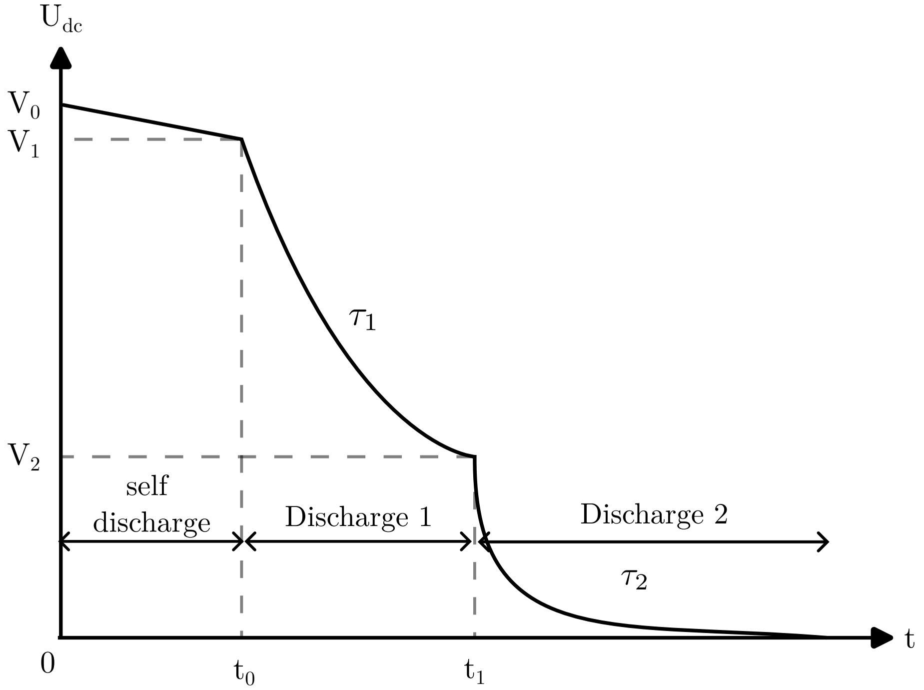

Figure 3.7: Discharge profile of VEN

As most of the power dissipated from branch 1 of VEN is thermal, care should be taken to properly select an appropriate initial voltage of the DC-link (V_1). This can be derived from the power dissipated through the resistor conforming to Eq. 3.13. P_X1 is the maximum power rating of the resistor in branch 1.

$$V_{1_\mathrm{max}} \leq \sqrt{P_\mathrm{X1} \cdot R_\mathrm{X1}} \tag{3.13}$$

Due to low resistance value in branch 2, high discharge current flows through the switch making a shorter discharge time. The maximum voltage level before discharge 2 can take place is calculated by Eq. 3.14. I_d is the maximum pulse drain current of the switch used.

$$V_{2_\mathrm{max}} < I_\mathrm{d}(R_\mathrm{ESR} + R_\mathrm{X2}) \tag{3.14}$$

Using both equations 3.11 and 3.12, capacitance and R_ESR can be acquired as per 3.15. As $R_\mathrm{ESR} << (R_\mathrm{bj}||R_\mathrm{X2})$ and $R_\mathrm{X2} << R_\mathrm{bj}$, the equations can be further simplified and the parameters can be estimated only with the help of τ_1 and τ_2.

$$
\begin{aligned}
C &= \frac{\tau_1}{[(R_{\mathrm{bj}}||R_{\mathrm{X1}}) + R_{\mathrm{ESR}}]} \approx \frac{\tau_1}{(R_{\mathrm{bj}}||R_{\mathrm{X1}})} \\
R_{\mathrm{ESR}} &= \frac{\tau_2}{C} - (R_{\mathrm{bj}}||R_{\mathrm{X2}}) \approx \frac{\tau_2}{C} - R_{\mathrm{X2}}
\end{aligned}
\tag{3.15}
$$

Simulations were performed in MATLAB/Simulink environment to get an estimate of the time scale of different discharge periods. It was found that discharge 1 took $3.32s$, $2.33s$ and $4.26s$ for three different capacitors. Additionally, $905\mu s$, $705\mu s$ and $1115\mu s$ were observed for completion of discharge 2. A mean relative error of 0.045% and 0.071% were noticed for the estimation of capacitance and ESR between these capacitors.

The method was also validated through experiments with the VEN connected as an external unit to the system and controlled with MCU. Table 3.1 summarises the results obtained from experiments conducted on different capacitors. All the capacitors were of electrolytic type and tested at an ambient temperature of $10°C$.

Table 3.1: Experimental results of capacitor health estimation in [22]

	τ_1	τ_2	**C**		**R$_{\mathrm{ESR}}$**	
	(s)	(μs)	Actual (μF)	% Error	Actual ($m\Omega$)	% Error
Cap 1	7.94	8.69	7911.1	2.40	17.32	0.58
Cap 2	7.86	8.58	7886.3	1.70	17.16	-1.52
Cap 3	7.95	8.98	8168.6	-0.82	21.34	-2.01
Cap 4	6.21	6.73	6178.6	2.54	16.15	0.87
Cap 5	4.77	5.63	4803.1	1.42	24.90	2.75

A temperature sensitivity analysis was also done to test the robustness of the method against a varying temperature of $10°C$ to $90°C$ and found no significant variation from the ground truth measurements with a LCR meter tested at $1kHz$. As the method uses two different discharge curves for the estimation of parameters and the control parameters can be tuned externally with software makes it flexible to be used on a variety of systems. Also the VEN network can be designed to be a built-in part or an external unit attached to a system. This possibility makes it easier to implement onto an existing system.

3.5 Method 4

Method discussed in [23] is aimed at monitoring of DC-link capacitors present in electric vehicles with a topology shown in Fig. 3.8. A battery provides the energy to drive the electric motor through a two level inverter operating at $300V$. Due to large currents transmitted through the DC-link, film capacitors were deployed for suppressing the voltage ripple. The additional paths for switch S_x and R_start are provided for precharging the capacitor during the startup period. The sensors for measuring the DC-link voltage, phase currents and battery current are present for the purpose of control.

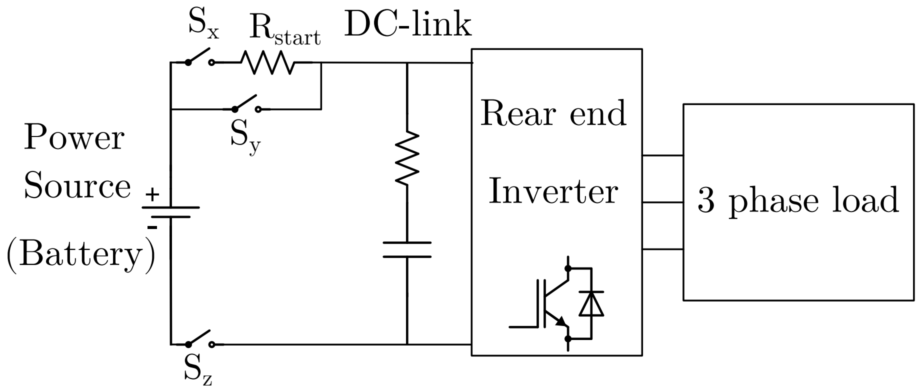

Figure 3.8: Topology of capacitor operation in [23]

When the motor is standstill during the shutdown phase or in the initial phase of startup after precharging, the switches S_x, S_y and S_z can be used to detach the DC-link capacitor from battery. As the self discharge rate for the capacitor is low, the DC-link voltage can be assumed to be constant during this period. The capacitor is discharged through the motor stator windings and care is taken to only produce d-axis current so as not to generate any torque. The absence of a dedicated capacitor current sensor is compensated by utilizing the existing phase current sensors and the inverter switching information. Since the battery is disconnected with the rest of the system, all the current from the capacitor goes through the inverter and the capacitor current can be reconstructed as per Eq. 3.16. Also a very short window is sufficient for monitoring the health of the capacitor.

$$i_\mathrm{dc} = S_\mathrm{a} i_\mathrm{as} + S_\mathrm{b} i_\mathrm{bs} + S_\mathrm{c} i_\mathrm{cs} = -i_\mathrm{cap} \tag{3.16}$$

where $S_\mathrm{a}, S_\mathrm{b}, S_\mathrm{c}$ are the inverter switching functions of respective legs, $i_\mathrm{as}, i_\mathrm{bs}, i_\mathrm{cs}$ are line current of respective phases, i_dc is the inverter current drawn after DC-link which is same as the capacitor current i_cap.

As the motor winding resistance is negligible, there is a possibility of large surge current when discharged directly from the capacitor. A current control loop is thus designed and added to the stator current control to limit the same. By considering the voltage model of PMSM drive system and the instantaneous power balance between the DC-link and the motor stator, a governing equation for the discharge current is dervied as per Eq. 3.17.

$$i_\mathrm{cap} = -\frac{3}{2u_\mathrm{dc}}\left[R_\mathrm{s} {i^r_\mathrm{ds}}^2 + \frac{L_\mathrm{d}}{2}\frac{d({i^r_\mathrm{ds}}^2)}{dt}\right] \tag{3.17}$$

where,

u_{dc} is the DC-link voltage

R_{s} is the stator resistance in motor standstill condition

L_{d} is the d-axis inductance of the motor

i^{r}_{ds} is the d-axis current

With the relation from 3.17 and the assumption that the changes of stator current control is much faster than that of the discharge current from capacitor, an outer loop is made onto the existing stator current loop. As the current path is not reversed during the entire estimation process, a linear relationship can be recognised between ${i^{r}_{\mathrm{ds}}}^{2}$ and i_{cap} and a controller is formulated as per Fig. 3.9. The controller consists of a pole at $\frac{2R_{\mathrm{s}}}{L_{\mathrm{d}}}$ and an integrator with gain set to $\frac{2\omega_{\mathrm{c}}}{L_{\mathrm{d}}}$. Here ω_{c} is the bandwidth of the closed loop controller.

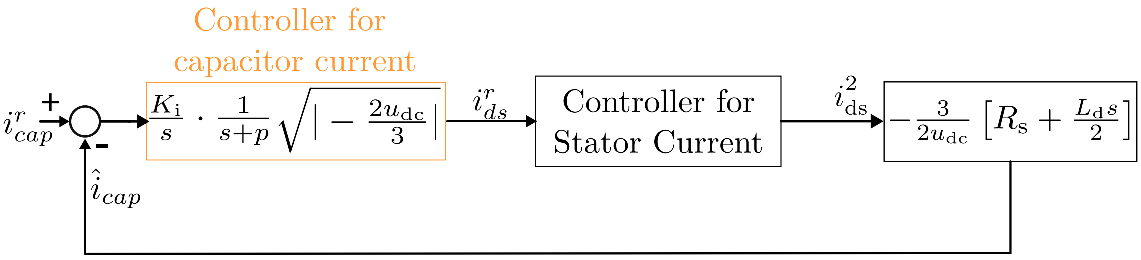

Figure 3.9: Capacitor current control loop for discharging

Experimental results were carried out to implement the method onto a PMSM drive unit with both electrolytic and film capacitors. The capacitor current controller was made to track a reference of $-0.16A$ with a bandwidth of $50Hz$. The stator bandwidth was set to $500Hz$ and the entire estimation process took $80ms$. The estimated capacitance settled around the actual value within $20ms$ with a steady state accuracy of 1.94% and 1.46% for electrolytic and film capacitors with a nominal values of $567\mu F$ and $410\mu F$ respectively.

3.6 Method 5

The method proposed in [24] is applicable for ASD system with a topology as shown in Fig. 3.10. A power source is used for driving a three phase AC machine with an inverter to control the power. The power source is supplying voltage at $380V$ and a film capacitor is used to link the power source and inverter. Two main contact switches S_{x} and S_{y} act as the circuit breaker for safeguarding and isolating the rest of system with the power source when not in use.

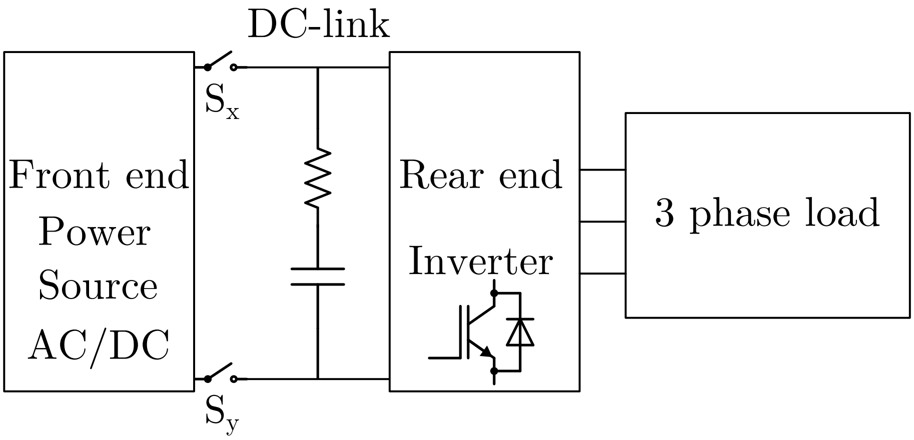

Figure 3.10: Overview of machine operation

After performing normal machine operation, when the machine enters the shutdown phase, the main contact switches are opened and the charged capacitor is made to discharge completely through the motor stator windings as shown in Fig. 3.11.

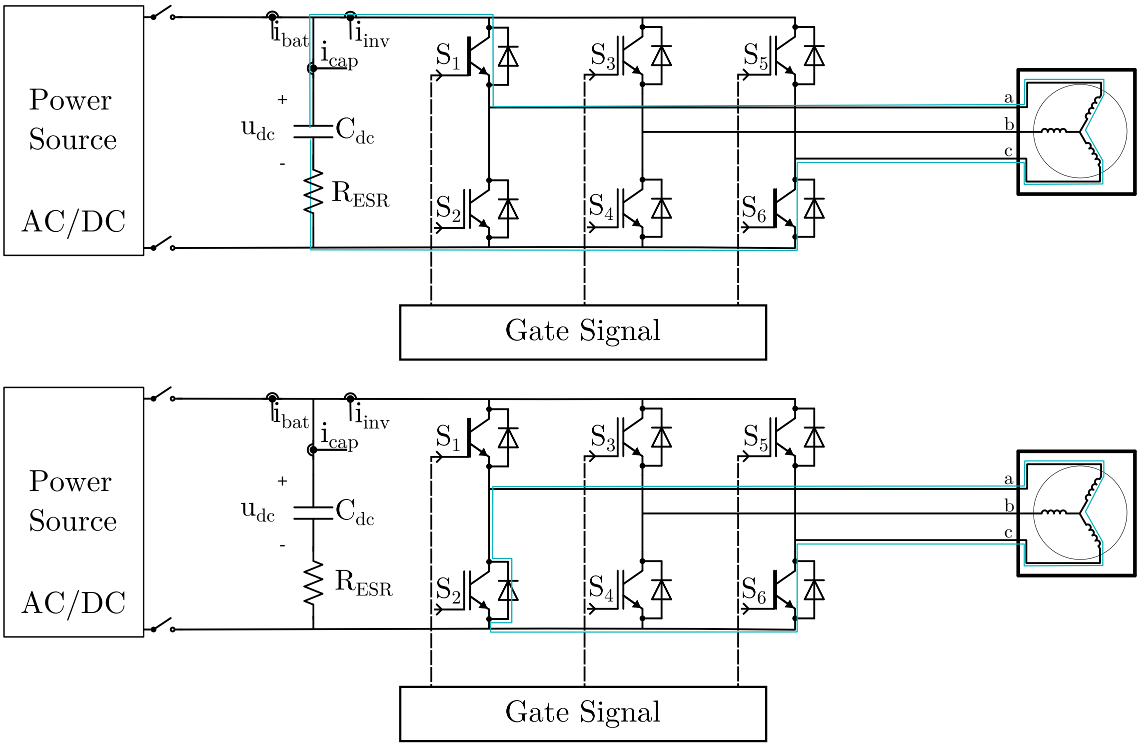

Figure 3.11: Topology of capacitor operation in [24]

As a large surge current is expected during this period, care is taken to only use certain combination of inverter switches so as to discharge the capacitor through two stator windings by actuating switches S_1 and S_6. With very little resistance offered by the motor coils, the resonance current quickly shoots to its maximum according to part 1 of Fig. 3.12. In the second part of the discharge process i.e., when the DC-link voltage drops completely to zero, the diode connected to switch S_2 prevents the reverse charging by providing an alternate path for the current to dissipate its energy. Thus the current oscillates and have an exponential decay. The discharge currents can be accurately measured with the help of existing phase current sensors and no additional hardware is required to carry out the health monitoring of the capacitor.

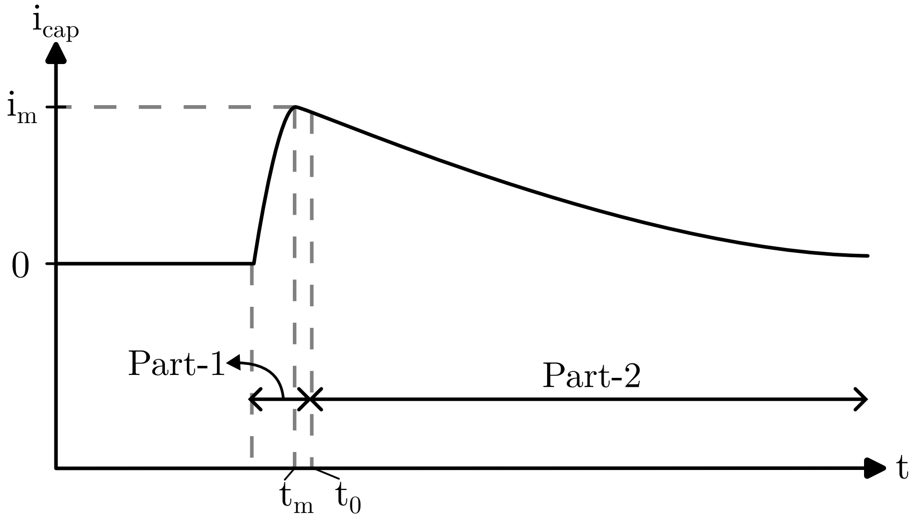

Figure 3.12: Discharge profile of capacitor during estimation

A mathematical expression can be formulated to estimate the resonance current during the first part of the discharge by considering the machine inductance and capacitance of the capacitor as per Eq. 3.18.

$$\begin{aligned} i(t) &= \alpha_1 \cdot e^{\alpha_2 t} \cdot sin(\alpha_3 t) \\ \alpha_1 &= \frac{u_{\mathrm{init}}}{\omega L_{\mathrm{s}}} \\ \alpha_2 &= -\frac{R_{\mathrm{ESR}} + R_{\mathrm{s}}}{L_{\mathrm{s}}} \\ \alpha_3 = \omega &= \sqrt{\frac{1}{L_{\mathrm{s}} C} - \left(\frac{R_{\mathrm{ESR}} + R_{\mathrm{s}}}{L_{\mathrm{s}}}\right)^2} \end{aligned} \tag{3.18}$$

where u_{init} is the initial DC-link voltage before discharge, R_{ESR} and C are the ESR and capacitance of the DC-link capacitor which need to be estimated, R_{s} and L_{s} are motor stator resistance and inductance respectively.

During the second part of discharge, only the motor parameters i.e., inductance (L_{s}) and resistance (R_{s}) majorly influence the freewheeling current and the dissipation can be modelled as per Eq. 3.19 where t_{m} is the time at which the resonant current reaches its maximum value as depicted in Fig. 3.12.

$$i(t) = [\alpha_1 \cdot e^{\alpha_2 t_{\mathrm{m}}} \cdot sin(\alpha_3 t_{\mathrm{m}})] \cdot e^{-\frac{R_{\mathrm{s}}}{L_{\mathrm{s}}}(t - t_{\mathrm{m}})} \tag{3.19}$$

As the equations in 3.18 and 3.19 contain mostly non-linear sinusoidal components, a multivariate nonlinear regression (MNR) is chosen for finding the best fit approximation. The data is successively tuned by iterative least squares (ILS) with forethought initial values. It should be noted that only one part of the curve is sufficient for accurate estimation of parameter. The rising part is preferred as the current is more accurately measured with an existing line current sensor. After estimating the optimal values for coefficients, capacitance is calulated according to Eq. 3.20.

$$C = \frac{\alpha_1 \cdot \alpha_3}{u_{\mathrm{init}}(\alpha_2^2 + \alpha_3^2)} \tag{3.20}$$

Simulation was performed for verifying the equations and found to have a good association with the resonant current curves. A notable increase in the values of t_{m} and i_{m} can be made with increasing values of capacitance. Experimental studies were also carried out on a $3kW$ induction machine with stator resistance and inductance of 1.8Ω and $7.2mH$ per phase respectively. Opting $100V$ as the initial voltage for the estimation process, $5ms$ and $20ms$ were taken for completing the rising part and the freewheeling part of discharge process.

Overall the method was proved to estimate with an accuracy of $< 0.27\%$ and $< 0.47\%$ for electrolytic and film capacitors with different values when tested at $25°C$ ambient. The test was further extended to analyze the sensitivity of the algorithm to variation in system parameters like stator resistance and inductance. The changes in parameters emulate the effect of temperature variations or other parasitic influence on the machine and still found the estimation accuracy to be under 1%. Similarly noise and other interferences were introduced during the operation and found no significant effect on the convergence of the algorithm. The method was also tested in different topologies like subway traction, doubly fed induction generator (DFIG) wind turbine and grid connected systems. The performance was maintained in all the systems with an exception of grid connected systems where some modification were necessary before implementing.

3.7 Method 6

The method discussed in [25] uses the discharge profile of capacitor in order to estimate its parameters. The topology of the system is modelled according to Fig. 3.13. A single phase AC is rectified with diode before connecting to the DC-link and inverter. The topology also consists of additional branches like 2F frequency filter and braking chopper to assist the operation of railway power trains. Film capacitors were used as the DC-link which was operating at $1500V$.

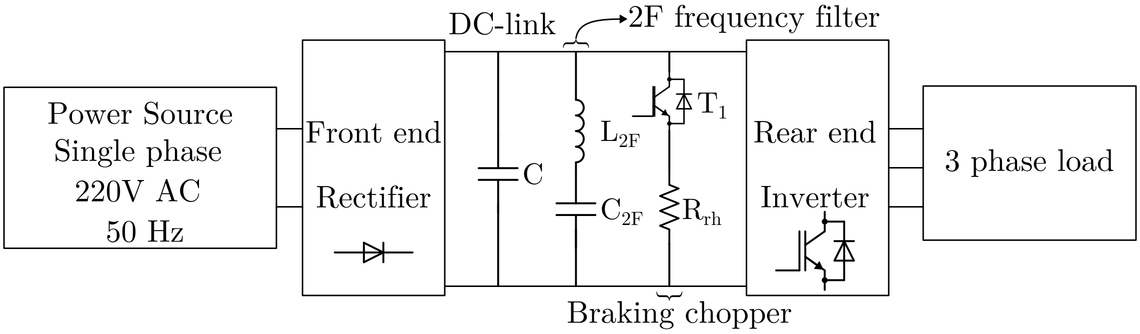

Figure 3.13: Topology of capacitor operation in [25]

After completing the normal operation of railway train, when the system enters the shutdown phase, the capacitors in DC-link and 2F filters gets de-energized slowly through their respective discharge resistors which are typically in the order of ~ $10^4\Omega$. A braking chopper with a resistor value of ~ $10^0\Omega$ is thus employed to have a faster discharge as shown in Fig.3.14.

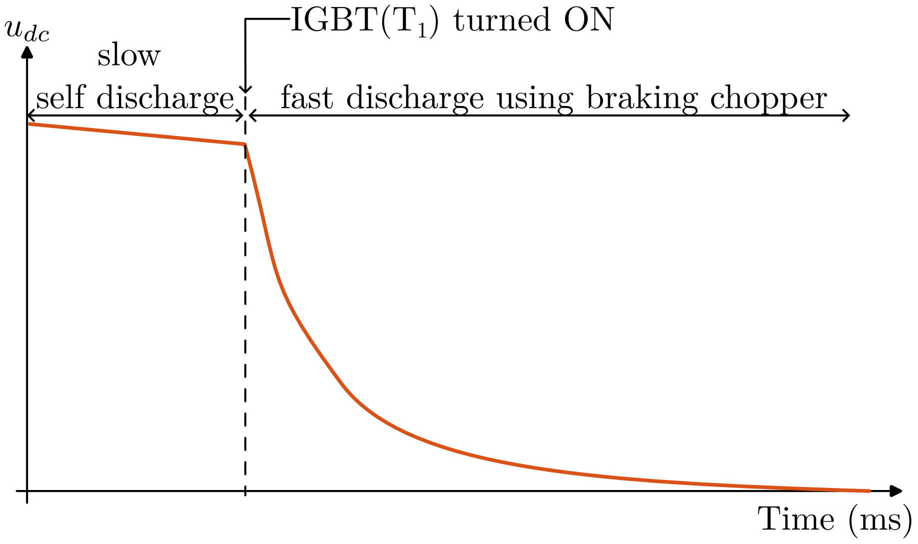

Figure 3.14: Discharge curve during algoritm operation

Two differential equations can be formulated according to Eq. 3.21 based on the DC-link voltage and current through 2F frequency filter branch ($i_{2\mathrm{F}}$) as the state variables. As there are second order derivate terms in the equations, a continuous time solution is implemented to deduct these variables. A n-order polynomial approximation is made for the functions and the derivatives are deduced by considering a data window of $2m+1$. With the availability of measurement data of state variables, least mean square (LMS) algorithm is applied again and corresponding equations in terms of $C_{2\mathrm{F}}$, $L_{2\mathrm{F}}$, R_{rh} and C_{dc} are obtained.

$$\begin{aligned} C_{2F}\frac{du_{dc}}{dt} - L_{2F}C_{2F}\frac{d^2 i_{2F}}{dt^2} &= i_{2F} \\ C_{dc}\frac{du_{dc}}{dt} + \frac{1}{R_{rh}}u_{dc} &= -i_{2F} \end{aligned} \tag{3.21}$$

The implementation is better explained through a flow chart shown in Fig. 3.15

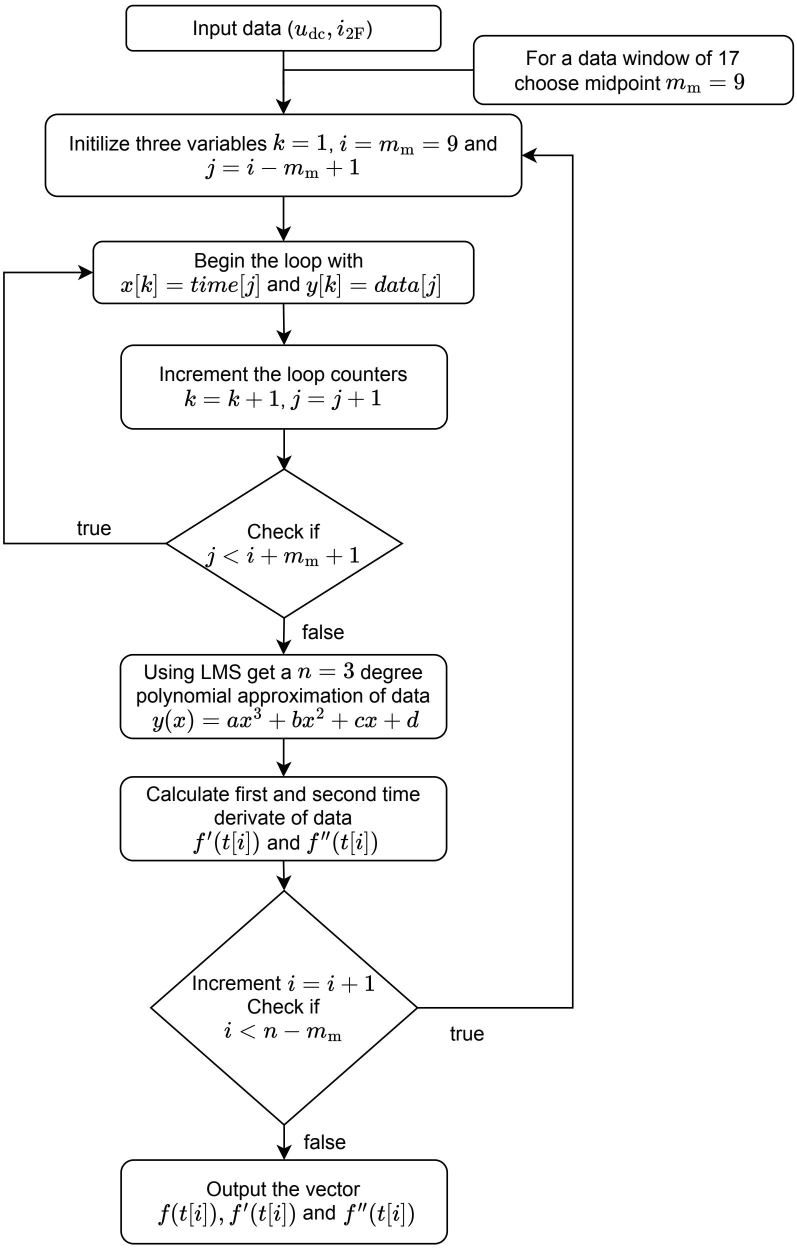

Figure 3.15: Algorithm for formulating the derivatives

Considering a third degree polynomial approximation ($n = 3$) and a sliding window of 17 ($m = 8$), simulation was done and resulted in an accuracy of < 0.7% for the parameter estimation using LMS algorithm. It should be noted that the data was acquired at a sampling frequency of $15kHz$. Experimental study was also carried out on a $1.2MW$ high speed train working at an ambient of $25°C$ and found the algorithm to perform with an accuracy of < 2.5%.

3.8 Method 7

As discussed in the earlier section 1.1.1 and from Fig. 1.5 a typical PMSM drive system with two level inverter for EV traction consits of six inverters which helps in driving three phases of the output to motor. A carrier based unipolar SVPWM is used for driving the gate signals and control the power output. These gate pulses employ a complementary switching strategy to avoid shorting the input and thus eight possible inverter switching states are possible based on which of the swiches are active at any given moment. The switching action of IGBTs induces ripple in voltage and current parameters of the DC-link capacitor. Table 3.2 shows the possible combination of states along with the output of inverter.

Table 3.2: Table of operation for inverter

Inverter State	**Transistors ON**	**Current $\mathbf{i}_{\text{inv}}$**
1(Zero State)	S_2, S_4, S_6	0
2	S_2, S_4, S_5	i_{c}
3	S_2, S_3, S_6	i_{b}
4	S_2, S_3, S_5	$i_{\text{c}} + i_{\text{b}}$
5	S_1, S_4, S_6	i_{a}
6	S_1, S_4, S_5	$i_{\text{a}} + i_{\text{c}}$
7	S_1, S_3, S_6	$i_{\text{a}} + i_{\text{b}}$
8(Zero State)	S_1, S_3, S_5	0

It can be noted from the above table that during two zero states (1 and 8), the inverter system is isolated from the battery. During these states the capacitor is getting charged from the source. As the current drawn from the inverter is zero, all the current from the battery is directed to charging the capacitor (i.e., $i_{\text{bat}} = i_{\text{cap}}$). The voltage change can be measured with the existing voltage sensor across the DC-link.

The capacitor is then estimated from the values of capacitor current and change in DC-link voltage by using the Eq. 3.22. It has to be noted that the zero states also contain the dead time compensation for IGBT switching which should be accounted while estimating the capacitance. As the estimation is limited only to one transistor state and doesnot require any interruption or special condition of system operation, this method can be categorised as completely online monitoring which can be implemented into system during nominal conditions. The method is primarily applied to aerospace drive system as per [26] which ensure reliability of the method as it has been demonstated in more robust and fault tolerant system topology.

$$\hat{C} = \frac{\int i_{\mathrm{cap}}\, dt}{\Delta u_{\mathrm{dc}}} \tag{3.22}$$

The method can be summerized using the flow chart shown in Fig. 3.16 from the perspective of implementation on the actucal system. Capacitor estimation is the primary focus of estimation from this approach as it was intended to be used for monitoring of film capacitor.

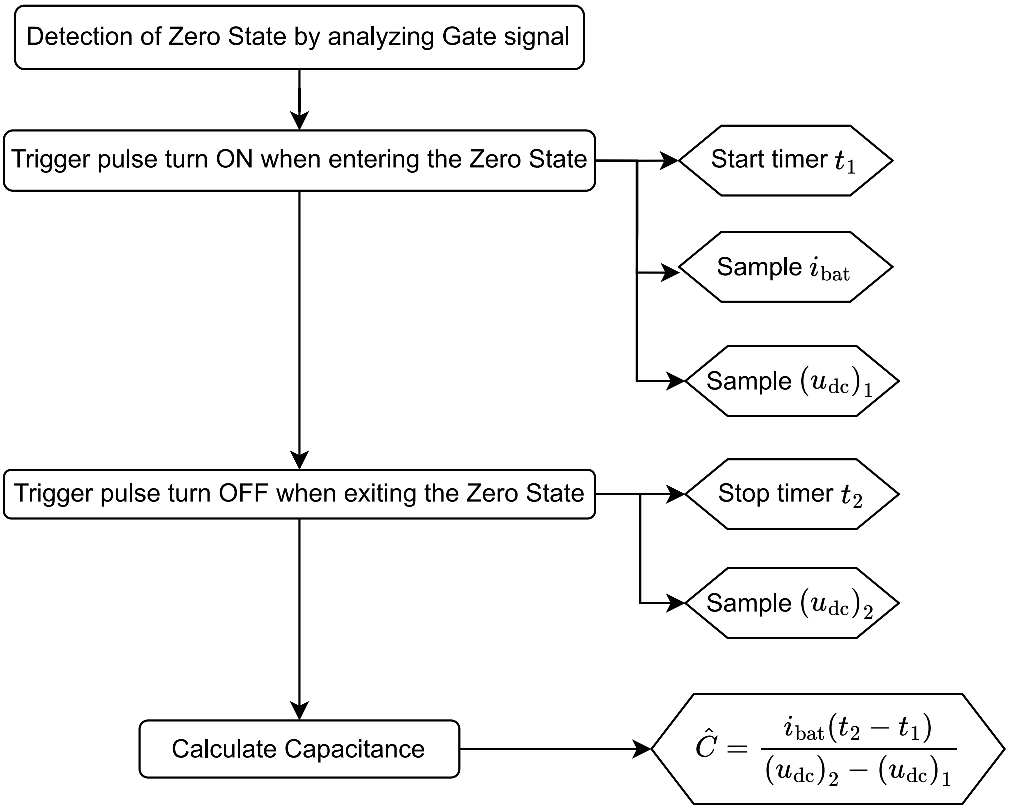

Figure 3.16: Flow chart for method demonstrated in [26]

3.9 Method 8

In the proposed method from [27], a special operating condition of the drive system when the motor is stationary typically during the startup phase of the drive system is chosen. During this stage, the capacitor is charged to the battery voltage with the help of a pre-charge circuit. It has to be noted that during the pre-charge operation, the inverter is non-functional and the Motor is isolated from DC-link and battery. The charged capacitor is then partially discharged through two phase lines of the motor winding so as not to generate any torque or motion of the motor. The discharge is carried out by incorporating a low frequency constant duty unipolar PWM stategy to any two switches of different inverter legs. As an example, considering the notations from Fig.1.5, if *a* and *b* legs are chosen for the discharge operation, S_4 would be closed and a constant duty PWM is applied to S_1. Thus, the current will pass through S_1 and S_4 whenever S_1 is ON and freewheels through Diode at S_2 when the S_1 is OFF. The equivalent circuit during the discharge operation is shown in Fig. 3.17.

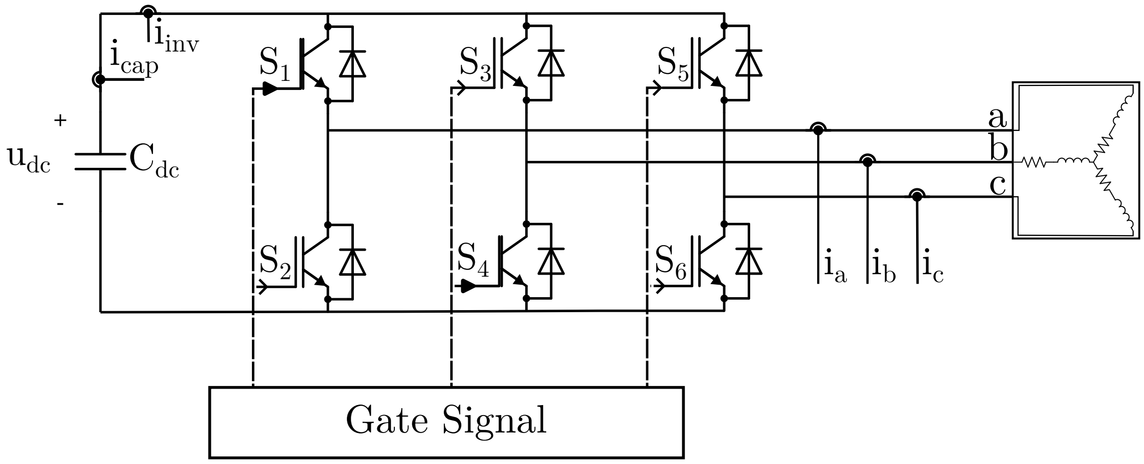

Figure 3.17: Topology of capacitor operation in [27]

As the capacitor current is passing through phase lines, it can be accurately measured with the existing line current sensors. The capacitance is estimated by dividing the current discharged with the change in DC-link voltage across the capacitor. Notably only the DC component of discharge current is accounted for calculation i.e., current discharged during the ON period of duty pulse and not the current which freewheels through the diode. The method can be summerized with the following flow chart in Fig. 3.18.

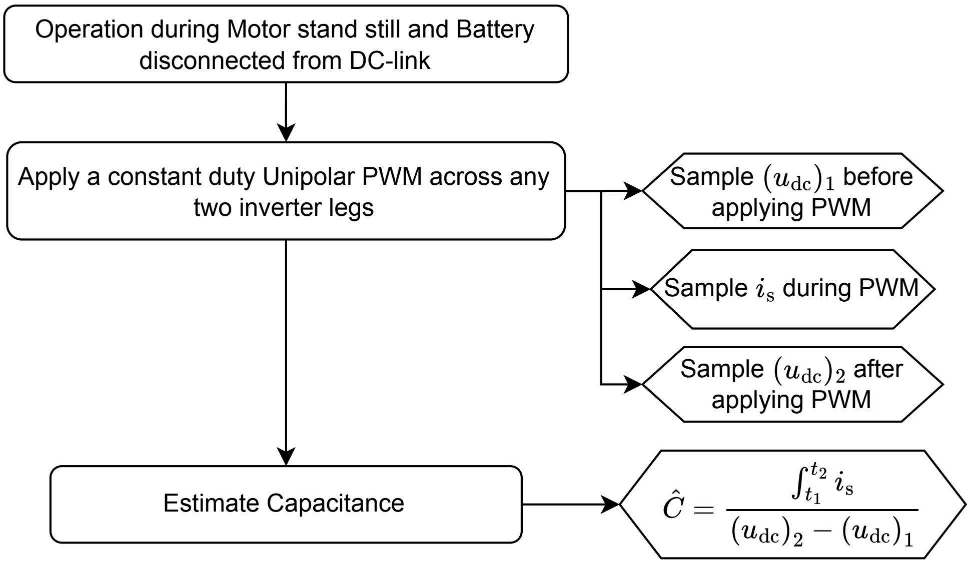

Figure 3.18: Flow chart for method demonstrated in [27]

3.10 Selection of methods

An overview of these methods is also presented in table 3.3. It is clear that most suggested methods utilize the fundamental equation 2.1 of capacitor for estimation purpose. Much of the methods also rely on parameter estimation algorithms to estimate the parameters of capacitor model. This requires to obtain a mathematical modelling of the system according to Fig. 2.2 and specific operating conditions for the parameters to converge to its optimal values. Hence based on the simplicity and convenience of implementation in traction inverters [26] and [27] are chosen as two methods and discussed further in the upcoming sections.

Table 3.3: Overview of state of the art CM methods

Ref.	Operation Principle	Formula
[20]	Model the system by choosing suitable parameters. Choose an optimization algorithm like LMS to converge the model parameters	Parameter Adaptation Algorithm (PAA)
[21]	Model the system by choosing suitable parameters. Choose an optimization algorithm like RLS to converge the model parameters	Recursive Least Squares (RLS)
[22]	During shutdown process, utilizing VEN obtain the characteristic discharge curves and calculate the time constants to estimate ESR/capacitance	$ESR = \frac{\tau_2 R_{\mathrm{X1}}}{\tau_1} - R_{\mathrm{X2}}$
[23]	A capacitor current controller is used to discharge the charged capacitor through motor stator windings at a steady rate without inducing torque and use the voltage change and current information to estimate capacitance	$\hat{C} = \frac{\int_{\Delta\mathrm{t}} i_{\mathrm{c}}\, dt}{\Delta v_{\mathrm{c}}}$
[24]	Charged capacitor at a pre defined voltage value is discharged through motor stator windings and current discharge profile is used to curve fit a best match for capacitance	Iterative Least Square (ILS)
[25]	Utilizing the braking resistor, discharge the capacitor and estimate parameters using Least Mean Square (LMS) algorithm	Least Mean Square (LMS)
[26]	During zero state of inverter (capacitor charging), obtain the voltage difference across DC-link and integrate the value of estimated capacitor current to get an estimate of capacitance	$\hat{C} = \frac{\int_{t_1}^{t_2} i_{\mathrm{c}}\, dt}{u_{\mathrm{dc}}(t_2) - u_{\mathrm{dc}}(t_1)}$
[27]	Operation during system startup. With planned inverter states, observe the voltage difference and stator currents over a particular duty cycle	$\hat{C} = \frac{D\, T_{\mathrm{s}}\, I_{\mathrm{as}}}{\Delta u_{\mathrm{dc}}}$

4

Results

From the conclusion of previous chapter, the two methods suitable for further evaluation and implementation is referred as method 7 for process outlined in [26] and method 8 for technique suggested in [27].

4.1 Implementation

Due to the constraints of limited access to all the hardware components of the traction inverter and to have a safety check of methodology before deploying it onto the actual hardware, the circuit was modelled and simulated using PLECS in Simulink. Although the simulation results only reflect an idealized response of the system, it is good to debug any errors in the early stage and correct them. The simulation also gives a baseline for what can be expected in the experiment which act as a good exemplar for comparison.

PLECS is a circuit simulation tool primarily focused on system level analysis of power converter. Although a standalone variant of the software exists, the project is carried out by the add-on version which is integrated inside a Simulink environment and simulated using a Matlab script.

4.1.1 Simulation model for method 7

The simulation was performed using two models of the traction drive system. Firstly it was implemented using a simple RL model to test the working and then it was simulated using a complex PMSM drive model. Analysis of both the models are discussed in their respective chapters.

4.1.1.1 RL model

RL model is a simplification of the complex variables of the drive motor like stator and rotor resistance, inductance, slip, torque and simplify into the resistance (R) and inductance (L) values. It has to be noted that this simplification is accurate only if the motor is stationary or loaded under a constant value. Any dynamic changes will not be captured by this model and will be an inaccurate description of the system. Fig. 4.1

shows the overview of simulation setup in Simulink which consists of several blocks for different functionality of the drive system and other components such as DC-link capacitor bank, inverter. The variables R_d and L_d models the combined effect of cable and DC-link resistance, cable and DC-link inductance respectively. The capacitor bank consists of two capacitors C_1 and C_2 with their respective ESR values of R_1 and R_2. The main contact switches S_1 and S_2 are used to safeguard the entire system by disconnecting from battery when not in use. Most of the parameters like line voltages and currents, DC-link volatge and current are measured withe help of corresponding sensors. Although the capacitor current is not used in the calculations directly, is still measured for comparision with the estimation and determining the accuracy. The stator windings of the drive motor are represented by three phase series connected RL which is interconnected again by a Y network (star configuration).

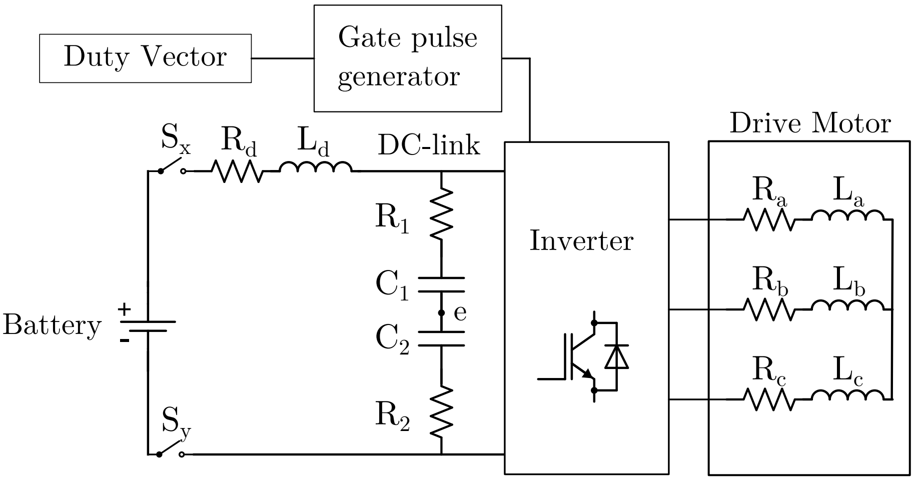

Figure 4.1: Overview of simulation setup for method 7

The duty vector block generates three sinusoidally varying signals of constant amplitude and frequency which are phase shifted by 120 degrees from each other. These duty vectors are then compared against a triangular carrier wave to generate a gate signal for each of the switch according to Table. 1.1. These signals are then used to operate and control the IGBTs arranged in the configuration similar to Fig. 1.5. The IGBTs are modelled as an ideal switch with no ON resistance, initial conductivity or delay. The effect of temperature are also not included in the modelling. The anti-parallel diodes conncted along with IGBTs are also modelled as an ideal component offerring zero resistance when forward biased. Assuming an equal voltage division between each of the capacitor, the common point e is chosen as the reference for the phase lines.

The simulation was performed with the parameter values as per A.1. As the method mainly relies on DC-link voltage and current, these were captured along with the inverter state as shown in Fig. 4.2. The capacitor bank had a total capacitance value of $330\mu F$ with a total ESR of $0.4m\Omega$. A switching frequency of $20kHz$ was chosen for carrier wave. The electric motor was modelled to have a stator resistance of $500m\Omega$ and stator inductance of $0.56mH$ in each of the phase line. The R_d and L_d values were decided to be $1001\mu\Omega$ and $3.4\mu H$ respectively. The DC-link voltage can be seen to have an average of $400V$ with a variation of $\pm5V$ and the current having a DC bias of $150A$. The system attains a steady state of operation after about $3ms$.

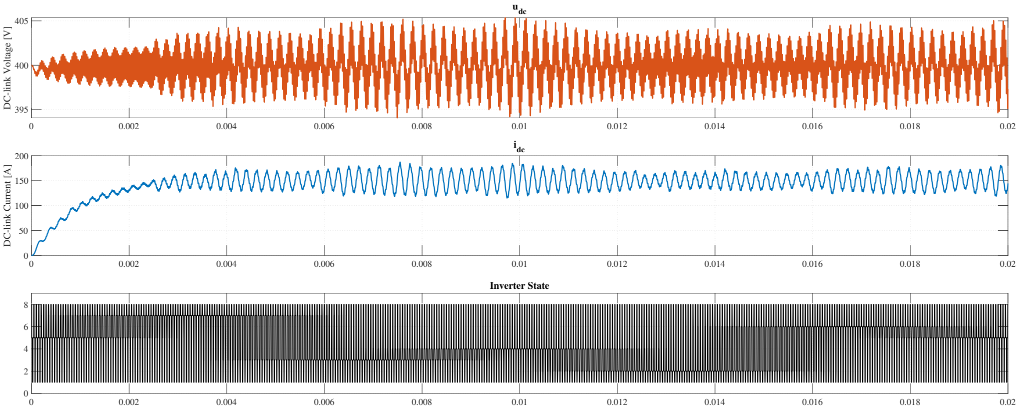

Figure 4.2: Simulation results for method 7 implementation in RL model

A zoomed version of the same is shown in 4.3 which captures the variation across two carrier cycles. The inverter is seen to be oscillating between states $1, 3, 7$ and 8 as per table 3.2. State 7 takes a significant share of the carrier cycle in which most of the power is utilized and the capacitor can be seen compensating for the instantaneous power by a slight decrease in DC-link voltage. As the inverter enters either of the zero states (1 or 8), the DC-link voltage can be seen to increase, indicating the charging of the capacitor bank.

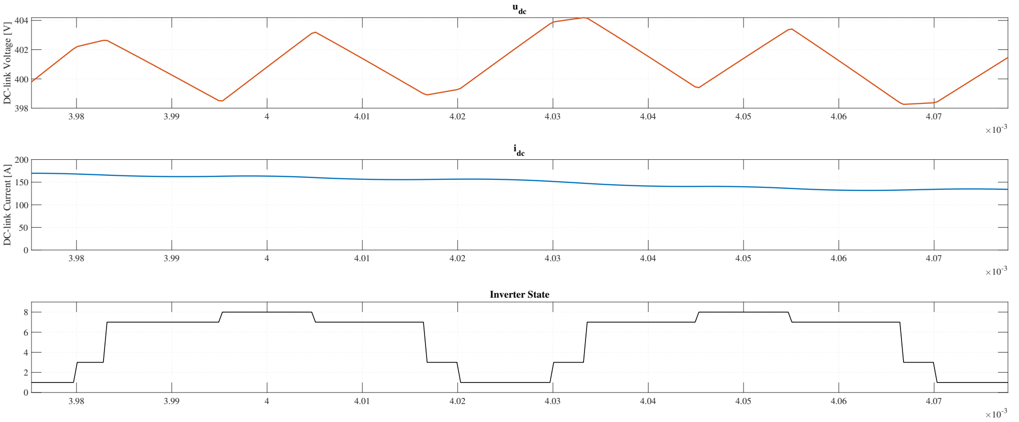

Figure 4.3: Zoomed view of two carrier cycles

The method explained in [26] is slightly modified to adapt to the simulation environment and ease of calculation. Firstly, the duty vector is analyzed and modified to compute the duration of zero vectors. This duration is used to generate a rectangular trigger with some margin to account for dead time compensation. The edges of the trigger is then utilized to sample the DC-link voltage and current. As during this capture interval, DC-link current itself is the capacitor current, an average value is considered for calculation. This average value of current is divided with the difference in DC-link voltage during the trigger interval to obtain an accurate estimate of capacitance as per equation 3.22. The entire process is better illustrated using a flow diagram as shown in Fig. 4.4.

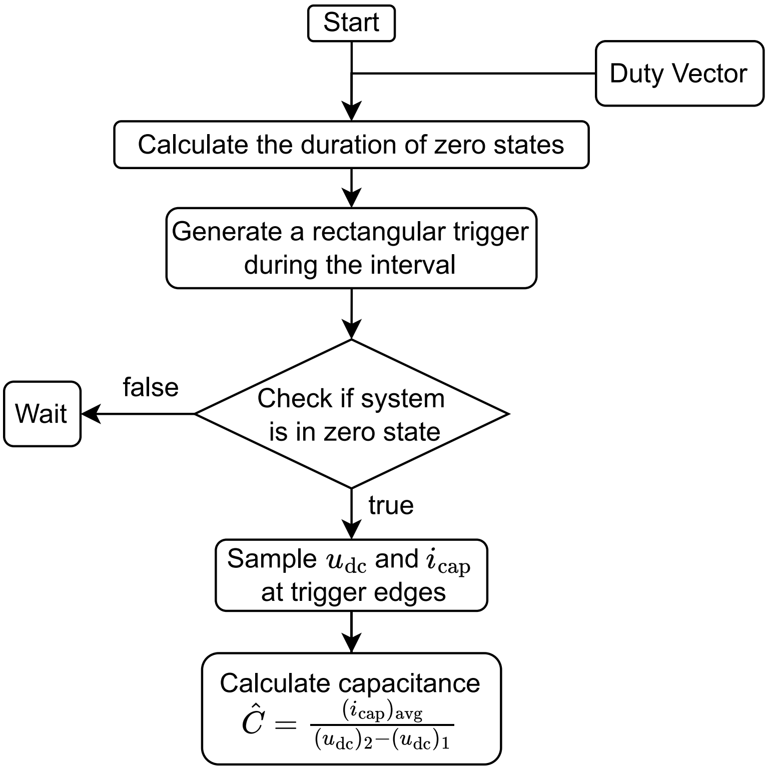

Figure 4.4: Logical flow diagram of capacitance estimation algorithm

The entire calculation for capacitance estimation was implemented as a MATLAB function shown in A.2. The capacitance was estimated with close proximity to actual value as shown in Fig. 4.5. The variations in the estimation signal can be seen to have a frequency of $250Hz$, which is quintuple the fundamental frequency of reference signal used to generate the sinusoidal waveform of $50Hz$. As in every carrier cycle, the zero states are ubiquitous, capacitance can be realised in a very short duration of machine operation. However care has to be taken so as to not generate a short pulse which will be difficult to generate distinct samples of variables. Thus, a threshold of 0.4 to 0.6 is recommened for the duty ratio. An accuracy of 99.36% was achieved with this method for a duty ratio of 0.54.

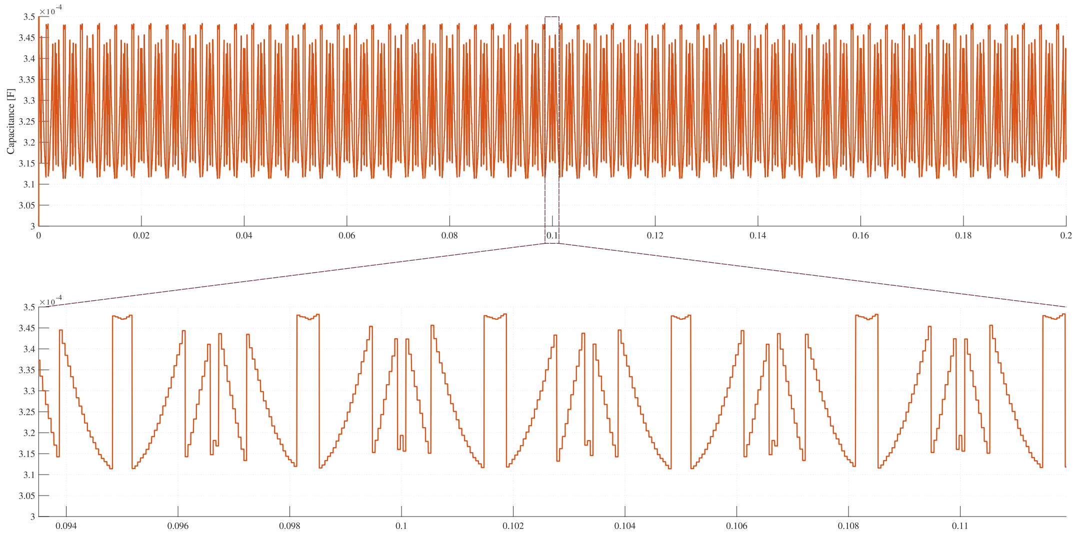

Figure 4.5: Capacitance estimation waveform for method 7

4.1.1.2 PMSM model

The general outline of a PMSM drive model is similar to that of a RL model as shown in the Fig. 4.1. The major changes are present in the controller and drive motor blocks. The drive motor consists of a non-excited synchronous machine model which can be configured. The motor consists of four pole pairs with the values of magnetic flux for *d* and *q* axes are measured and provided as a lookup table for simulation. Two sensors are used additionally, one for monitoring the electrical torque and another for measuring the rotational speed and position of the rotor.

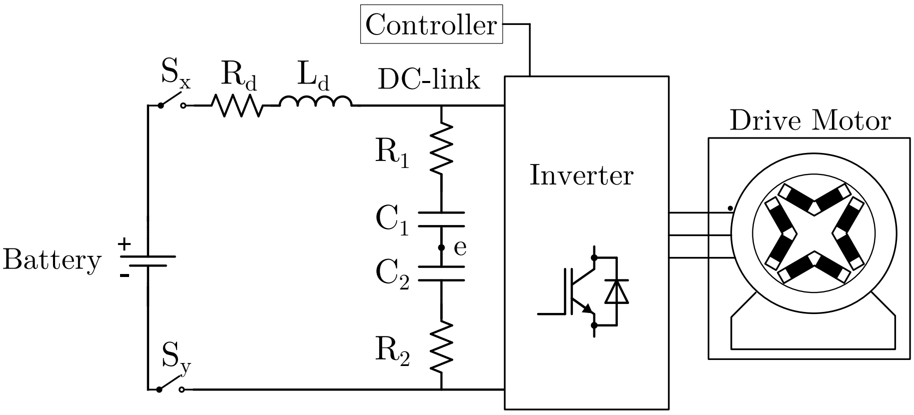

Figure 4.6: Overview of PMSM drive model

The controller consists of many blocks typically present in a FOC system as represented in Fig. 4.7. The measurement block helps to translate the encoder values into speed (ω) and angle (θ) of rotor along with the phase currents as *d* and *q* axis currents. The speed controller gets speed reference from a predefined speed profile of the machine and outputs a torque reference. The torque reference along with the actual speed information is fed to a 2-D lookup table to obtain *d* and *q* axis current reference values in the current reference calculation block. The current controller takes in all the information like DC-link voltage, speed and angle of rotor, actual d and q axis current with its reference and generates a voltage reference for all three phases. The modulator helps to generate the gate signal needed for control of IGBTs.

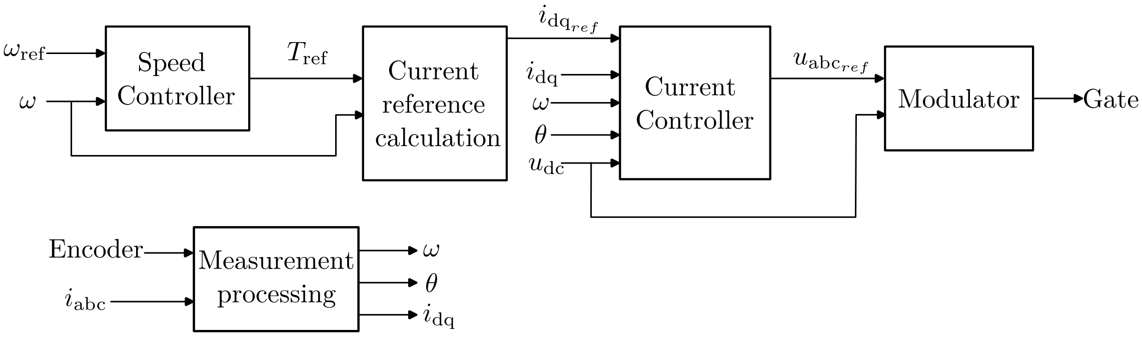

Figure 4.7: Overview of controller block for PMSM drive simulation

As this is an extensive model of the drive system, most of the dynamics of the system can be captured and analysed in detail. The motor is made to ramp up to a speed reference of 1500rpm in 0.25s and then maintain a constant speed with no load. After attaining the steady state, a gradual load of 180Nm is applied onto the motor. Since much of the torque is generated during this phase and power is consumed, this region is chosen for applying the estimation algoritm of [26]. Fig. 4.8 shows the waveforms obtained during the simulation results. The DC-link voltage is seen to be varying in a trapezoidal manner with the top gradual increase indicating the capacitor charging during zero state operation. The simulation was performed with the model parameters as per A.3 and the capacitance was estimated with an error of 22%.

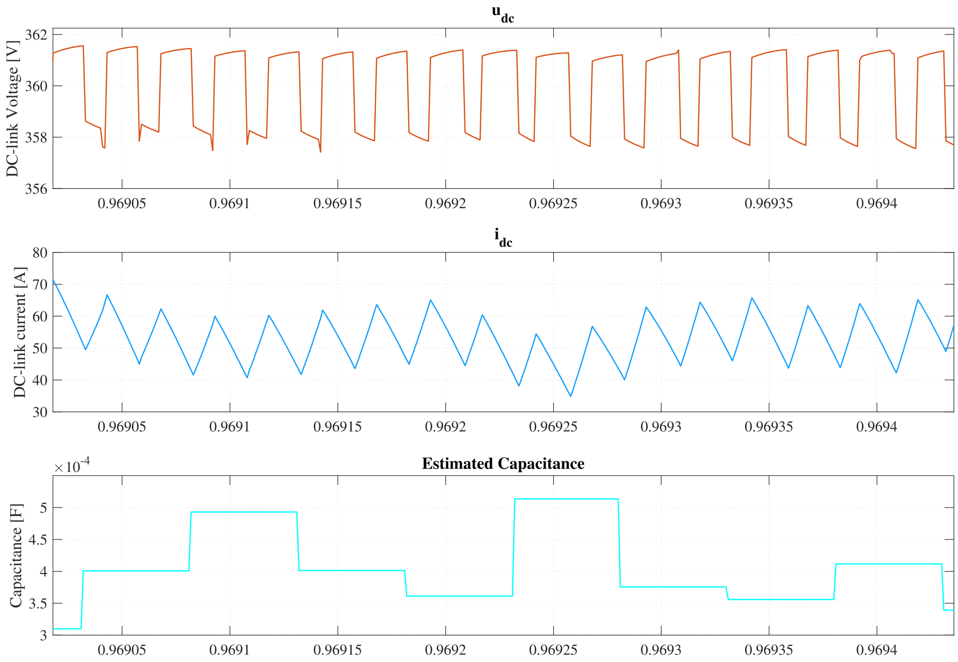

Figure 4.8: Simulation results for method 7 implementation in PMSM model

4.1.2 Simulation model for method 8

As the method discussed in section 3.9 is quasi-online, the simulation was performed only in the RL model of the drive system. The overall simulation setup and the parameter values are similar to the implementation of method 7, with some modifications being done for generating the gate pulses as shown in Fig. 4.9. Since the method is applied during the shutdown or startup phase, main contact switches are opened to isolate the DC-link from battery. Only two legs of the inverter are utilized for the operation as per Fig. 3.17. The unipolar PWM block generates a constant duty PWM gate pulses for switch S_1 while switch S_4 is constantly turned ON. The gate signal is generated as per the MATLAB function shown in A.4.

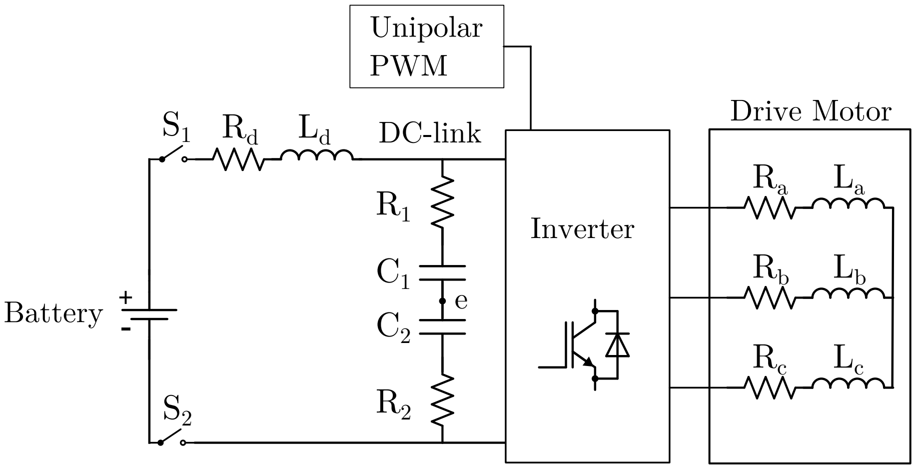

Figure 4.9: Overview of simulation setup for method 8

All the critical parameters required for the estimation of capacitance were captured and represented in Fig. 4.10. As the gate pulse is applied onto the switch, the DC-link voltage reduces in a staircase manner. The capacitor current forms a triangular waveform due to the increase in current initially during ON time of the switch S_1 and a slow exponential decay due to freewheeling across the diode. With the help of an existing phase current sensor for measuring the discharge current from the capacitor, the estimation of capacitance was achieved with a high accuracy of 99.95%.

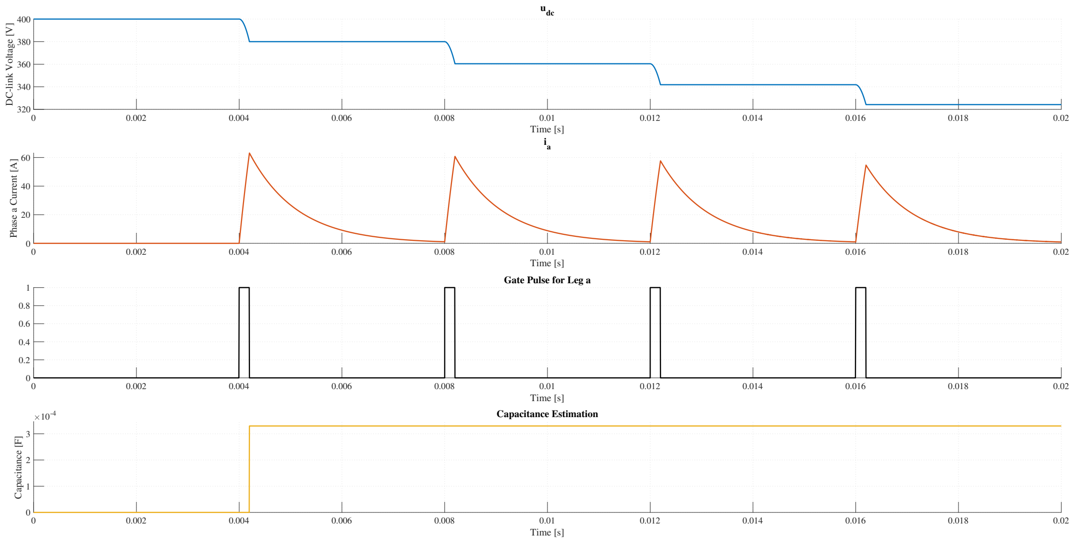

Figure 4.10: Simulation results for method 8 implementation

5

Conclusion

5.1 Remarks

This thesis provides a feasible way to monitor a capacitor which is one of the critical component of drive train unit in a BEV. Different capacitor technologies were also discussed along with their respective advantages and disadvantages in various applications. Considering MPPF as the suitable candidate to be used as the DC-link for traction inverters, cardinal causes of stresses were examined.

By choosing capacitance as the health monitoring parameter and an application convergance to ASD, many methods were reviewed for suitable adoptation which met most of the criterion and required no additional hardware. Two of these methods were selected for additional validation through simulation. One of the method being completely online was validated with two different models of drive train (RL and PMSM). In both the simulations, the model performed well within the required accuracy for CM of a MPPF capacitor. Another quasi online method had the best accuracy among the two although it was only validated using RL model.

In conclusion both of these methods are completely suitable for implementing onto an existing EV to monitor the health of DC-link to improve the reliability of the system by reducing system failures and unprecedented breakdowns.

5.2 Future work

As the scope of the thesis is focussed on monitoring the health of the capacitor with the help of capacitance, further evaluation can be done to include the efficacy of ESR into the calculation.

Additionally the monitored health of the capacitor can be further cross checked with the RUL calculations in order to substantiate the estimation.

As with most of the components, the temperature variations during operations will affect the characterstics and inturn the accuracy of estimation which can be evaluated by considering an analytical model of temperature fluctuations.

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A

Appendix 1

A.1 Parameter values for simulation of RL model

```
% Initialization file for simulation of 3 phase RL Load
clc
clear
close all

%% Power supply
Udc = 400;  % DC -link voltage for inverter [V]
Ldc = 2.4e-6;   % Inductance of DC source [H]
Rcable = 1e-3;  % Resistance of DC cable [ohm]
Lcable = 1e-6;  % Inductance of DC cable [H]
iL0 = 0;    % Initial current through the inductor

%% Inverter
Resr = 0.4e-3;  % Total ESR of DC link capacitor [ohm]
Cdc = 3*110e-6; % DC link capacitance [F]
Rdc = 1e-6;     % DC cable resistance [ohm]
fSW = 20e3;     % Switching frequency [Hz]
tSW = 1/fSW;    % Switching period [s]
Ts = tSW;       % Sampling period

%% Load
% R = 17.7e-3;  % Resistance [ohm]
R = 500e-3;     % Resistance [ohm]
L = 0.56e-3;    % Inductance [H]

%% Reference
u_s_amp = 150;  % Phase voltage amplitude
freq = 50;      % Fundamental frequency [Hz]

%% Simulation setup
k = 1;
nStep = 64;         % Number of time step per switching
   period
tStep = tSW/nStep;  % Step size of simulation [sec]
```

```
tStart = 0;          % Start time of simulation [sec]
tCycle = 1 / freq;   % Cycle time [sec]
nCycle = 2;          % Number of fundamental cycle
tStop = 5*tCycle;    % Stop time of simulation [sec]
tDuration = nCycle * tCycle; % Duration of data capture.
   Should be tStop for dynamic test [sec]

result = sim('Three_phase_RL.slx',[tStart, tStop]);
```

A.2 Method 7 capacitance estimation function

```
function[Cdc,trigger,i_C_1,u_DC_1] = fcn(measurement,time
   ,zero_vector,Cdc,trigger_old,i_C_1,u_DC_1)

t = mod(time,5e-05);    % Get Time in one Carrier
   Interval
dt = (0.8*0.5*zero_vector*5e-05);   % Calculate the
   interval of Zero Vector
t_on = 0.5*(5e-05-dt);  % Turn on time for Trigger
t_off = 0.5*(5e-05+dt); % Turn off time for Trigger

i_DC = measurement(7);
u_DC = measurement(8);

% Trigger
if t<25e-06 && t > t_on
    trigger = 1;
elseif t>25e-06 && t < t_off
    trigger = 1;
else
    trigger = 0;
end

% Sampling Capacitor Voltage and Current
if (trigger_old ~= 1) && trigger ==1

    i_C_1 = i_DC;
    u_DC_1 = u_DC;

elseif (trigger_old == 1) && trigger ~=1

    Cdc = abs(( 0.5 * (i_DC - i_C_1) +  i_C_1)* dt / (
       u_DC - u_DC_1));

end
```

```
end
```

A.3 Parameter values for simulation of PMSM model

```
% Initialization file for simulation of PMSM Drive
clc
clear
close all

tic

%% Load data
load 'MinCu - 360 V - 90 & 20.mat'      % FEM data
clearvars -except EM FEM

load 'PMSM Current reference 360V.mat'  % Current
   reference map
I_s_d = currentReference.idRef;
I_s_q = currentReference.iqRef;
OMEGA = currentReference.omegaRotor;
T_shaft = currentReference.TRef;

%% Power supply
Udc = 360;      % DC -link voltage for inverter [V]
Rdc = 0.096;    % Resistance of DC source [ohm]
Ldc = 1e-6;     % Inductance of DC source [H]
Rcable = 1e-3;  % Resistance of DC cable [ohm]
Lcable = 2.4e-6;% Inductance of DC cable [H]
iL0 = 0;        % Initial current through the inductor

%% Inverter
Resr = 40e-3;   % Total ESR of DC link capacitor [ohm]
Cdc = 330e-6; % DC link capacitance [F]
Rdc = 1e-6;     % DC cable resistance [ohm]
fSW= 20e3;      % Switching frequency [Hz]
tSW = 1/fSW;    % Switching period [s]
Ts = tSW;       % Sampling period

%% Machine
p = EM.p;                       % Number of pole pairs
Rs = EM.R_s;                    % Stator resistance [ohm]
Lend = EM.L_s_end;              % End winding inductance
   [H]
```

```
% Values matched with 5.0A q-axis reference step
J = 0.047;                        % Moment of inertia [kg*m
   ^2]
B = 8.9300e-04;                   % Viscous damping [N*m*s/
   rad]
% T_0 = 0.96;                     % Viscous damping [N*m*s/
   rad]

%% Current controller parameters
alphaI = 1e3;                     % Bandwidth of current
   controller [rad/s]
kUlim = 1;                        % Voltage limit factor
Psim = 0.0694;                    % No load d-axis flux
   linkage [Wb]
Ld = 4.4e-3;                      % No load d-axis
   inductance [H]
Lq = 1.3e-3;                      % No load q-axis
   inductance [H]
Kpd = Ld * alphaI;                % Proportional gain of
   current controller d-axis
Kpq = Lq * alphaI;                % Proportional gain of
   current controller q-axis
Rad = Kpd - Rs;                   % Active damping constant
    d-axis
Raq = Kpq - Rs;                   % Active damping constant
    q-axis
Kid = Ld * alphaI^2;              % Integral gain of
   current controller d-axis
Kiq = Lq * alphaI^2;              % Integral gain of
   current controller q-axis

%% Speed controller parameters
Jc = 0.053;                       % Moment of inertia [kg*m
   ^2] for control
Bc = 0.02;                        % Viscous damping [N*m*s/
   rad] for control
alphaS = 20;                      % Bandwidth of speed
   controller [rad/s]
Kps = alphaS * Jc;                % Proportional gain of
   speed controller
enableAD = 0;                     % Enable active damping
Ba = (Kps - Bc) * enableAD;       % Active damping constant
Kis = alphaS * (Bc + Ba);         % Integral gain of speed
   controller
Tmax = 200;                       % Maximum torque [Nm]
```

```
enableTff = 1;                  % Enable feed forward of
   load torque

%% Reference
array_speed  = 1500;      % Rotor speed reference [rpm]
array_torque =   180;     % Load torque [Nm]
tStepUpOmegaRef = 0.05;   % Rotor speed reference step up
   time [sec]
tStepDownOmegaRef = 3;    % Rotor speed reference step
   down time [sec]
tStepUpTload = 0.8;       % Load torque step up time [sec]
tStepDownTload = 3;       % Load torque step down time [
   sec]
omegaSlew = 6e3;          % Rate limit for rotor speed
   reference [rpm/sec]
TSlew = 600;              % Slew rate of load torque [Nm/
   sec]

Tload = array_torque;
OmegaRef = array_speed;
Pmax = 50e3;

%% Simulation setup
freq = OmegaRef * p / 60;       % Fundamental frequency [
   Hz]
nStep = 50;                     % Number of time step per
    switching period
tStep = tSW/nStep;              % Step size of simulation
    [sec]
tStart = 0;                     % Start time of
   simulation [sec]
tCycle = 1 / freq;              % Cycle time [sec]
nCycle = 2;                     % Number of fundamental
   cycle
tStop = 1;                    % Stop time of simulation [
   sec]
tDuration = nCycle * tCycle;    % Duration of data
   capture. Should be tStop for dynamic test [sec]
N.torque = length(array_torque);
N.speed = length(array_speed);
N.data =  N.torque * N.speed ;
N.sample = round(tDuration / tStep);

sim('PMSMDrive',[tStart, tStop])

filename = string(compose('Drive simulation results %d
```

```
   rpm %d Nm.mat', array_speed, array_torque));
%save(filename);

n = 1;

postProcess

toc
```

A.4 Method 8 signal generation

```
function [Scont, Sa, I]  = MethodB_Sa(Iold, tChrg, tStep,
    dcont, da)

I = tStep / tChrg + Iold;

if I >= 1

    I = 0;

end


if (I >= 0 ) && (I  <  dcont)

    Scont = 1;
    Sa = 0;

elseif (I > 2 * dcont ) && (I  <  2 * dcont + da)

    Scont = 0;
    Sa = 1;

elseif (I > 4 * dcont ) && (I  <  4 * dcont + da)

    Scont = 0;
    Sa = 1;

elseif (I > 6 * dcont ) && (I  <  6 * dcont + da)

    Scont = 0;
    Sa = 1;

elseif (I > 8 * dcont ) && (I  <  8 * dcont + da)
```

```
    Scont = 0;
    Sa = 1;

else

    Scont = 0;
    Sa = 0;

end


end
```

A.5 Method 8 capacitance estimation function

```
function [ia, i_cap, u_dc,  Q, C, u_dc1] = Cap_est(
   Measurement,Sa, Saold, QCold, C,u_dc1,  tStep)

ia = Measurement(1);     % Phase a current [A]
u_dc = Measurement(8);    % DC-link Voltage [V]

i_cap = ia * Sa;

Q = i_cap * tStep + QCold; % Charge

if Sa > Saold

    u_dc1 = u_dc;

    Q = 0;

elseif Sa < Saold

C = Q / (u_dc1- u_dc);

end

end
```

DEPARTMENT OF ELECTRICAL ENGINEERING
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden
www.chalmers.se

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