

Point of Load converters with coupled inductors for fast transient

Master's thesis in Sustainable Electric Power Engineering and Electromobility

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inductors for fast transient**

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Abstract

In today's rapidly advancing technological landscape, the demand for high-speed operations extends to the communication sector, necessitating faster and more responsive devices. This thesis investigates the use of various inductor topologies in multiphase buck converters, which serve as critical power supplies for numerous components. The focus is on analyzing the transient behavior of different inductor configurations to enhance current rise time. Specifically, the study compares common discrete inductors (DL), coupled inductors (CL), notched coupled inductors (NCL), and Trans-Inductor Voltage Regulators (TLVR) in terms of their dynamic response, output voltage ripple, and efficiency. The research is divided into two phases:

- **Simulation:** This phase evaluates the performance of all inductor couplings, examining their efficiency, dynamic response, power system rejection ratio, and stability.
- **Hardware Implementation:** This phase focuses on two inductor couplings, DL and CL, to validate the simulation results concerning efficiency, stability, and voltage ripple through physical testing.

The study was conducted with all topologies having similar stability margins. The results reveal that coupled inductors and their variants achieve higher efficiencies, with CL and NCL reaching a maximum efficiency of 95% compared to 91% for DL and TLVR. This trend was also observed in physical testing. In terms of transient performance, DL achieved the highest current slew rate of $-19.59 \text{ A } \mu\text{s}^{-1}$ during load release. The voltage and current ripples in CL and NCL contained only high-frequency components, whereas DL and TLVR exhibited both high and low-frequency components. Additionally, the PSRR was better in CL, with a gain ($\frac{V_{out}}{V_{in}}$) of 0 dB compared to DL, which had a gain of 60 dB.

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List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

ADI	Analog Devices, Inc.
CCM	Continuous Conduction Mode
CL	Coupled Inductor
DCM	Discontinuous Conduction Mode
DL	Discrete Inductor
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FCM	Forced Continuous Mode
FOM	Figure of Merit
FRA	Frequency Response Analyzer
GND	Ground
IC	Integrated Circuit
MPBC	Multi-Phase Buck Converter
NCL	Notch Coupled Inductor
OCL	Open-circuit Inductance
PSM	Pulse-skipping mode
PSRR	Power System Rejection Ratio
TL	Trans-Inductor
TLVR	Trans-Inductor Voltage Regulator
SM	Synchronization Mode

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1

Introduction

1.1 Background

Buck converters are a type of DC/DC converter that reduce the voltage magnitude from the input to the output. They are used in a wide range of applications, such as radio systems, battery management systems, and motor controllers. The operation of a single-phase buck converter is limited by the maximum current it can provide. Higher currents can lead to decreased overall efficiency due to excessive resistive (I^2R) losses, depending on application [1]. For applications with higher current demands, such as application-specific integrated circuits (ASICs) requiring currents of 600 A and current slew rates of $1200 \text{ A } \mu\text{s}^{-1}$ [2], a single-phase buck converter may not be feasible. In these cases, multi-phase buck converters (MPBCs) may be more advantageous [1].

The increasing use of MPBCs over the past decades is driven by the rising power demands of applications such as processors [3, p. 457]. This has created a need for flexible operations between low-power and high-power applications using the same converter. Conventional multi-phase converters with discrete inductors (DL) perform worse in low-current applications compared to single-phase buck converters [4]. The implementation of coupled inductors (CL) at the output of MPBCs is a relatively new but growing concept that enhances the efficiency of MPBCs in low-current applications [4]. Examples of a CL setup used in MPBCs is the Notch Coupled Inductor (NCL).

In a previous study at Ericsson, a comparison between the use of Trans-Inductor Voltage Regulator (TLVR) and conventional DL showed that TLVR was more beneficial [5]. In this thesis, we will conduct a comparison of CL and NCL with DL, and TLVR by simulation and physical testing.

A previous study at Ericsson compared the use of TLVR and conventional DL, finding TLVR to be more beneficial [5]. In this thesis, we will compare NCL with DL in an experimental setup and in simulation. A comparison will be made to TLVR, which will only be tested through simulation.

1.2 Aim

Compare the performance of a multi-phase buck converter using four different types of inductor topologies: DL, CL, NCL, and TLVR. This comparison includes efficiency, output voltage ripple, and load step response. Additionally, the thesis involves conducting simulation tests for all inductor topologies, and hardware tests specifically for DL and CL using test boards provided by Analog Devices Inc. (ADI).

2

Theory

This section aims to introduce and explain various concepts important for investigating the objective of this thesis. The buck converter is detailed for both single-phase and multi-phase implementations. Different inductor topologies are described and contrasted, and the integrated circuit (IC) to be used in simulations and on the test boards is detailed. Furthermore, system stability concepts are introduced, as they are crucial for determining the viability of a simulation model or on-board implementation. Finally, the simulation software to be used is presented.

2.1 Buck converter

The buck converter is a type of DC-DC converter which transforms a given input voltage V_{in} to a lower output voltage V_{out} . The action of reducing, or stepping down, the voltage level is why the buck converter is also known as a step-down converter. The principle of operation can be explained in regards to Figure 2.1a where a purely resistive load R is used. To realize the stepping down of the voltage level to the load a switch Q is used. Neglecting losses, when Q is switched on for a time period t_{on} V_{out} will equal V_{in} . Correspondingly when Q is switched off for a time period t_{off} , V_{out} will equal zero.

The total time taken for Q to change from the on- and off state to a new on-state is defined as the switching time period T_s and is the sum of t_{on} and t_{off} . This time period, or switching cycle, is the inverse of the switching frequency f_{sw} which defines how many switching cycles occur during one second. The average output voltage $V_{out,RMS}$ can be controlled by adjusting the duty cycle D , which defines the ratio between t_{on} and T_s . An increase of D will lead to an increase in the average output voltage $V_{out,RMS}$; similarly, a decrease of D will lead to a decrease in $V_{out,RMS}$. However, an implementation of this simple schematic would result in large output voltage ripples ΔV_{out} which may not be suitable for many applications.

Hence, a more realistic schematic of the buck converter is presented in Figure 2.1b. Three additional elements are introduced: a diode d , an inductor L and a capacitor C . Assuming lossless operation, during t_{on} both R and L are provided with V_{in} , and d remains reverse biased. L acts as an energy storage element so that during t_{off} R receives current from L , and a current path is provided by d being forward-biased. C and L constitute a low-pass filter which attenuates harmonics and in turn reducing ΔV_{out} . Note that in practical implementations d is substituted by another switch Q .

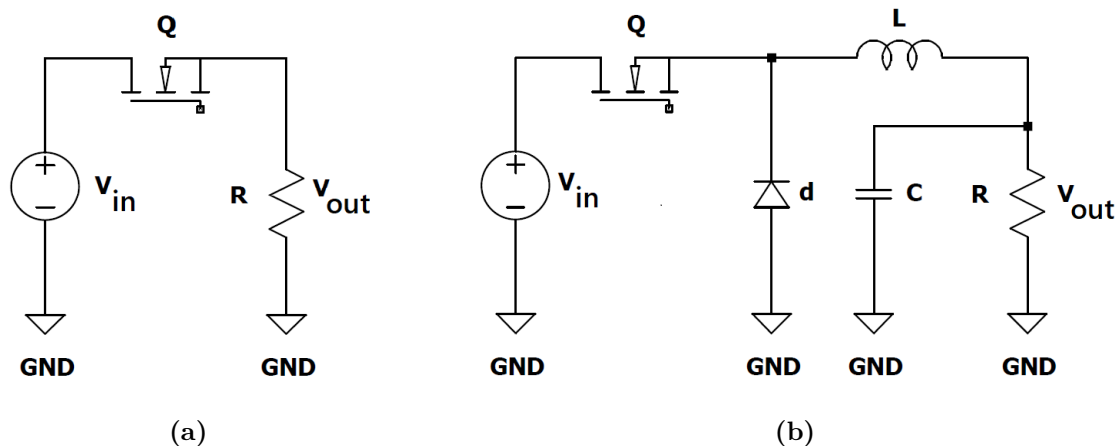


Figure 2.1: (a) Simplified schematic of the buck converter. (b) Complete schematic of the buck converter.

There are equations of interest when considering the buck converter. One is the ratio between V_{out} and V_{in} during continuous conduction mode (CCM) which means that the inductor current i_L never reaches zero which would be the case for discontinuous conduction mode (DCM). The ratio between V_{out} and V_{in} is defined for CCM operation as the duty cycle D and can be expressed as

$$\frac{V_{out}}{V_{in}} = D \quad (2.1)$$

where V_{out} is the output voltage, V_{in} is the input voltage, and D is the duty cycle. Another equation of interest, which is not specific to the buck converter, is the current slew rate of the inductor $\frac{di}{dt}$. This can be expressed as

$$\frac{di}{dt} = \frac{V_L}{L} \quad (2.2)$$

where $\frac{di}{dt}$ is the inductor current slew rate, V_L is the voltage across the inductor, and L is the inductor value. (2.2) can be used to highlight why the single-phase buck converter may be unsuitable for high-current applications. Processor loads are characterised by fast transient responses, meaning that the current demand changes rapidly and $\frac{di}{dt}$ is high. This necessitates that an inductor provides fast $\frac{di}{dt}$ which requires a small inductor. In contrast, sensitive applications such as processors demand a limited output voltage ripple ΔV_{out} which would necessitate having a large value of L which may both increase cost and size of the inductor. Given that these attributes directly contradict each other, the single-phase buck converter may be a non-viable solution. Furthermore, for high-current applications, the single-phase buck converter can be unsuitable due to excessive resistive losses. To address these issues, the multi-phase buck converter may be a more suitable alternative [1].

2.1.1 Multi-phase buck converter (MPBC)

The MPBC is essentially a parallel connection of N single-phase buck converters where the load is shared among the converters. Each branch, or phase, is phase-shifted and shares a common voltage source. This influences the permissible duty cycle D which can be used. The sum of D for all phases should be less than or equal to 1 [3, pp. 516-517]. According to [6, p. 3], this can be expressed as

$$D \leq \frac{1}{N} \quad (2.3)$$

Where D is the duty cycle, N is the number of phases. One benefit of using multiple phases as opposed to the single-phase buck converter is that a higher load current i_o can be achieved. i_o also contains less ΔV_{out} as ripple currents Δi in each phase are cancelled due to an increase in ripple frequency. This ripple cancellation is due to the interleaving, or parallel connection, of the phases where each phase operate at the same f_{sw} . Yet, the output experiences an effective switching frequency $f_{sw,eff}$ which is a multiple of f_{sw} depending on N , and can thus be expressed as

$$f_{sw,eff} = N f_{sw} \quad (2.4)$$

where $f_{sw,eff}$ is the effective switching frequency, f_{sw} is the switching frequency of a single phase, and N is the number of phases. Given that f_{sw} can be kept low in each phase, the active power losses (losses occurring during switching) are reduced. Furthermore, the ripple cancellation reduces the requirements for output filtering, reducing the required size of the output capacitance C_{out} [3, pp. 516-517]. An important aspect of high current applications, such as ASICs, is that transient performance is enhanced. Compared to a single-phase solution, for a given i_o , each phase's L is reduced in size as the load is shared among the phases. This reduces the energy storage capabilities of each inductor and thus makes the inductor respond faster to load variations, i.e., transients [3, p. 460].

The operation principle is essentially the same as for the single-phase buck converter and can be explained with reference to Figure 2.2. T_s can be divided into three parts: t_1 , t_2 and t_3 . During t_1 , switch Q_1 is on and R is supplied with V_{in} as the current path goes through the inductor L_1 while the diode d_1 is reverse-biased. Switch Q_2 is off, and the energy stored in inductor L_2 is dissipated to R where the current path loops around L_2 and R through diode D_2 , which is forward-biased. During t_2 , both Q_1 and Q_2 are off, and energy stored in L_1 and L_2 is dissipated to R , with the current path looping through respective diodes d_1 and d_2 as they are forward-biased. During t_3 , switch Q_2 is on and R is supplied with V_{in} as the current path goes through L_2 while d_2 is reverse-biased. Q_1 is off, and the energy stored in L_1 is dissipated to R where the current path loops around L_1 and R through d_1 , which is forward-biased [3, pp. 516-519]. As for single-phase buck converters, d_1 and d_2 may be substituted with switches Q for MPBCs.

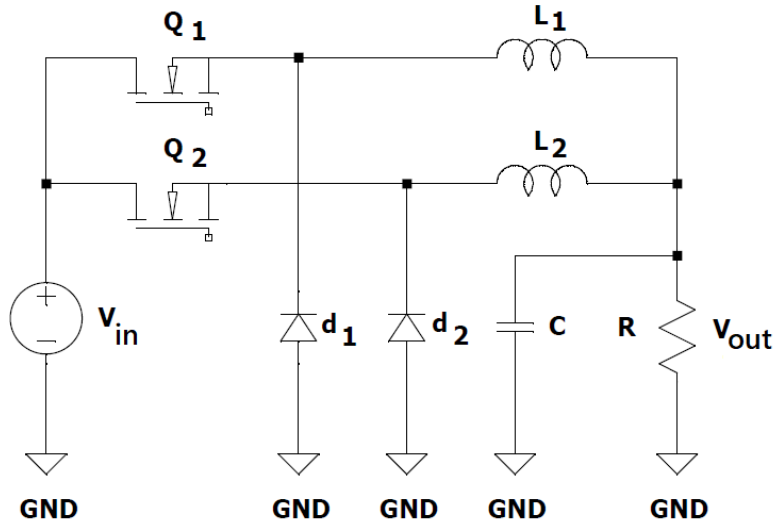


Figure 2.2: Schematic of multi-phase buck converter using $N=2$ phases.

2.1.2 Discrete inductors in MPBCs

Discrete inductors (DL) are conventionally used in MPBCs. To implement DLs in a MPBC, the design procedures in [7] can be followed to determine appropriate values. For the selection of a DL, its value is selected based on V_{out} , V_{in} (as D depends on it), f_{sw} and maximum allowable ripple current through the inductor I_{PP} . The value of L can be calculated according to [7] as

$$L = \frac{V_{out}(1-D)}{f_{sw} \cdot I_{PP}} \quad (2.5)$$

where V_{out} is the output voltage to the load, D is the duty cycle, f_{sw} is the switching frequency for a single phase, and I_{PP} is the maximum allowable ripple current through the inductor which in accordance with [7] can be expressed as

$$I_{PP} = \frac{0.25I_{max}}{N} \quad (2.6)$$

where I_{PP} is the maximum allowable ripple current through the inductor, I_{max} is the maximum current to the load and N is the number of phases in the MPBC.

By applying (2.6) and (2.5), the equivalent inductance L_{eq} can further be calculated. L_{eq} is the total inductance value present during a transient event. Essentially, during a transient response such as a step load, the PWM signals to the individual phases start overlapping. This causes multiple phases to conduct simultaneously, in essence placing them in parallel by N phases. In this state, the inductance is reduced by an amount by N . L_{eq} for a DL can be calculated as

$$L_{eq,DL} = \frac{L}{N} \quad (2.7)$$

where $L_{eq,DL}$ is the combined equivalent inductance for a DL during a transient event,

L is the inductance value of a single phase during steady-state and N is the number of phases in the MPBC.

2.1.3 Output capacitors in MPBCs

Similar to the inductor, [7] can be followed to determine what appropriate capacitor values might be. According to [7], there are several ways to calculate the minimum C_{out} required to keep the system within the tolerances specified by the tolerated DC and AC ripples present on the output of the MPBC to the load. One way is to consider the DC ripple relating to $\Delta V_{out(DC)}$. This is the steady-state voltage ripple caused by the current ripple through the inductor. Another way is to consider the AC ripples relating to $\Delta V_{out(AC)}$.

The AC ripples are transient ripples caused by stepping (increasing) the load or releasing (decreasing) the load. A voltage dip is the result of a step load, as it takes some time for the MPBC to supply the demanded current. Thus, current is drawn from the output capacitors, which results in a voltage dip (undershoot). The opposite occurs for a load release, where excess charge needs to be stored in the capacitors, causing the voltage to rise (overshoot) at the output. Between the DC ripple and AC ripples, the overshoot determines the required C_{out} [7, p. 15]. The time taken for V_{out} to stabilize after releasing the load is given by

$$t_{overshoot} = \frac{L_{eq} I_{step}}{V_{out}} \quad (2.8)$$

where L_{eq} is the equivalent inductance during the transient, I_{step} is the maximum load step and V_{out} is the output voltage.

In order to calculate the required output capacitance during an overshoot $C_{overshoot}$ the charge during $t_{overshoot}$ needs to be calculated as

$$Q_{overshoot} = \frac{1}{2} \cdot t_{overshoot} I_{step} \quad (2.9)$$

where $t_{overshoot}$ is the time taken for V_{out} to stabilize after releasing the load and I_{step} is the maximum load step.

$C_{overshoot}$ is then given by

$$C_{overshoot} = \frac{Q_{overshoot}}{\Delta V_{out(AC)} + I_{step} \cdot DCLL} \quad (2.10)$$

where $Q_{overshoot}$ is the charge stored by the output capacitors during a load release, $\Delta V_{out(AC)}$ is the allowable transient output voltage ripple in V, I_{step} is the maximum load step and DCLL is the DC load line (which may be assumed zero).

2.1.4 Coupled inductors

The use of MPBCs solves the issue of applications demanding both a high current and a low current ripple, while also rendering an improved transient performance [1]. To reduce the current ripple of MPBCs using conventional inductors, or discrete inductors (DL), the DLs require a large L . This has a poor effect on the current slew rate during transients as $\frac{di}{dt}$ reduces meanwhile large voltage spikes are generated [8]. By replacing the DLs in each phase with coupled inductors (CL) this effect may be counteracted [8].

CLs are inductors which are coupled together magnetically: the inductors in the setup share a magnetic core by which the flux generated by the individual inductors interact with each other through a common flux path [9]. Due to this coupling, there exists a difference in inductance magnitude between the steady-state and transient states. To quantify this difference, we are considering a figure of merit based on [8].

The figure of merit (FOM) here denotes the ratio of the rate of change of current in the transient state to that in the steady state. This metric allows us to assess how an inductor's transient performance compares to its steady-state performance. A higher FOM indicates better transient performance, implying a faster rate of current change during transients. According to [6], achieving a higher FOM is possible by

Figure 2.3 depicts how CLs can be implemented in a MPBC using three phases. Inductors are connected individually to each phase of the buck converter and all the inductors are magnetically coupled to each other indicated by the dashed lines between the inductors in Figure 2.3.

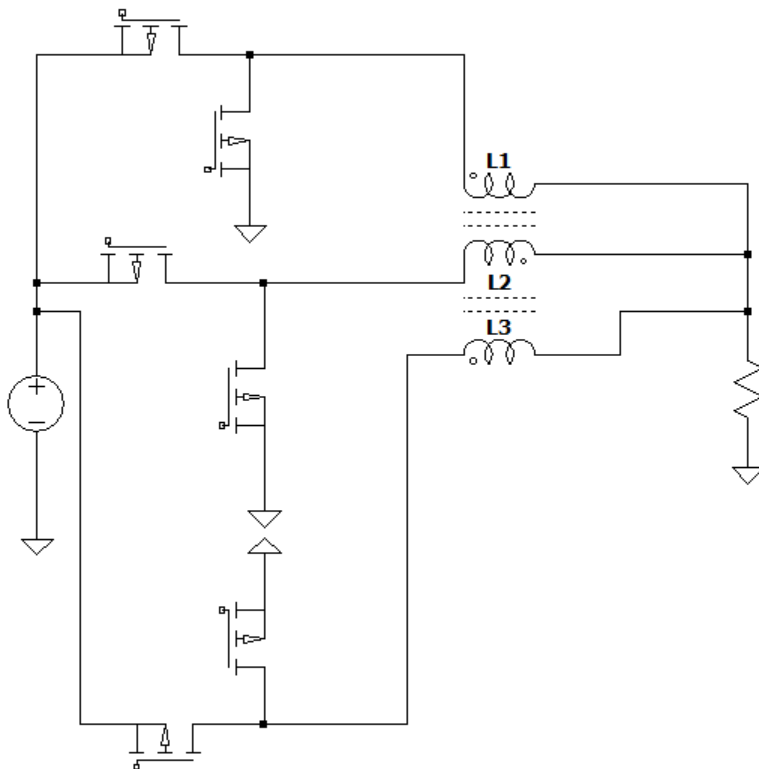


Figure 2.3: CLs in MPBC [4].

The inductor can be represented as a transformer, where L_m represents the magnetizing inductance per phase, and L_k denotes the leakage inductance per phase. In simulations, the inductors L_1 , L_m and L_{s1} , L_{s2} symbolize ideal transformer couplings, where the secondary sides of the transformers for each phase are connected in series to simulate magnetic coupling between the inductors (CLs). This configuration is designed for systems with more than two phases, ensuring proper orientation of magnetic coupling in coupled inductors (CLs). In this orientation, the current flowing through the conducting inductor is opposite in direction to the currents in other mutually coupled phases. Figure 2.4 illustrates these concepts for a two-phase CL configuration. In CL datasheets, L_m may also be referred to

as open-circuit inductance (OCL).

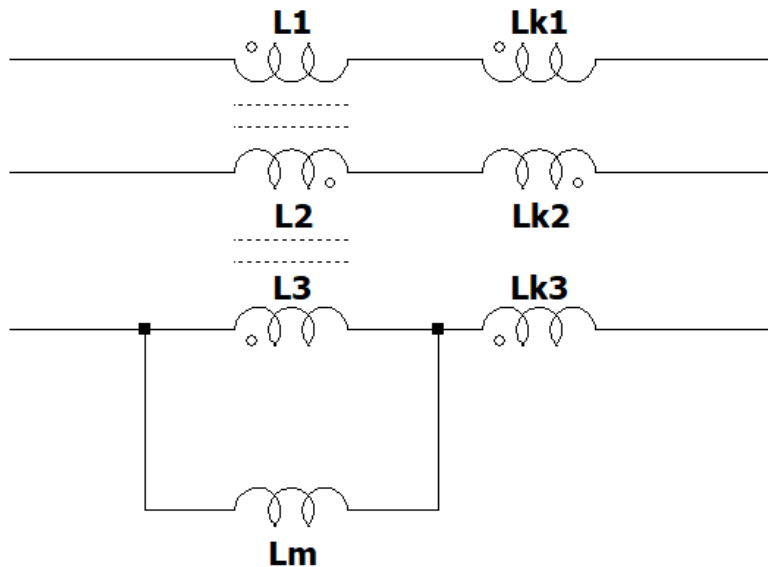


Figure 2.4: CLs as a transformer [4].

According to [6], achieving a higher FOM involves maximizing the L_m/L_k ratio. A higher L_m enhances flux linkage between phases, thereby improving transient performance. Additionally, the duty cycle also influences FOM performance. When the duty cycle approaches $\frac{1}{N_{ph}}$, where N_{ph} represents the number of phases, FOM improves [6].

2.1.4.1 Notch Coupled Inductor

The notch coupled inductor (NCL) is a modification of the CL. The main difference between the two is that the NCL has an increased ratio of L_m/L_k . One way in which this is achieved is to reduce the physical size of the leakage plate surrounding the inductor constituting for L_k . This leaves volume for which L_m can be increased. In this way the ratio of L_m/L_k can be increased [6, p. 634]. According to [6, p. 632] there are several benefits of using NCL over CL in an MPBC. One is that an improved ripple cancellation can be achieved which can either improve the transient performance or lower f_{sw} .

Moreover, the higher L_m/L_k ratio in NCL leads to a higher FOM, which improves ripple cancellation [10, p. 1]. This benefit can be leveraged to enhance transient response and reduce component size or to lower f_{sw} within the same footprint, thereby achieving higher overall efficiency. By removing the leakage plate, L_k reduces. The remaining volume can then be used to maximize L_m for a given I_{sat} . This approach for an NCL configuration is depicted in Figure 6(c) in [6, p. 635]. Alternative NCL structures are also feasible [6, p. 634].

2.1.5 Trans-inductor Voltage Regulator

The trans-inductor voltage regulator (TLVR) is a relatively novel technology first proposed in 2020. Its origin can be traced to 2007 [10] in which a setup with indirectly coupled inductors are used. The secondary windings are electrically linked between phases which effectively traps the AC-ripple current [11, p. 114]. This type of inductor is called a trans-

inductor (TL) [2, p. 2005]. An MPBC utilizing TLVR can be described as a modification of a conventional MPBC where the DLs have been switched out to TLs. A TL consists of magnetizing inductances on the primary side L_m and secondary side L_s with respective leakage inductances lumped as L_k . To form a TLVR, the secondary windings of the TLs are tied together, essentially series connecting the L_s of each TL [12, p. 377]. This series connection is terminated in a separate tuning inductor L_c which effectively tunes the ratio between L_m and L_k of the TLVR [2, p. 1]. The combination of N amount of TLs with secondary windings series connected and terminated by L_c forms a TLVR. A two phase representation of a TLVR can be seen in Figure 2.5.

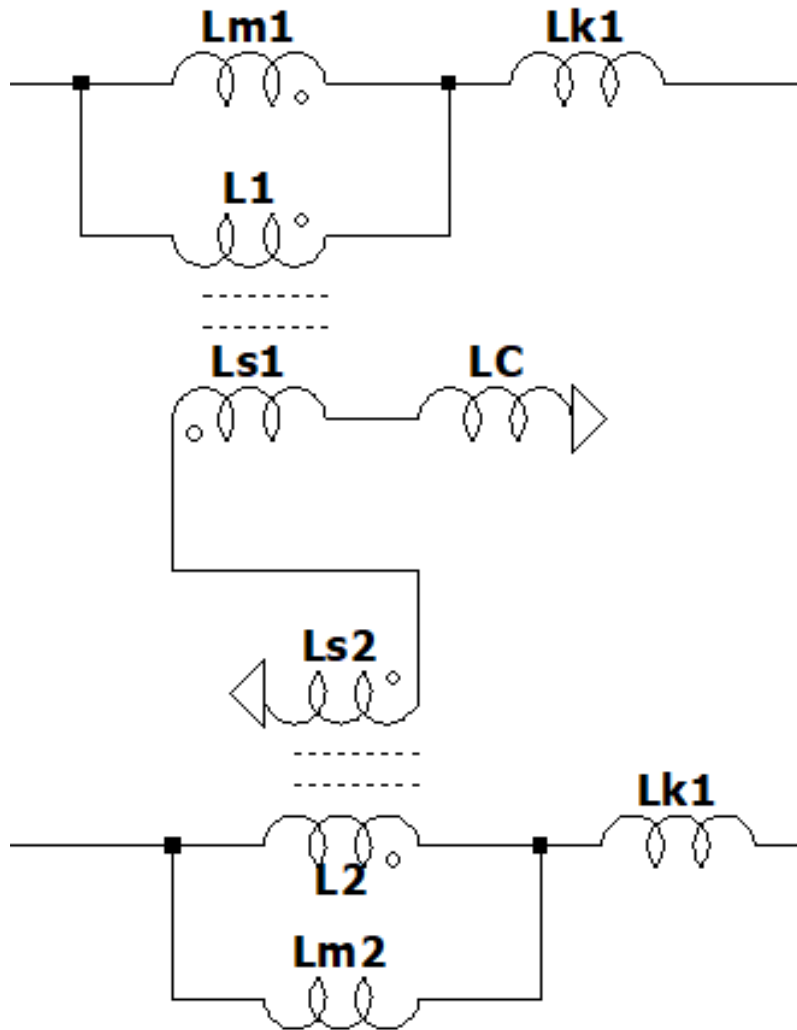


Figure 2.5: Simulation model of TLVR as a transformer [10].

As for the use of CLs in MPBCs, the TLVR's equivalent impedance per phase in steady-state $L_{eq,ph}$ can also be calculated. The coupling coefficient k comprises L_m and L_k . The primary distinction between TLVR and CL lies in their configurations: CLs feature magnetically coupled inductors, whereas TLVRs can be conceptualized as transformers arranged across different phases, with their secondary windings connected in series to couple primary inductors. Specifically, it is the secondary winding current that couples

the primary inductors within the phases of the TLVR. Another key difference is that in TLVR, L_m is included in the complete equivalent inductance. Therefore, when comparing to DL, the inductance value is divided between L_k and L_m [6].

2.2 Integrated Circuit

The IC used for testing is the LT8627SP from Analog Devices, Inc. (ADI). It is a buck converter operating with an input voltage range of 2.8 V to 18 V and has an operating frequency range of 300 kHz to 4 MHz. The LT8627SP supports a maximum continuous output current of 16 A and enables multiphase operation up to 12 phases [13, p. 1].

2.2.1 Operation

The switching frequency of the LT8627SP is set via the RT pin by connecting a resistor R_T between the RT pin and ground (GND). The signal from the RT pin is fed to an oscillator, which provides the turn-on signal for the control MOSFET each cycle. The current through the control MOSFET I_d is received from the power supply through the PV_{IN} pin. As I_d passes through the inductor, its current increases until it reaches a peak value set by the voltage on the V_C pin, determined by an internal error amplifier comparing the O_{UTS} and SET pin voltages. The output current from the inductor is measured and supplied to the O_{UTS} pin, where it applies a voltage. The SET pin acts as a reference voltage, set by connecting a resistor R_{SET} between the SET pin and GND. When the output of the internal error amplifier meets the voltage set by V_C, the control MOSFET turns off, and the sync MOSFET turns on. The inductor current falls, and for CCM operation, the cycle repeats as the next switching time period T_s (clock cycle) initiates [13, p. 13].

The LT8627SP operates in three modes: Forced Continuous Mode (FCM), Pulse-Skipping Mode (PSM), and Synchronization Mode (SM). FCM forces the IC to operate in CCM, avoiding Discontinuous Conduction Mode (DCM) and allowing negative current through the inductor at light loads or during large transients, making it suitable for loads requiring fast transient responses or with large load variations. PSM does not allow negative inductor current, leading to DCM operation during light loads. SM synchronizes the oscillator to an external frequency, which must have a square-wave characteristic, and may be provided by an external clock generator. In SM the IC operates with the characteristics of FCM [13, pp. 11, 17].

2.2.2 Pins

The LT8627SP has 16 unique pins, but not all are relevant for this thesis. The functions of key pins are summarized in Table 2.1. FCM can be achieved by tying the SYNC/MODE pin to the INTV_{CC} pin, leaving the INTV_{CC} pin floating, or connecting the SYNC/MODE pin to an external clock generator to operate in SM. For SM, the INTV_{CC} pin should be decoupled with a low ESR 1 μ F MLCC, and R_T should be adjusted to set the programmed f_{sw} 20% lower than the external f_{sw} .

The SV_{IN} pin supplies the internal circuitry, requiring a voltage exceeding 700 mV of the SET pin V_{SET} . SV_{IN} can be tied to PV_{IN}, which provides current to internal circuitry and control MOSFET, ensuring a soft start for the IC. SV_{IN} may also be tied to a separate voltage source bypassed through a 1 μ F capacitor which improves efficiency [13, pp. 11, 13].

The EN/UVLO pin enables switching when the voltage exceeds 1.32 V and causes shut-down below 400 mV, which can be used as a feature or tied to PV_{IN} if not needed. The SET pin sets the reference voltage for V_{out} , determined by R_{SET} , with C_{SET} improving noise performance and preventing overcharging which in turn may temporarily short the output to GND. C_{SET} should have a value of 1 μ F [13, pp. 24-25].

The LT8627SP can use a fast start-up logic which requires a resistive voltage divider to be connected between L and GND, where the midpoint of the resistive voltage divider is tied to PGFB pin. The PGFB voltage must be within 462.5 mV and 537.5 mV for proper function [13, p. 11]. Formulas and a table in the datasheet provide resistor values for the voltage divider [13, p. 25].

The V_C pin is a control pin that helps stabilize the voltage at the output. Adding a resistor and capacitor in series to the V_C pin improves the control capability of the overall IC and aids in faster stabilization of transients. In our case, the values of the resistor and capacitor were chosen through multiple trials in simulations to ensure that the loop bandwidth of all setups is similar for fair testing.

Table 2.1: Functions of pins of LT8627SP.

LT8627SP Pins	
Name	Description
SW	Output of switches to inductor.
GND	Ground connection.
PV_{IN}	Power V_{IN} . Provides current for internal circuitry and control MOSFET.
SV_{IN}	Signal V_{IN} . Provides current for internal circuitry and regulator.
EN/UVLO	Voltage on pin enables switching.
$INTV_{CC}$	Internal 3.4V Regulator Bypass Pin. Internal power drivers and control circuits are powered from this voltage.
PHMODE	Phase shift of clock signal of CLKOUT pin.
SET	Reference voltage for internal error amplifier.
V_C	Voltage on pin controls peak switch current.
OUTS	Measures output voltage to adjust V_C .
PGFB	Power Good Feedback.
RT	Sets switching frequency.
PG	Power Good.
SYNC/MODE	Operation mode (CCM/DCM/FCM).
CLKOUT	Output clock signal for multiphase operation. Phase determined by the state of PHMODE pin.
BST	Drive voltage for control MOSFET.

2.2.3 Multiphase operation

Multiphase operation can be achieved by using multiple LT8627SP ICs in parallel to supply a common load. In this setup, the V_C pins of each IC should be tied together, sharing a single R_C and C_C , and the OUTS pins should also be connected together [13, pp. 25-26].

To enable multiphase operation the PHMODE pin is used to determine the phase shift between the phases. For two-phase operation, the PHMODE pin is connected to GND for a 180° phase shift. For three-phase operation, the PHMODE pin is left floating for a 120° phase shift. For four-phase operation, the PHMODE pin is connected to $INTV_{CC}$ or an external supply for a 90° phase shift. For more than five phases, up to a maximum of 12, the PHMODE pin should be connected to different voltage levels [13, pp. 10, 26]. Table 2.2 summarizes the connection types for the PHMODE pin.

Table 2.2: Connection types of PHMODE pin for multiphase configuration.

Phases	Phase shift	PHMODE pin connection
2	180°	GND.
3	120°	Floating.
4	90°	$INTV_{CC}$ pin / external supply.
5 - 12	$72^\circ - 30^\circ$	Differing voltages.

2.2.4 System stability

System stability for the LT8627SP is influenced by several factors. One factor is the value of the output capacitors; if too low, they may cause loop instability [13, p. 20]. Parasitics such as ESR and ESL may also affect the internal error amplifier by distorting the signal on the OUTS pin, which can be decoupled with a 150 pF capacitor. Components tied between the V_C pin and GND, specifically a resistor R_C and capacitor C_C , are part of the control loop which directly influences system stability. This loop consists of a modulator, the MOSFETs and inductor, and C_C . The modulator, MOSFETs and inductor generates a current determined by the voltage on the V_C pin. The output capacitors integrates this current and C_C integrates the output current of the internal error amplifier to which the output current is fed to. This results in two poles in the control loop, with a zero being provided by R_C [13, p. 22].

2.3 Simulation software

The primary simulation software used is LTSpice [14]. This tool allows simulation of circuits and measurement of various parameters, such as output voltage, load step response, total harmonic distortion (THD), and loop stability. IC manufacturers may provide simulation files for their ICs in LTSpice. Simulation and measurement results may differ due to non-ideal behaviors, such as the DC-bias characteristic of multi-layer ceramic capacitors (MLCCs), which reduces their capacitance values under certain voltages and temperatures.

3

Case setup

This section will detail the necessary information for setting up simulations and test configurations. Simulation details will include the selection of IC parameter values, the process of constructing IC and inductor models, and steps taken to develop simulation models. Test setup specifics will cover aspects such as inductor configuration, board modifications, simulation setup, and parameters considered during testing.

3.1 Testboard

The testboard provided by ADI is a six-phase MPBC using the LT8627SP as the buck-converter IC for each phase. Three test boards in total were supplied by ADI as backup but also for convenience as to mount different inductor types on the boards. The only parameter aimed to be changed between different measurements are the inductors themselves. Thus the intention is for the remainder of the board to remain unchanged as for standardisation between tests unless otherwise specified. One of the testboards without inductors mounted can be seen in Figure 3.2.

As described in section 2.2.3 the PHMODE pin should be connected to differing voltage levels to realize a six-phase operation. However, for the board this is not the case. The PHMODE pin of each phase is connected to GND. As seen in Table 2.2 this means a 180° phase shift between the ICs. Despite appearing so, this does not mean the MPBC is operating as a two-phase setup. There is a six-phase operation consisting of three parallel two-phase operations. Due to the layout this means that the following phase configurations are operating with a phase shift of 180° to each other: PH1 and PH4, PH2 and PH5, PH3 and PH6; where PH1 through PH6 correspond to the first through the sixth phase. Despite these phase pairs switching with a D of 0.5 with respect to each other they are still operating within a common T_s . Hence each phase's maximum on-time results in (2.3) remaining true with D being less than or equal to $\frac{1}{6}$. The phase configuration can be seen in the SYNC voltages of each phase as illustrated in Figure 3.1 where the colored text represent the two-phase pairs.

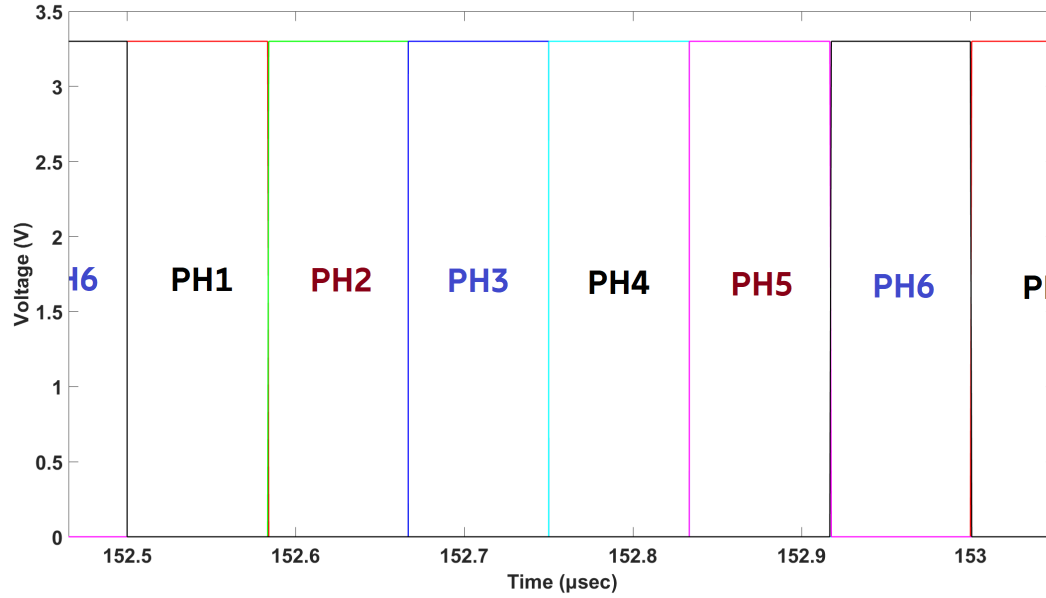


Figure 3.1: Simulated SYNC voltage distribution.

The SYNC voltages in turn are driven by an external clock-circuit consisting of the IC LTC6909. It is an oscillator capable of providing up to eight synchronized outputs and thus able to provide the SYNC signals for the six-phase setup on board. It operates with a supply voltage between 2.7 V and 5.5 V. The output frequency is set by a resistor connected to the SET pin of the LTC6909 $R_{SET,LTC}$ and its value can be calculated according to [15, p. 1] with

$$f_{OUT} = \frac{20\text{MHz} \cdot 10\text{k}}{R_{SET,LTC} \cdot N} \quad (3.1)$$

where f_{OUT} is the output frequency of the LTC6909, $R_{SET,LTC}$ is the SET resistor for LTC6909, and N is the number of outputs being driven by the IC. As a 16.5 k Ω resistor is tied to the SET pin of the LTC6909 on the testboard (3.1) gives f_{OUT} a value of 2.02 MHz with this resistor size. Considering the resistor's tolerance of $\pm 1\%$ this gives f_{OUT} a range between 2.00 MHz and 2.04 MHz.

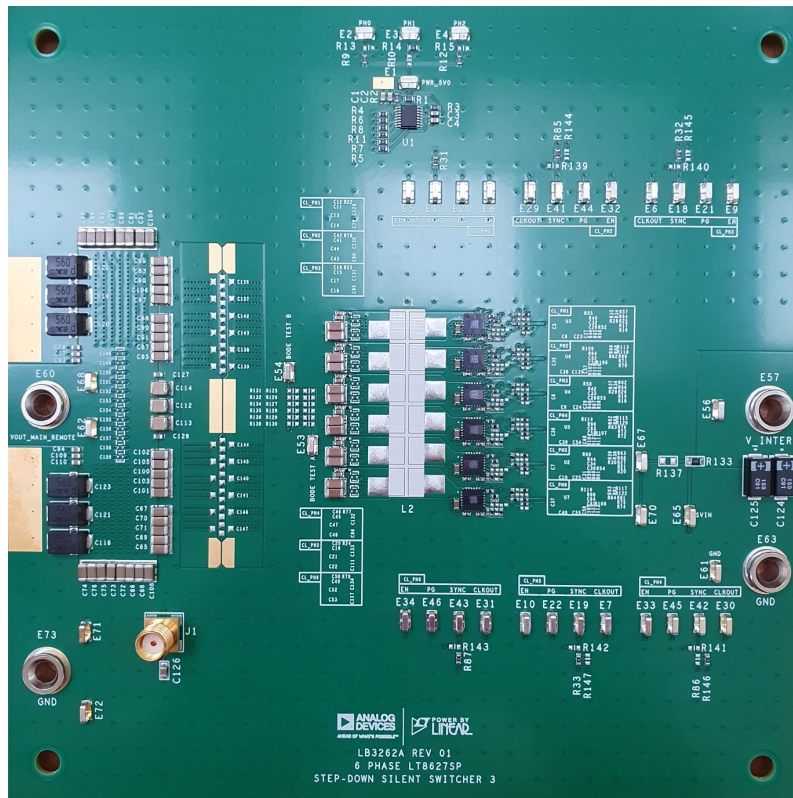


Figure 3.2: Testboard provided by ADI.

3.1.1 Modifications

Despite attempting to mimic the testboards, some adjustments are made in order to ease performing simulations. For multiphase operation, the V_C pins of all phases should be tied together and share a single R_C and C_C as mentioned in section 2.2.3. In the schematic of the testboard this is done, but in the implementation on the board R_C and C_C are only tied to PH1. Therefore R_C and C_C are tied to PH1 as well. According to the schematic, the values for R_C and C_C on the board are $348\ \Omega$ and $1000\ \text{pF}$ respectively with a capacitor sized $10\ \text{pF}$ placed in parallel. In reality, these are not placed, since the schematic was for a different set of inductors. For our application we had to find a suitable R_C and C_C which we got after some trial and error in the simulations. After performing stability measurements with different values for R_C and C_C , their values were chosen to $10\ \Omega$ and $10\ 000\ \text{pF}$ respectively.

3.2 Simulation setup

For simulations the software LTspice will be used. Different configurations of MPBCs will be constructed within the software, meaning different inductor topologies will be integrated with the MPBCs being: DL, CL and TLVR. The simulations were carried out with the IC LT8627SP. The simulations were intended to be comparable between each other and to the testboards. This means constructing simulation models which resemble the testboards as closely as possible with the only difference between simulations being the inductor used; yet the equivalent inductance should remain the same. The major parameters which remain the same such as V_{in} and f_{sw} are summarized in Table 3.1.

Table 3.1: Main parameters to be used in simulations.

Parameter	Value	Unit	Description
V_{in}	12	V	Input voltage.
V_{out}	1	V	Output voltage.
f_{sw}	2	MHz	Switching frequency.
N	6		Phase count.
I_{step}	60	A	Maximum load step.
$\frac{di}{dt}$	120	$A \mu s^{-1}$	Transient step size.

3.2.1 Investigation parameters

The simulation tests to be performed contain a number of variables. One variable is loop bandwidth and stability of the configuration. Another is step-load response, meaning how the system responds to sharp transients. This entails a number of phenomena: how ΔV_{out} is affected and if it remains within acceptable levels, whether the switch voltage between the output of the MOSFETs and input of the inductors overlaps between phases. Furthermore, power supply rejection ratio (PSRR) will be investigated. This means that if noise is present from the Power source, how much voltage variation would be present at the output. Additionally different V_{in}/V_{out} ratios will be investigated to see how the above mentioned variables behave in response to a change in this ratio. A final variable is the efficiency where different V_{in}/V_{out} ratios will be compared between different inductor topologies for MPBCs where an efficiency comparison will be done by comparing the power received to the circuit and power supplied to the load.

3.2.2 Differences between simulations and testboard

The value of C_{SET} . When running simulations with the value of $1 \mu F$ being mounted on board the simulations significantly slowed down. Namely, a long simulation time was required for V_{out} to reach its intended level. Therefore, for simulations, C_{SET} is given a value of 10 pF for a fast rise of V_{SET} .

Other resistors and capacitors which are not described further in this section are ideal. These are for instance the R_T resistor and $INTV_{CC}$ capacitor. Further, there are ideal voltage sources placed in the simulation models with 0 V and no series resistance. These are used for current measurement. The primary voltage source supplying V_{IN} is also an ideal voltage source.

3.2.3 Inductors

Provided by Ericsson is a component library including custom inductor models which exhibit non-ideal characteristics and can be implemented into LTspice. While unclear exactly what type of non-ideal characteristics that are present for the components, they may still be considered as more realistic models than ideal parameters. However, no inductors are chosen from the component library. For DL the reason is that selecting inductors from the component library results in large, irregular spikes in the output voltage which are deemed non-realistic. The inductors chosen are however modeled to an extent after the DL used on board. They have an ESR of $0.22 \text{ m}\Omega$ which is close to its nominal

value of $0.29 \text{ m}\Omega$ and the DLs have a value of 100 nH .

In reference to section 2.1.2 equations (2.6) and (2.5) can be used to determine whether a value of 100 nH is appropriate. For (2.5) V_{out} and f_{sw} are simply applied from Table 3.1. D is calculated according to (2.1) as $\frac{1}{12}$ with values of V_{out} and V_{in} in Table 3.1. I_{PP} is taken as 25% of maximum current per phase in accordance with [7, pp. 10-11]. Applying (2.6) using I_{max} of 90 A from the load profile in Figure 4.3 gives I_{PP} a value of 3.75 A , which applied to (2.5) gives L a value of 122 nH . This value is 22% larger than the chosen value for DL, hence the chosen value for DL might not be optimal, due to the size constraint and availability, 100 nH was chosen.

The models for CL, NCL, and TLVR are not part of the standard simulation library. Therefore, equivalent models were created based on the guidelines provided in [10], which detail various inductor models and their differences. A critical aspect when modeling inductors in simulations is ensuring that all inductors are oriented in the same direction [16].

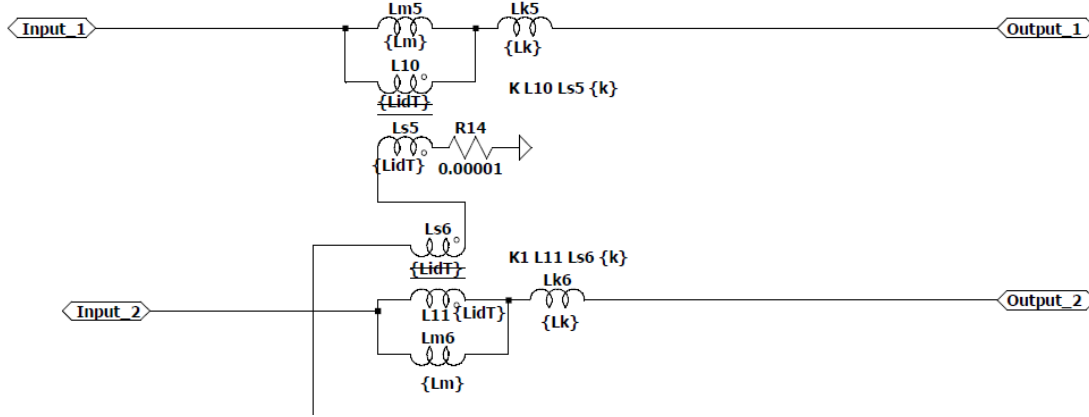


Figure 3.3: Two Phase CL.

Figure 3.3 illustrates two phases of the six-phase model made in simulation. The entire model is found in Appendix A in Figure A.6. In Figure 3.3, L_m is 300 nH , and L_k is 100 nH , derived from the datasheet of the CL1208-6-100TR-R inductor used in the experimental setup, where the open circuit inductance is 400 nH and the short circuit inductance is 100 nH . Considering these, L_m can be calculated as

$$L_m = \text{opencircuitinductance} - \text{shortcircuitinductance} = 300 \text{ nH} \quad (3.2)$$

The ESR is set at $0.1 \text{ m}\Omega$ per phase, distributed uniformly across all inductors, resulting in an ESR per phase of $0.1 \text{ m}\Omega$. The coupling factor k for CL typically reaches 0.95 [17]. In contrast, NCL achieves a higher L_m/L_k ratio compared to CL [6], maintaining L_k at 100 nH while increasing L_m to 2000 nH .

For TLVR, the overall inductance value is the sum of L_k and L_m , where the 100 nH total is divided between L_m (70 nH) and L_k (30 nH). However, the structure of both NCL and TLVR remains the same as CL for simulations [10].

3.2.4 Output Capacitance

Another deviation from the testboards are the output capacitors used in simulation. For one, they are lumped together on the output between the MPBC and the load. For simulation purposes this should have little to no impact as opposed to placing the capacitors in exact accordance with the schematic as V_{out} . For the other, custom capacitor models are used from Ericsson’s component library. The capacitors chosen from this library are intended to be as close as possible to what is mounted on the board. The capacitor values and tolerances have been prioritized, where other characteristics such as package size and max temperature are less prioritized. One electrolytic capacitor and six different MLCCs are chosen in total. These are listed in Table 3.2 with a total nominal capacitance value of 4430.7 μF consisting of 75 capacitors. In Table 3.2 the capacitor EEFHX0D561R4 is an electrolytic capacitor while the remainder are MLCCs.

Table 3.2: Chosen output capacitors for simulation.

Capacitor	Value [μF]	Amount	Total [μF]
EEFSX0D561E4	560	6	3900
GRM32ER71E226ME15	22	12	264
GRM21BR60J226ME39	22	36	792
GRM21BR71H105KA12	1	8	8
GRM033C80J105ME05	1	6	6
GRM1555R71H104KE14	0.1	6	0.6
GRM188R71H104KA93	0.1	1	0.1

In reference to section 2.1.3 the steps in calculating $C_{overshoot}$ can be followed to determine whether a C_{out} of 4430.7 μF is sufficient or not. Applying (2.8) with L_{eq} of 20.33 nH for DL, V_{out} of 1 V and I_{step} of 60 A according to Table 3.1 gives $t_{overshoot}$ a value of 1.22 μs . With this value, (2.9) gives $Q_{overshoot}$ a value of 36.6 μC . Applying (2.10) and assuming a strict value for $\Delta V_{out(AC)}$ of $\pm 2\%$ gives $C_{overshoot}$ a value of 1830 μF . The different capacitance values are summarized in Table 3.2. The chosen value for C_{out} of 4430.7 μF is 242 % greater than the calculated $C_{overshoot}$. Hence a C_{out} of 4430.7 μF should suffice to keep $\Delta V_{out(AC)}$ within $\pm 2\%$. Furthermore, it should not cause loop instability as described in section 2.2.4.

3.3 Lab setup

This section aims to describe the equipment used for measuring different variables of interest, presenting these variables, describe the test board.

3.3.1 Equipment

To perform measurements on the board different types of equipment were required. The equipment used is summarized in Table 3.3.

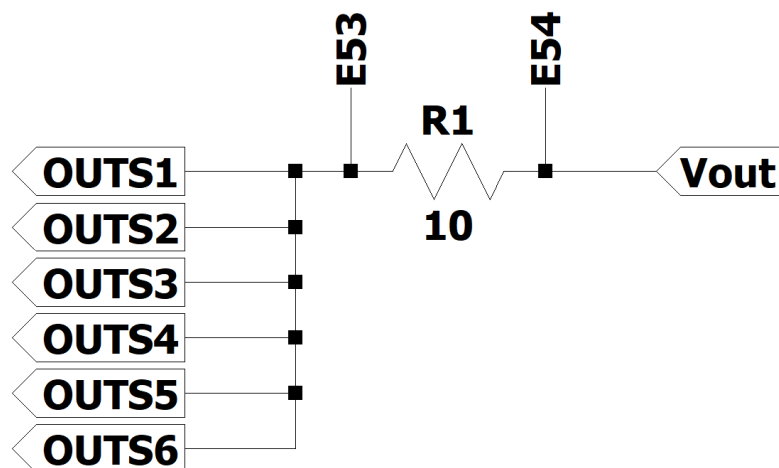
Table 3.3: Equipment used for measurements.

Part	Name	Manufacturer
Power supply	SM70-45D	Delta Elektronika
Clock circuit power supply	SM70-AR-24	Delta Elektronika
Electronic load	Chroma 6312A	Chroma
Oscilloscope	HD4096	Teledyne Lecroy
Stability analyzer	Bode 100	OMICRON Lab
Injection Transformer	B-WIT 100	OMICRON Lab
Multimeter	TX3	Tektronix

3.3.2 Adjustments

Some adjustments had to be made to the board in order to perform certain measurements. One adjustment that was made was to let the OUTS pins of each IC share a common resistor. Prior to this adjustment each IC had a $100\ \Omega$ resistor tied between its OUTS pin and the common V_{out} . After adjustment, the $100\ \Omega$ resistors were removed from each phase and resistors were mounted in parallel between the OUTS pin of each phase and a common point connected to a Bode test point. To illustrate the change

With reference to Figure 3.5, R125 through R130 were connected with steel wires, i.e. between the pads in row 3 and row 4. Essentially this connects all OUTS with the measurement point labeled BODE TEST B. This however assumes there is a connection between the pads in row 1 and row 2. A single resistor was mounted between two pads in row 2 and row 2 sized $10\ \Omega$.

**Figure 3.4:** Disturbance injection setup

The figure 3.4 shows the connection made where the E53 and E54 are the injection points which is across the $10\ \Omega$ resistor. The disturbance is given by an instrument namely Bode 100 which can inject the disturbance of a frequency sweep across the resistor and receive the response of the setup giving a bode plot through the UI when connected to

3. Case setup

the computer.

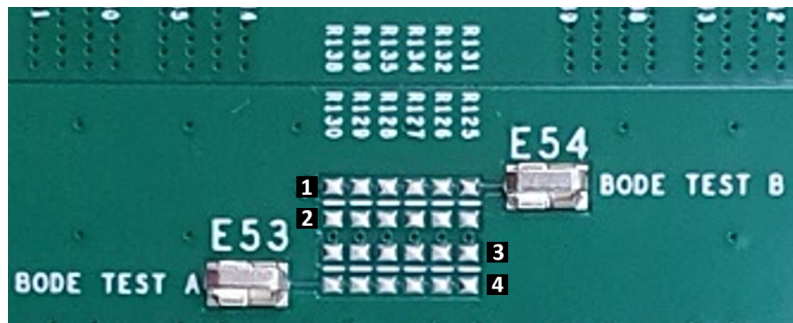


Figure 3.5: Part of the board dedicated to Bode measurement.

The picture in figure 3.5 shows the place at which the above-mentioned connection was made.

4

Implementation

4.1 LT8627SP

This section will cover the implementation of the LT8627SP and its use with DL, NCL, CL and TLVR as a six-phase configuration.

4.1.1 General simulation model

The general simulation model is based on the board as already described in section 3.2. The configuration can be seen in Figure 4.1 where Figure 4.1a depicts the first phase and Figure 4.1b depicts the third phase. The remaining phases are identical to phase 3. The load is shared between the converters where the point of connection lies past each phase's power inductor as seen by the A connection. Between the load and A lies the lumped output capacitors. The simulation model can be seen in its entirety in Appendix A.

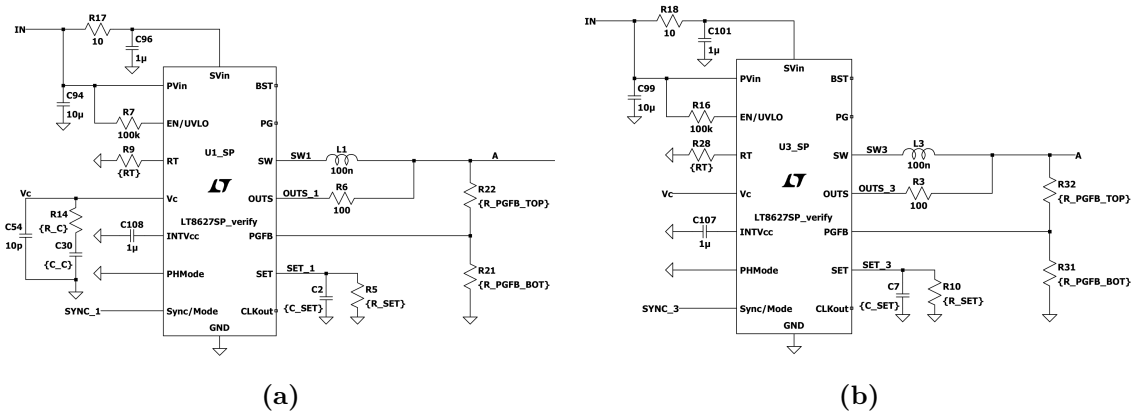


Figure 4.1: General six-phase configuration of LT8627SP showing (a) the first phase and (b) third phase.

4.1.2 Stability analysis

For the stability analysis, a frequency response analyzer (FRA) was employed to assess the circuit's frequency response. The FRA was inserted in place of the resistor connected to the OUTS1 of the first phase, with the OUTS pins of all other buck converters connected, placing the FRA in series between the OUTS pins of all buck converters and the output voltage. The FRA operates by introducing a disturbance into the circuit—a frequency

sweep across the specified range—and plots a Bode plot by analyzing the ratio of V_{in} to V_{out} . The parameters for the FRA analysis are shown in Figure 4.2.

Figure 4.2: FRA parameters.

The disturbance range was set from 10 kHz to 1 MHz to test a wide frequency spectrum and observe the gain at each disturbance frequency. Additionally, the phase change at each frequency was monitored, as it impacts stability. The analysis commenced at 80 μ s to allow the circuit to stabilize, and each frequency disturbance was analyzed for 10 μ s. The parameters pp0 and pp1 refer to the amplitude of the disturbance voltage, typically prescribed to be less than 1% of the output voltage. Hence, a disturbance voltage of 0.005 V was used, considering the output voltage is 1 V. This will be the first test done to see what values of resistor and capacitor is needed at the V_C to make the circuit stable for the operation with the respective inductor setup.

4.1.3 Efficiency

Efficiency simulations were conducted under two scenarios to allow for comprehensive comparison. In the first scenario, a load profile of 19.92 A was used, and the circuit's

efficiency was tested with a voltage sweep. The voltage was incrementally adjusted, allowing sufficient time for parameter stabilization, and the RMS values of input voltage, input current, output voltage, and output current were recorded to calculate efficiency. Efficiency readings at various points were plotted for analysis.

In the second scenario, a constant input voltage of 12V was applied, followed by a current sweep. The load demanded each current value for 100 μs to ensure steady-state conditions before taking the necessary readings.

4.1.4 Step load response

The step load response test utilized the load profile depicted in Figure 4.3. An input voltage of 12V was applied, and the response was monitored in terms of output voltage ripple and rate of change of current. The load profile involved a load step from 30 A to a constant 90 A, followed by a load release back to a constant 30 A. This profile simulated four states for the multi-phase buck converters (MPBCs): low-load steady-state, transient load step, high-load steady-state, and transient load release. The transient steps occurred over 500 ns, yielding a $\frac{di}{dt}$ of 120 A μs^{-1} . The steady-state conditions were maintained long enough for oscillations to stabilize, with low-load steady-states simulated for 50 μs and high-load steady-state for 99 μs . The total simulation time was 350 μs , with data collection commencing at 150 μs to ensure stability.

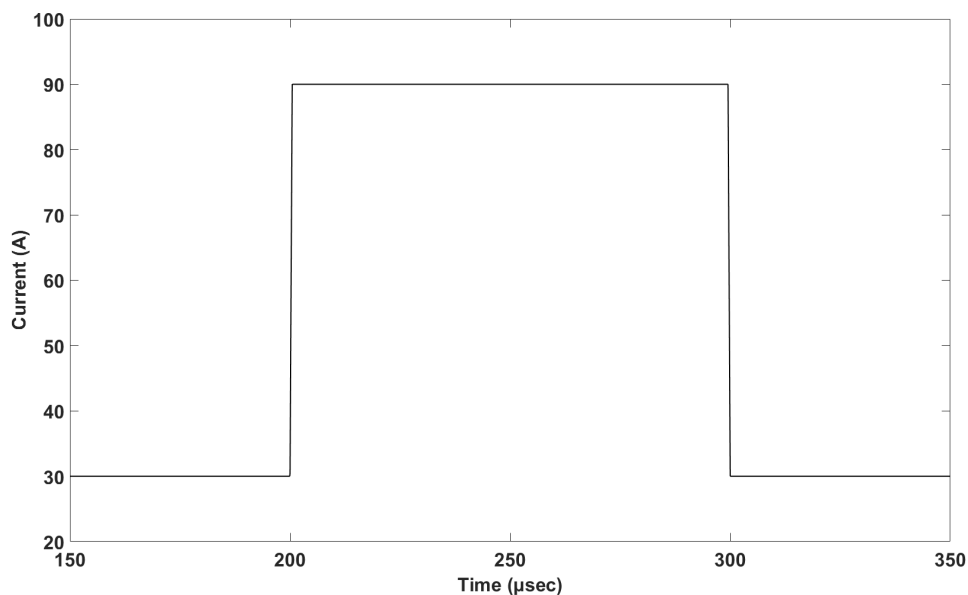


Figure 4.3: Simulation load profile.

4.1.5 Power system rejection

To evaluate the effect of input power variations on different inductor setups, an FRA was used in series with the input supply. The FRA generated a sinusoidal disturbance through a frequency sweep, allowing the observation of how this disturbance impacted the output. The FRA parameters are shown in Figure 4.4

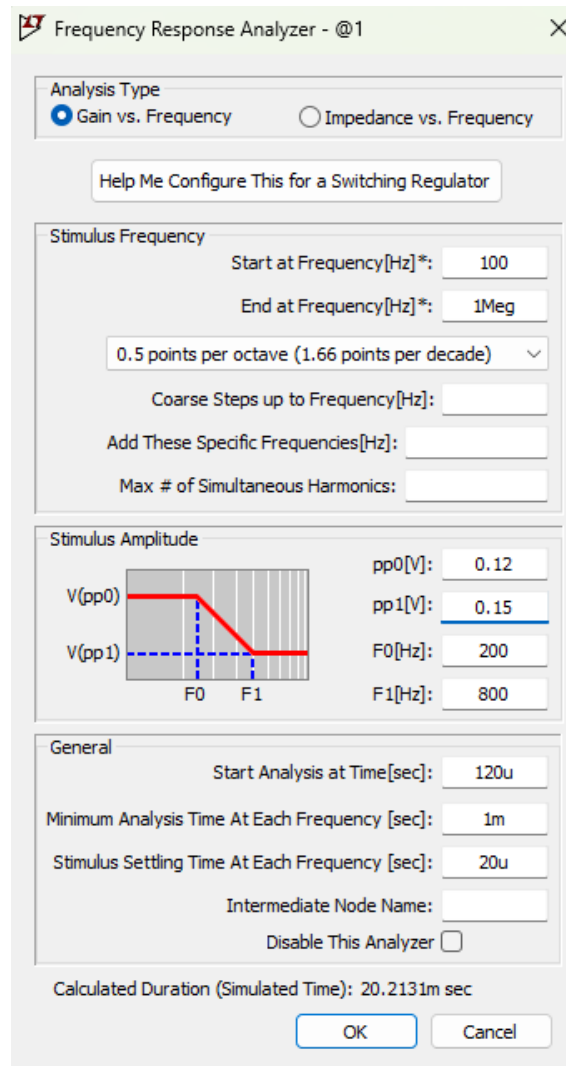


Figure 4.4: FRA of PSRR parameters

The frequency sweep ranged from 100 Hz to 1 MHz, with a disturbance amplitude of 0.12 V. Each frequency was analyzed for 1 ms to ensure comprehensive evaluation.

4.2 Building & testing physical model

This section details the implementation of the physical test board.

4.2.1 Stability analysis

Stability measurements were performed with the modification described in section 3.3.2. A Bode 100 was connected to an injection transformer supplying a disturbance signal to the board, with the receiver connected to the Bode 100 to analyze the output voltage from the converters. A frequency sweep from 10 kHz to 3 MHz was applied with a source level of -19 dBm. A 20 dB attenuator was used due to the sensitivity of the buck converter, and an internal attenuation of 10 dB was configured in the Bode 100 UI. The receiver's bandwidth was set to 100 Hz to obtain a noise-free reading.

4.2.2 Efficiency

Efficiency tests were conducted under two scenarios:

1. Voltage sweep with a constant 20 A load.
2. Current sweep with a constant 6 V input voltage.

Voltage and current were varied, and at each variation, the RMS values of input voltage, input current, output voltage, and output current were recorded to calculate and plot the efficiency curve.

4.2.3 Voltage ripple

Voltage ripple measurements were taken under various conditions to observe the ripple variations with different voltage and current settings. An oscilloscope was used to measure the ripples for different input voltages and currents, comparing the variations between CL and DL configurations.

5

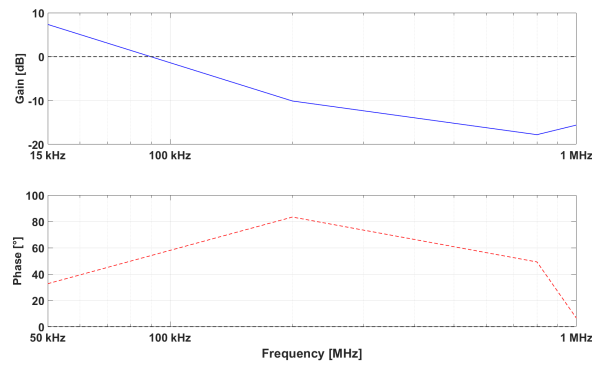
Results

This section presents and discusses the results from both simulations and laboratory testing. Initially, simulation results are showcased, including tests performed for DL, NCL, TLVR and CL. Subsequently, results from the laboratory experiments involving DL and NCL are presented.

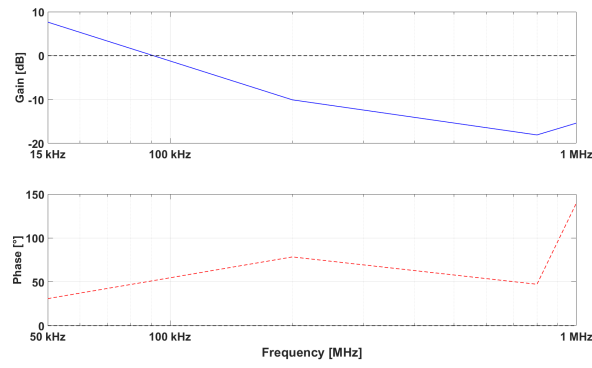
5.1 Simulations

5.1.1 Stability Response

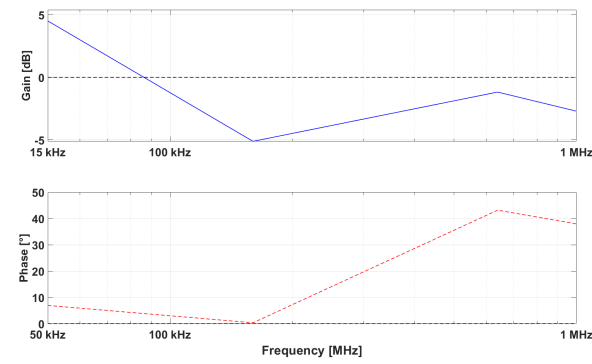
The first test done was the stability response of the circuit with different configurations of the inductors. For the DL and CL configuration the value of R_C and C_C was chosen as $10\ \Omega$ and $10\ \text{nF}$ respectively, With that the loop bandwidth for CL is $90.9\ \text{kHz}$ and the phase margin for CL is 51.4° . For DL the loop bandwidth is $89.7\ \text{kHz}$ and the phase margin is 53.40° . For TLVR we had to choose different values of R_C and C_C . The values of $50\ \Omega$ and $14\ \text{nF}$ were chosen where we got the loop bandwidth of $76.1\ \text{kHz}$ and the phase margin of 58.2° . And lastly for NCL the values of $0.1\ \Omega$ and $2\ \text{nF}$ were chosen for R_C and C_C where we got the loop bandwidth of $86.2\ \text{kHz}$ and the phase margin of 3.9° . Figure 5.1 shows the bode plots we obtained in the simulations of all four configurations.



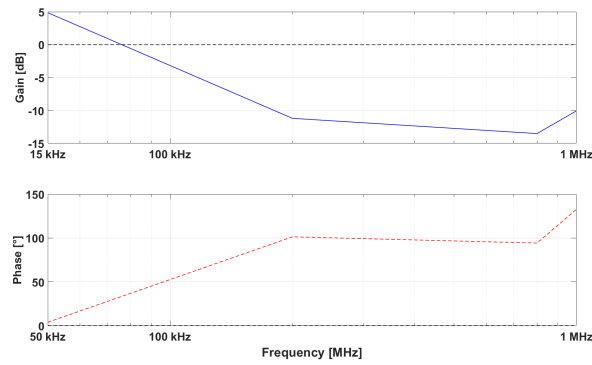
(a) DL



(b) CL



(c) NCL



(d) TLVR

Figure 5.1: Bode plots from FRA Analyser

5.1.2 Step Response

Figure 5.2 illustrates the phase inductor currents during a steady-state load of 30 A. DL and CL exhibit similar characteristics; however, the current ripple through CL is significantly lower than that through DL. Specifically, the current ripple in CL is approximately 1.2 A, whereas for DL, it is around 4.8 A. This indicates that the current ripple in DL is 400 % higher than in CL. This discrepancy is expected because CLs are magnetically coupled, allowing for a more uniform distribution of current ripple, unlike DLs. This trend is also evident in NCL, where the current ripple is about 0.6 A for the inductor in PH4 (I_{L4} in Figure 5.2c). The current ripple in NCL is 50 % lower than in CL and only 12.5 % of that in DL, highlighting the significant impact of higher magnetizing inductance on reducing output current ripple. Additionally, the current ripples in NCL occur at a higher frequency. In any given phase, roughly five cycles of inductor charge and discharge occur for NCL compared to DL, CL, or TLVR. This higher frequency may reduce the requirement for output capacitance but could introduce higher-order harmonics. For TLVR, the magnetic coupling influences each phase's current such that when one phase's current decreases and another's increases, a small increase in the current of the falling phase is observed. However, the overall current ripple is around 5.6 A for any phase, similar to DL due to the design of TLVR, where the total inductance is split between magnetizing and leakage inductance, unlike CL and NCL.

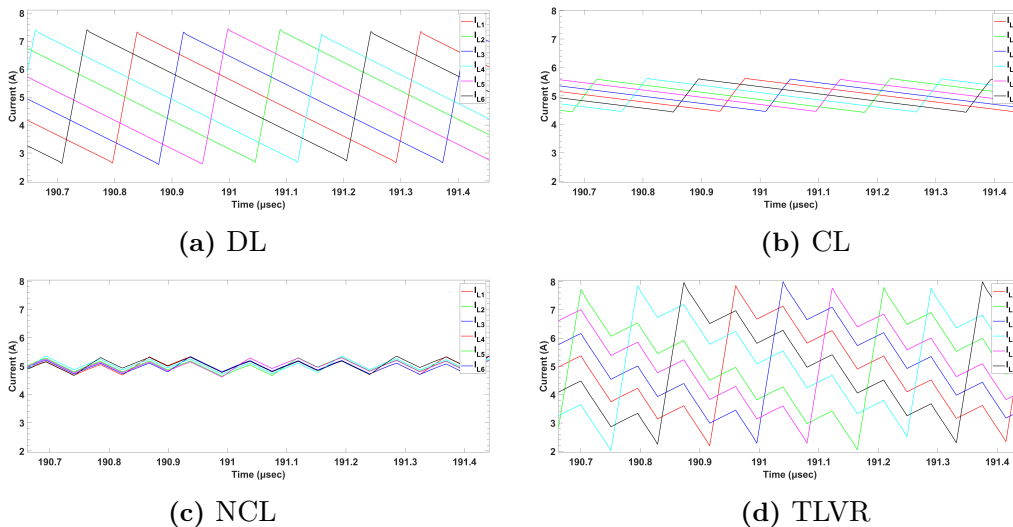


Figure 5.2: Phase inductor currents during 30A load.

Figure 5.3 shows the phase inductor currents during a steady-state load of 90 A. The analysis is similar to that of Figure 5.2, with the approximate current ripple being 5 A for DL, 1.2 A for CL, 0.7 A for NCL, and 6 A for TLVR. A noteworthy observation at the higher load of 90 A is the presence of distortions across all inductor topologies. These distortions are most apparent in CL, where dips and overshoots are seen at the respective bottom and top peaks of the current. The most severe distortion is observed in NCL (Figure 5.3c), where the inductor current waveforms show variations in the magnitude of current ripple, with rounded peaks. There seems to be no consistent pattern to these distortions.

Additionally, as seen in Figures 5.2c and 5.3c, there is almost no phase difference between the currents of each phase. This is attributable to the high L_m in NCL, which ensures

5. Results

even current distribution between phases. The high L_m results in significant flux linkage between the phases, contributing to the observed even current distribution.

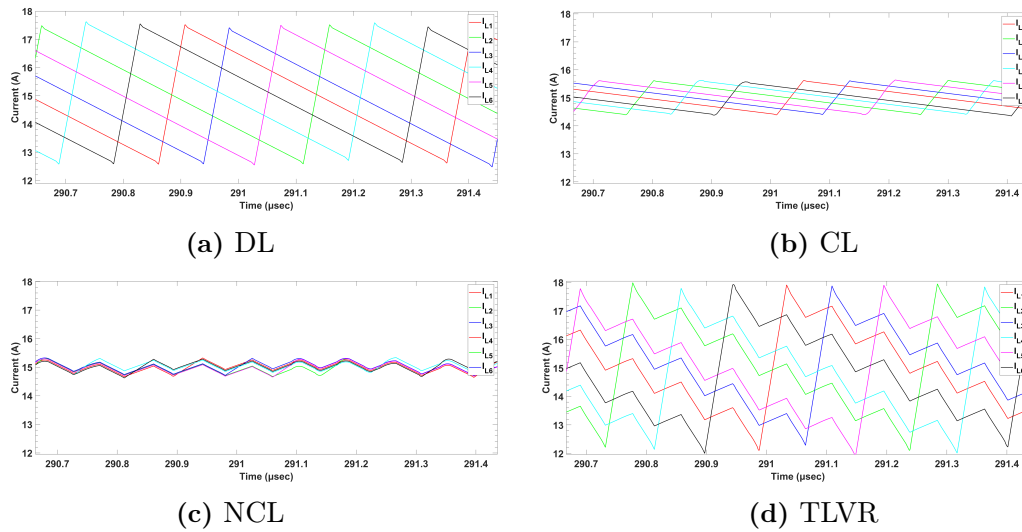


Figure 5.3: Phase inductor currents during 90A load.

Figure 5.4 displays the load profile and combined inductor currents. The figure also highlights the upper and lower margins needed to calculate the current slew rates of the load step and load release. The lowest current overshoot occurs in CL with 114.0 A, confirming its previously noted lowest current ripple in Figures 5.2 and 5.3. However, CL exhibits the worst current undershoot, reaching -46.9 A, while other inductor topologies remain above 0 A. Despite this, CL seems to stabilize faster and with less ringing than the other inductors. The waveforms of DL and NCL are similar in both ripple and overshoot/undershoot characteristics, with NCL showing slightly smaller undershoot. It is noted that the overshoot and undershoot are influenced by the high capacitance on the output side, which can be controlled by adjusting the capacitors.

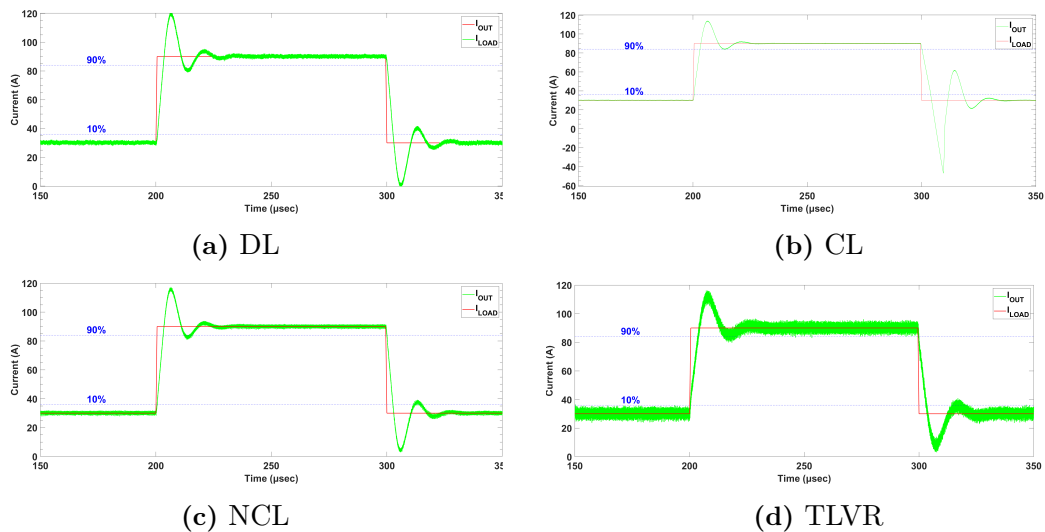


Figure 5.4: Load profile and combined inductor currents.

Figure 5.5 provides a closer view of the load profile and combined inductor currents during the load step. Marked in each subfigure are the current values and times at which the combined inductor currents cross the margins. By considering the 10% and 90% thresholds, $\frac{di}{dt}$ during the load step can be calculated with

$$\frac{di}{dt} = \frac{i_{90} - i_{10}}{t_{90} - t_{10}} \quad (5.1)$$

where $\frac{di}{dt}$ is the current slew rate through the inductor, i_{90} is the current value at 90% of the final value, i_{10} is the current value at 10% of the final value, t_{90} is the time at 90% of the final value, and t_{10} is the time at 10% of the final value. These values, taken from the subfigures in Figure 5.5 and applied to equation (5.1), yield the $\frac{di}{dt}$ during the load step for each inductor topology, presented in Table 5.1. The fastest response is observed in DL at $19.05 \text{ A } \mu\text{s}^{-1}$ while the slowest is in TLVR at $15.24 \text{ A } \mu\text{s}^{-1}$.

Table 5.1: Calculated $\frac{di}{dt}$ during load step.

Inductor	$\frac{di}{dt}$ [$\text{A } \mu\text{s}^{-1}$]
DL	19.05
CL	18.92
NCL	18.56
TLVR	15.24

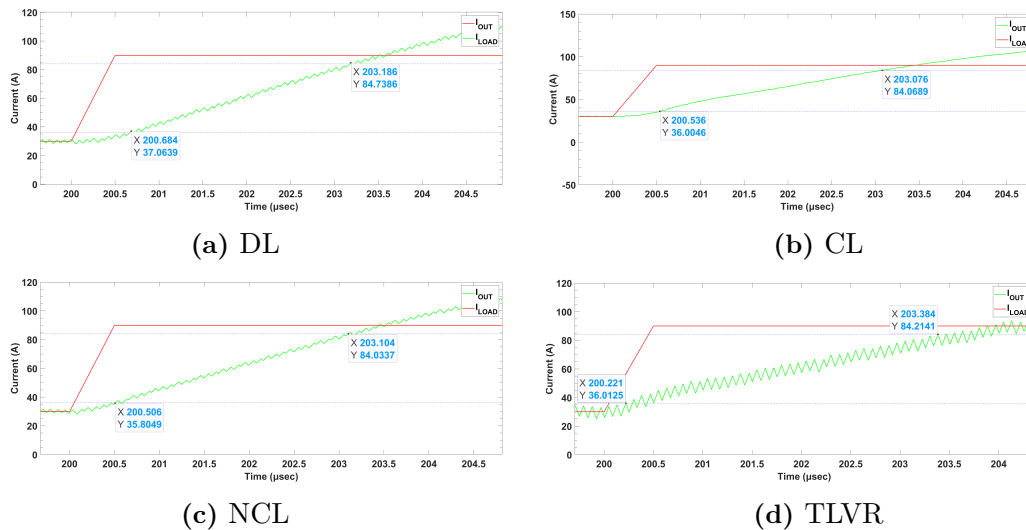


Figure 5.5: Load profile and combined inductor currents during load step.

Figure 5.6 shows a closer view of the load profile and combined inductor currents during the load release. Using the same analysis as for the load step, the $\frac{di}{dt}$ during the load release is calculated with (5.1) for each inductor topology, with results presented in Table 5.2. Negative values indicate a falling current. These values differ from the trend observed during the load step. Notably, DL still exhibits the fastest response at $-19.59 \text{ A } \mu\text{s}^{-1}$. While most inductor topologies show similar rising and falling $\frac{di}{dt}$, NCL is an outlier, being

slower during the load release with $-12.51 \text{ A } \mu\text{s}^{-1}$ compared to its load step performance of $18.56 \text{ A } \mu\text{s}^{-1}$.

Table 5.2: Calculated $\frac{di}{dt}$ during load release.

Inductor	$\frac{di}{dt} [\text{A } \mu\text{s}^{-1}]$
DL	-19.59
CL	-12.51
NCL	-18.61
TLVR	-15.12

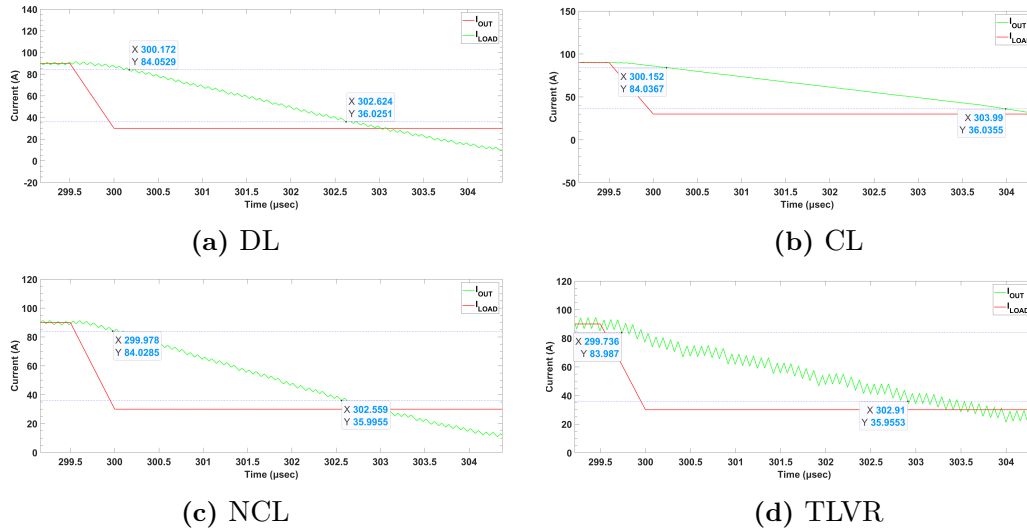


Figure 5.6: Load profile and combined inductor currents during load release.

Figure 5.7 illustrates the voltage drop at the onset of an increase in current demand. In DL, the voltage drop and subsequent rise are more pronounced compared to the other configurations, with a drop to just under 0.96 V and an overshoot reaching 1.02 V . For CL, the voltage drop is slightly above 0.96 V , with an overshoot marginally below 1.01 V . NCL exhibits a similar voltage drop to DL at 0.96 V but with a smaller overshoot of 1.01 V . TLVR outperforms DL in this scenario, with a voltage drop slightly exceeding 0.96 V and an overshoot slightly below 1.01 V . It is noteworthy that TLVR has the highest voltage ripple amplitude, while CL exhibits the lowest.

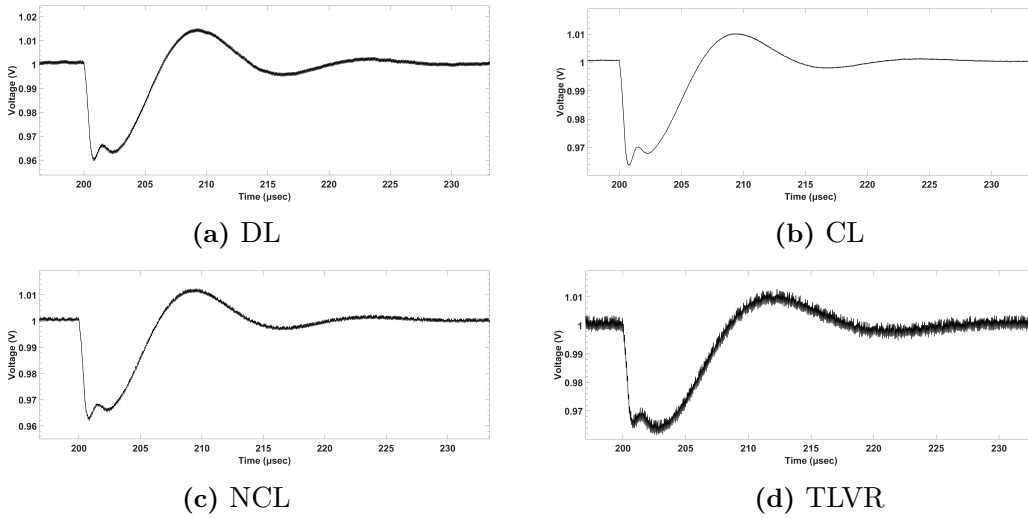


Figure 5.7: V_{OUT} during load step.

Figure 5.8 shows the voltage overshoot during the load release. Similar patterns are observed as in Figure 5.7 for the load step. The waveforms for DL and NCL are similar in response to the load release, appearing as inverses of the load step waveforms. DL exhibits the highest overshoot at 1.042 V. However, for CL, the overshoot during the load release is sustained, and the undershoot followed by the overshoot is sharper and greater in magnitude compared to the other inductor topologies, reaching a minimum of 0.94 V.

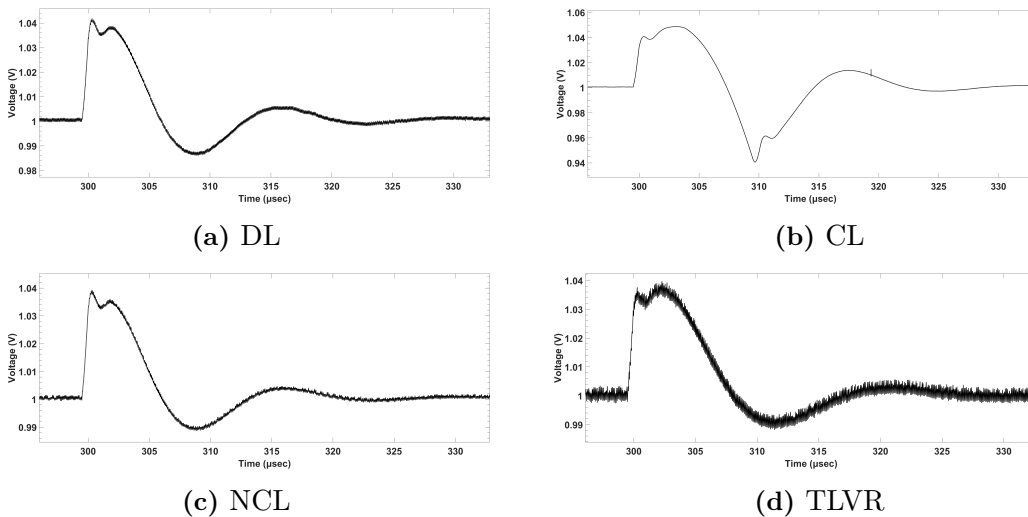


Figure 5.8: V_{OUT} during load release.

Figure 5.9 depicts V_{SW} for each phase during the load step. The load step is initiated at 200 μ s, and its effect is visible around 200.5 μ s onwards, where the V_{SW} for each phase is active for longer durations than before the load step. This indicates proper functioning, as longer on-time means more power is supplied to the load. Additionally, no overlapping of V_{SW} signals occurs, signifying that each phase is switching independently.

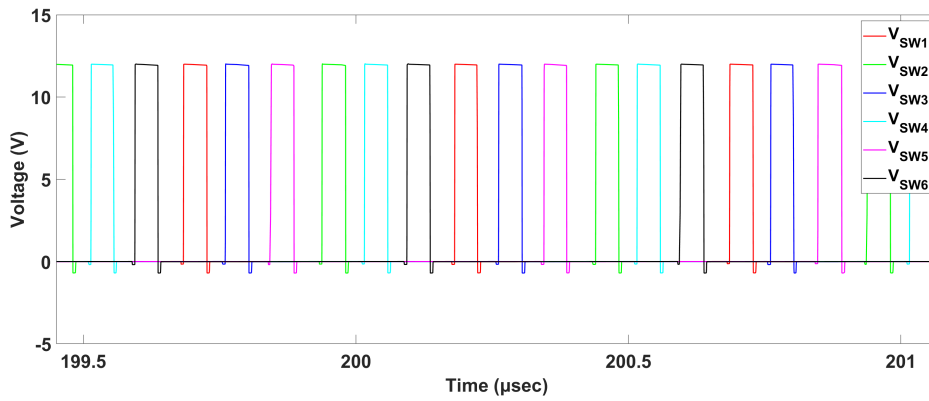
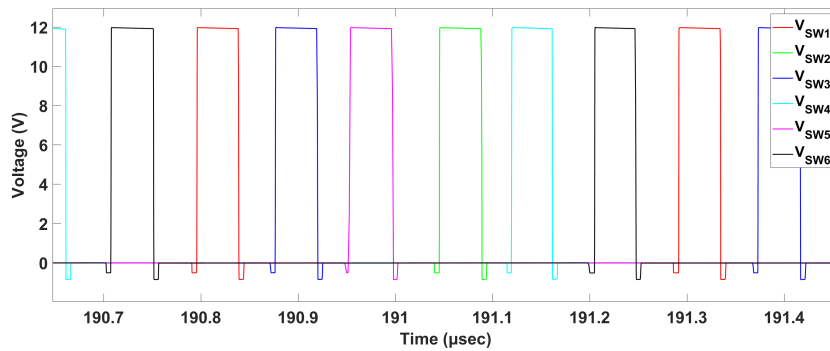
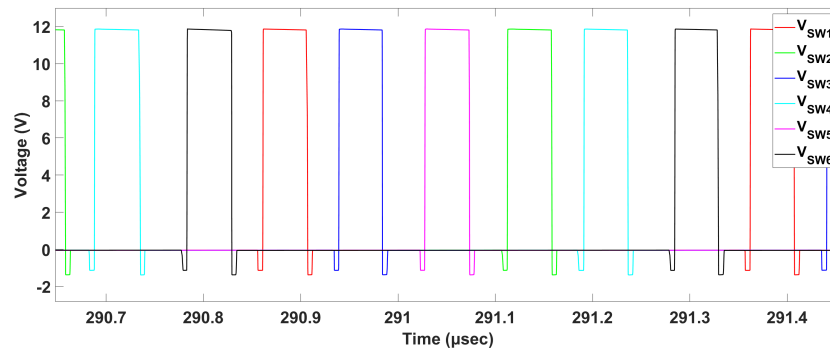


Figure 5.9: Phase V_{SW} during load step.

Figure 5.10 depicts each phase's V_{SW} during the two steady-state loads. Although difficult to discern, any V_{SW} in 5.10b has a longer on-time compared to Figure 5.10a, corroborating the prior analysis regarding Figure 5.9.



(a) 30A



(b) 90A

Figure 5.10: Phase V_{SW} during steady-state load.

5.1.3 Efficiency

Figure 5.11 shows the efficiency of different inductor setups during a voltage sweep, keeping the load constant. From the figure, we can see that the efficiency of CL and NCL is almost the same, in the same way, the efficiency of DL and TLVR is almost the same, but

comparing all the cases the efficiency of the CL and NCL setups are higher compared to DL and TLVR. In all cases the efficiency decreases with an increase in voltage, this might be because of the LT8627's internal voltage divider which is present in the chip to supply 3.5 V to the internal excitation in the chip. We tested the same in the hardware where we got similar efficiencies. One thing to note is that the CL and NCL efficiencies rise near the 6 V mark, this is because of the notching effect which is mentioned in 2.1.4.

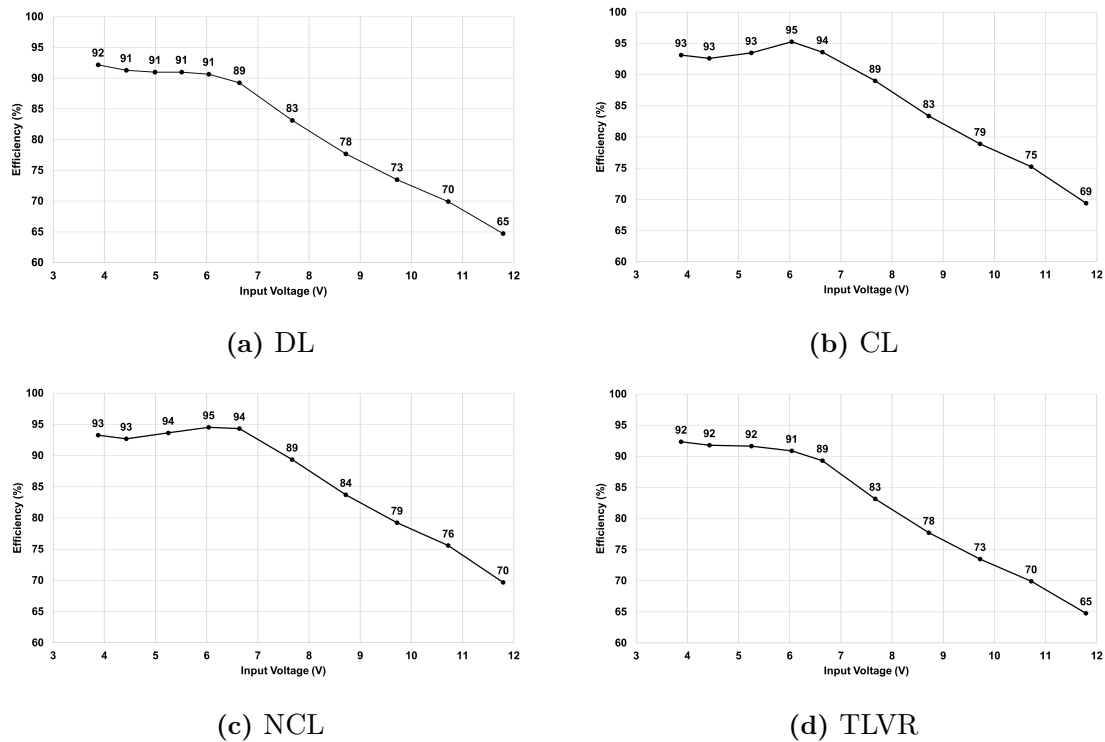


Figure 5.11: Efficiency with 20 A constant load.

Figure 5.12 shows the efficiencies with current sweep with a constant input voltage of 12 V. For CL and NCL the efficiency slope is a decreasing slope the max efficiency reaching 69%, whereas the efficiency of DL and TLVR increases in the first step after which there is a decreasing slope with the maximum efficiency of 68%. Comparing all cases, the efficiency of CL and NCL is slightly higher and the trend of efficiencies can be comparable to the results in 5.2.2

5. Results

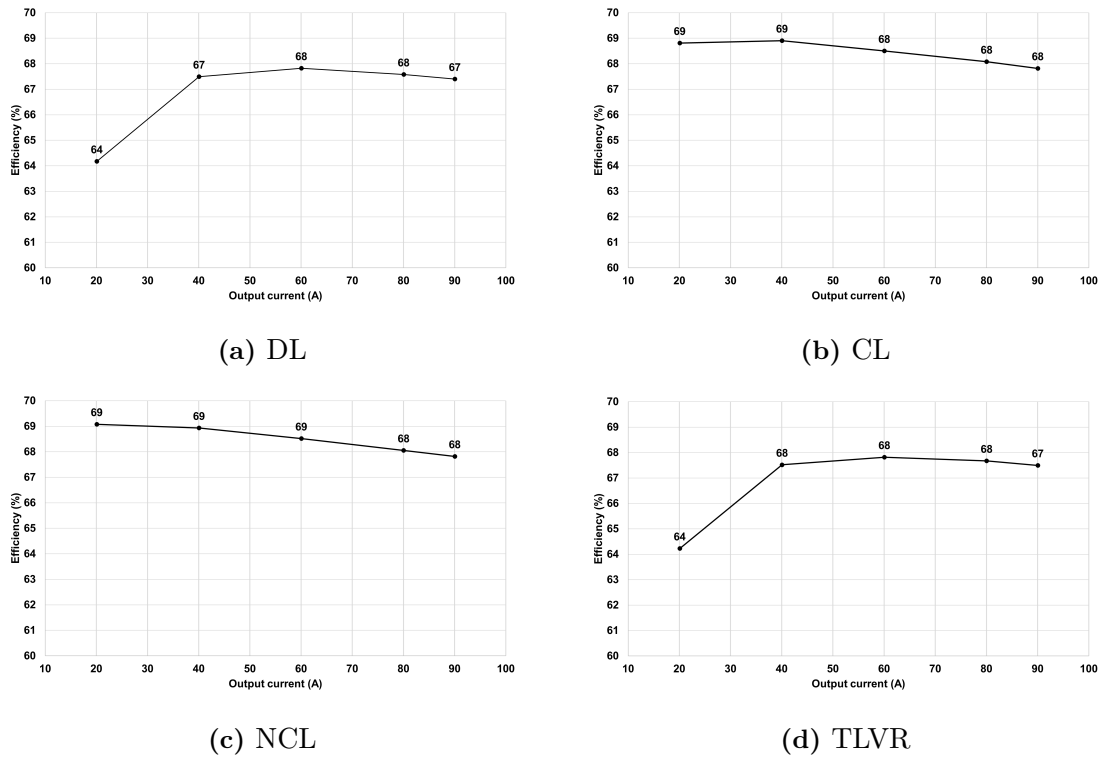


Figure 5.12: Efficiency with varying load with 12 V supply.

5.1.4 Power system rejection ratio

In Figure 5.13, we examine the gain with respect to V_{out}/V_{in} ratio using FFT analysis. The DL configuration shows a maximum gain reaching up to 50 dB, whereas the gain with CL peaks at 0 dB. This indicates that the DL circuit is more susceptible to transmitting noise, while the CL circuit is more effective at rejecting the noise supplied.

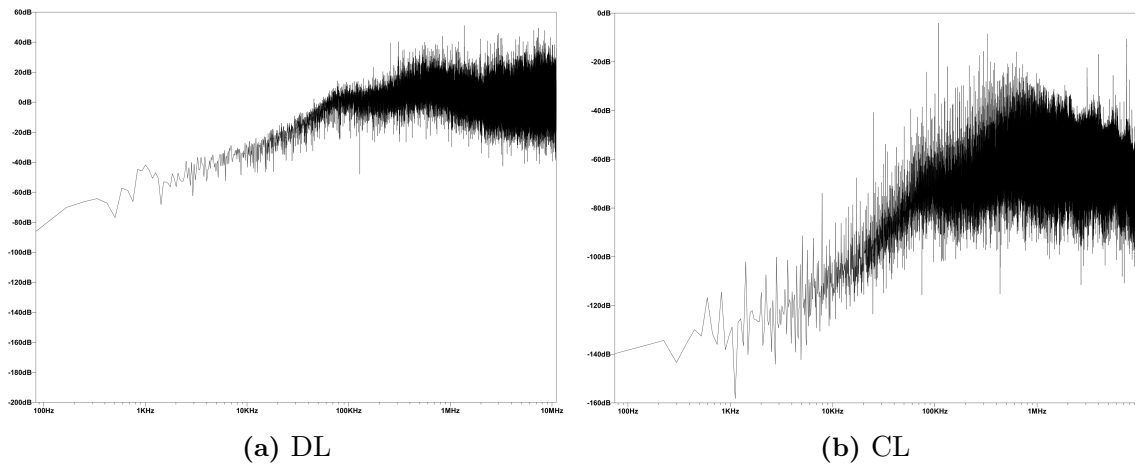


Figure 5.13: PSRR plots of DL and CL

5.2 Lab

5.2.1 Stability measurement

Figure 5.14 presents the Bode plots acquired from the physical setup for both CL and DL configurations. The chosen values for R_C and C_C were $10\ \Omega$ and $10\ \text{nF}$, respectively. The loop bandwidth for CL was observed to be $79.9\ \text{kHz}$, with a phase margin of 44.3° . In contrast, the loop bandwidth for DL was $73.8\ \text{kHz}$, and the phase margin was 39.2° .

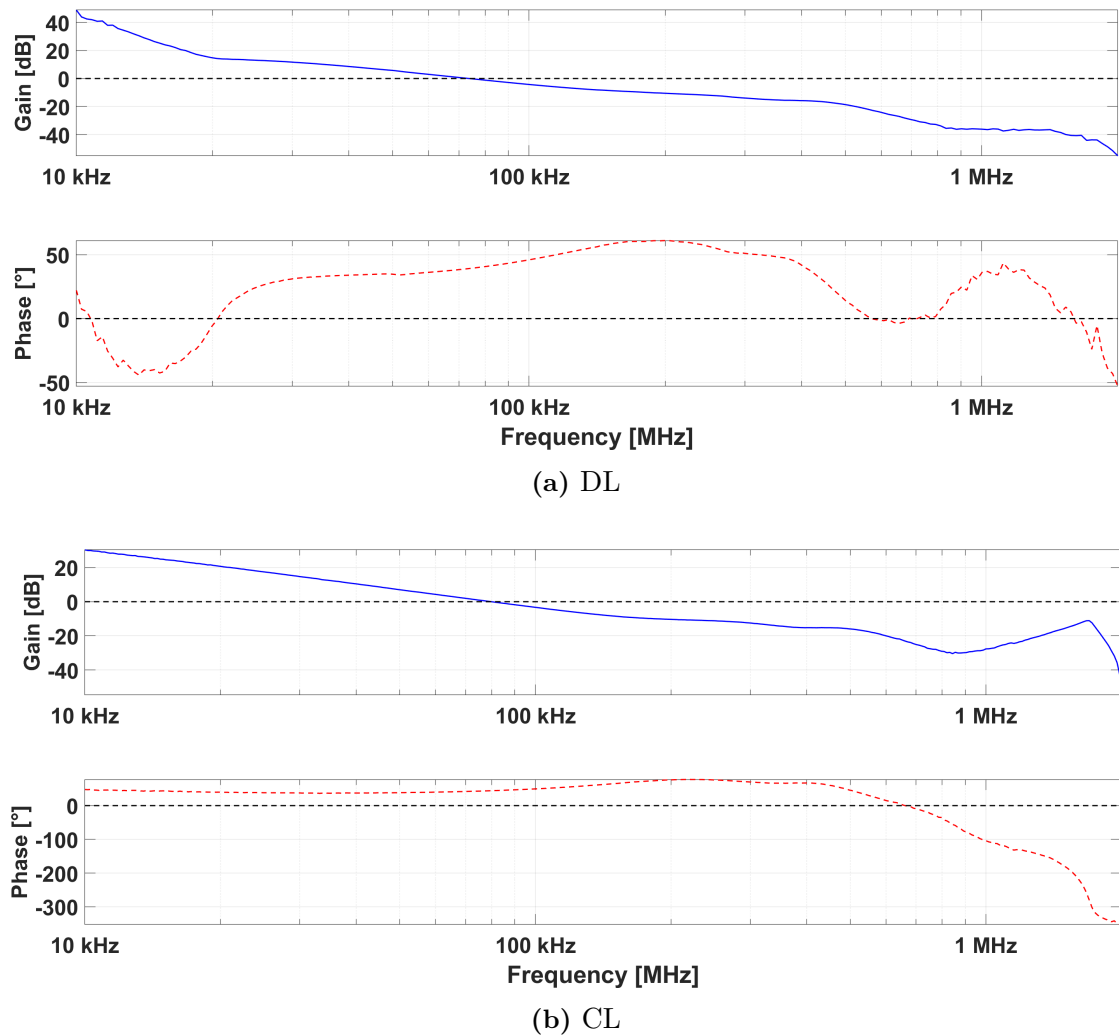


Figure 5.14: Measured Bode plots of DL and CL

5.2.2 Efficiency

The measured efficiencies align with the trends observed in Section 5.1.3. Figure 5.15 illustrates the efficiency of the circuit with a $6\ \text{V}$ input voltage, showing that CL achieves a higher maximum efficiency (87%) compared to DL (86%).

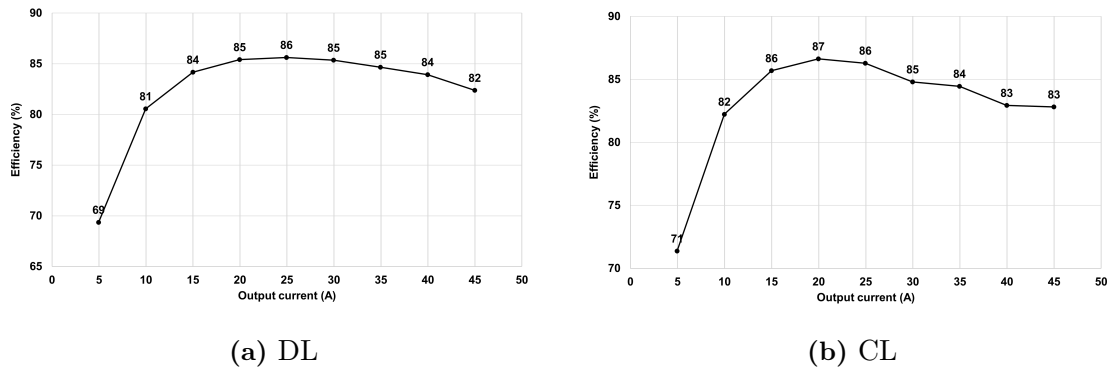


Figure 5.15: Efficiency for varying load with 6V supply.

Figure 5.16 demonstrates the efficiencies of CL and DL when subjected to a voltage sweep with a constant load of 19.94 A. Again, CL shows higher efficiency with a maximum of 89 %, whereas DL peaks at 87 %.

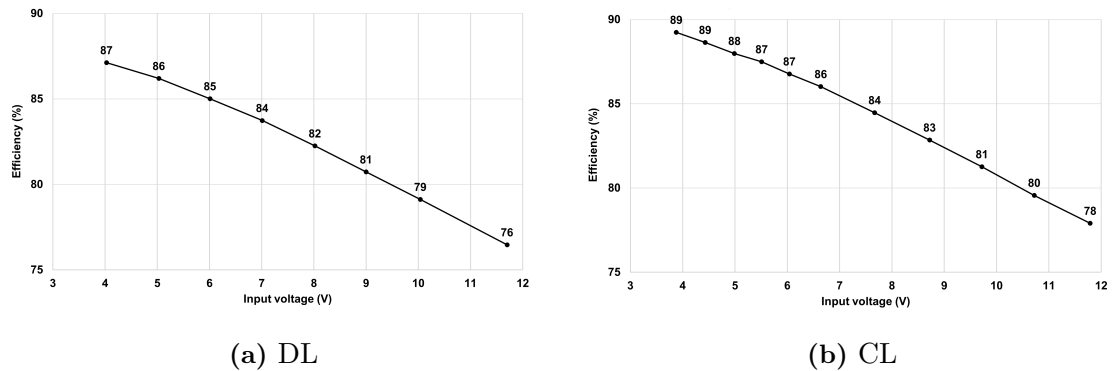


Figure 5.16: Efficiency for varying voltage with constant 20 A load.

5.2.3 Voltage Ripple

Output voltage ripples were tested under multiple conditions, and it was observed that the voltage ripple amplitude remained constant. Figure 5.17, although not clear in detail, shows the output ripples measured using an oscilloscope. While the peak-to-peak amplitude of the ripples is approximately 3 mV for both CL and DL, there is a notable difference in their shapes. One more thing to mention is that the voltage ripple in DL has ripples with low frequencies and High frequencies whereas the voltage ripples from CL has ripples only of high frequencies. This can be taken into consideration as if used in radio applications it may effect the radio signals.

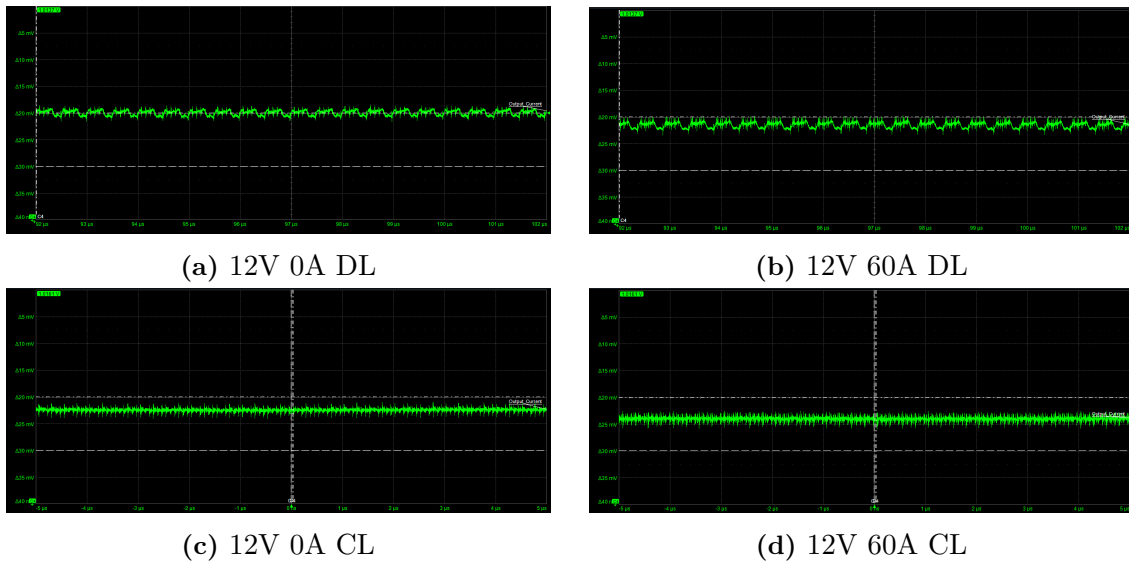


Figure 5.17: Measured Voltage Ripple

6

Conclusion

From the simulation results, it can be concluded that NCL and CL exhibit comparable efficiency. Additionally, they demonstrate higher efficiency than both DL and TLVR across most duty cycles, as indicated by the input voltage sweep simulation with efficiencies of CL and NCL at 95% compared to 91% for DL and TLVR at 6 V. For lower loads, CL and NCL outperform DL and TLVR, having efficiencies of 69% compared to 64% for a load of 20 A. At higher loads, the performance is similar, albeit slightly higher for CL and NCL in the 90 A case, with efficiencies of 68% compared to 67% for DL and TLVR. These efficiency trends observed in simulations are corroborated by hardware implementation results, further demonstrating the influence of inductor configuration on efficiency and voltage ripple.

The implications of these findings extend to the sustainability and ethical impact of power electronics design. The enhanced efficiency observed in CL and NCL configurations leads to reduced power consumption and thermal stress, resulting in lower energy costs and a diminished carbon footprint, crucial for environmental sustainability.

In terms of current slew rate, DL achieves the highest with $19.05 \text{ A } \mu\text{s}^{-1}$, while TLVR has the lowest with $15.24 \text{ A } \mu\text{s}^{-1}$ during the load step. For the load release, DL again proves to be the fastest at $-19.59 \text{ A } \mu\text{s}^{-1}$, whereas NCL is the slowest at $-12.51 \text{ A } \mu\text{s}^{-1}$. CL exhibits better performance regarding the magnitude of current overshoot, achieving the lowest at 114.0 A during the load step and an improved return to steady-state. However, CL's performance during the load release is less favorable, reaching -46.9 A . When evaluating the output voltage drop from load steps and releases, all inductor topologies show similar behavior, with the voltage dropping to 0.96V and the recovery voltage overshoot having a maximum magnitude of 1.01V. Overall, the comparative analysis of DL, CL, NCL, and TLVR highlights the advantages of CL and NCL in achieving higher efficiency and improved noise rejection capabilities. This analysis provides a foundational understanding that can guide the design and optimization of power converters towards more sustainable and reliable electronic systems.

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A

Simulation models

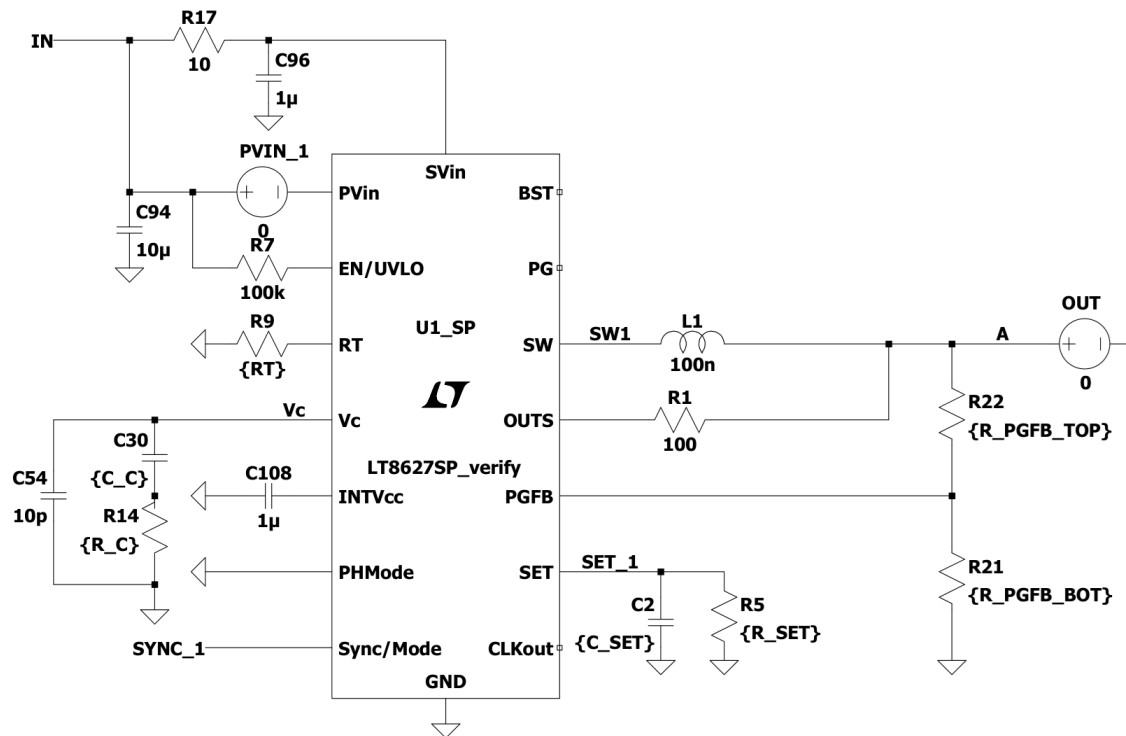


Figure A.1: PH1 of simulation model with DL.

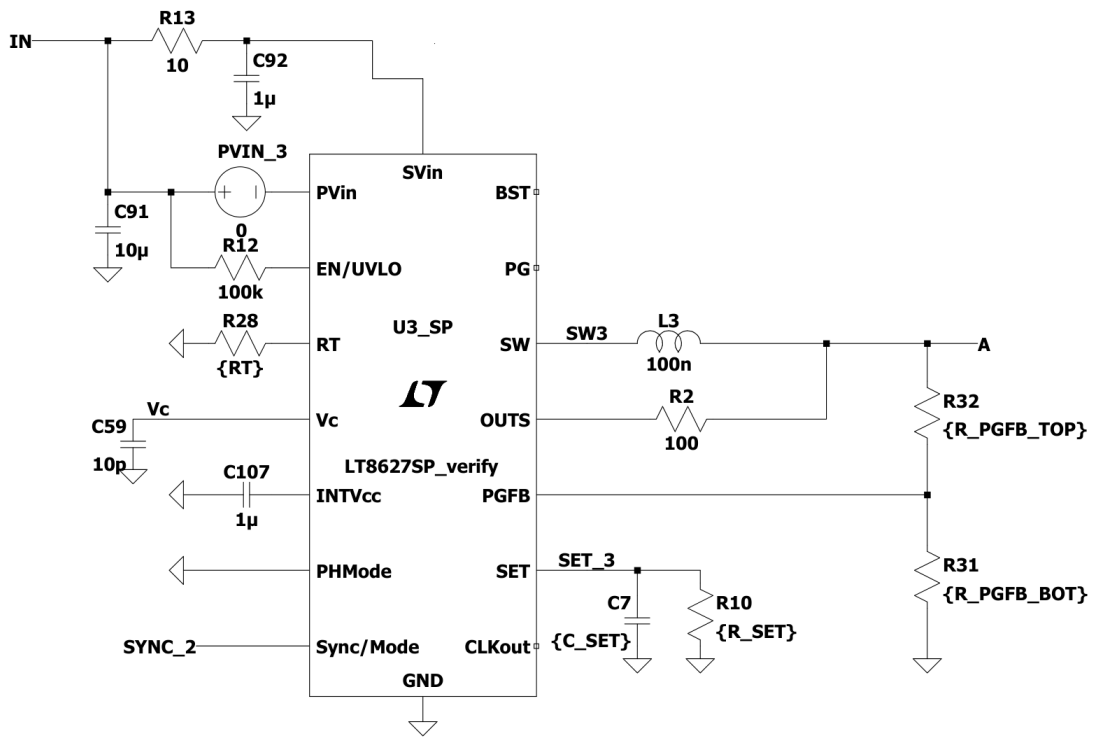


Figure A.2: PH3 of simulation model with DL.

External clock generator

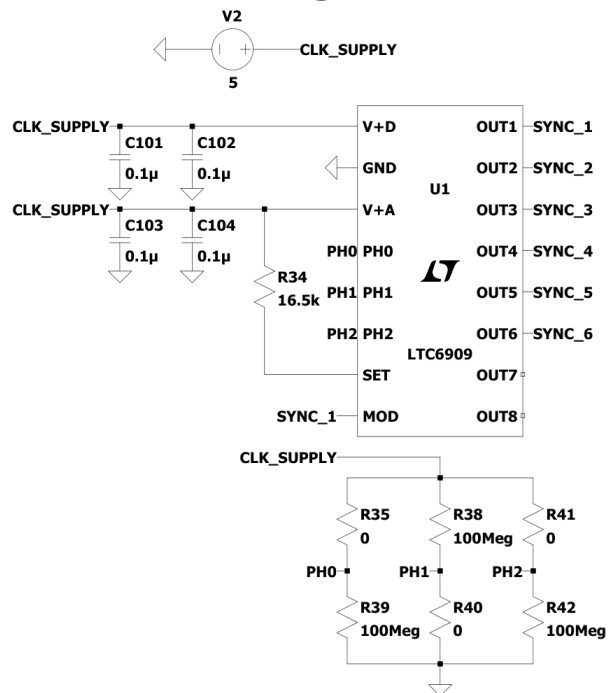


Figure A.3: Clock generator LTC6909.

Parameters

.param VIN=12	Input voltage.
.param R_PGFB_TOP=49.9k	PGFB Voltage Divider Top Resistor. Activates Fast Start-up.
.param R_PGFB_BOT=49.9k	PGFB Voltage Divider Bottom Resistor. Activates Fast Start-up.
.param R_SET=10k	SET resistor. Adjusted for Vout=1V.
.param C_SET=10p	SET capacitor.
.param RT=54.9k	Sets switching frequency.
.param R_C 10	Resistor Vc. Compensates control loop.
.param C_C=10000p	Capacitor Vc. Voltage on pin determines peak switching current.

Figure A.4: Parameters used for simulation.

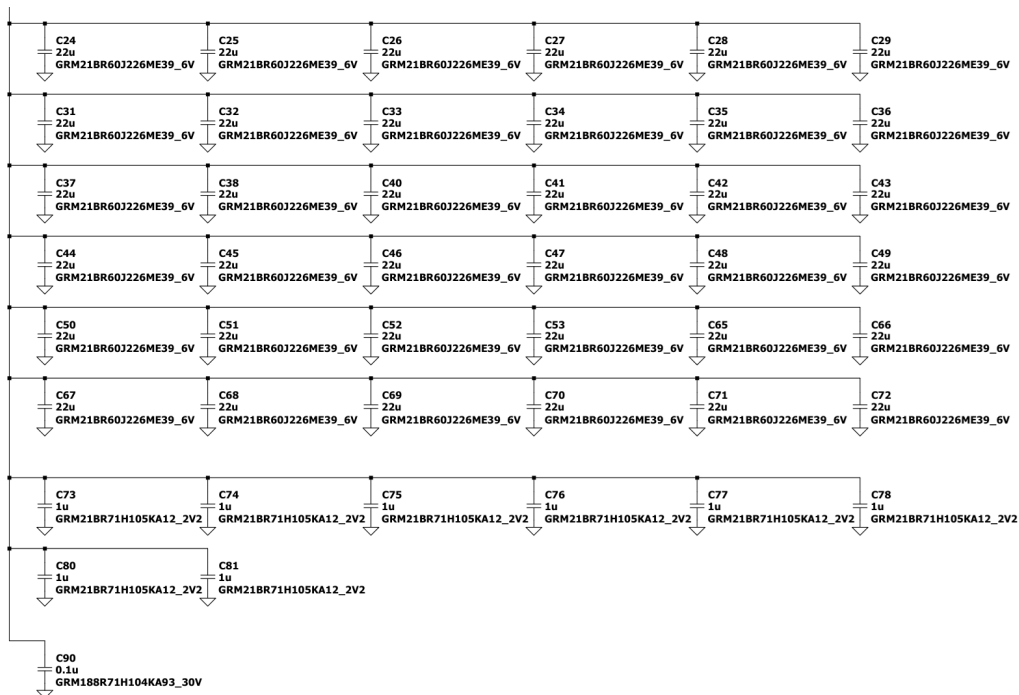


Figure A.5: Section of output capacitors.

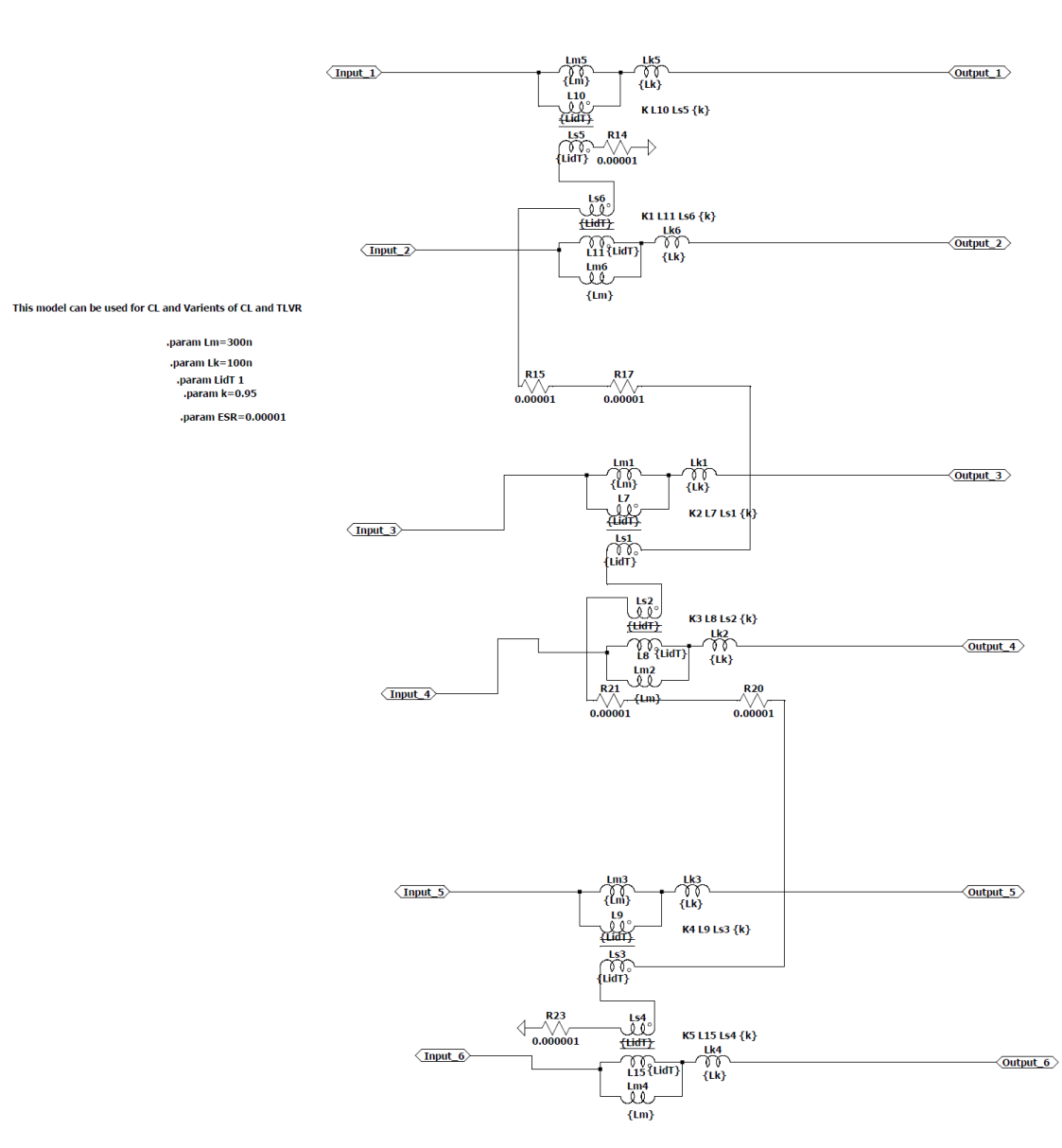


Figure A.6: Six Phase CL.

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