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Bias Circuit for RF Power Amplifiers

Master of Science Thesis in Wireless and Photonics Engineering

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To my parents

with love

ABSTRACT

Bias circuits often affect the instantaneous bandwidth (the bandwidth of the signal that is taken through the PA at a given time) over which a pre-distorter can linearize the transmitter's output signal. The resulting nonlinearity is difficult to remove completely even by most advanced pre-distortion techniques. In order to keep up with the increasing data rates in telecom industry, there is a desire to increase the mentioned bandwidth. This thesis describes clearly the effects of bias circuit which causes the baseband currents to generate significant variations in the baseband voltages at the transistor terminals. This paper proposes internal decoupling (large capacitance inside the drain package of the transistor) to lessen baseband resonance problem by moving the resonance to much lower frequency with a weaken amplitude. It also proposes the use of snubber circuit ($\frac{\lambda}{4}$ DC-Feed line together with a small resistor) to attenuate the weak resonance. Two models of packaged RF power transistor were available. These were identical except that one had internal drain baseband decoupling and the other not. Both were internally pre-matched Si LDMOS transistors designed mainly for class AB operation in the 1.8 GHz band. The transistor with internal decoupling seems to alleviate the baseband impedance variation problem thus making it easier to pre-distort.

Simulation result gave a baseband impedance of 0.3Ω at 11 MHz and 11Ω at 194 MHz for the transistor with internal decoupling and for the standard transistor respectively. The measurement results gave 2Ω(manufacturers measured with un-optimized board and it was 16Ω) at 242 MHz and 4Ω at 164 MHz again for the transistor with internal decoupling and for the standard transistor respectively. For RF performance, both transistors were designed for best efficiency and gave 58% for the transistor with internal decoupling and 55% for the standard transistor. Both transistors gave output power more than 100W.

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Contents

Chapter 1

1. Introduction

1.1 Background

Not so many years ago, most mobile radio transmitters were required to handle only a single analog voice channel mainly with constant envelope frequency modulation. As a result, the kinds of bias networks used to stabilize large RF power transistors were restricted. The bias networks seen in older manufacturers' catalogs were presented with large inductors wound on ferrite rings. This was quite acceptable as long as the modulation was either constant envelope, or had a very low signal bandwidth. On the other hand, Modern wireless systems use amplitude modulated signals with bandwidth capability in MHz, or tens of MHz, regions [7].

The oscillatory behavior of RF power transistors is a well-known short coming of RF Power Amplifier (PA) design. Its effects are most common at baseband frequencies (in the MHz to VHF range), where the terminating impedance of an RF power device is mainly defined by the bias insertion network. Voltage modulation that appears at the output terminal of the PA is caused by any impedance which is placed in the bias supply path; this modulation will in turn cause additional distortion products by modulating the gain and phase of the amplifier. Therefore it is mandatory to ensure that this impedance is sufficiently low so that the resulting voltage modulation has acceptably low amplitude. Due to the mentioned facts, for stable operation, the design of bias networks in any RF power amplifier plays an important role [7].

To achieve the required RF output power within the maximum allowed DC power consumption, the amplifiers of current base station transmitters operate under non-class A. There are harmonic currents generated when amplitude modulated signals pass through a Power Amplifier operating in a class other than class A. At baseband frequency (the zeroth harmonic band), significant current flow in the PA's drain and gate bias circuits. This current varies following the peaks and dips of the amplitude-modulated signal envelope [7]. The bias circuits are designed in such a way that the RF signal is isolated from the power supply (PA gets only DC power from the power supply and sets the transistor operating point). For this purpose inductive, capacitive and possibly resistive elements are used. Current RF power transistor packaging technology and the PA building practice limit the performance of these bias circuits which causes the baseband current to generate significant variation in the baseband voltages at the transistor terminals, which in turn modulates the transistor's operating conditions. This may inflict dynamic distortion on the amplified signal, and may even in extreme cases lead to transistor breakdown failure. To achieve the output signal linearity requirements, one sometimes uses a technique where the transmitter corrects for its nonlinearities, which are mainly caused by the PA, using adaptive digital pre-distortion. But in some cases the mentioned dynamic variation cannot be pre-distorted or it becomes too costly to pre-distort as the signal and RF bandwidth increases. Thus, the PA dynamic distortion should be kept at a level that most cost effective pre-distortion algorithms can handle.

1.2 Aim of thesis work

The main purpose of thesis work is to study the isolation of RF Power Amplifier (PA) from its power supply and also investigate new solutions to alleviate the problems encountered. The power supply should be isolated except that the RF PA gets DC power from the supply. By doing so there are

possible problems arising. These problems arise both at the gate and drain of the transistor of the PA and can be described as

1. There is parallel resonance (caused by the bias circuit low frequency inductance and the transistor drain/gate capacitance) around the baseband frequency which together with the RF baseband current causes a variation in the baseband drain/gate voltage. This variation will modulate the transistor operating point causing dynamic distortion on the amplified signal. Due to the described reason, it is important to have low enough impedance seen by the transistor over large enough base-band frequency region.
2. The bias circuit should present very high impedance over large RF bandwidth as seen by the transistor not to affect the RF match of the system. However the second problem is, there is not high enough impedance seen into the bias circuit by transistor over large enough frequency region around fundamental RF frequency.

1.2 Report Organization

This report has two major goals: first, to provide the reader with an introduction to the effects of the bias circuit on RF PA design together with general PA theory; and second, to discuss ways on how to overcome the mentioned effects. The format of this report will thus be,

Chapter 2 discusses the common topologies used in Power Amplifier design, as well as briefly explains different bias networks and their effect on PA performance.

Chapter 3 contains the brief description of how two different PAs were designed for two different transistors. These PAs were used mainly to study the baseband performance.

Chapter 4 contains all the simulation and measurement results for the two PAs designed and fabricated.

Chapter 5 contains comparative analysis of the simulation and measurement results that were obtained from realizations of the two different PAs.

Chapter 2

2. Theory

2.1 Amplifier Classes

Depending on class of operation, RF power amplifiers used in transmitter circuits exhibit varying degrees of nonlinearity. While keeping constant RF input signal, the output current's harmonic content varies with the DC bias at the gate of the LDMOS device. The transistor conduction RF cycle depends on a bias level for specific application. This chapter discusses eight classes of power amplifier operation, in which the first four are often used in RF power amplifiers. Figure 2.1 shows these four classes based on the transistor transfer characteristics.

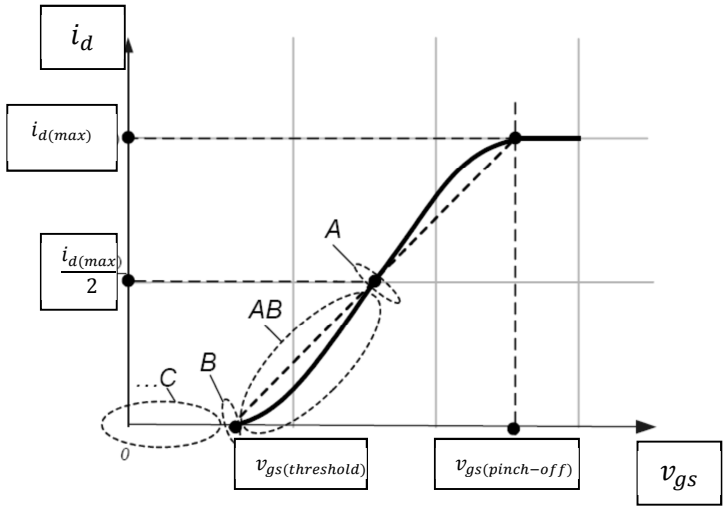


Figure 2.1. Classes of Operation of Power Amplifiers [1]

Where,

v_{gs} : is the instantaneous gate to source voltage of a transistor

i_d : is the instantaneous drain current

$v_{gs(threshold)}$: is the minimum voltage needed to turn on a transistor

$v_{gs(pinch-off)}$: the v_{gs} (for this very amplifier) that causes the v_{ds} that the transistor goes out of pich-off: Maximum instantaneous drain current

---- (dotted graph): ideal characteristic of transistor operation

2.1.1 Class A

In this class of amplifier, shown in figure 2.2, the transistor is biased at the middle of the DC characteristics and conducts through the whole RF cycle. This means that it's conducting with a conduction angle (Θ) of 360° or 2π. It also works in its linear range for low amplitude signals since as the RF amplitude gets smaller, smaller part of the transistor characteristic is visited. But for large RF signal amplitude (figure 2.2), larger and less linear transistor characteristics are visited. Class A has

higher gain than all other classes. The disadvantage of this amplifier is it has DC consumption without any RF input signal and also for low-amplitude RF input. Therefore, this class of amplifier is very inefficient but is less complicated and linear. Class A amplifier is usually used for low power or small signal applications [2],[5].

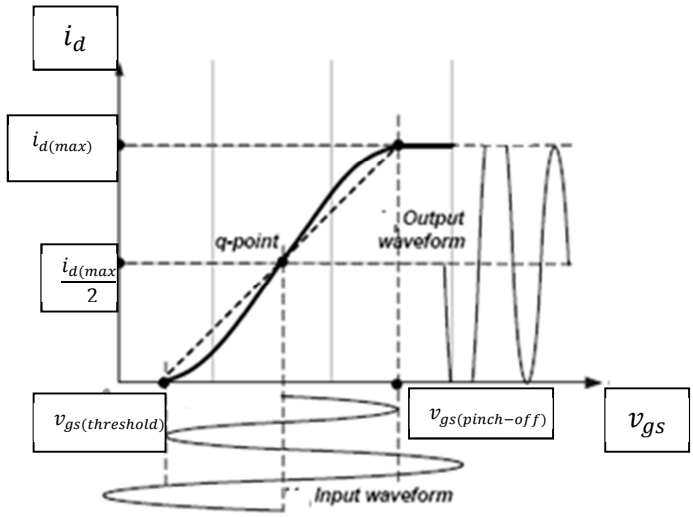


Figure 2.2 Transfer Characteristics for Class A operation [1]

2.1.2 Class B

In this class of amplifier, shown in figure 2.3, the transistor is biased at pinch off and conducts 50% of the RF cycle which corresponds to Θ = 180° or π. This means, the transistor works in its linear range (instantaneous output current of the transistor being linear function of the instantaneous input voltage) for half of the RF cycle and is turned off for the other half. The main advantage of Class B amplifiers over Class A is, there is no current consumption when there is no RF input. In addition, the DC current consumption decreases (approximately linearly) with decreasing RF amplitude. For large input amplitude (still below saturation and greater than $V_{\text{threshold}}$) the gain to a good approximation will be the constant gain of ideal class B (ideal in that transconductance could be considered constant for $v_g > v_T$). Whereas for much lower amplitude (figure 2.3) where the lowest transconductance towards $V_{\text{threshold}}$ becomes more dominant, the gain will drop from ideal class B to zero. This strong non-linearity is sometimes called cross over distortion [2],[5].

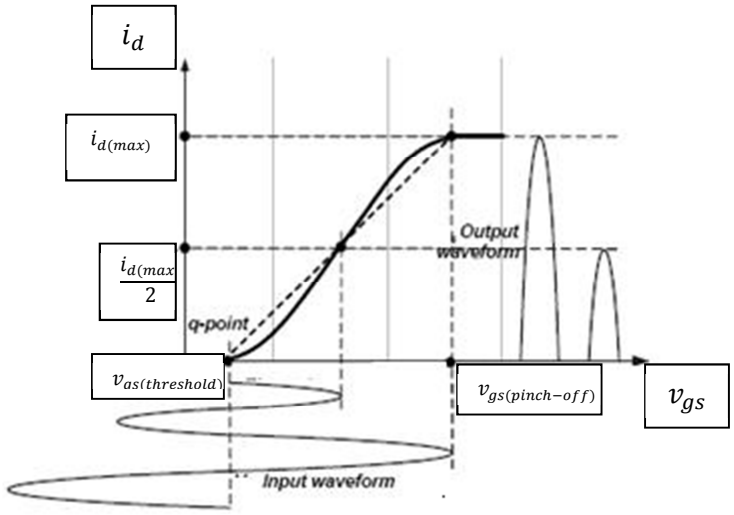


Figure 2.3 Transfer characteristics for Class B operation [1]

2.1.3 Class AB

In this class of amplifier, shown in figure 2.4, the transistor is biased in the operating point somewhere between Class A and Class B. The cross over distortion in this class goes significantly down compared to Class B. The cross over distortion never goes to zero, on the other hand the high amplitude saturation distortion is somewhat lower for class AB than class A. For the same saturation distortion, the maximum output power is somewhat less for class A than for class AB. As a result, it is not possible to say that Class A is more linear than class AB. But for class A, it is possible to get as high linearity as one wants by reducing the maximum used output power which is not possible for realistic class AB. Most Radio Frequency (RF) Power Amplifiers are class AB rather than Class B. This is because class AB is more linear than Class B. This linearity is achieved by having quiescent current (consumes DC-current even at zero RF amplitude) [2],[5].

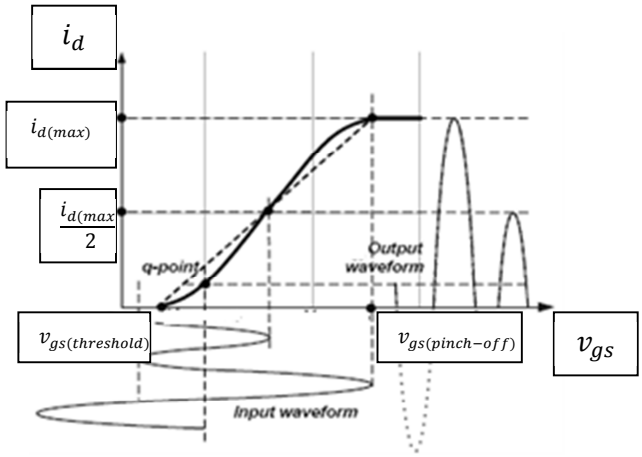


Figure 2.4 Transfer characteristics for Class AB operation [1]

2.1.4 Class C

In this class of amplifier, the transistor is biased below pinch off and conducts less than 50% of the time which corresponds to Θ < 180°. The advantage is, it has a higher efficiency than all Class A, Class B and class AB. The main drawback is that the linearity is worst with high distortion [2].

2.1.5 Class D

This class can be considered as a high power signal generator. This class use switching to get very high power efficiency. By allowing each output device to operate in a way that it is either fully off or on, losses are minimized in an idealized model, for more realistic however, that might not be the case. [2]

2.1.6 Class E

In this class, the switch in the driver circuit is driven with 50% of the time. Device capacitance Cs is absorbed into network. Load network is derived to provide ZVS and dVds/dt = 0. The main drawback of the Class E amplifier is that the voltage swing across the device is very large (3.6×VDD). [2]

2.1.7 Class F

In this class, harmonic termination is used to square wave shaping of intrinsic drain voltage (the voltage at the intrinsic drain inside the transistor package). The third harmonic, and possibly also some higher odd order harmonics, are terminated in very high impedance. This limits the maximum efficiency to be approximately 80%. But if an infinite number of harmonics can be considered in ideal case, the efficiency can reach up till 100% at maximum output power. [2]

2.1.8 Class F^{-1}

This class of amplifier is dual to the class F amplifier. The difference here is that, here shapes of the intrinsic drain current (the current at the intrinsic drain inside the transistor package) and voltage curves are interchanged relative to the class F; here a square-wave drain current is used. The second harmonic is terminated in a close to infinite impedance (and possibly higher order even harmonics). [2]

All of the above described amplifiers except ideal class A, take different current for different RF amplitude, and therefore the reactance of bias circuitry is important for them.

2.2 Analytically analyzing PA

Power Amplifier is one of the most sophisticated and important parts in a radio design. For this reason, it is very important to understand what is really going on inside this unit. In order to understand such a complex unit, it is important to start with simplified approach. In this section a simple ideal class B amplifier drain circuit is analyzed for investigating effects of bias circuit. The most important building blocks of the drain circuit are seen in figure 2.5 below

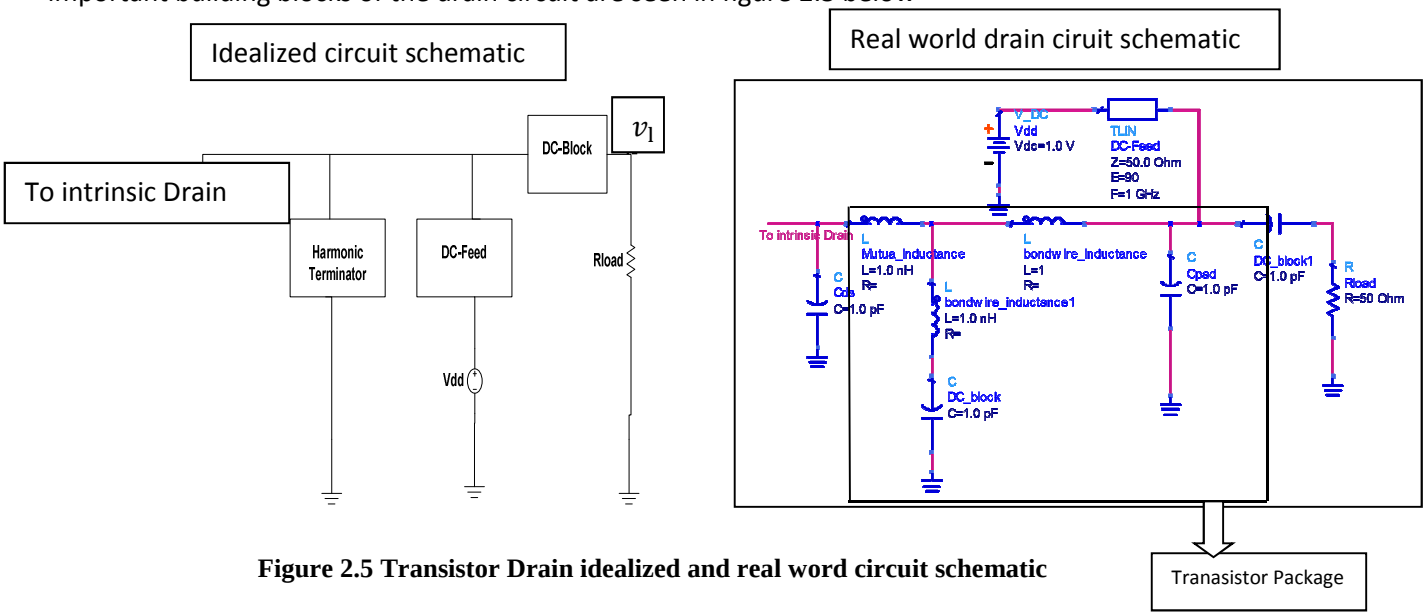


Figure 2.5 Transistor Drain idealized and real word circuit schematic

From figure 2.5 the harmonic terminator is part of the drain circuit inside the transistor package which is usually made by the transistor manufacturers. The values given in the real world circuit are not realistic and are inserted just as an example. The mutual inductance (L mutual_inductance which is explained in section 2.31) is very small and of importance only for more exact quantitative considerations.

The harmonic terminator gives a reasonably good approximation to a zero-impedance path to ground for 2nd, 3rd…harmonics of i_d (in figure 2.5 it is idealized and gives exactly zero ohm) so that v_d can only contain Fourier components in the baseband and fundamental RF region.

The DC Feed in figure 2.5 should present zero impedance to ground at baseband frequencies and infinite impedance at RF frequencies. So all baseband Fourier components of v_d are then zero except for the zero frequency component which is V_{dd}. The only non-zero Fourier component of V_d are therefore the ones in the fundamental RF region and the zero-frequency component that equals the drain supply voltage.

The DC-Block in figure 2.5 ideally should give infinite impedance at zero frequency. In addition, it is also assumed to give zero impedance over the whole fundamental RF region. For a more practical PA it should also give reasonably high impedance over the whole baseband region, but in the ideal case this is not an issue since here exact DC (Zero hertz) is the only baseband Fourier component of v_d .

As a result, all the RF Fourier components of the load voltage v_1 are the same as the drain voltage v_d . These two voltages are equal except for the supply voltage V_{dd} that is present for v_d but not for v_1. And the Fourier components of v_1 and v_d in the fundamental RF region will be proportional to those of the drain current i_d with constant of proportionality equal to R_{Load}.

2.2.1 Continuous Wave (CW)

This is un-modulated signal where the RF input power is constant. In the ideal model the instantaneous drain current is,

$$i_d(t) = g_m * (v_g(t) - v_T)\text{ , for } v_d > 0 \; and \; v_g > v_T$$

Where, g_m is the transconductance of the transistor

v_T is the threshold voltage

$i_d(t) = 0$, for $v_d > 0$ and $v_g < v_T$

v_T is handled by the gate bias that is not much of interest now, so assume $v_T = 0$ and zero gate bias (Ideal class B operation which is discussed in section 2.1.2)

Under these conditions, the gate voltage is given by

$$v_g = A * \cos(\omega_c * t) \tag{2.1}$$

$$i_d(t) = g_m * A * \cos(\omega_c * t)\ ,\ \frac{-\pi}{2} \le \omega_c * t \le \frac{\pi}{2} \tag{2.2}$$

$$i_d(t) = 0,\quad -\pi \le \omega_c * t \le \frac{-\pi}{2} \text{ and } \frac{\pi}{2} \le \omega_c * t \le \pi \tag{2.3}$$

The DC current is,

$$I_{DC} = \frac{1}{2*\pi}\int_{-\pi}^{\pi} i_d(t) * d(\omega_c * t) = \frac{g_m * A}{2*\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \cos\varphi \, d\varphi = \frac{g_m * A}{\pi} \tag{2.4}$$

And the fundamental RF current

$$I_{RF} = \frac{1}{\pi}\int_{-\pi}^{\pi} i_d(t)\cos(\omega_c * t) d(\omega_c * t) \tag{2.5}$$

$$= \frac{g_m * A}{2\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \cos^2(\omega_c * t) d(\omega_c * t) \tag{2.6}$$

$$= \frac{g_m}{2} * A \tag{2.7}$$

So the drain current can be described in a Fourier series form

$$i_d(t) = g_m * A * \left(\frac{1}{\pi} + \frac{1}{2}\cos(\omega_c * t) + \text{second and higher harmonics}\right) \tag{2.8}$$

And the instantaneous drain voltage becomes

$$v_d(t) = V_{dd} - \frac{g_m * A}{2} * R_{load} * \cos(\omega_c * t) \tag{2.9}$$

$$v_l(t) = -\frac{g_m * A}{2} * R_{load} * \cos(\omega_c * t) \tag{2.10}$$

Here the minus sign comes from the current direction of i_d was taken positive to be downwards

eliminating the input amplitude A in (2.4) by use of (2.7)

$$\mathrm{I_{DC}} = \frac{2}{\pi} * \mathrm{I_{RF}} \tag{2.11}$$

Using equation 2.7 the RF voltage across the load is,

$$V_{\mathrm{RF}} = \frac{g_m * A}{2} * R_{load} = R_{load} * I_{RF} \tag{2.12}$$

Using 2.9 and 2.12 the instantaneous drain voltage becomes,

$$v_{\mathrm{d}}(\mathrm{t}) = \mathrm{V_{dd}} - \mathrm{V_{RF}} * \cos(\omega_{\mathrm{c}} * \mathrm{t}) \tag{2.13}$$

From equation (2.13), it can be seen that $\mathrm{V_d} \geq 0$ all the time if $\mathrm{V_{RF}} \leq \mathrm{V_{dd}}$, this implies that the maximum amplitude of RF output voltage is equal to the drain supply voltage.

The maximum instantaneous voltage that occur during an RF cycle is,

$$v_{\mathrm{d,max}} = \mathrm{V_{dd}} + \mathrm{V_{RF}} \tag{2.14}$$

For $\mathrm{V_{dd}}$=$\mathrm{V_{RF,max}}$, leads to

$$v_{\mathrm{d,max}} = 2 * \mathrm{V_{dd}} \tag{2.15}$$

The value given in equation (2.15) should be less than the transistor break down voltage ($\mathrm{V_{break-down}}$) which is > 2∗ $\mathrm{V_{dd}}$ for the transistor not to break down. Maximum possible $\mathrm{V_{dd}}$ for the transistor not to break down at maximum output amplitude for that $\mathrm{V_{dd}}$ is $V_{\mathrm{dd,max}}$=$\frac{V_{breakdown}}{2}$, and so maximum possible intrinsic drain voltage output amplitude for a given transistor is $V_{RFmax,transistor}$=$\frac{V_{breakdown}}{2}$.

The RF output power is,

$$\mathrm{P_{RF}} = \frac{\mathrm{V_{RF}} * \mathrm{I_{RF}}}{2} \tag{2.16}$$

In Equation (2.16) the power is considered as an average power over one RF cycle and the load is considered to be purely resistive

$$\mathrm{P_{RF}} = \frac{\mathrm{V^2_{RF}}}{2 * \mathrm{R_{load}}} \tag{2.17}$$

The maximum output power then becomes

$$\mathrm{P_{RF,max}} = \frac{\mathrm{V^2_{dd}}}{2 * \mathrm{R_{load}}} \tag{2.18}$$

Using (2.11) together with generalized DC power formula, the drain power-supply power used to produce this RF power is,

$$\mathrm{P_{DC}} = \mathrm{V_{dd}} * \mathrm{I_{DC}} = \mathrm{V_{dd}} * (\frac{2}{\pi} * \mathrm{I_{RF}}) \tag{2.19}$$

The drain efficiency is then,

$$\frac{P_{RF}}{P_{DC}} = \frac{\pi}{4} * \frac{V_{RF}}{V_{RF,max}} \quad (2.20)$$

So if high efficiency is needed which is almost always the case, R_{load} should be chosen so that the maximum available output power from the PA equals the maximum output that is needed. Of course the transistor cannot deliver however large current, so there is an absolute maximum output power a given transistor can deliver at a chosen V_{dd}. This value of the load impedance is called R_{opt} [7]

$$R_{opt} = \frac{V^2{}_{dd}}{2*P_{RF,max}} \quad (2.21)$$

Properly designing the matching circuit makes sure that the load impedance actually presented to the intrinsic drain is R_{opt} , and this shows how important it is to design the matching circuit carefully.

2.2.2 Modulated Two-Tone Signal

In this case there are two equally strong input sinusoids whose frequencies are plus and minus of the modulation frequency from the center frequency. The two-tone test is a simple yet effective test to investigate the behavior of the PA for modulated signals. Taking two equal amplitude signals with a modulation angular frequency $\omega_m = \frac{\Delta\omega}{2}$,

$$v_g(t) = \frac{B}{2}\left(\cos\left(\omega_c - \frac{\Delta\omega}{2}\right)t\right) + \cos\left(\left(\omega_c + \frac{\Delta\omega}{2}\right)t\right) \quad (2.22)$$

$$= B*\cos\left(\frac{\Delta\omega}{2}t\right)*\cos(\omega_c * t)$$

$$= A(t)*\cos(\omega_c * t)$$

Where

$$A(t) = B*\cos\left(\frac{\Delta\omega}{2}t\right)$$

From (2.7) and (2.4) respectively,

$$I_{RF}(t) = \frac{g_m*B*\cos\left(\frac{\Delta\omega}{2}t\right)}{2} \quad (2.23)$$

$$I_{baseband}(t) = \frac{g_m}{\pi} * B * \left|cos\left(\frac{\Delta\omega}{2}t\right)\right| \quad (2.24)$$

So the baseband current has Fourier components at $\omega_0 = 0, \omega_1 = \omega, \omega_2 = 2 * \Delta\omega$ and so on

For non-ideal DC-feed (DC source not being short circuit at all frequency which is explained in detail in section 3.3.1)

$$V_{idbb}(t) = V_{dd} - \sum_{n=1}^{nmax} Re(Z_{DC\text{-}feed}(n*\Delta\omega)*C_n*e^{i*n*\Delta\omega*t}) \quad (2.25)$$

where, $V_{idbb}(t)$ is the intrinsic drain baseband voltage

C_n is fourier coefficient of I_{idbb} (intrinsic drain baseband current) for $\omega = n*\Delta\omega$

n_{max} here is the highest Fourier component intended to be included, because this simplified model can't be valid at arbitrary high frequency and RF components cannot be included. Therefore, n does not go all way up to infinity.

$Z_{DC\text{-}feed}$ is not the impedance of the box DC-feed in the figure 2.5, but the total impedance seen by intrinsic drain in the baseband frequency region. If the DC-feed box is actually ideal, which is exactly zero impedance in baseband frequency region and presenting infinite for all RF regions, then intrinsic drain sees zero ohm regardless of what impedances the other boxes present. But if the DC-feed box is non-ideal, which is non-zero impedance in baseband region, then the impedance seen by intrinsic drain will depend on also other boxes. As a result, the whole drain bias circuit is not just the DC-feed box, but also part of the RF circuit (harmonic terminator, RF match).

If $|Z_{DC\text{-}feed}(\omega)|$ is small except for a peak at $\omega=\omega_{res}$, then emphasis can be on looking at modulation frequencies $2*\omega_{mod}=\Delta\omega=\omega_{res}$, $4*\omega_{mod}=2*\Delta\omega=\omega_{res}$, $6*\omega_{mod}=3*\Delta\omega=\omega_{res}$, etc. This is due to, only for those modulation frequencies there will be a Fourier coefficient of the drain baseband current that has a frequency where the impedance is not small, and thus creates a significant contribution to the drain voltage. If it is the n'th baseband harmonic that hits the peak/resonance ($n*2*\omega_{mod}=n*\Delta\omega=\omega_{res}$), then the drain baseband voltage is,

$$V_{idbb}(t)=V_{dd}-Re(Z_{DC\text{-}feed}(\omega_{res})* C_n * e^{i*n*\Delta\omega*t}) \quad (2.26)$$

$$V_{idbb}(t) = V_{dd}-|Z_{DC\text{-}feed}(\omega_{res})|*|C_n|*\cos(n*\Delta\omega*t+\arg(Z_{DC\text{-}feed}(\omega_{res}))) \quad (2.27)$$

So the minimum drain baseband voltage over a cycle is

$$V_{dd}-|Z_{DC\text{-}feed}(\omega_{res})|*|C_n| \quad (2.28)$$

From previous subsection, we then know that the maximum possible RF voltage amplitude (measured at intrinsic drain) is then reduced from

$$V_{dd} \rightarrow V_{dd}-|Z_{DC\text{-}feed}(\omega_{res})|*|C_n|$$

For the idealized class B amplifier, although that is an idealized model, this can be used as a qualitative estimate for what will happen for a realistic amplifier. Only a small reduction of the relative value of the maximally achievable output RF amplitude can be accepted, and so at worst the accepted reduction of effective V_{dd} is one or a few percent of V_{dd}.

In ideal class B case: the absolute value part of the non-linear function (baseband intrinsic drain current) in (2.27) is what makes the baseband spectrum much wider/broader than the fundamental RF spectrum (the actual signal spectrum). If it had not been for the absolute-value, then the baseband current had been proportional to $\cos((\Delta\omega/2)*t)$, and the drain baseband current would have had only one single Fourier component (for this two-tone modulation) at $\omega=\Delta\omega/2$. It is the non-linearity of the absolute-function (for ideal class B, similar but not exactly the same function for realistic amplifiers) that makes instead a Fourier series with components at $\Delta\omega$, $2\Delta\omega$, $3\Delta\omega$, $4\Delta\omega$ etc.

The maximum RF output power is achieved when the intrinsic baseband voltage is equal to V_{dd} which results,

$$P_{RF,max}(t) = \frac{V^2_{idbb}(t)}{2*R_{load}} \qquad (2.29)$$

From the above discussion, it is evident that when dealing with non-ideal DC-feed, at angular modulation frequencies Δω, 2Δω, 3Δω, 4Δω etc the baseband impedance is not small (which explains the importance of resonances at high baseband frequency). This will reduce the maximum RF voltage amplitude by increasing ($|Z_{DC\text{-}feed}(\omega_{res})|*|C_n|$). This implies that the bias circuit has to be designed carefully to present low baseband impedance for the maximum achievable RF output power not to deteriorate significantly for realistic modulated signals.

2.3 Investigating Effects of Bias Circuit

In PA design, the performance can be limited by the type of the bias circuit used. The DC feed line impedance can have an adverse effect on the performance of the PA in-terms of RF bandwidth or signal bandwidth. For this reason it is very important to study these effects by using different types of bias circuits. Different biasing circuits are discussed in the next sub topics.

2.3.1 Standard (Conventional)

This drain bias model is the conventional way of biasing a circuit; it is shown in the figure 2.6

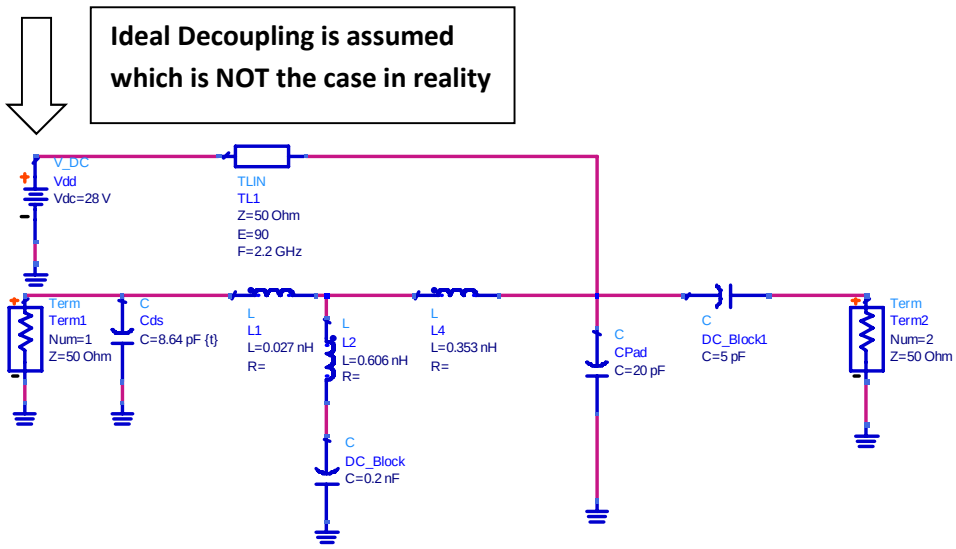


Figure 2.6 Conventional Drain Bias Circuit and RF parts

In figure 2.6, The transistor package represents the drain to source capacitance (Cds), DC-block capacitance(DC_Block), bond wire inductance L2 and L4(for connecting the capacitances), and pad capacitance (used for connecting the out-bond-wire to the external circuit by mechanically holding the package together), mutual inductance L1 between L2 and L4. The values presented here are just an example and RF match is not taken into consideration since that is not the point of this subsection. The terminations in the circuit are inserted just to run S-parameter simulation in Advanced Design System (ADS) and study the bias circuit intrinsic drain impedance. But in reality, L1

together with Cds is connected to the intrinsic drain of the transistor. The right side of the circuit which is terminated with Term 2 is connected to RF match and load. The DC-feed transmission line (TL1 in figure 2.6) gives a short to the power supply V_DC so that DC voltage is feed into the circuit. But it presents an infinite impedance to the point of the matching network where it connects (because "quarter wave" at fc and AC ground termination at other end) so it does not affect the RF performance at f=fc. So this circuit in figure 2.6 is ideal at exactly f=0 and f=fc, but non-ideal in giving non-zero impedance at baseband for f>0 and non-zero admittance for RF not equal to fc.

The circuit in figure 2.6 is simulated and the magnitude of the intrinsic drain impedance was found to look as seen figure 2.7

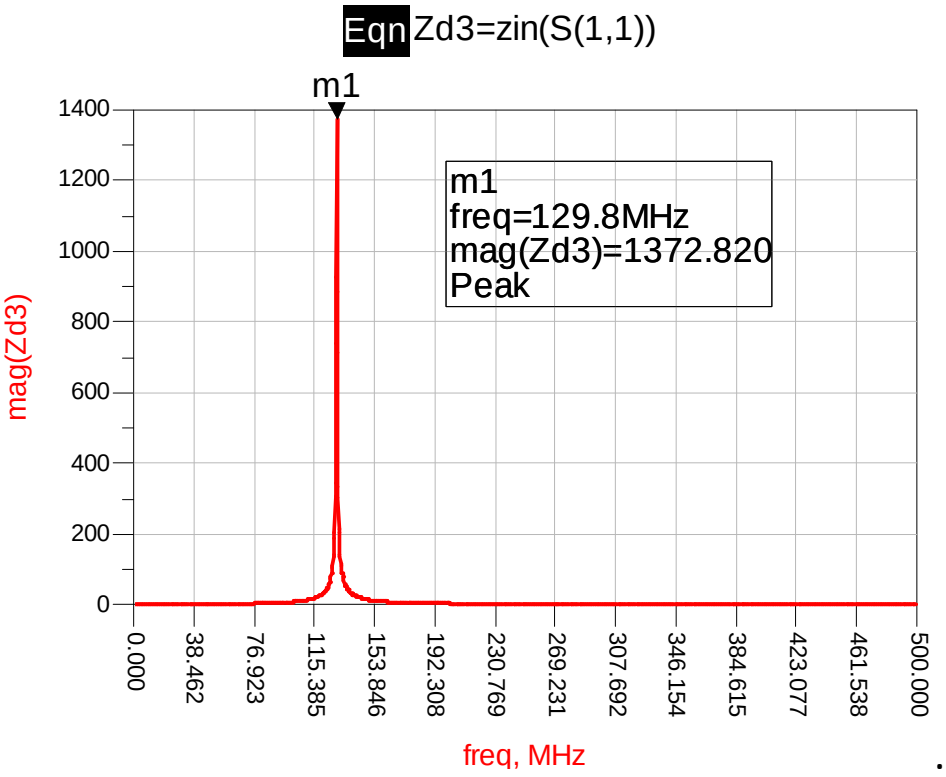


Figure 2.7 Intrinsic Drain Impedance of Conventional Drain Bias Circuit

The quarter wave line low frequency inductance is given by,

$$L_o = \frac{Z_o}{4 * f_c} \tag{2.30}$$

Where, $f_c = 2.14\ GHz$

The low frequency inductance in (2.30) together with the DC-block capacitance (C DC_Block in figure 2.6) gives parallel resonance at

$$f_{res} = \frac{1}{2*\pi\sqrt{L_0 * C\ DC\_Block}} \tag{2.31}$$

As a result in this case f_{res} =129.8 MHz. This is one of the main problems described at beginning where there is not low enough impedance as seen by transistor over large enough base-band frequency. This resonance gives very high baseband termination impedance at frequencies close to the resonant frequency. This in turn can lead to complicated memory non-linearity that not all DPD – linearizers can handle. In the worst case scenario, voltage spikes can lead to transistor breakdown.

2.3.2 Separate DC-feed

In this model DC voltage is supplied by negligible inductance (where the inductance of the line in figure 2.6 is ignored), the circuit model can be seen in figure 2.8,

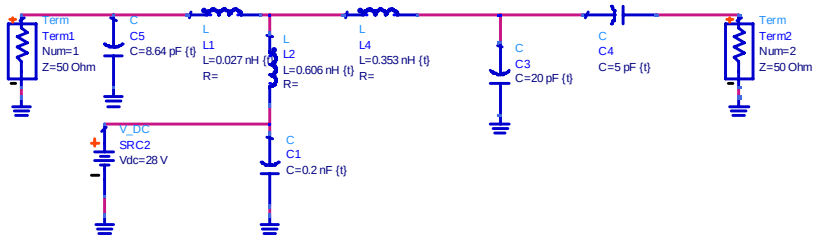


Figure 2.8 Separate DC feed model for Drain Bias Circuit

In figure 2.8 C1 is supposed to be close to ideal DC-block, i.e. the upper terminal of C1 should ideally be at AC ground. So therefore the DC supply can be connected there without disturbing the RF performance of the circuit. That is advantageous at baseband because the low frequency inductance L_0 of the DC-feed transmission line is eliminated. And it is good at fundamental RF because the potentially disturbing admittance the "DC-feed" transmission line contribution at its connection point to the matching network for f not exactly equal to f_c is eliminated.

When simulating the circuit in figure 2.8, the resonance is moved to a higher frequency since the inductance of the transmission line is eliminated. This response is seen in the figure 2.9

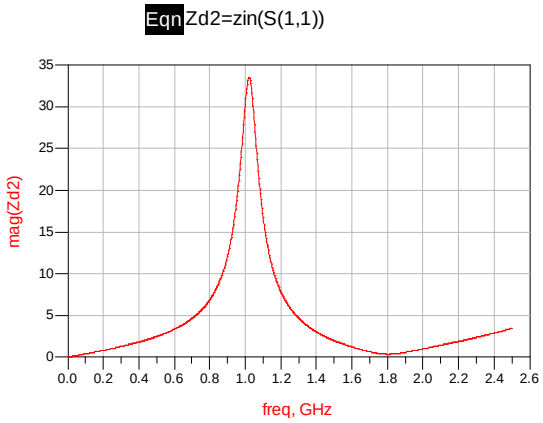


Figure 2.9 Intrinsic Drain impedance of the separate DC-feed bias circuit

The resonance frequency in figure 2.9, which is equal to 1.022GHz, is less of a problem since it's not in the lower baseband frequency region or near to the RF frequency region where the signal spectrum is present. Nevertheless, in practice to keep the lower terminal of L2 at constant potential (at AC ground) is difficult to achieve by connecting to something outside the transistor package due to parasitic inductance in connection. But the grounding of the DC supply almost never is good by itself to keep a good AC ground. That is achieved in practice instead mostly by decoupling capacitors on the PA circuit board (which is briefly discussed in section 3.3.1).

2.3.3 Combined conventional and separate DC feed

In this model, the ordinary quarter wave transmission line Dc supply feed is used. The same basic effect was supposed to be achieved as the circuit of section 2.3.2 by simple taking the decoupling capacitor inside the transistor package and connect it very closely to the lower terminal of L2 to achieve very low parasitic inductance. The circuit to this model is seen in figure 2.10

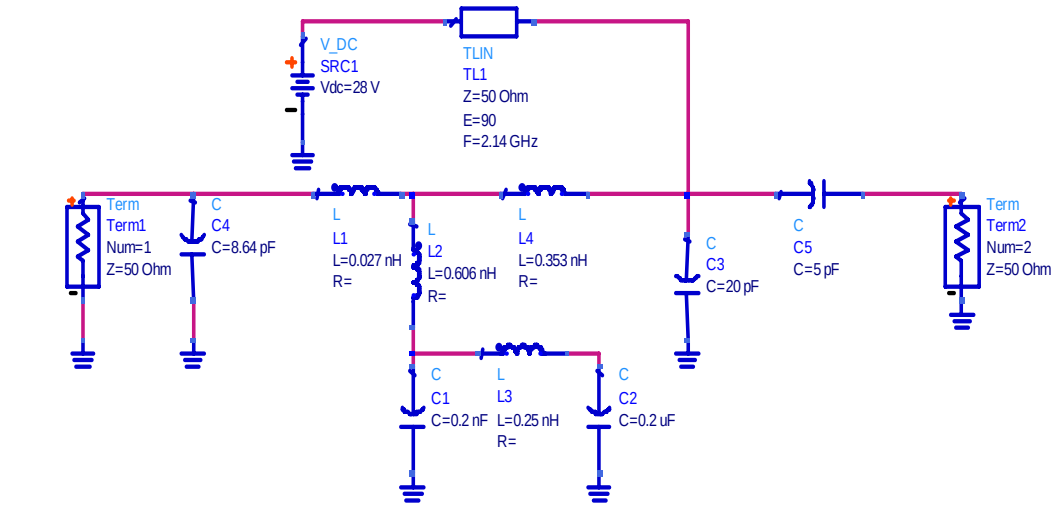


Figure 2.10 Combined conventional and separate DC feed drain bias circuit

By keeping L_0, the low frequency inductance of the DC Feed Line constant, the parallel resonance witnessed in figure 2.7 can be moved to a much lower frequency. The resonance in this case is given by,

$$f_{res} = \frac{1}{2*\pi\sqrt{L_o*C_2}} \qquad (2.29)$$

The resonance at such lower baseband frequency region could be very dangerous, but since L_0 is kept constant and only the decoupling capacitor (C2) is increased to a high value, the reactance ωres*L_0 would be very small so that small resistance might kill it. As a result, the magnitude of intrinsic drain impedance will be much lower than the one witnessed in figure 2.7. The simulated result of the circuit model in figure 2.10 is show below in figure 2.11

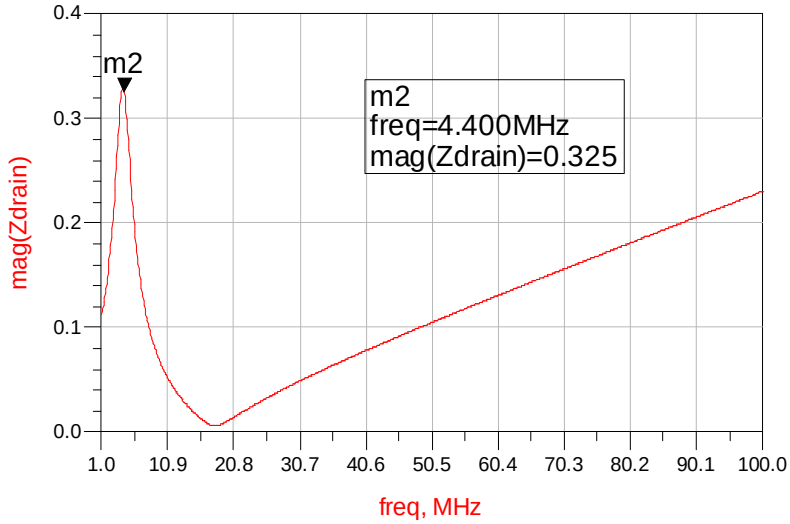


Figure 2.11 Intrinsic Drain Impedance of transistor package with internal decoupling

From figure 2.11 it can be seen that the resonance frequency is at 4.2 MHz which is quite dangerous but as discussed above it can be attenuated by a small resistance. In this case the second terminator (Term 2 in figure 2.10) attenuates the resonance to a smaller value which is 0.3Ω.

2.4 Different Models for Gate and Drain Bias Circuit

After studying the effects of the bias circuit, it was possible to understand the effect the bias circuit has. Then it is necessary to mitigate these effects by studying different Bias circuit models which are discussed in the next sub sections.

2.4.1 A quarter wave transmission line with a snubber resistor

In this model, the DC-feed transmission line TL1 is not connected directly to the transistor part of the circuit but via the resistor R1 that attenuates the baseband resonance. This model looks like shown in figure 2.12

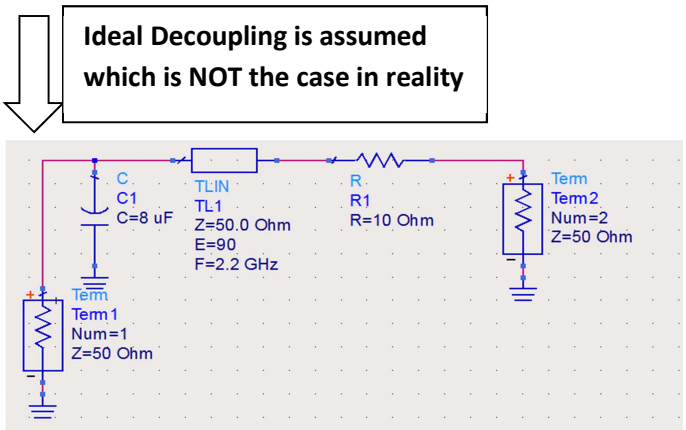


Figure 2.12 Gate Bias Circuit Model I

This type of bias circuit can be used for the gate side but not for the drain because we want extremely low loss on the drain side. The right side of the circuit will be connected to the gate of the transistor and the left side will be connected to a DC source (gate biasing voltage). The Capacitor (C1) will give RF signal ground by presenting a very low reactance. The input gate impedance as seen by the transistor should be very high at the center frequency (f_c =2.2 GHz), since the quarter wave transmission line will present infinite impedance when seen from the transistor. But here in this model only the impedance at the center frequency is kept at infinity but it is also necessary to have a zero impedance at f=0. The least impedance seen at 0 Hz in this model is the series snubber resistor 10Ω which can cause dissipation but since there is not much current on the gate side the dissipation is negligible. The simulated result of the DC-feed impedance is shown in figure 2.13

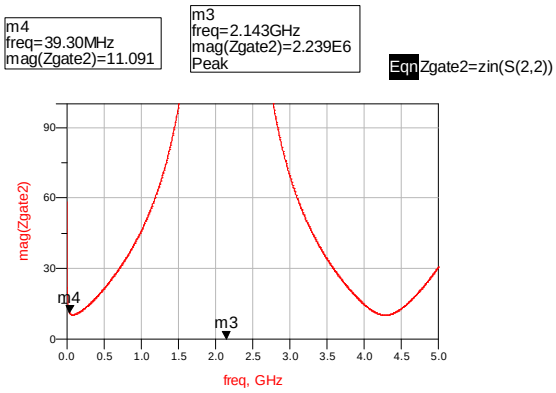


Figure 2.13 Gate Impedance seen from the transistor

As described above we see very high impedance at the center frequency which is desirable not to affect the RF match. Also the least absolute magnitude of impedance we have at the lower frequency is equal to the order magnitude of the snubber resistor. Note that figure 2.13 is not the same type of result as presented in figures 2.7, 2.9, 2.11 since for the latter are the whole drain circuit.

2.4.2 Two quarter wave transmission lines in parallel and Snubber resistor in series

This model can be used both for the gate and drain biasing. In this model, two quarter wave length transmission lines are used and one transmission line is in series with the snubber resistor. The model seen in section 2.4.1 is actually a special case of this model with the parallel transmission line (TL2) characteristic impedance equal to infinity. The circuit model of this circuit can be seen in figure 2.14, in this model also ideal grounding is assumed which is not the case in reality and different decoupling capacitors should be used.

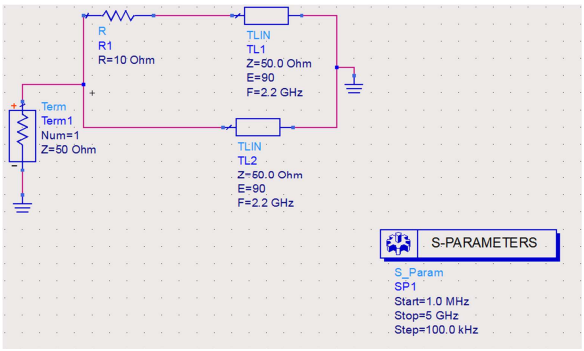


Figure 2.14 Gate and drain bias circuit model II

Here the second transmission line presents a zero impedance path for the DC, which means there is 0 Ohm impedance at 0 Hz. In addition, the snubber resistor with the first transmission line attenuates the baseband resonance. As the case in model one, the first and second transmission lines present infinite impedance at the center frequency. The model in figure 2.14 was simulated and the impedance as seen from the gate or drain of the transistor was plotted. This plot can be seen in figure 2.15

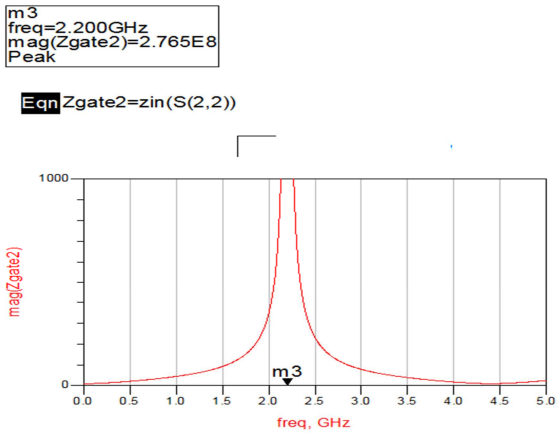


Figure 2.15 Gate or drain Impedance as seen by the transistor

We can see that when using two transmission lines, the impedance at the 0 Hz frequency is zero and infinite impedance is kept at the center frequency. Again note that figure 2.14 is not the same type of result as presented in figures 2.7, 2.9, 2.11 since for the latter are the whole drain circuit.

Chapter 3

3. Design Method

For the design of RF PAs to experimentally test different bias circuits, two models of packaged RF power transistor were available. These were identical except that one had internal drain baseband decoupling and the other not. Both were internally pre-matched Si LDMOS transistors designed mainly for class AB operation in the 1.8 GHz band. The nominal maximum output power was 140 W at a nominal drain bias voltage of Vdd = 28 V. One PA was designed from each transistor model, with an attempt to optimize the bias circuits as much as each transistor package model and the limited data available allowed. The optimization aimed particularly at minimizing the impedance presented to the intrinsic drain and gate as much as possible over as large base-band-width as possible. Although the focus was placed on the base-band-width, some attention was also directed to the RF bandwidth. This, however, seemed to be rather limited by the package, and rather insensitive to the exact matching and bias circuits used which was proved by simple and very rough studies carried out.

The transistors were prototype designs without product numbers. No transistor package models become available during the design work. Therefore the design was based entirely on measurements; Load-pull measurements for RF match designs, and simple low-frequency measurements of capacitance on the transistor package terminals for a simple very approximate assessment of resulting impedance presented to intrinsic gate and drain at low base-band frequency. Only two copies of each transistor model were available. For this reason the design was made for a somewhat reduced Vdd = 26 V in order to reduce the risk of transistor failure.

For reference also a design using a traditional non-optimized drain bias network was made for the transistor with and without internal base-band decoupling which is not analyzed due to lack of time.

3.1 Load Pull Measurement

As discussed in the beginning of chapter 3, the transistor package information was lacking so a Load/Source Pull measurement was performed. The objective is to determine optimal impedance presented to the external gate and to be presented to the external drain, at RF (1.8 GHz). This measurement will help prove if the two transistors (with and without internal decoupling) has the same performance at RF so that the analysis at baseband becomes fair enough. The measurement principle for the Load/Source pull measurement is shown in figure 3.1

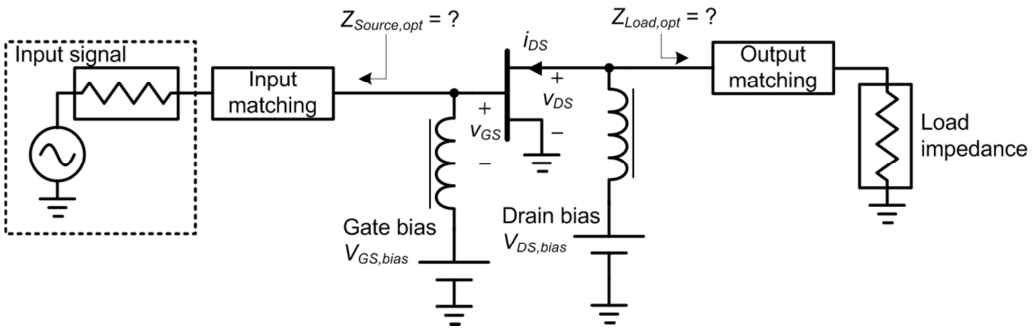


Figure 3.1 Load/Source Pull Measurement Principle [2]

In this measurement it is possible to see the preferred load and source impedances to present to the transistor package terminals. Once these impedances are known, then the PA design is based on these values. The measurement setup can be seen in figure 3.2

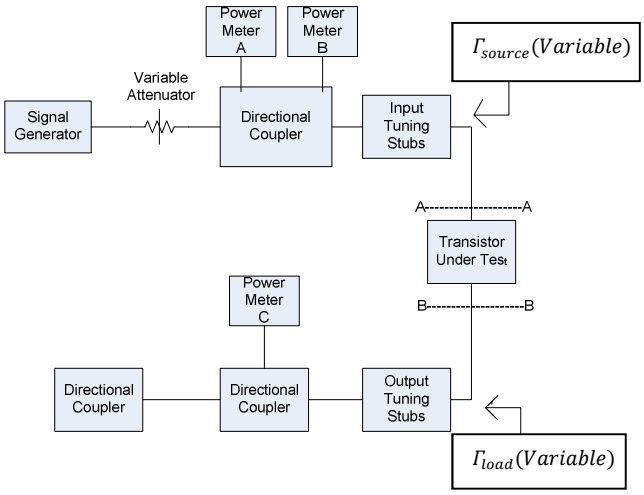


Figure 3.2 Load/Source Pull measurement setup [8]

During the measurement, frequency was swept (1780-1900) MHz, RF input Power (pulsed with 10% duty cycle and 10 µs pulse width) was swept from 25 dBm until 3 dB compression is achieved. Gain, Efficiency and RF output power were studied. Since there is no model given for the transistor, different Vg were swept to see the performance (I-V curve) of the transistor. The I-V curve is shown in figure 3.3

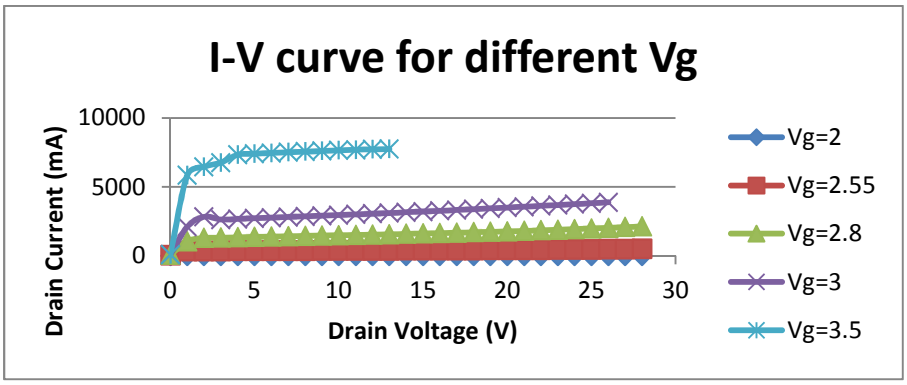


Figure 3.3 Transistor Operating Region

An abrupt change can be seen in the I-V curve when switched from 3V to 3.5V. Since the number of transistors are limited, it was preferred to run the transistor with bias level Vg=2.55V and Vdd=26V.

Load/Source Pull Measurement results for the transistor with internal decoupling were recorded for best power and best efficiency. This is shown in table 3.1 and 3.2

Frequency (MHz)	Vdd (V)	Idq(mA)	Zload(Ω)	Zsource(Ω)	Pout (dBm)	Gain (dB)	Effi (%)
1780	26	450	0.89-j2.09	1.23-j4.25	52.6	13.5	57.6
1805	26	450	1.01-j2.2	1.37-j4.61	51.8	13.81	45.1
1845	26	474	0.89-j2.1	1.59-j5.02	52.7	14.08	51.6
1880	26	474	1.11-j2.29	1.95-j5.84	52.5	14.75	59.6
1900	26	474	1.06-j2.31	2.61-j6.15	52.2	14.74	49.2

Table 3.1 Load/Source pull results for the transistor with internal decoupling optimized for best power at 3-dB compression

Frequency (MHz)	Vdd (V)	Idq(mA)	Zload(Ω)	Zsource(Ω)	Pout (dBm)	Gain (dB)	Effi (%)
1780	26	450	1.71-j1.23	1.23-j4.25	50.5	13.5	57.6
1805	26	450	3.37-j0.67	1.37-j4.61	50.1	13.81	58.4
1845	26	474	1.26-j1.29	1.59-j5.02	51.8	14.08	59.4
1880	26	474	2.1-j0.8	1.95-j5.84	50.4	14.75	59.9
1900	26	474	1.86-j1.32	2.61-j6.15	51.04	14.74	57.9

Table 3.2 Load/Source pull results for the transistor with internal decoupling optimized for best efficiency at 3-dB compression

From table 3.1 and 3.2, it can be seen that when going for the best power at the frequency very close to the center frequency (1805 MHz), the efficiency is degraded significantly. But when choosing the impedance for the best efficiency, the power drop is only 2 dB. Because of this, the PAs were designed for best efficiency. The recorded Load/source measurement results for the standard transistor for best power and efficiency are shown in Table 3.3 and Table 3.4 respectively

Frequency (MHz)	Vdd (V)	Idq(mA)	Zload(Ω)	Zsource(Ω)	Pout (dBm)	Gain (dB)	Effi (%)
1780	26	450	0.9-j2.2	1.18-j4.18	52	14.2	43.8
1805	26	450	0.91-j2.26	1.34-j4.53	51.24	14	44.6
1845	26	474	0.89-j2.38	1.51-j4.55	52.1	13.26	43.6
1880	26	474	1.06-j2.3	2.01-j5.55	52	13.89	48.4
1900	26	474	0.9-j2.42	1.93-j5.81	51.7	14.35	41.9

Table 3.3 Load/Source pull results for the standard transistor optimized for best power at 3-dB compression

Frequency (MHz)	Vdd (V)	Idq(mA)	Zload(Ω)	Zsource(Ω)	Pout (dBm)	Gain (dB)	Effi (%)
1780	26	450	1.98-j1.51	1.18-j4.18	51	14.2	61.4
1805	26	450	2.07-j1.39	1.34-j4.53	50.5	14	58.2
1845	26	474	1.9-j1.84	1.51-j4.55	50.7	13.26	56.4
1880	26	474	2.05-j1.05	2.01-j5.55	49.5	13.89	54.1
1900	26	474	1.87-j1.77	1.93-j5.81	50.4	14.35	53.9

Table 3.4 Load/Source pull results for the standard transistor optimized for best efficiency at 3-dB compression

From the above four tables it can be verified that both transistors (standard transistor and transistor with internal decoupling) have the same RF performance. Also it can be seen that the source impedances of both transistors are quite similar. This confirms the information given from the manufacturer that the two models are identical except for internal decoupling on drain. From the above four tables, table 3.2 and table 3.4 are the ones used which are optimized for best efficiency. The preferred impedances and the corresponding expected RF performance for designing goal is listed below,

Preferred Optimal Measurement results for $f = 1805\ MHz$:

Transistor Type	Zext,drain (Ω)	Zext,gate(Ω)	Power(dBm)	Efficiency (%)	Gain (dB)
Internal Decoupling	3.37-j0.67	1.36-j4.57	50	58.5	14
Standard	2.07-j1.39	1.36-j4.57	50	58	14

Table 3.5 Preferred Optimal Measurement results used to design PAs

From table 3.5, it can be seen that the design impedance value used for the transistor with internal decoupling is quite different from other values in table 3.2. This is because the efficiency contour was quite wide which gives large range of impedance values. Also, the external gate impedance is computed by taking the average between 1.37-j4.61, Gain=13.8dB, for internal decoupling and 1.34-j4.53, Gain 14dB, for standard transistor.

3.2 Drain and Gate Capacitance Measurement

Since transistor model is not given from the manufacturer, the gate-source and drain-source capacitances were measured using a multi-meter. The measurement setup is shown in figure 3.4 below,

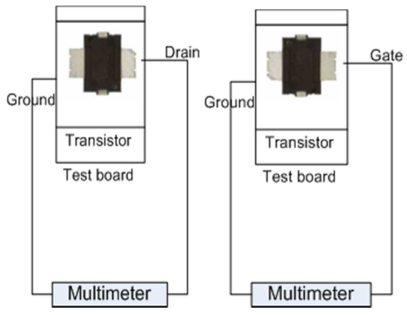


Figure 3.4 Drain and Gate Capacitance measurement setup

Both transistors with and without internal decoupling were measured. The measured values are the same for the two transistors on the gate side. But for the drain side, as expected the capacitance for the one with internal decoupling was much higher.

3.3 Drain and Gate Circuit Design

The drain and gate circuits have been designed and optimized using the following three goals

- 1. DC-feed line presenting a very high impedance to the transistor at f_c so that the bias circuit does not affect the RF performance
- 2. Get the RF match to the chosen impedances from Load/Source pull, the RF performance characterization cannot be achieved without having a good match at $f = f_c$
- 3. Low enough impedance as seen by intrinsic drain or gate over large enough base-band-width.

3.3.1 Non-Ideal decoupling of DC-Feed

When analyzing the effects of different bias circuit, an ideal grounding was used which is short circuit at any frequency. But that is not the case in reality. Due to this, designing a non ideal grounding for the DC-feed was necessary. It is not possible to decouple all frequencies with only one capacitor so three capacitors were used for this purpose. There is of course a problem when combining several capacitors together that the parasitic inductances will create a parallel resonance that will give very bad decoupling in a frequency region close to resonance. First capacitor, for decoupling of the RF frequency (Murata Ceramic Capacitor, 15pF, 250V ,has series resonance at the center frequency). Second one for decoupling of the high baseband frequency (Murata Ceramic Capacitor, 10 uF, 50V) is used. Third one, for the low baseband frequency, this capacitor model was designed using ADS so that it can give very low reactance to the very low frequencies. The design model is shown in figure 3.5. The overall circuit design was symmetric configuration. The symmetric configuration is that not only one of those basic three capacitor decouplings, but two are placed symmetrically on the microstripline. Two such decouplings symmetrically are placed on the outer end of each DC-feed quarter wave microstripline. And then two DC-feed quarter wave line-units (consisting of two quarter-wave lines at drain, one of them with snubber resistor, and each decoupled at the other end as described above) placed symmetrically on the microstripline connecting to the transistor package. So this will reduce effectively parasitic series inductance and series resistance to half twice, effectively resulting in a reduction to one quarter of that of one single three-different capacitor unit. Even though that was the original intention, later due to practical difficulties this is done only for the 15 pF and 10 µF capacitors. Further advantages of this configuration includes: Parasitic resistance and inductance can be reduced by half, current crowding can be reduced. This configuration is the only way which alleviates the probability of extra resonances.

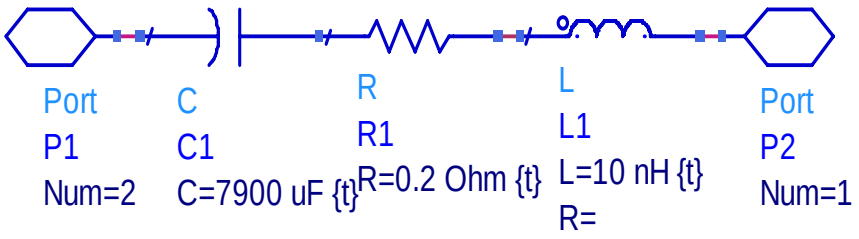


Figure 3.5 Electrolytic Capacitor Model

In figure 3.5, all model values were tuned to get as good fit to reality as possible but while doing so problems might occur since the capacitor models designed by manufacturers is more complicated than this. But this model was good enough to use it in simulation.

The circuit diagram for non-ideal decoupling can be seen in figure 3.6

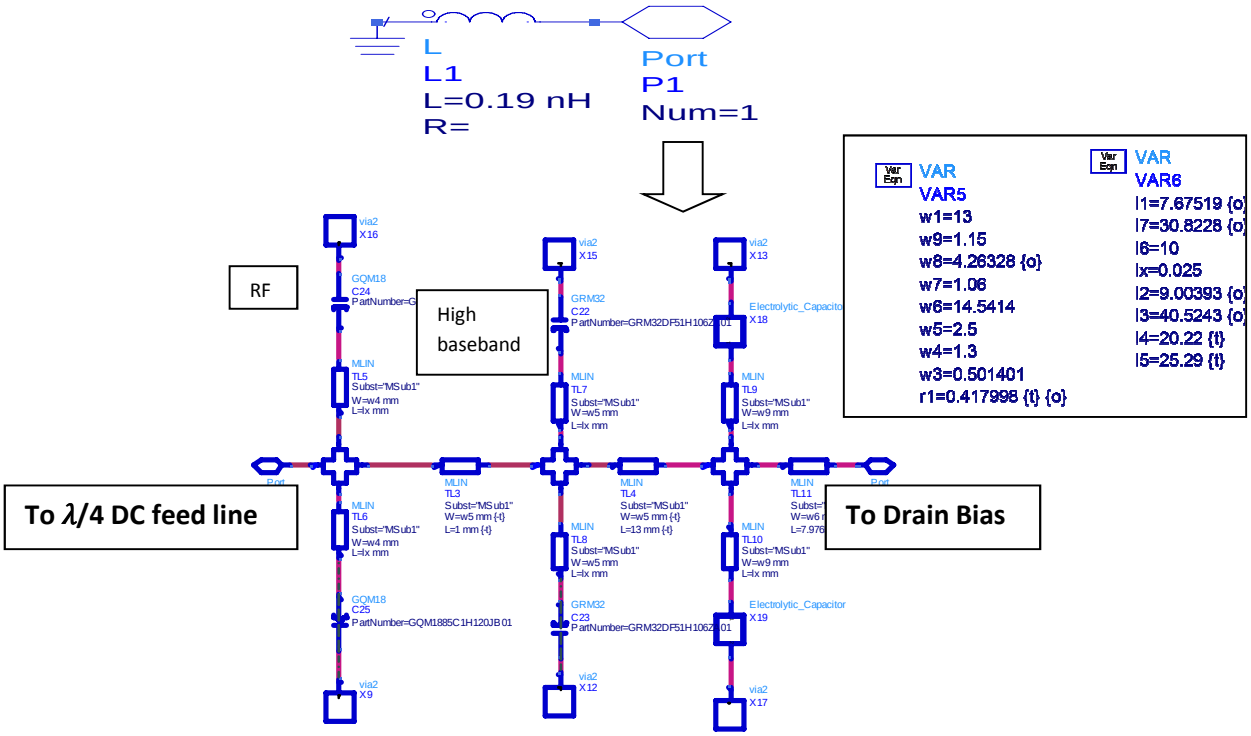


Figure 3.6 Non-ideal Decoupling Circuit Diagram

In figure 3.6, the vias were modeled using inductance to ground. The actual inductance value was finally computed from the Electromagnetic Simulation (EM) using momentum in ADS. The two capacitors GQM21 and GRM32 are the Murata capacitors described in the first paragraph of this section which are taken from Murata's model library. The electrolytic capacitor is the model shown in figure 3.5. The simulation result for the circuit shown in figure 3.6 is shown in figure 3.7

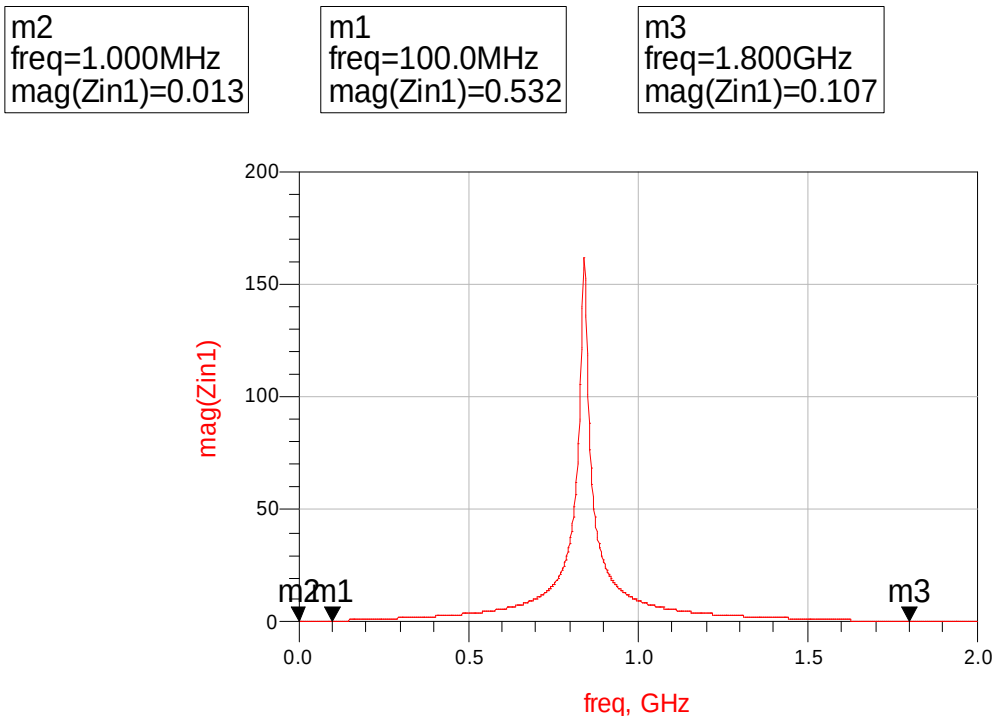


Figure 3.7 Simulation Result for Non-Ideal Decoupling

From the simulation result it can be seen that the non-ideal decoupling gives low enough impedance to all relevant frequencies. This will isolate the PA from its power supply (PA only gets DC power from the power supply)

3.3.2 Drain and Gate Circuit

3.3.2.1 Drain Circuit

The drain bias circuit discussed in section 2.4.2 is used for the design of these PAs. The length and the width of the two microstrip lines (TL1 and TL2) were optimized so that they can be a λ/4 line at f_c=1.8 GHz presenting very high impedance as seen from the transistor. The drain and gate circuits for the transistor were designed separately. Symmetric configuration is used for the reason explained in section 3.3.1 and the overall drain circuit is shown in figure 3.8,

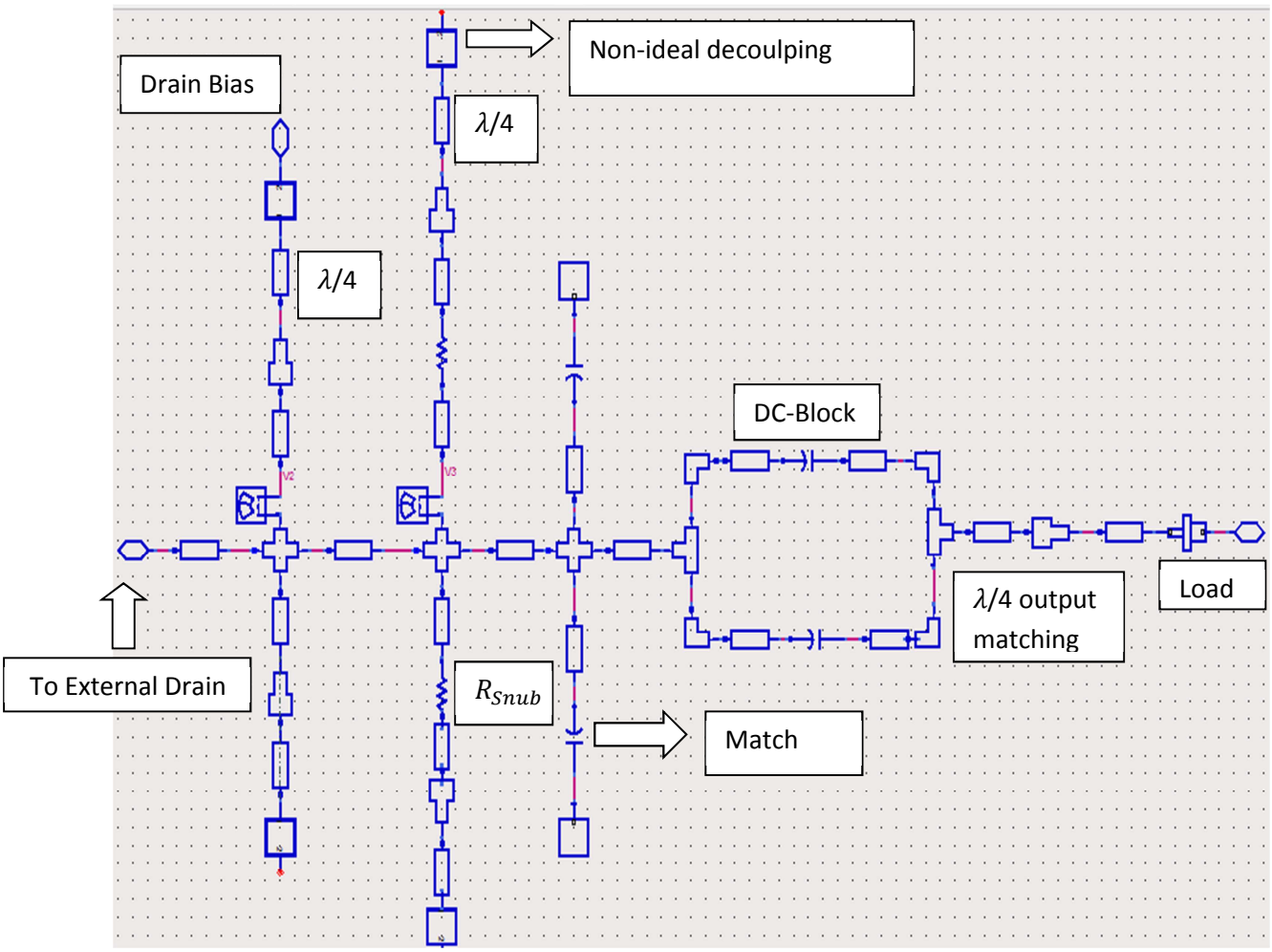


Figure 3.8 Drain circuit schematic

The drain circuit schematic seen in figure 3.8 is used for both transistors, but the actual values are different, obtained by using the same goal discussed in section 3.3. The left side of figure 3.8 will be connected to the external drain of the transistor and the right side will be connected to the 50 Ω load. The width of the microstrip line to the external drain was carefully optimized so that the minimum width value should be greater than or equal to the width of transistor lead. This was done to make sure that the transistor lead fits perfectly on the microstrip line by having few mm higher margins.

For the transistor with internal decoupling, the width of the bias line without the snubber resistor after optimization using ADS was 0.5 mm and for the one with snubber resistor it was 9.32 mm. For the standard transistor, 6.485 mm and 7.91 mm were obtained for the quarter wave line without and with snubber resistor respectively. The characteristic impedance of both lines for the two different transistors can be analyzed using the standard idealized formula [4],

$$Z_0 = \frac{t}{w}\sqrt{\frac{\mu_0}{\varepsilon_0 * \varepsilon_r}} \qquad (3.1)$$

where, t=substrate thickness 0.508 mm, w=width of the microstrip line, μ_0=permeability constant of vacuum π*4e-7 Vs/(Am) and ε_0=dielectric constant of vacuum=8.854e-12 As/(Vm), ε_r= relative

dielectric constant=3.66. The idealized formula gives a good accuracy if t is much smaller than w which is not the case here. But it would be interesting to compare these results with the linecalc functionality present in ADS (opposite to 3.1 where impedance is given to calculate the width). For all the design the substrate used was Rogers 4350, which is shown in figure 3.9

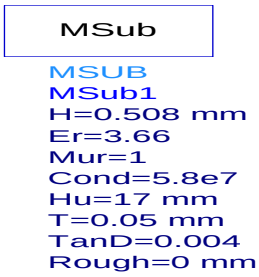


Figure 3.9 Substrate definition for Rogers 4350

The characteristics impedances of the DC Feed lines for the transistor with internal decoupling was $Z_{0,without,snubber}$=73Ω with linecalc (200Ω when using equation (3.1)) $Z_{0,with,snubber}$=9Ω with linecalc (10.7Ω when using equation (3.1)). The value of the optimum snubber resistor used to find the smallest possible absolute magnitude of the resonance was $R_{snubber}$=0.42 Ω . For the standard transistor, $Z_{0,without,snubber}$=13Ω with linecalc (15.42Ω when using equation (3.1)), $Z_{0,with,snubber}$=10.7Ω with linecalc (12.6Ω when using equation (3.1)) and $R_{snubber}$=8.4 Ω. From the above it can be seen that for t much smaller than w the results between the idealized formula and linecalc are close enough. Whereas, when t and w are close then the results are very different.

For matching and DC-block Murata library model capacitors were used. For the transistor with internal decoupling GQM1885C2A2R0CB01 (0603, 2pF, 100V) was used for matching and GQM2195C2A3R0CB01 (0805,3pF, 100V) was used as dc-block. For the standard transistor, GQM1885C2A2R3CB01 (0603, 4.3pF, 100V) was used for matching and GQM2195C2A6R8DB01 (0805, 6.8pF, 100V) for DC-block. The layout of the drain circuit for both transistors is shown in figure 3.10 and figure 3.11

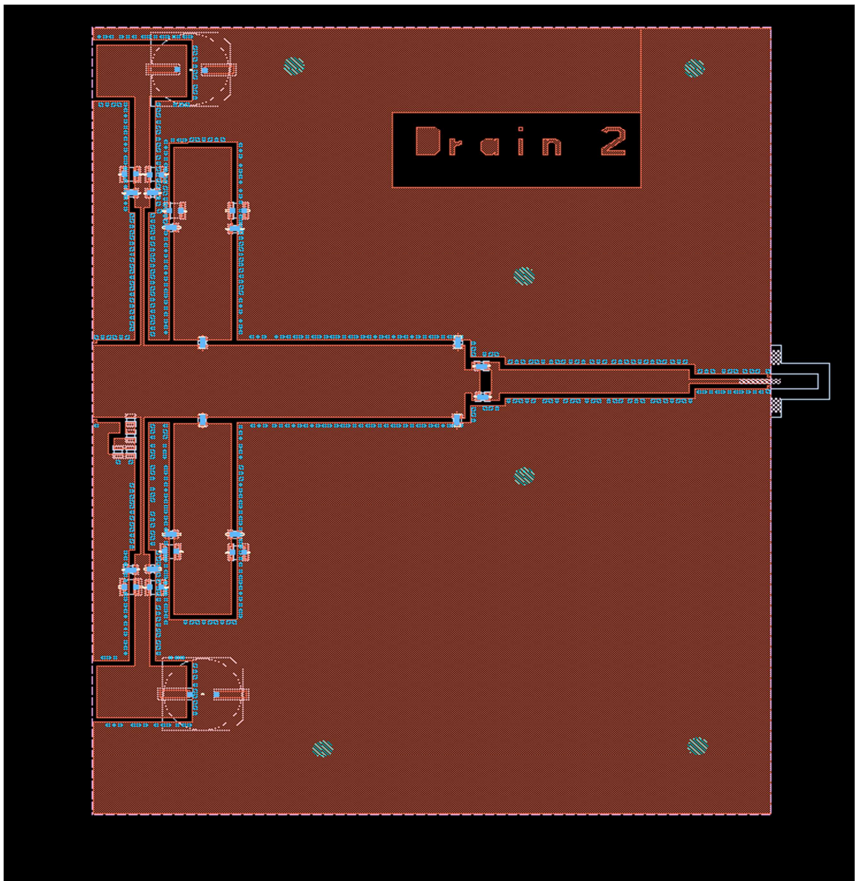


Figure 3.10 Drain circuit Layout for the transistor with Internal Decoupling

The optimization goal is described in section 3.3. Each goal was implemented in ADS. For the first goal, the minimum value of the impedance magnitude was set to 500 Ω with no limitation to the maximum which will be considered as open at the center frequency. For the second goal, the load pull real and imaginary impedance values from (table 3.5) were set on the goal with ± 0.1 for maximum and minimum values respectively. For the third goal, the minimum intrinsic impedance was set to 0Ω and the maximum to 0.1Ω over the whole baseband frequency (0 to 500 MHz). Goal 1 and goal 2 were satisfied 100 % except Goal 3 but the values obtained are the minimum possible. From the load-pull, a few very oversimplified/idealized match designs were made. Which was like simple shunt capacitance match and series capacitance match, not yet including bias circuits and not yet necessarily DC block and not yet necessarily going to the finally wanted impedance level, but just going to some simple purely real-valued impedance. By comparing the impedance obtained in a few idealized matching circuits and the impedance the transistor package should see according to load-pull a very first, very crude estimate of RF band-width is done. This turned out not too good, but at least some ~50 MHz. The DC feed line without snubber resistor has much higher characteristic impedance and thus much higher baseband inductance than the line with snubber resistor. The resonance impedance will be the parallel combination of the inductance of the snubber line in series with the snubber resistance, the package capacitance and inductance of the line without snubber resistor. Since the inductance of the line with snubber resistor is much smaller, a reasonable approximation at the baseband resonance should probably be the parallel combination of the snubber resistance, the package capacitance, and the inductance of the line without snubber

resistor. The absolute magnitude of this resonance impedance will thus be order of the snubber resistor. At low frequency the line without snubber will short circuit the line with snubber resistor since the flow of current chooses the path with least impedance. At the center frequency, both quarter wave DC feed lines will present an open towards RF match. Due to this reason, ideally there should not be any loss in the snubber resistors used at the second DC Feed line for both transistors.

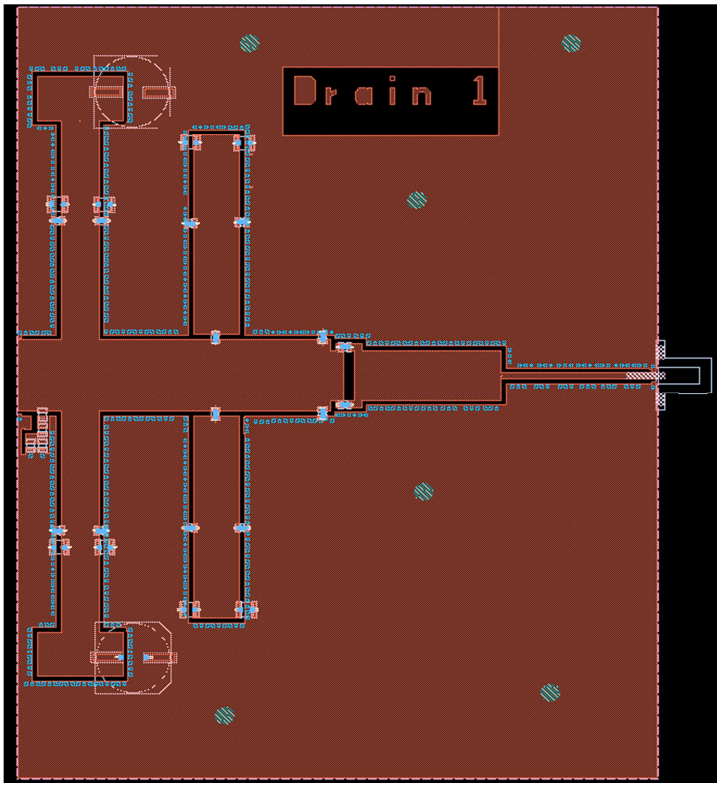


Figure 3.11 Drain circuit Layout for the standard transistor

For the drain bias circuit of the standard transistor, the DC feed line without snubber resistor is expected to have lower characteristic impedance for better base-bandwidth by increasing the resonance frequency. The performance of the dc feed lines with and without snubber resistor are the same as discussed for the transistor with internal decoupling.

3.3.2.2 Gate Circuit

According to transistor manufacturers which is consistent with load-pull measurements and package low-frequency capacitance measurements on gate, the two transistors types differ only with the high capacitance decoupling at the drain side on one of the transistors. For this reason, same gate circuit design was used for both transistors. The schematic circuit design is shown in figure 3.12

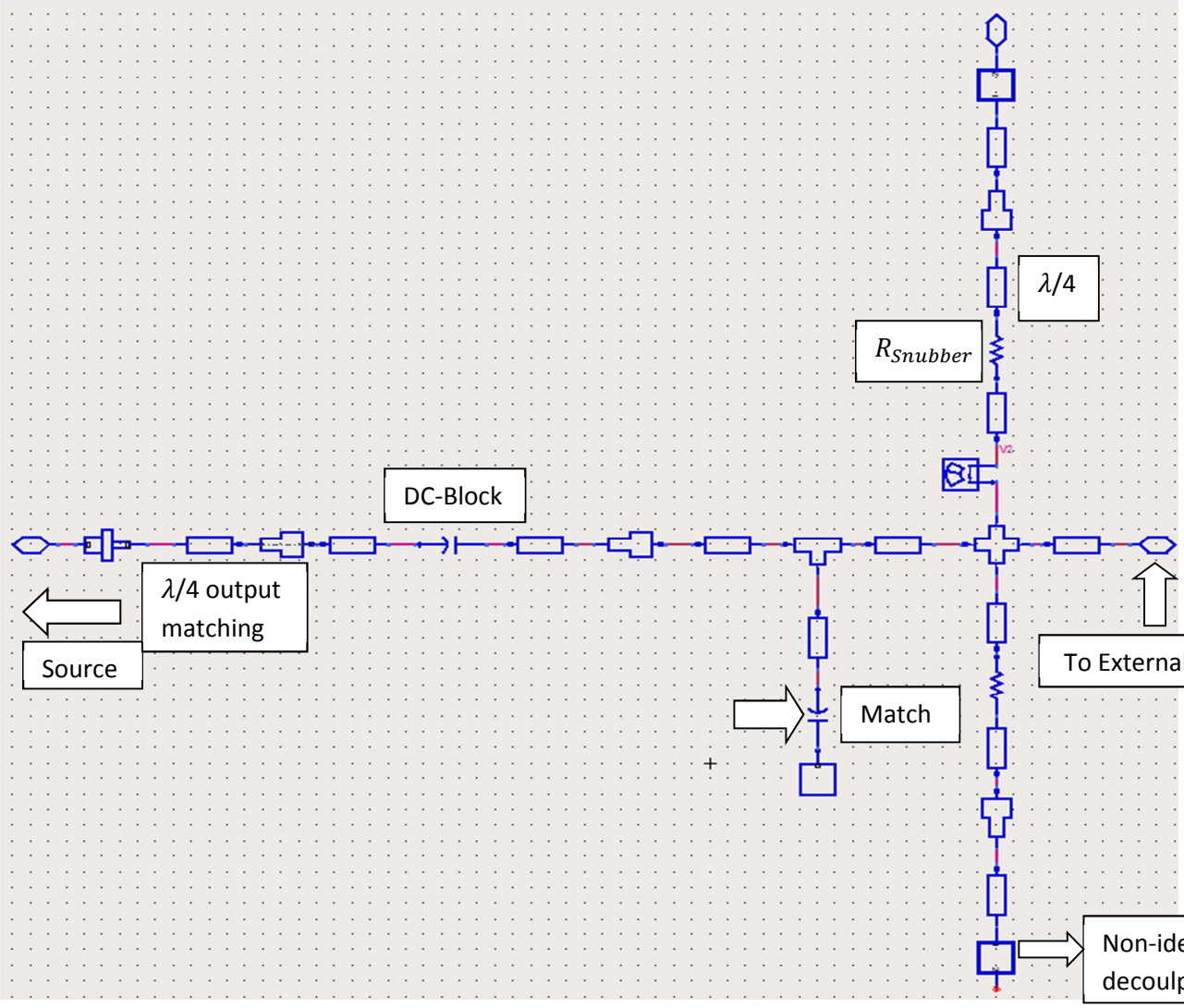


Figure 3.12 Gate Schematic Circuit Design for both transistors

The width of the quarter wave line is 8.9 mm and this corresponds to a characteristics impedance of Zdc-feed,line=9.5Ω with linecalc (11.2Ω when using equation (3.1)). The optimum snubber resistor value used for the least possible baseband resonance impedance was 6.6 Ω. This resistor is expected to have low dissipation in it since we don't have high current on the gate side. The right side of Figure3.12 will be connected to the external gate of the transistor and the left side will be connected to the generator (source). Here also, the width of the microstrip line to the external gate was carefully optimized so that the minimum width value should be greater than or equal to the width of the transistor lead. This gate circuit is designed with same principles and goals as for the drain.

3.3.2.3 Impedance measuring board

The design of both PA is based on the goal discussed in section 3.1. So in order to make sure if the impedance of the boards are the same as the simulation, another three impedance measurement boards were designed for the two drains and for the common gate. Each of the boards have two 50Ω SMA-connector ports. One port connects to an impedance transformer that transforms the 50 Ω (line width 0.5 mm) to the impedance 6 Ω corresponding to the line width (13 mm) of the transistor leads. The low-impedance end of the transformer connects to the external drain (or external gate) reference plane. The other SMA port connects to this reference plane from the other direction via the same drain (or gate) circuit as used in the PAs (the part of the drain or gate circuit external to the transistor package). In order to characterize this transformer (and including connector) and de-embed it in VNA measurement, Thru, Line, Reflect (TRL) boards were designed. The thru connection is made by directly connecting the two identical transformers at the desired reference plane. The reflect connection uses a load having a large reflection coefficient such as a nominal open or short. The line connection involves connecting the two identical transformers together through a length of matched transmission line [3]. The layouts for the impedance measurement boards and for the TRL lines are shown in figure 3.13 and figure 3.14

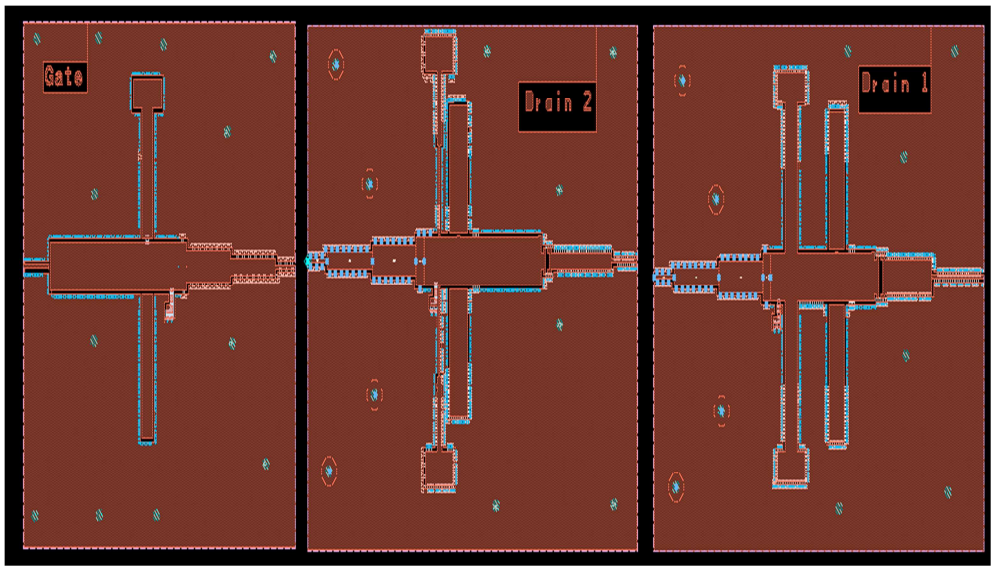


Figure 3.13 Impedance measuring boards for the gate and drain of both transistors

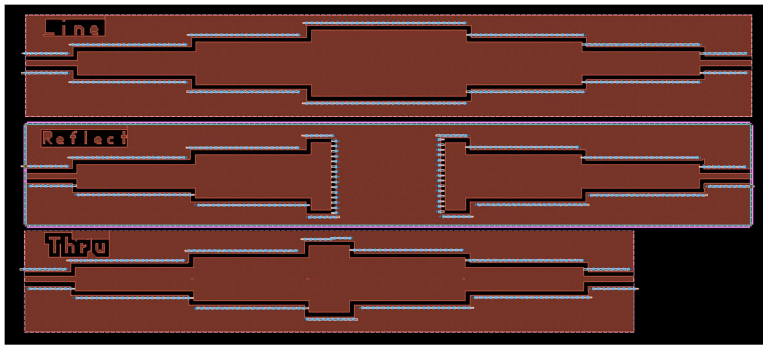


Figure 3.14 TRL structures

Chapter 4

4. Simulation and Measurement Results

4.1 Simulation Results

The simulation process was taken in two steps. First the circuit design was simulated to lead to a close enough approximation to the Electromagnetic (EM) simulation. Second Electromagnetic simulation was carried out using momentum in ADS which gives close enough approximation to reality. As described in section 3.3.2.1, the drain and gate circuit are designed and simulated independently. The simulation setup for the drain circuit of both transistors is shown in Figure 4.1

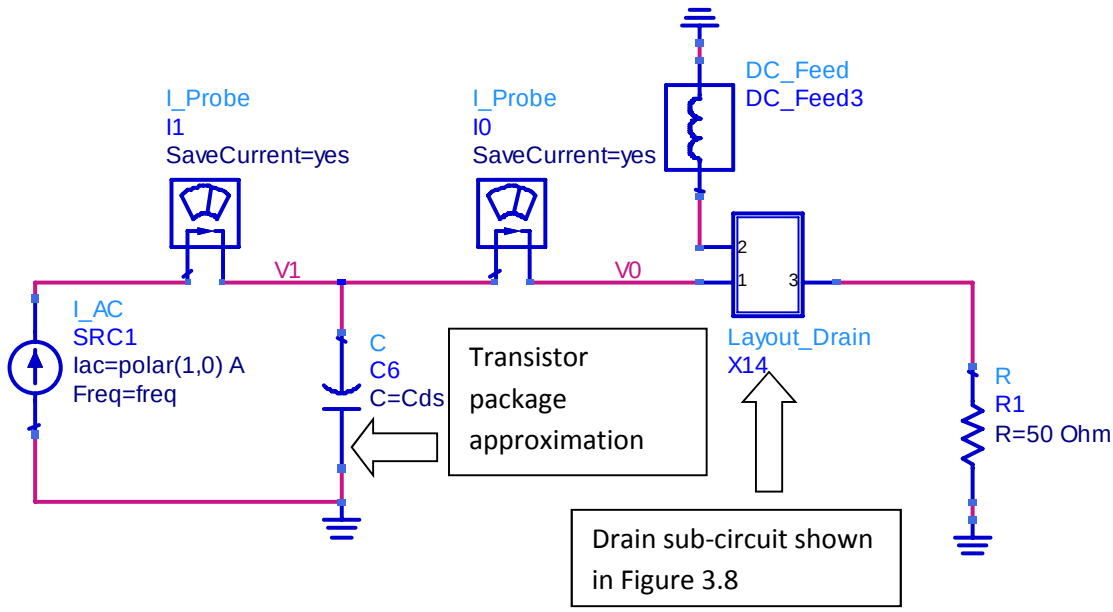


Figure 4.1 AC-Simulation setup for drain circuit of both transistors (the transistor package circuit model is expected to be valid approximately at low frequency)

AC simulation was performed in order to see different impedance levels in different parts of the circuit. The impedance Z1 (=V1/I1) represents the impedance seen from intrinsic drain of the transistor, Z0(V0/I0) represents the impedance seen from the drain reference plane of the transistor package and Z2 (=V2/I2) which is on figure 3.8 is the impedance looking into the $\lambda/4$ DC-Feed line.

It is of course not accurate to just approximate the transistor package by just capacitance at high frequency since the inductance of the bond wires is important at higher frequencies. For RF that is not a problem since from load-pull the impedance that ought to be presented to the package (Z_0 in this simulation) is known. But for the baseband performance evaluation, however, the best that can be done with the data available is to use the total capacitance value in an approximation for the impedance seen by intrinsic drain (Z_1 in this simulation). This is expected to be reasonably accurate at low frequency, even though a problem here is that there is no data available to estimate how low frequency is necessary for the approximation to neglect inductances (and resistances) of the package to remain reasonably accurate.

The same simulation control with only slightly different setup is used for the gate. For instance, Cds is replaced by Cgs, Rload should be replaced by Rgenerator .After the circuit simulation, EM simulation was performed by using the Rogers 4350 substrate model as described in section 3.3.2.1 and a component was created by using the EM dataset so that the model can be simulated and compare the results with the circuit model.

The simulation results comparing circuit and Momentum simulation for all the three impedances described above for the transistor with internal decoupling is shown in figure 4.2, 4.3 and 4.4

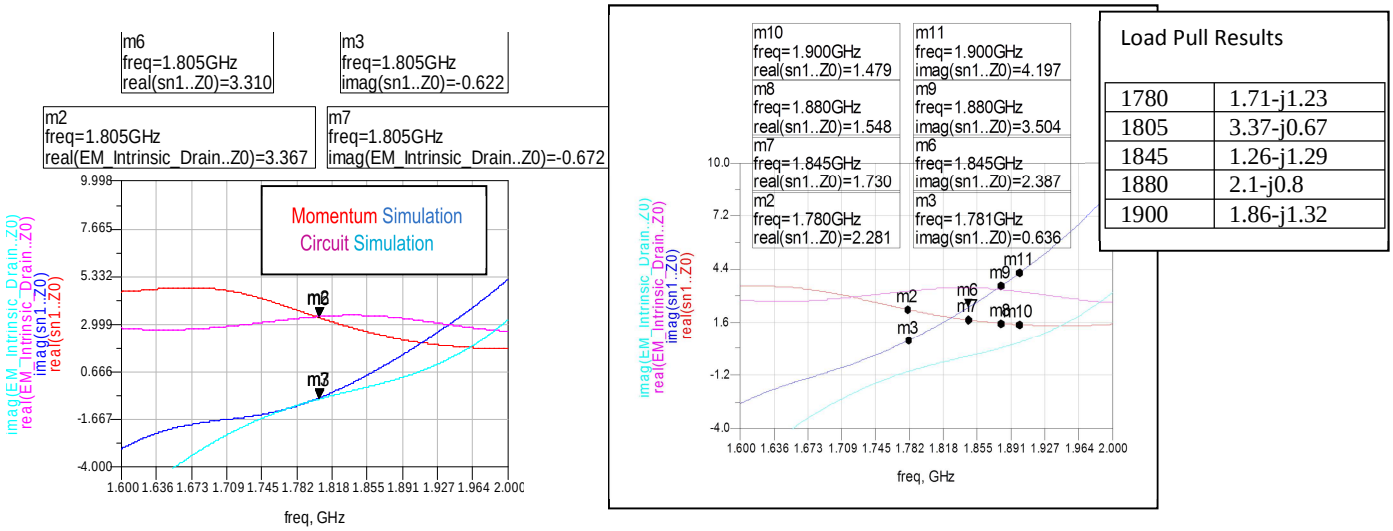


figure 4.2: RF impedances as seen from external drain transistor package with internal decoupling

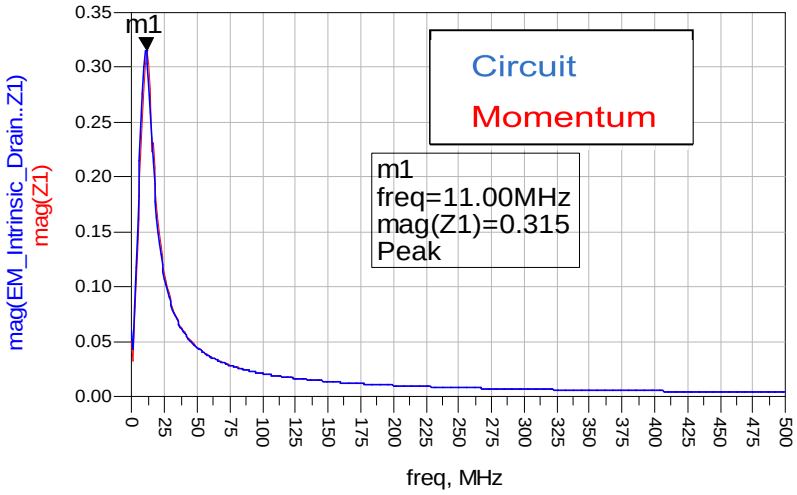


Figure 4.3 Baseband impedance seen from intrinsic drain

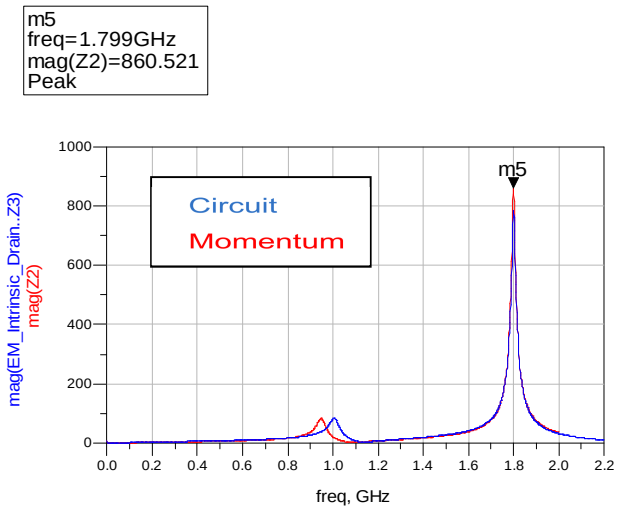


Figure 4.4 DC-Feed impedance seen from the transistor external drain

For the RF match the design goal is Zext,drain=(3.37-j0.67)Ω from the load-pull. From the simulation results (figure 4.2) it is evident that the result obtained is quite the same. But for the other Load Pull frequencies the values are quite different since the optimization is only done at 1805 MHz. For the baseband impedance (figure 4.3) it can be seen that the least possible impedance peak obtained was 0.3 Ω. The impedance seen into the DC-Feed line (figure 4.4) from the external drain approached close to infinity at 1.8 GHz which will act almost as an open at RF frequency not affecting the RF match. Only one of the DC-feed lines is presented here due to the fact that it was not possible to put current probe on the EM dataset created component. This was because for the line with the snubber resistor there was an internal port placed during the momentum simulation which will later enable to connect the snubber resistor after the component is created. But for the line without snubber there was no internal port placed when doing the simulation which implies that no pin is available to place a probe after the component is created. Due to this the presented result in figure 4.4 is for the line with snubber resistor.

The simulation results comparing circuit and Momentum simulation for all the three impedances described above for the transistor without internal decoupling is shown in figure 4.5, 4.6 and 4.7

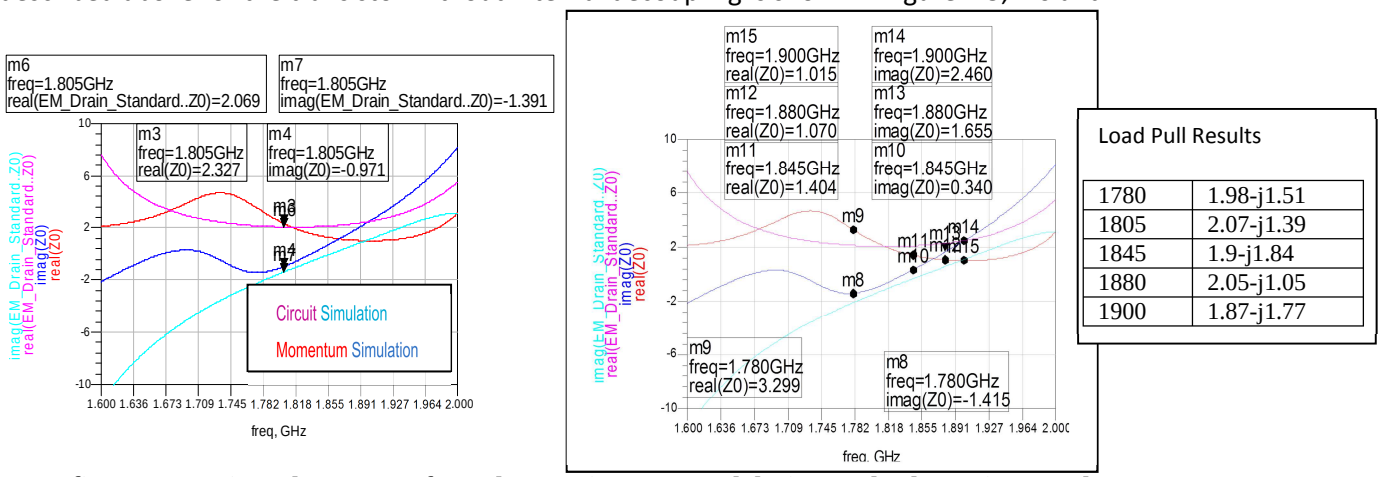


figure 4.5 RF impedances seen from the transistor external drain standard transistor package

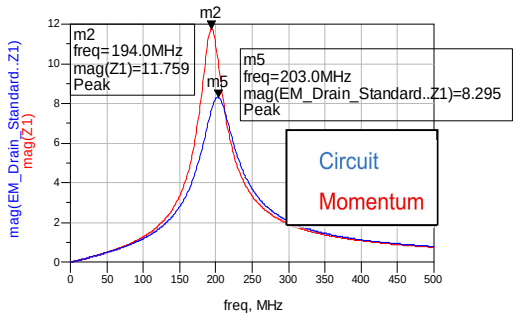


Figure 4.6 Baseband Impedance seen from the intrinsic drain

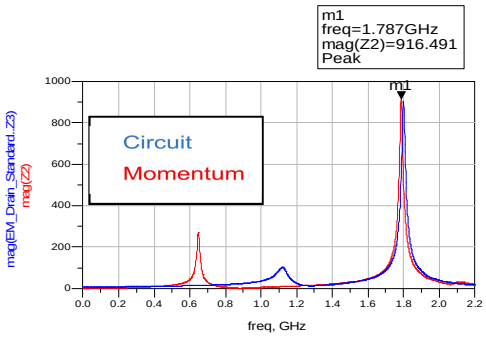
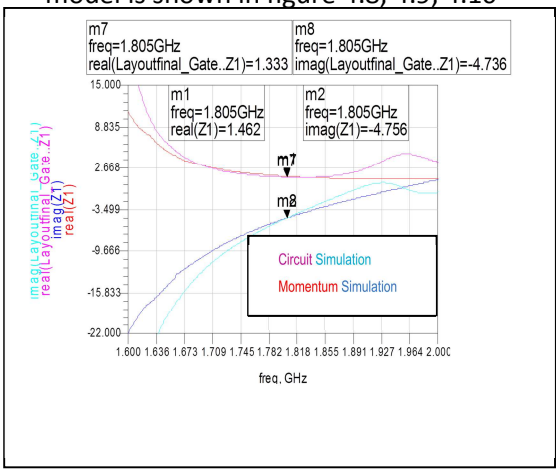
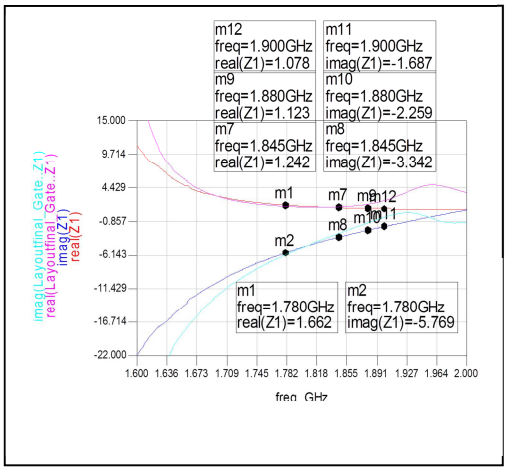


Figure 4.7 DC-Feed Impedance seen from the transistor external drain

For the RF match the design goal is Zext,drain=(2.07-j1.39)Ω from the load-pull. From the simulation results (figure 4.5) it is evident that the result obtained is quite the same. But for the other Load Pull frequencies the values are quite different since the optimization is only done at 1805 MHz. For the baseband impedance (figure 4.6) it can be seen that the least possible impedance peak obtained was 12 Ω which is significantly higher than the impedance variation seen from the transistor with internal decoupling in figure 4.3. The impedance seen into the DC-Feed line (figure 4.7) from the external drain approached close to infinity at 1.8 GHz which will act almost as an open at RF frequency not affecting the RF match.

For gate of both transistors the simulation results obtained both for the circuit and momentum model is shown in figure 4.8, 4.9, 4.10





Source Pull Results

1780	1.18-j4.18
1805	1.34-j4.53
1845	1.51-j4.55
1880	2.01-j5.55
1900	1.93-j5.81

Figure 4.8 Impedances seen from the transistor external gate transistor package

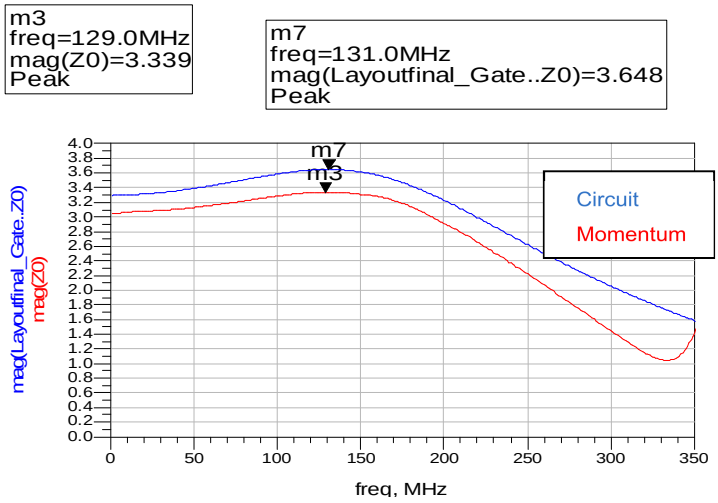


Figure 4.9 Baseband Impedance seen from the intrinsic gate

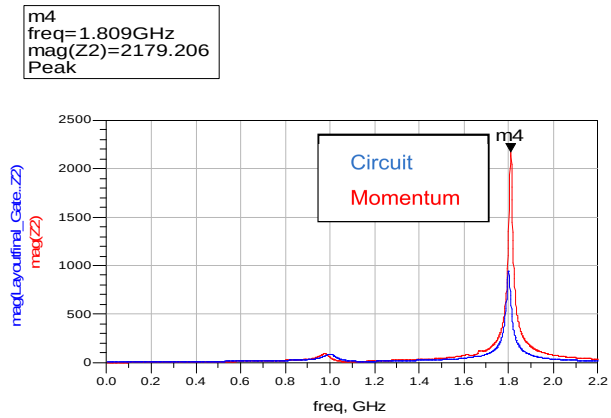


Figure 4.10 DC-Feed Impedance seen from the transistor external gate

For the RF match the design goal is Zext,gate=(1.36-j4.57)Ω from the load-pull. From the simulation results (figure 4.8) it is evident that the result obtained is quite the same. But for the other Load Pull frequencies the values are quite different since the optimization is only done at 1805 MHz. For the baseband impedance (figure 4.9) it can be seen that the least possible impedance peak obtained was 3.4 Ω which is not that much of a problem since there is no high current on the gate side. This also proves the theory discussed in section 2.4.1 and 3.3.1: the least impedance seen at 0 Hz in this model is the series snubber resistor which was 6 Ω, using symmetric configuration decreases the resistance by half since now we have 3 Ω at 0 Hz. The impedance seen into the DC-Feed line (figure 4.10) from the external gate approached close to infinity which will act almost as an open at RF frequency not affecting the RF match.

To clearly see the effects of the snubber resistors, each drain model snubber resistors were short circuited. The corresponding simulation result as compared to the optimal snubber resistors value for both transistors is shown in figure 4.11 and 4.12

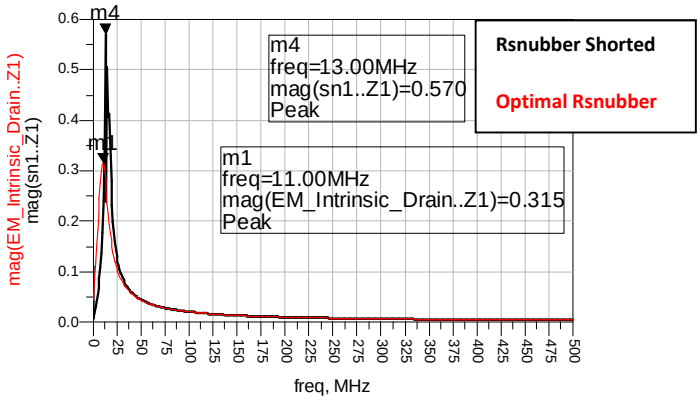


Figure 4.11 Baseband Impedance for the transistor with internal decoupling comparing shorting the snubber resistor with optimal resistor value

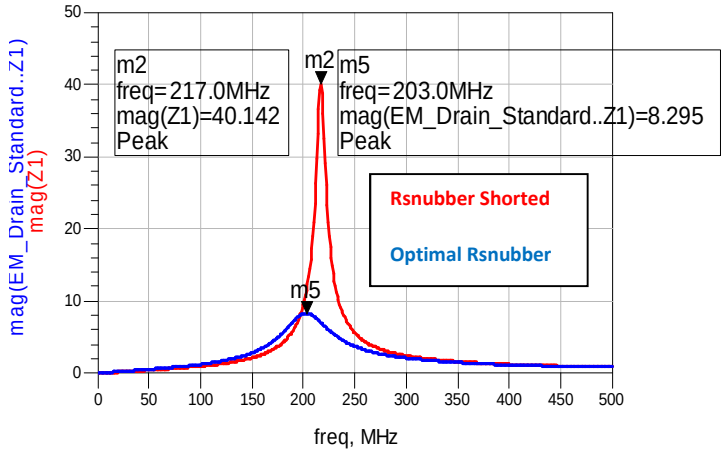


Figure 4.12 Baseband Impedance for the standard transistor comparing shorting the snubber resistor with optimal resistor value

4.2 Measurement Results

The generated layout was sent to fabrication which was then measured in the lab. The assembled PA for the transistor with internal decoupling is shown in figure 4.13

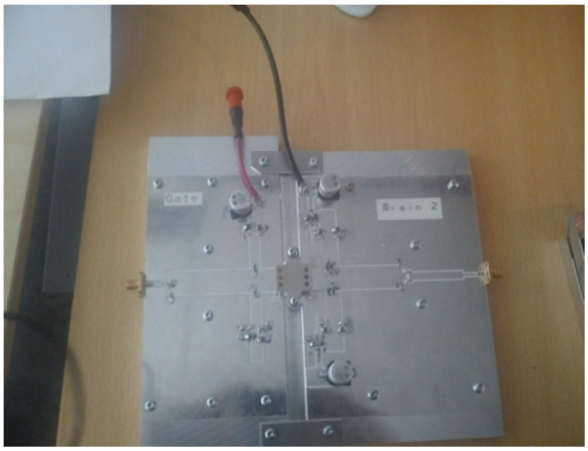


Figure 4.13 The whole PA assembled together for the transistor with internal decoupling

For the snubber resistors on the drain side, 0.4 Ω was not found in the lab so two 1 Ω resistors were used in parallel. Two 680 µF electrolytic capacitors were used in total for the drain (two on symmetrical configuration) and gate (one for the upper bias line) low baseband frequency decoupling. For the gate side, 6 Ω snubber resistor was not found so 6.8 was used instead which did not affect the baseband impedance much when tested on simulation.

The assembled PA for the standard transistor is shown in figure 4.14

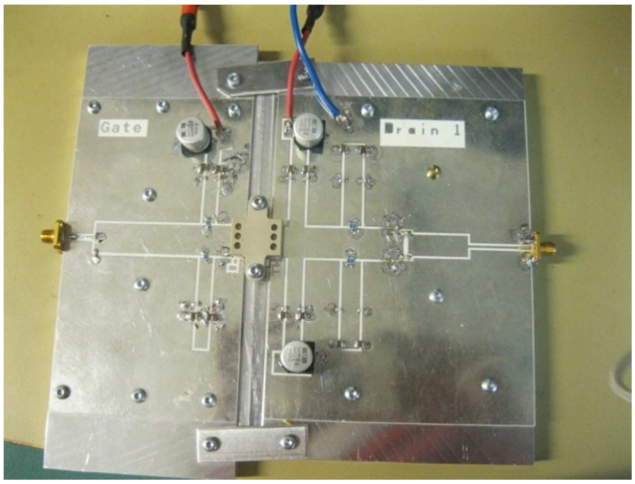


Figure 4.14 The whole PA assembled together for the standard transistor

Here also, the snubber resistors value 8.4 Ω was not found so two 18 Ω resistors were used in parallel.

4.2.1 Stability Test

The first measurement test for both PA's was stability test to check if the PA is stable. The measurement setup is shown in figure 4.15

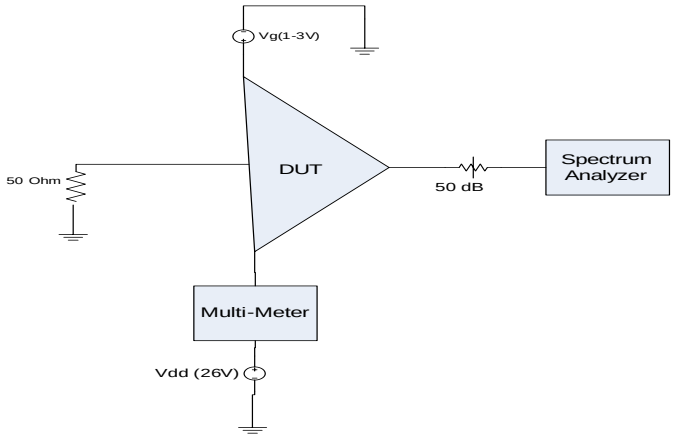


Figure 4.15 Setup for Stability test

In figure 4.15, Input of the PA SMA was terminated with 50 ohm and PA output SMA to 50 Ω, 500 W attenuator (20dB) and from that to the spectrum analyzer. The 50 dB attenuation seen in figure 4.15 is from the fact that 30dB attenuation was added not to reach the spectrum analyzer's damage level. The drain and the gate were biased at 26 V and 2.55 V (corresponding to Idq=0.457 A) respectively. The measurement result showed only noise on the spectrum analyzer as expected since the PA shouldn't amplify anything without input. To check instability first only gate bias is increased while leaving drain bias at 26 V. Due to current limitation (maximum 2A) in the multi-meter at the maximum Idq that was possible no oscillations were observed. Next, the drain bias was decreased and gate bias was increased gradually to the level, Vdrain=2V and Vgate=2.8V. At the described bias point oscillation was observed at 788 MHz and 1.6 GHz as shown in figure 4.16

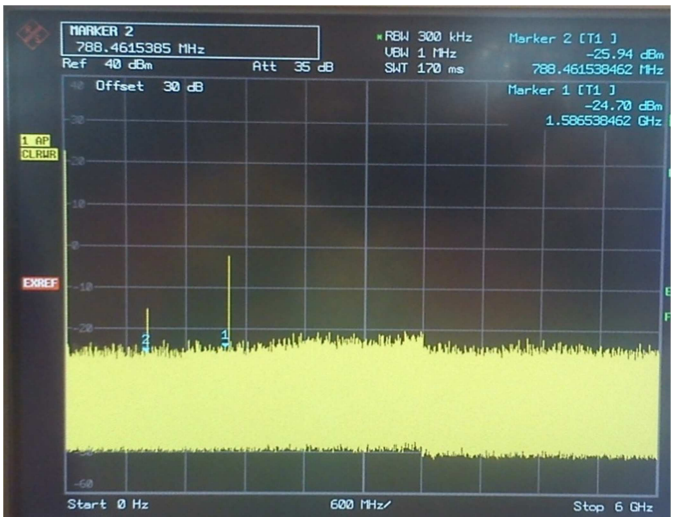


Figure 4.16 Instability observations for the transistor with internal decoupling

The measurement result shown in figure 4.16 is for the transistor with internal decoupling. This amplifier is stable enough, only at Vdd very far from intended are any self-oscillations observed. For the standard transistor, instability cannot be observed due to multimeter current limitation of 2 A. This can indicate that the transistor might have self oscillation for Idq greater than 2A but is definitely stable enough.

4.2.2 Small Signal Measurement

The first test of gain and gate RF impedance match was made by a VNA (Vector Network Analyzer). The measurement setup is shown in figure 4.17

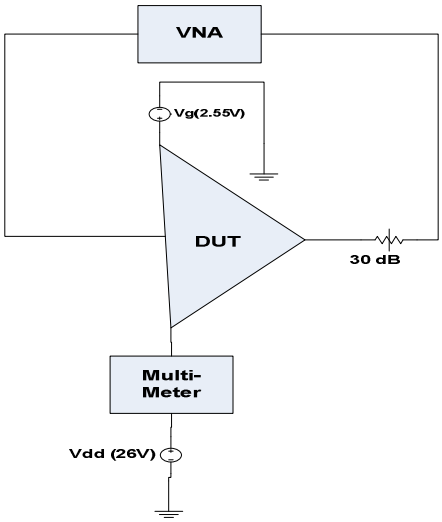


Figure 4.17 Small signal Measurement Setup

In figure 4.17, input of the PA SMA was connected to calibrate (which was calibrated using e-cal one port) VNA port one. PA output SMA is connected via 500 W attenuator to port two which was calibrated using thru response calibration of VNA. This calibration is required for transmission (gain in this case) test. This measurement gives a test if the amplifier is working in the first place and a real test of gate match and small-signal gain. To see if the PA is working, the gate voltage was varied and the gain was recorded accordingly. These values were recorded and shown in the table 4.1

Vgate(V)	Vdd (V)	Idq(A)	Gain(dB)
2.7	26	1.13	16.9
2.66	26	0.87	15.9
2.6	26	0.645	14.9
2.55	26	0.457	13.9
2.45	26	0.208	9.68
2.4	26	0.134	7.23
2.29	26	0.0044	0

Table 4.1 Gate voltage varied, Gain and Idq was recorded for transistor with internal decoupling at 1.8 GHz

From table 4.1 it can be seen that the transistor threshold is at Vg=2.29 V. The return loss was also recorded observing port 1 of the VNA. The response of the two ports is shown in figure 4.18

Figure 4.18 Port 1 return loss and Port 2 Gain at Vg=2.55 V and Vdd=26 V

From figure 4.18 it can be seen that around the center frequency the return loss is 16 dB which shows the input match is quite good.

For the standard transistor the same measurement was carried out and the result obtained was recorded and shown in table 4.2

Vgate(V)	Vdd (V)	Idq(A)	Gain(dB)
2.7	26	1.23	16.4
2.66	26	0.989	15.8
2.6	26	0.650	14.4
2.55	26	0.464	13.9
2.45	26	0.208	9.68
2.4	26	0.152	7
2.3	26	0.00556	0

Table 4.2 Gate voltage varied, Gain and Idq was recorded for the standard transistor at 1.8 GHz

From Table 4.2 it can be seen that the transistor threshold is at Vg=2.3. The insertion loss was the same since the same gate circuit was used for both transistors.

4.2.3 Pulsed Continuous Wave (CW) measurement

Large signal RF test: Pulsed CW was used for this purpose. The main reason to pulse the signal is to avoid the transistor being overheated. Pulse width of 10 µs and 10 % duty cycle was used. The measurement setup for this purpose is shown in figure 4.19

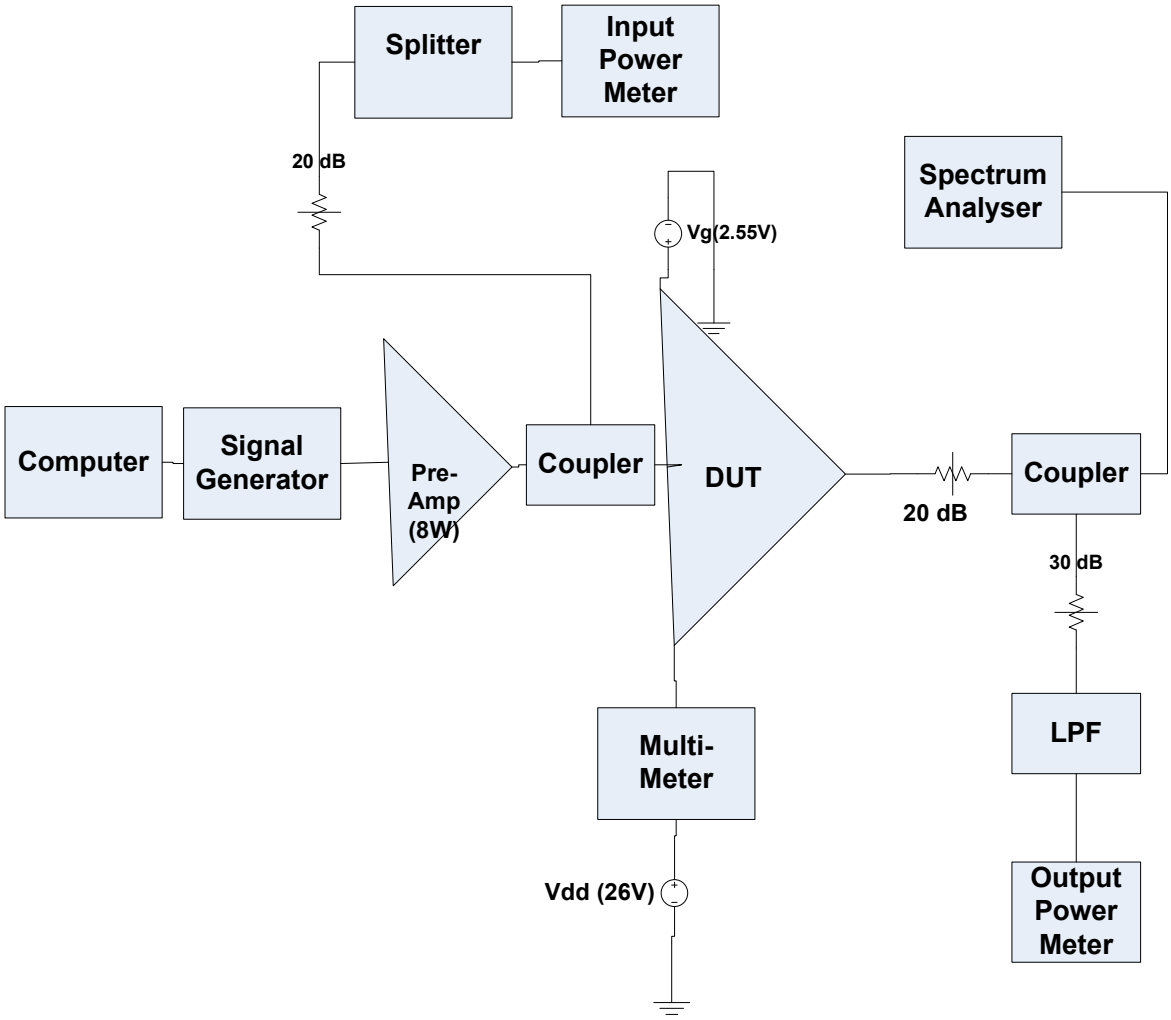


Figure 4.19 Measurement Setup for Pulsed CW with RF power Meters

In figure 4.19, the measurement setup used for the CW measurement is seen. The pre-amplifier is used to make sure sufficient input power is delivered to the DUT since its gain is low. The two power meters are used to sense the input and output power levels. The low pass filter (LPF) was used to make sure that only the fundamental RF is sensed by the output RF power meter. Both couplers used have 20 dB coupling. Matlab GPIB program was used to control each equipment by sending device specific programming commands. Before the measurement, calibration was made by setting input and output offsets so that the input and output reference plane move to the input and output of the DUT. After doing so, the pulsed CW measurement was performed. For this measurement the power supply was set to 27 V, so that after DC cable loss the PA was biased at 26V gate bias of 2.66 V (corresponding to Idq=0.9A) was used. This class of biasing is maximum linearity class AB while the previous bias (26 V and 2.55 V) is lower class AB which is closer to class B. There was a specific program written in matlab for doing so. The pulse can be seen in figure 4.20

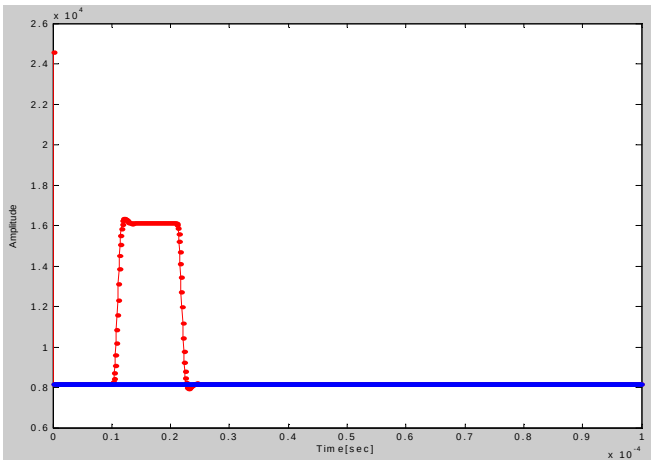


Figure 4.20.a Unit Pulse input signal with 10% duty cycle

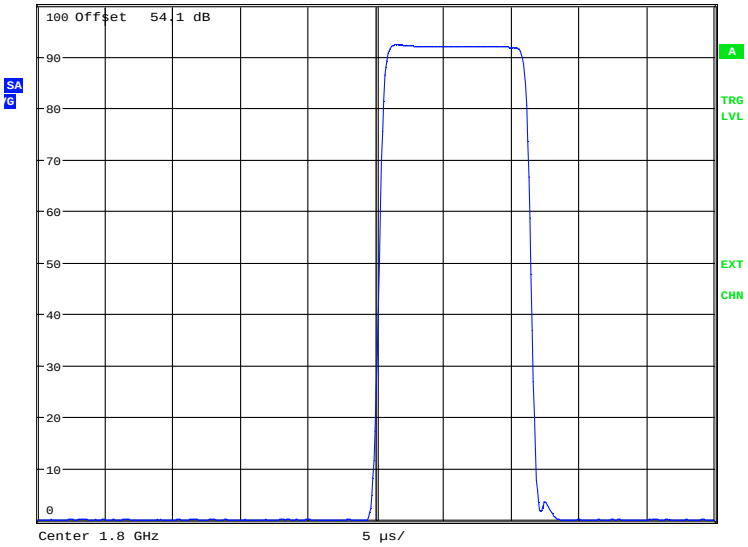


Figure 4.20.b Unit Pulse output signal

The red and blue plots in figure 4.20.a are the complex input signals (i.e the digital signal in the controlling computer). From figure 4.20.b it is verified that the output pulse is close enough to rectangular. When the PA with internal decoupling was first tested a frequency and power sweep was performed from 1.7 to 1.9 GHz and from -20 to 0 dBm respectively at pre-amplifier input. The efficiency obtained was not satisfactory (55%) so manual tuning was performed at the center frequency on the board by changing the position and the value of matching capacitors. The original capacitors used in the simulation are described in section 3.3.2.1. The desired RF performance was obtained at the same value capacitors (GQM2195C2E3R3BB12, 3.3pF, 250 V) for matching and DC_block**.** The matching capacitors were soldered a few millimeters to the left from the simulated place. One of the reasons for not getting the RF match as the simulation would be the capacitor models used in the simulation might not be good enough. Maximum Output Power [W], Efficiency, Gain [dB] vs frequency, and Gain vs. output voltage is shown in the following plots respectively.

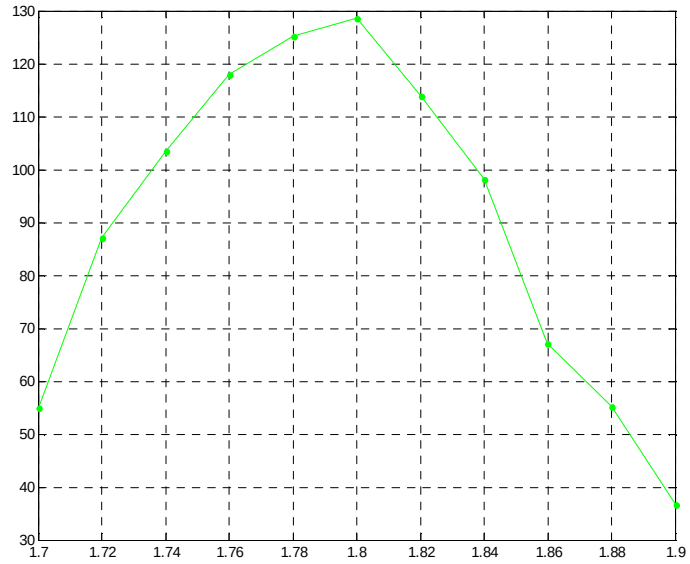


Figure 4.21 Maximum RF Output Power [W] Vs. Frequency [GHz] for the transistor with internal decoupling (129 W at 1.8 GHz)

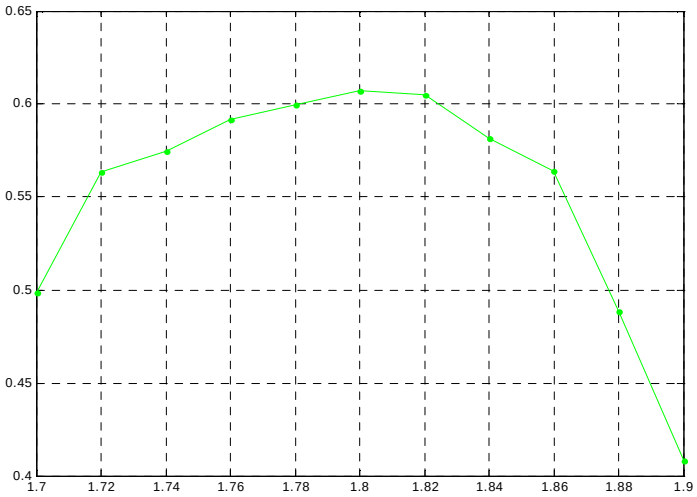


Figure 4.22 Maximum Efficiency Vs. Frequency [GHz] for the transistor with internal decoupling (61% at 1.8 GHz)

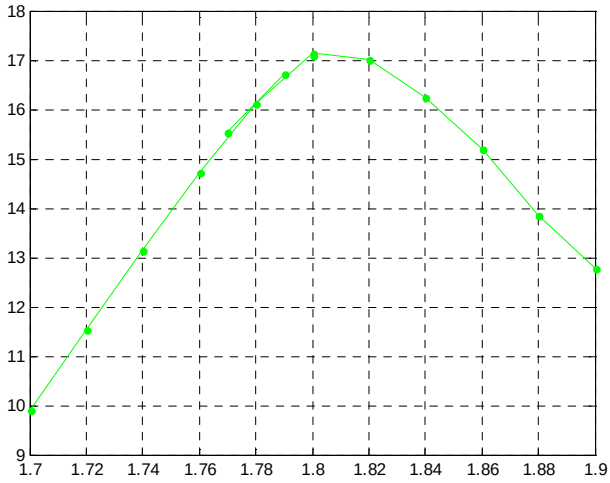


Figure 4.23 Gain [dB] Vs. Frequency for the transistor with internal decoupling

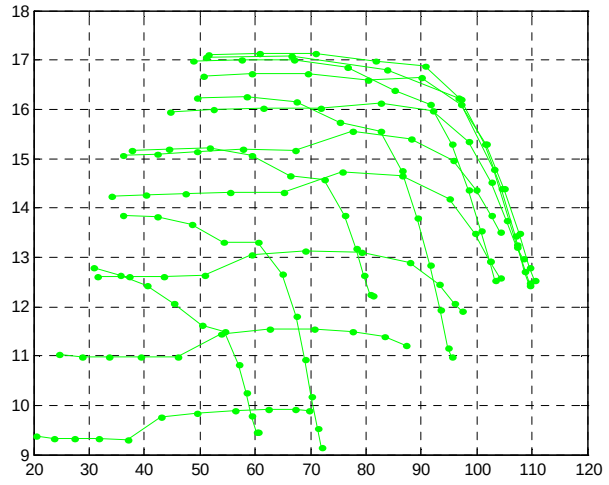


Figure 4.24 Gain [dB] Versus Amplitude Output Voltage [V] in 50Ω for different frequency sweep for the transistor with internal decoupling

From the above four figures, it can be seen that the load/Source Pull RF performance was achieved which was Pout=50 dBm, η=58.5% and Gain=14 dB. The performance obtained is even better which is because of higher bias point. Figure 4.22, which is the efficiency plot shows that the performance is quite broadband which is consistent with the fact that the PA is designed for the best efficiency. Whereas figure 4.21, which is the maximum output power over the given power sweeps, shows that the performance is quite narrow band or it is not as broadband as the efficiency performance.

Some approximate conclusion are made to what RF bandwidth is achieved, this of course depends on criterion but if maximum output power (figure 4.21) 120 W (down from 130 W) accepted as somewhat ad-hoc rough first estimate criterion, then RF bandwidth seems to be approximately 50 MHz for the drain circuit. The approximated maximum efficiency (figure 4.22) bandwidth at 58% (down from 61%) is around 70 MHz. For the maximum small signal gain (figure 4.23) and at 1dB compression the approximated bandwidth is 70 MHz.

The same procedure was carried out for the standard transistor and at first the efficiency was quite low (50%). So as the previous PA case, manual tuning was performed at the center frequency on the board using the same technique. Here it took much time to get a good enough RF performance. At the end due to the scope of the project which focuses on baseband impedance and lack of time the results obtained are taken as a good enough results. The best efficiency obtained at the center frequency was 55 %. The match and DC_block capacitors are GQM1875C2ESR6BB12 (5.6pF, 250V) and GQM2195C2A6R2DB01 (6.2pF, 100V). The matching capacitors were soldered a few millimeters to the left from the simulated place. The four most important plots which were described for the transistor with internal decoupling are shown below

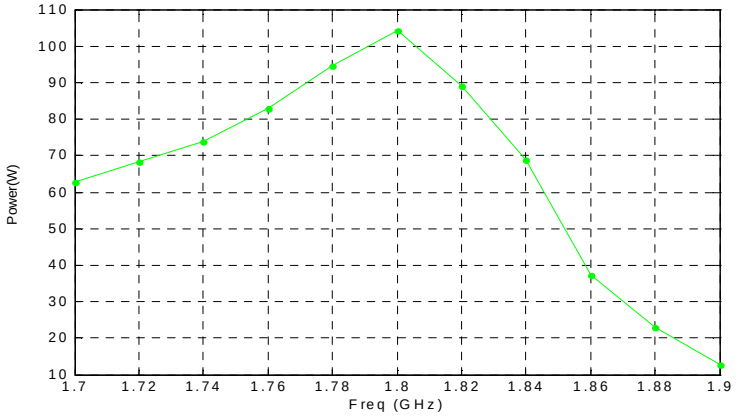


Figure 4.25 Maximum RF Output Power [W] Vs. Frequency [GHz] for the standard transistor (105 W at 1.8 GHz)

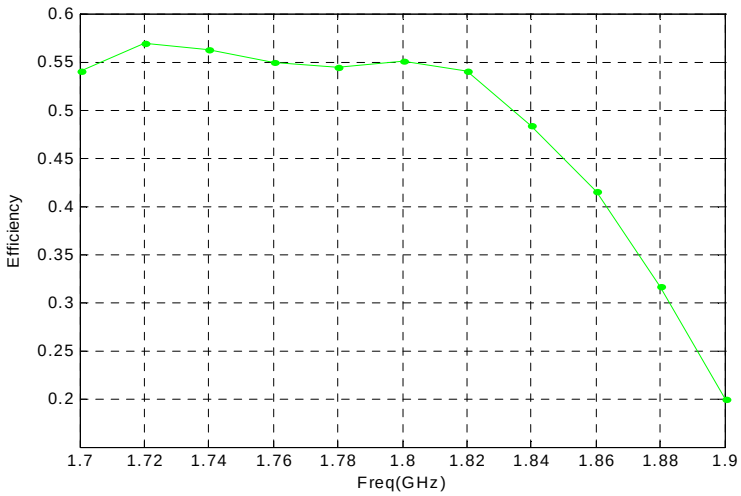


Figure 4.26 Maximum Efficiency Vs. Frequency [GHz] for the standard transistor (55% at 1.8 GHz)

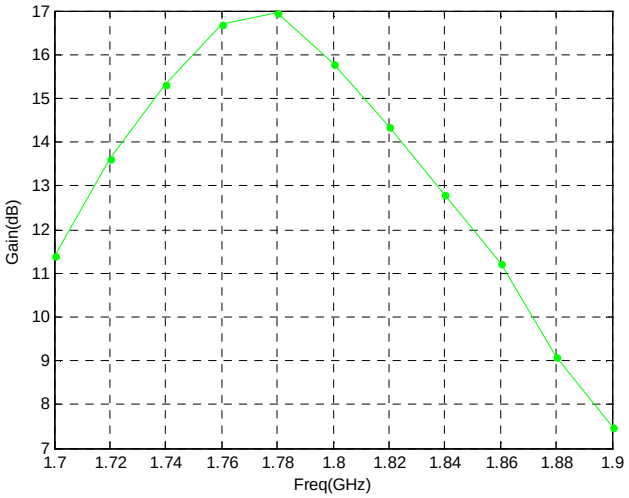


Figure 4.27 Gain [dB] Vs. Frequency for the standard transistor

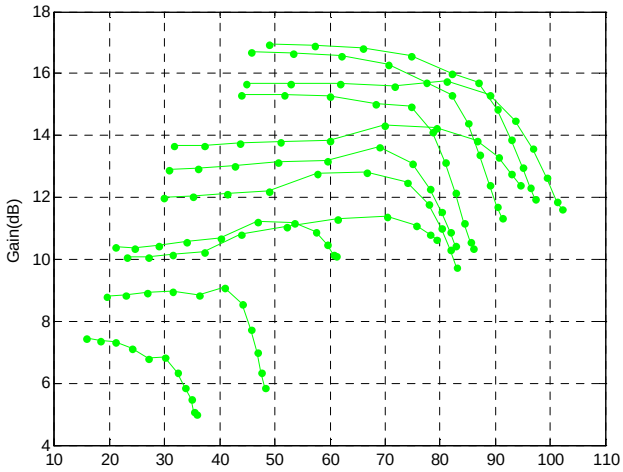


Figure 4.28 Gain [dB] Versus Amplitude Output Voltage [V] in 50Ω for different frequency for the standard transistor

From the above four figures, it can be seen that the load/Source Pull RF performance was not fully achieved for the efficiency which was, η=58.2% , the maximum efficiency at the center frequency was 55% which was not too bad. But the output power and gain were satisfied which were Pout=50.54 dBm, and Gain=14 dB. Figure 4.26, which is the efficiency plot, shows that the performance is quite broadband which is consistent with the fact that the PA is designed for the best efficiency. Whereas figure 4.25, which is the maximum output power over the given power sweeps, shows that the performance is quite narrow band or it is not as broadband as the efficiency performance.

Some approximate conclusion are made to what RF bandwidth is achieved, if maximum output power (figure 4.25) 90 W (down from 110 W) accepted as somewhat ad-hoc rough first estimate criterion, then RF bandwidth seems to be approximately 45 MHz for the drain circuit. The approximated maximum efficiency (figure 4.26) bandwidth at 55% is around 60 MHz. For the

maximum small signal gain (figure 4.27) and at 1dB compression the approximated bandwidth is 45 MHz.

4.2.4 Two-tone measurement

For this measurement the modulation frequency (f_m) was swept from 1 to 50 MHz and thus tone-spacing = 2*fm from 2 to 100 MHz. Also different input power levels were used which were Pin = [8 13 18 22] dBm. The above sweep was done at different center frequency f_c= [1.78 1.8 1.82 1.84] GHz. To see the baseband drain voltage variation a probe component was placed on the drain of both PA boards. The circuit diagram for this probe is shown in figure 4.29

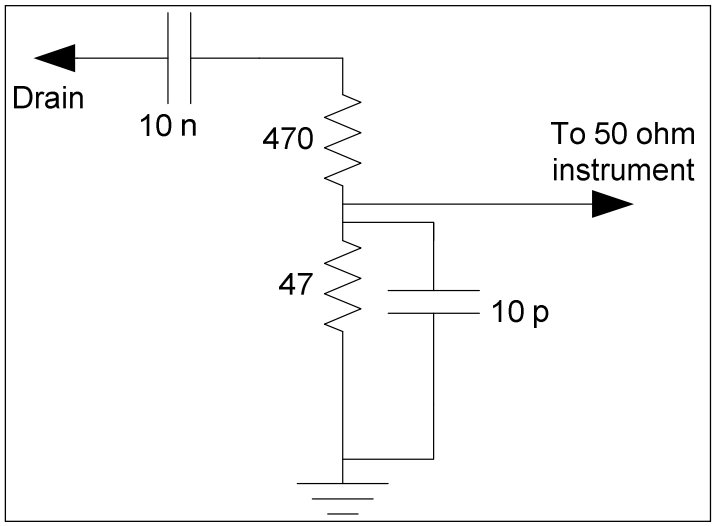


Figure 4.29 Probe components to be mounted on the PA board [6]

On the layout design, small islands were created for these components to be mounted on. These probe components have a property of a band pass filter in which it passes the AC baseband frequency components and block the DC and RF frequency components. The picture of the components soldered on the board is shown in figure 4.30

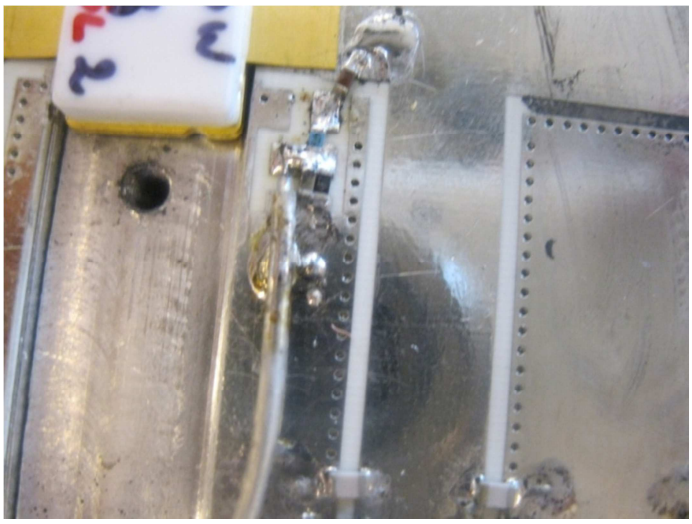


Figure 4.30 Probe components mounted on the PA board

After the probe components were soldered then a short coaxial cable with SMA connector was soldered which will be connected to the oscilloscope to see the baseband drain voltage variation. This probe is shown in figure 4.31

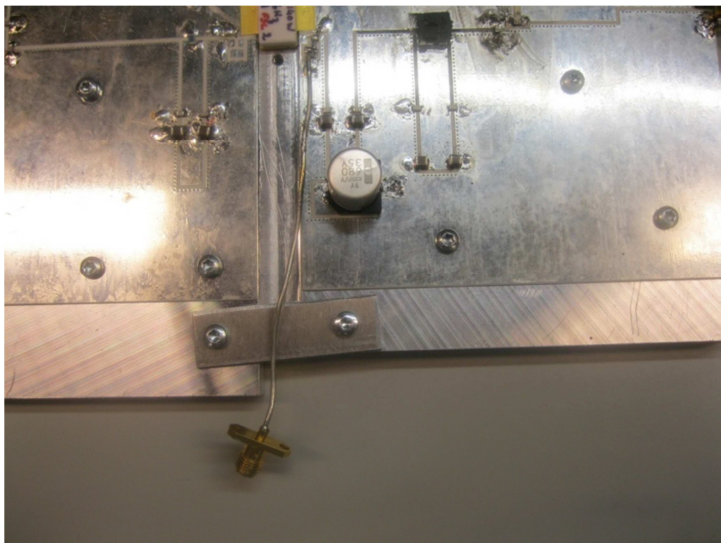


Figure 4.31 Baseband Probe used to connect to Oscilloscope

From this measurement it was possible to see the IM3 variation and baseband voltage variation versus tone spacing. The results presented here are for two center frequencies and also for the highest power level. These results are presented in figure 4.32 and 4.33 for different center frequency

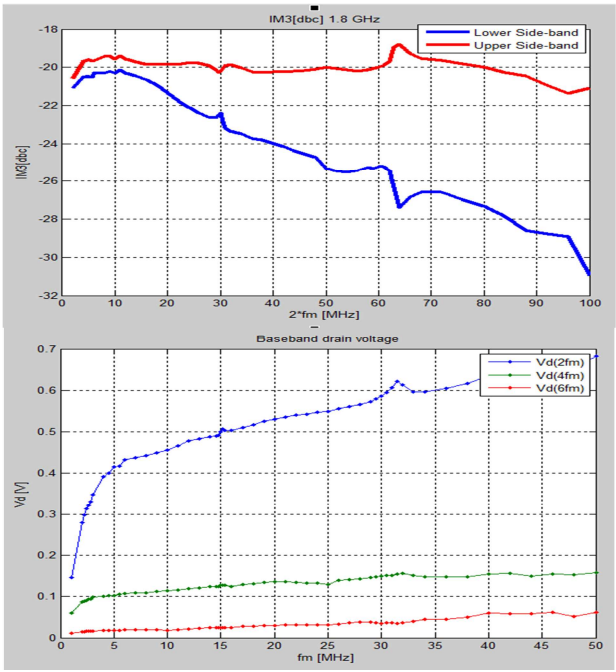


Figure 4.32 IM3 variation and baseband voltage variation versus tone spacing and modulation frequency for the transistor with internal decoupling for Pin=22dBm center at 1.8 GHz

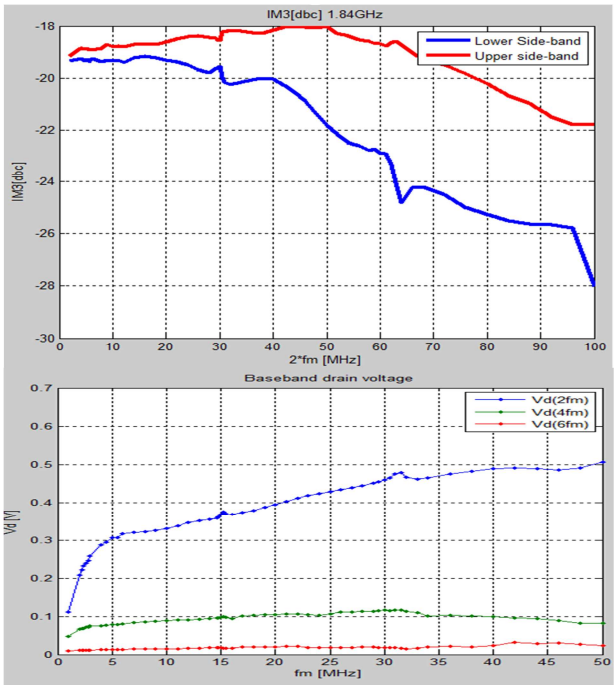


Figure 4.33 IM3 variation and baseband voltage variation versus tone spacing and modulation frequency for the transistor with internal decoupling for Pin=22dBm center at 1.84 GHz

From figure 4.32 and figure 4.33, it can be seen that there is some bandwidth limitation since both the IM3 products are not at the same power level. And also from that they are frequency dependent. In the drain voltage variation of both figures, the three different plots show variation for the fundamental, second and third harmonic of the fundamental baseband voltage ($2f_m$) computed by fourier transformation from oscilloscope values. Small voltage spikes are seen at around 15 and 30 MHz modulation frequency (corresponding to 30 and 60MHz tone spacing respectively) for the fundamental baseband voltage. The same corresponding variation is seen on the IM3 products at the same tone spacing described. This shows that the variation in IM3 is caused by baseband voltage variation. From different power sweeps it was observed that the higher the signal amplitudes, the more pronounced the effect of the nonlinearities, and the stronger the inter-modulation.

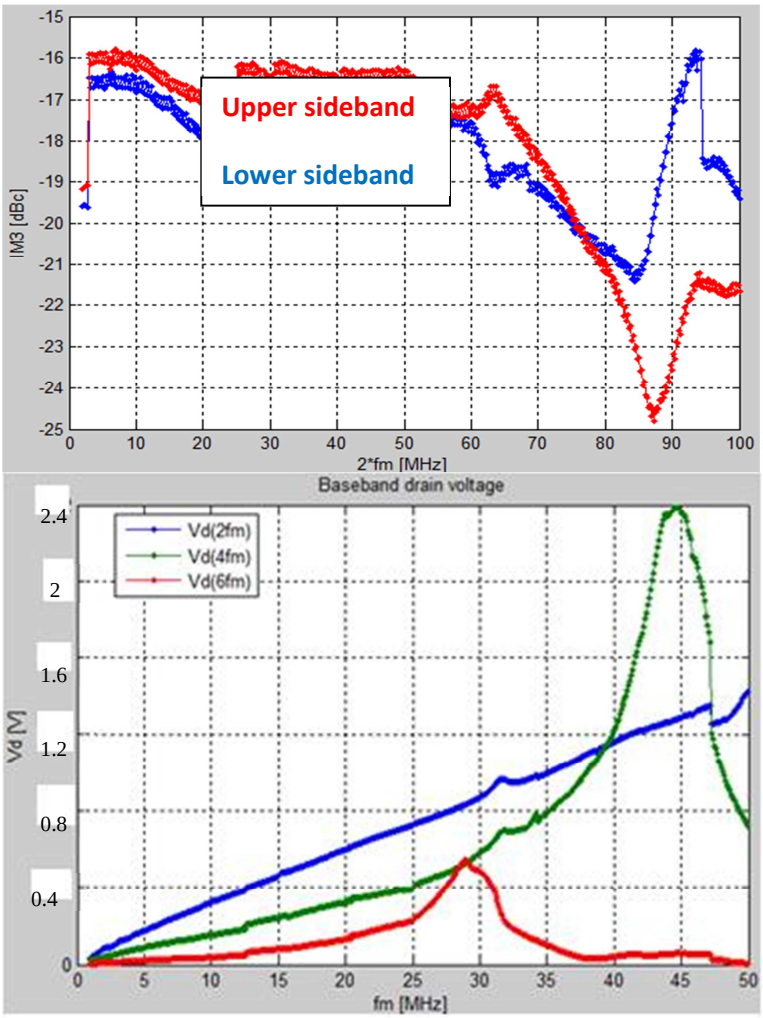


Figure 4.34 IM3 variation and baseband voltage variation versus tone spacing and modulation frequency for the standard transistor for Pin=22dBm center at 1.8 GHz

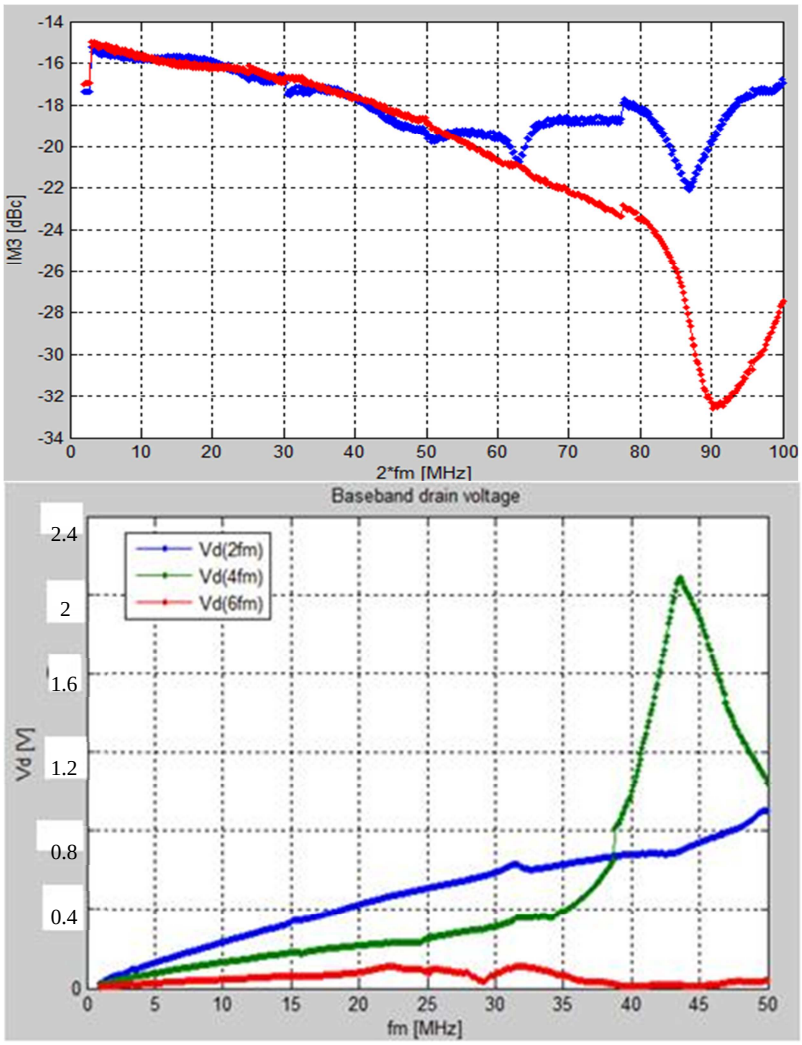


Figure 4.35 IM3 variation and baseband voltage variation versus tone spacing and modulation frequency for the standard transistor for Pin=22dBm center at 1.84 GHz

From figure 4.34 it can be seen that for the second and third harmonic corresponding to modulation (baseband) frequency around 45 MHz (2*(2*fm)=180 MHZ) and 30 MHz (3*(2*fm)=180 MHz) there is variation in baseband voltage. This variation can be seen causing another variation in the IM3 plot at (2*fm)=90 MHz and (2*fm)=60 MHz respectively.

From the above two tone measurement results, even though the transistor with internal decoupling show less variation in voltage, there was a voltage variation for both transistors. The difference in IM3 products power level is less for the standard transistor than for the transistor with internal decoupling.

4.2.5 Impedance Measurement

4.2.5.1 Baseband Impedance Measurement

The main aim of this thesis work is to study the baseband impedance and provide a solution for this problem. To do this, baseband impedance was measured for both transistors by the use of a probe. The probe was directly soldered very close to the drain and gate of the transistor package and it was then connected to VNA through DC block. The input and output SMA of the PA was terminated with 50 Ω. The probe can be seen in figure 4.36. It consists of simply two short 50Ω coaxial cables with SMA connectors.

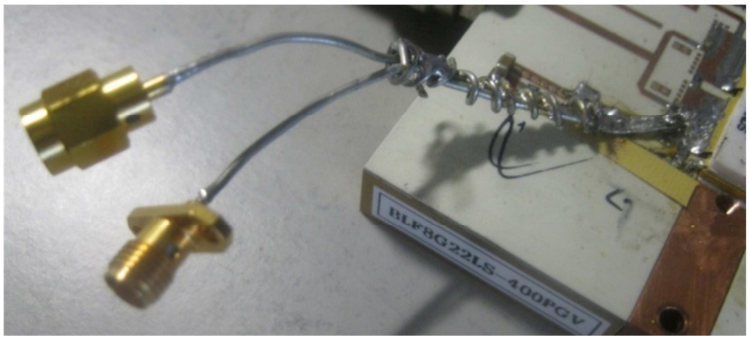


Figure 4.36 Picture of Probe used to measure Baseband Impedance

The baseband drain impedance comparison of the measurement with the EM simulation for the transistor with internal decoupling is presented in figure 4.37

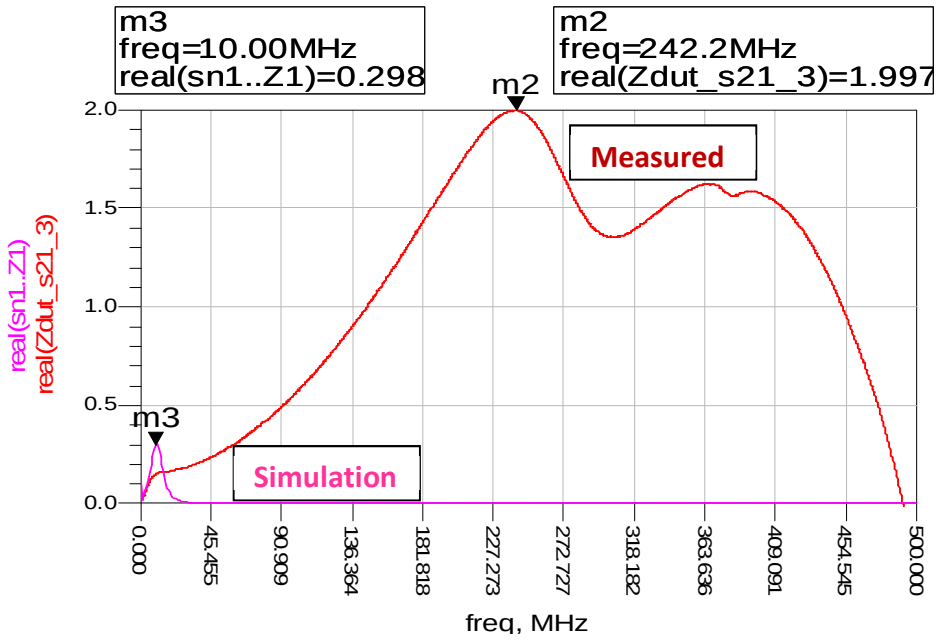


Figure 4.37.a Comparison between Measurement and Simulation for the Baseband drain impedance

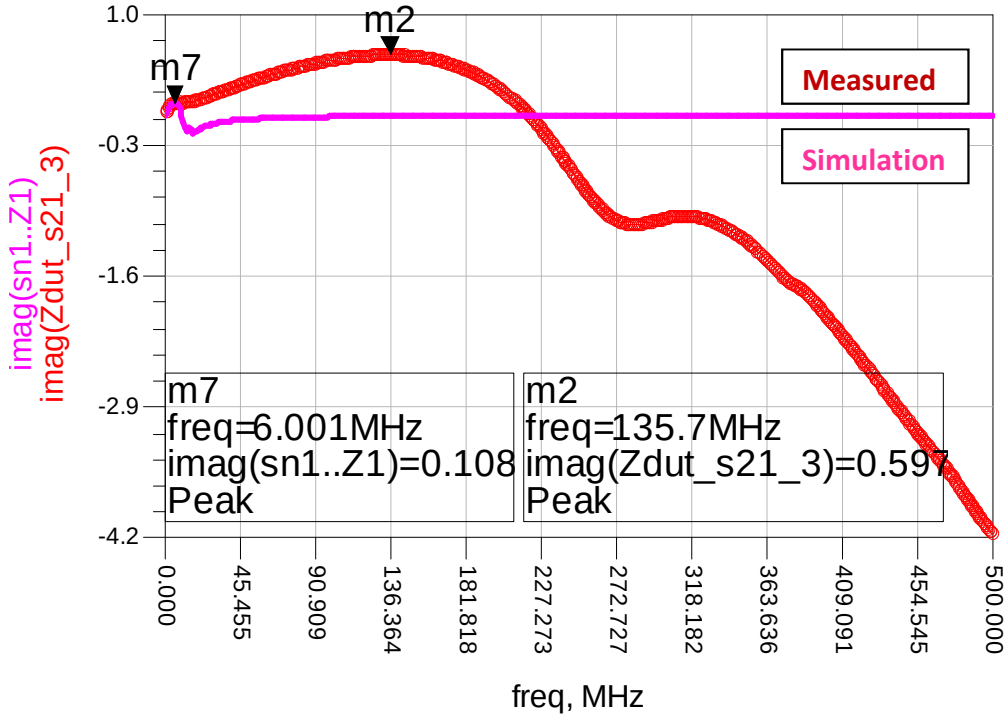


Figure 4.37.b Comparison between Measurement and Simulation for the Baseband drain impedance

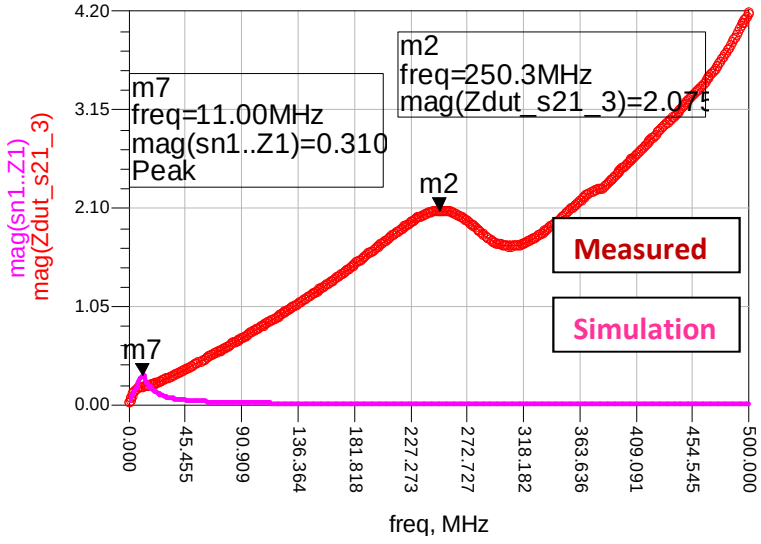


Figure 4.37.c Comparison between Measurement and Simulation for the Baseband drain impedance

From figure 4.38, it can be seen that the measurement and the simulation results are quite close below approximately 5 MHz and different for other frequencies.

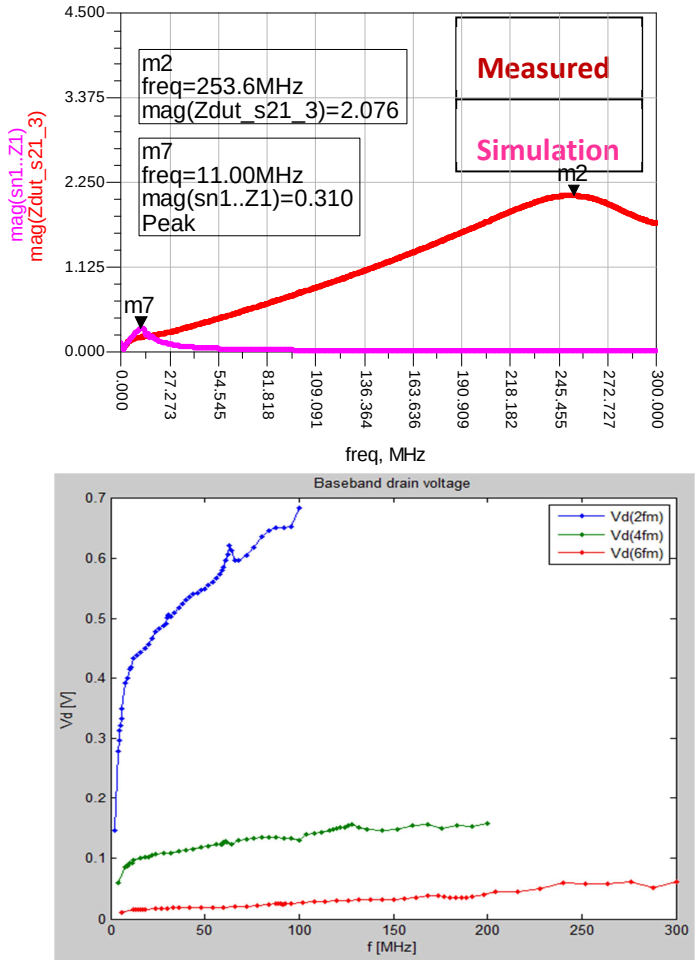


Figure 4.38 Baseband drain voltage variation compared with baseband impedance variation for the transistor with internal decoupling

From figure 4.38 it can be seen that for the very low frequencies where we have fast increase in baseband impedance, we also have fast increase in baseband drain voltage. But for somewhat higher frequencies with slower increase of impedance there is also a slower increasing baseband drain voltage variation. This shows a good consistency in the result.

The baseband impedance measurement obtained from the transistor manufacturer for non optimized board is shown in figure 4.39

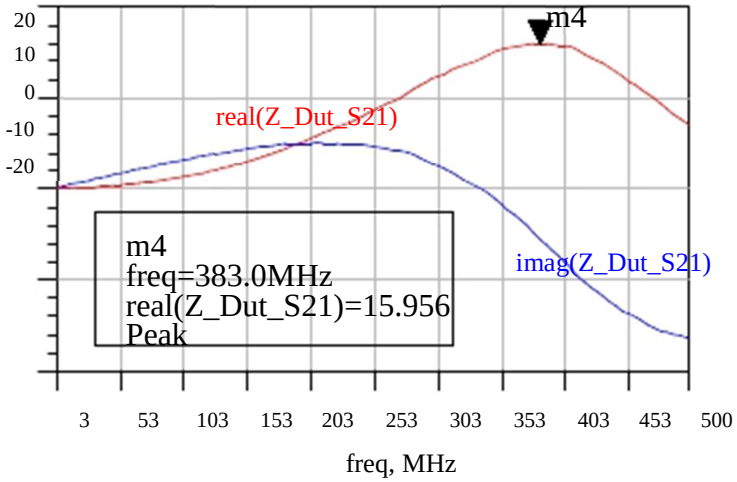


Figure 4.39 Baseband drain real and imaginary impedance measurements from the transistor manufacturer

Figure 4.39 shows that the impedance curve is similar to the measurement result shown in figure 4.38 but the magnitude of resonance is decreased significantly from 16 Ω to 2 Ω.

The baseband drain impedance comparison of the measurement with the EM simulation for the standard transistor is presented in figure 4.40

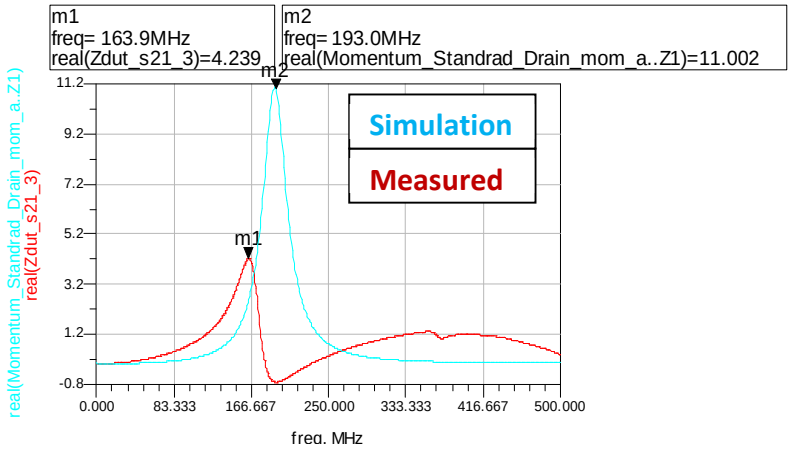


Figure 4.40.a Comparison between Measurement and Simulation for the Baseband drain impedance

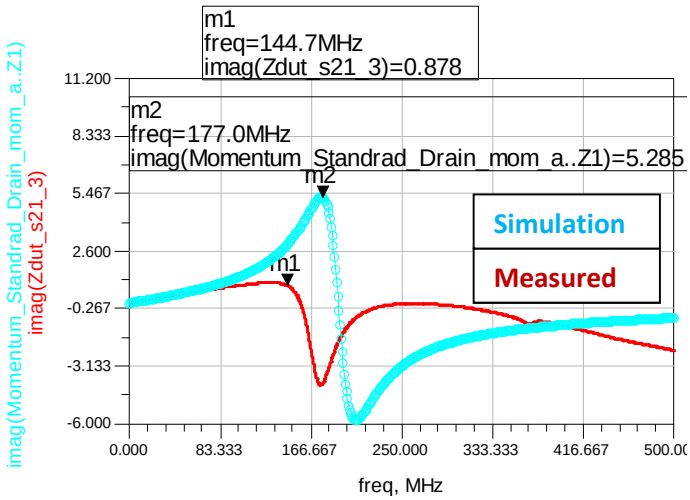


Figure 4.40.b Comparison between Measurement and Simulation for the Baseband drain impedance

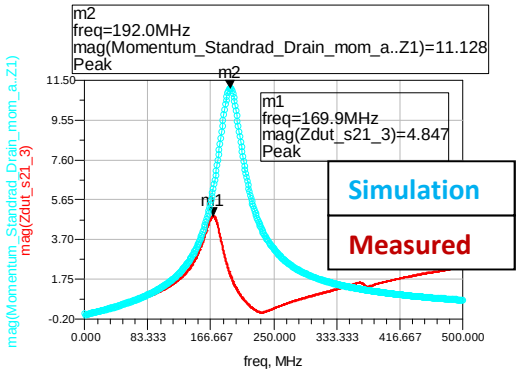


Figure 4.40.c Comparison between Measurement and Simulation for the Baseband drain impedance

From figure 4.40 it can be seen that, measured and simulated resonance frequencies are rather close but the measurement is lossier since the magnitude of the baseband impedance is decreased from 11Ω to 4Ω.

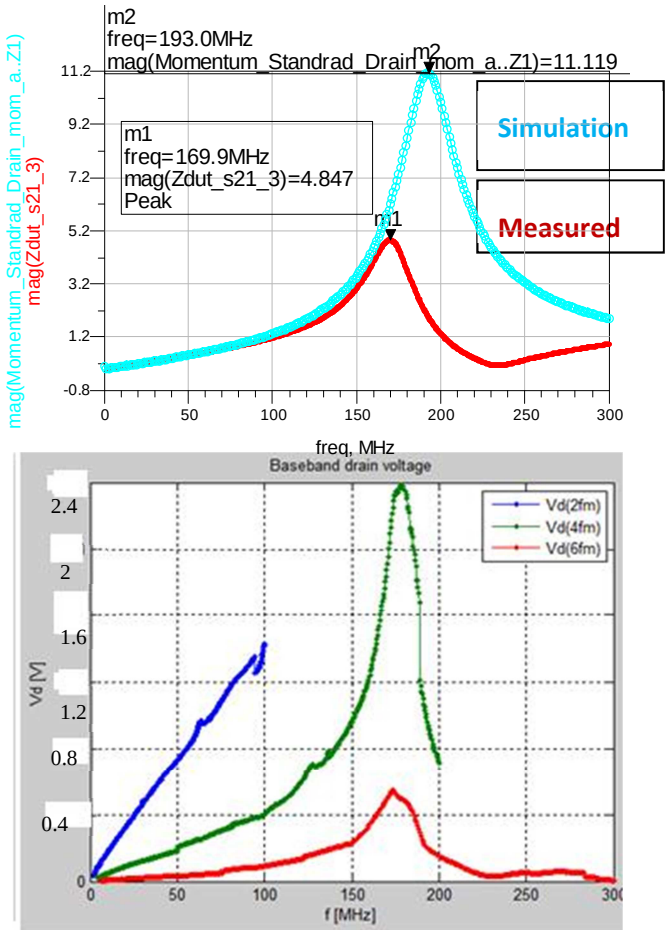


Figure 4.40.d Baseband drain voltage variation compared with baseband impedance variation for the standard transistor

Figure 4.40.d shows a baseband impedance resonance at 170 MHz , at this same frequency there is a strong voltage variation seen in the second and third harmonic of the fundamental baseband drain voltage.

The baseband gate impedance comparison of the measurement with the EM simulation for both transistors is presented in figure 4.41

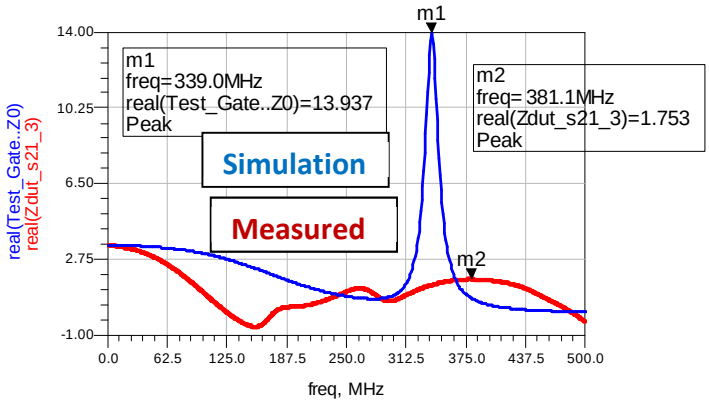


Figure 4.41.a Comparison between Measurement and Simulation for the Baseband gate impedance

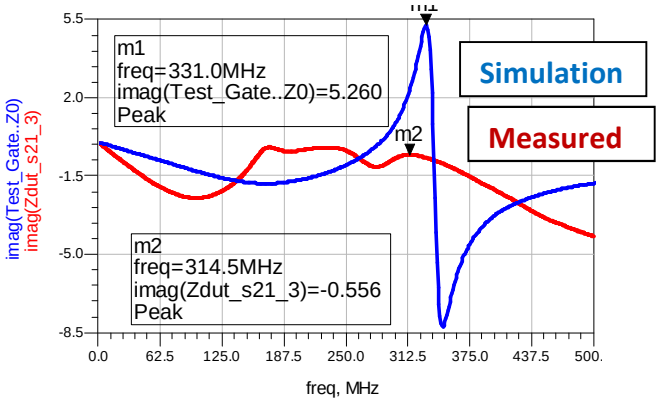


Figure 4.41.b Comparison between Measurement and Simulation for the Baseband gate impedance

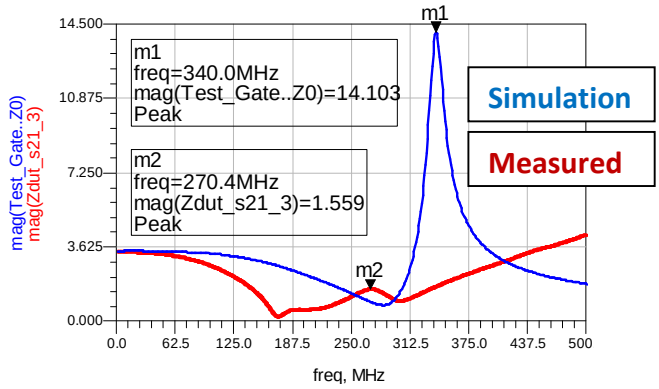


Figure 4.41.c Figure 4.41.b Comparison between Measurement and Simulation for the Baseband gate impedance

From figure 4.41 it can be seen the measurement and the simulation both have resonance at approximately the same frequency but the measurement (270 MHz) is much weaker than the simulated (340 MHz) and they have quite different shape for the high baseband frequencies. This difference might be due to the fact that approximating a transistor package just by capacitance is a good enough approximation for the very low baseband frequencies only. However, below approximately 50 MHz measured and simulated seem to be approximately the same.

The baseband impedance measurement was again carried out by increasing the optimal snubber resistor value and then short circuiting it with a small piece of metal. This measurement will help to see how much the snubber resistor attenuated the resonance. The measurement results for the standard transistor and for the transistor with internal decoupling is shown in figure 4.42 and 4.43 respectively

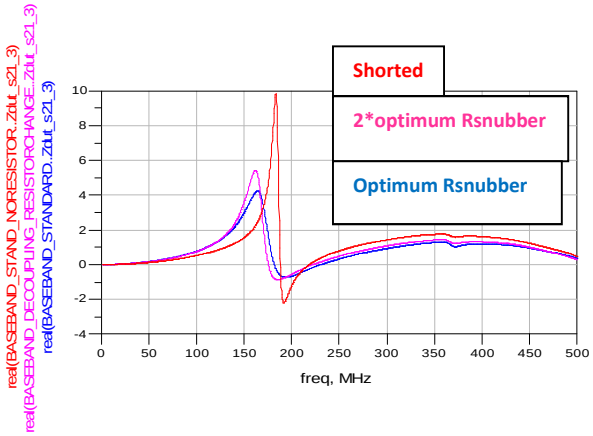


Figure 4.42.a Baseband drain Impedance comparison for different snubber resistor values and short circuiting the snubber resistors for the standard transistor

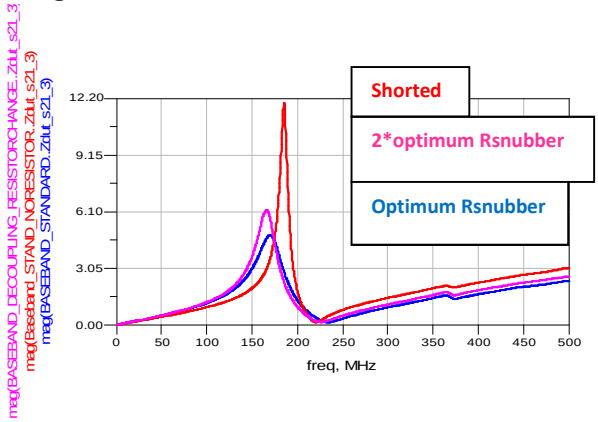


Figure 4.42.b Baseband drain Impedance comparison for different snubber resistor values and short circuiting the snubber resistors for the standard transistor

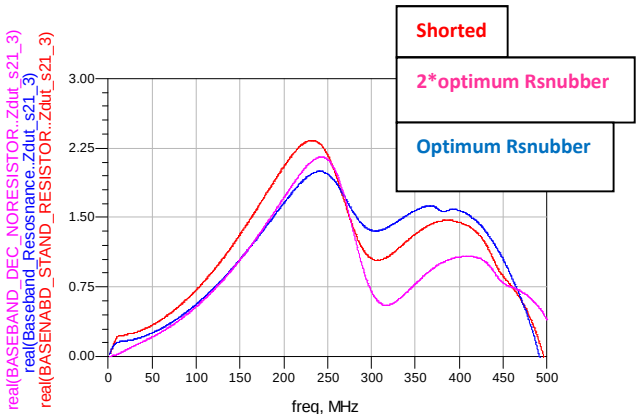


Figure 4.43.a Baseband drain Impedance comparison for different snubber resistor values and short circuiting the snubber resistors for the transistor with internal decoupling

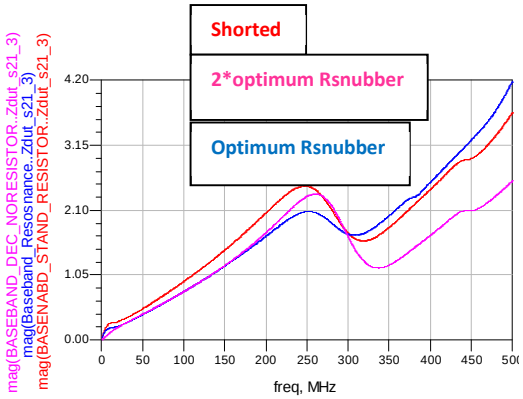


Figure 4.43.b Baseband drain Impedance comparison for different snubber resistor values and short circuiting the snubber resistors for the transistor with internal decoupling

From figure 4.42 and 4.43 it can be seen that when increasing the resistor value, the magnitude of the resonance increases, and the same is seen to be the case when it is short circuited. The effect is quite small for the transistor with internal decoupling than the standard transistor.

4.2.5.2 RF Impedance Measurement

The impedance measurement boards discussed in section 3.3.2.3 is used for this measurement. The picture of the drain impedance measurement board for the transistor with internal decoupling and the TRL structures are shown in figures 4.44 and 4.45

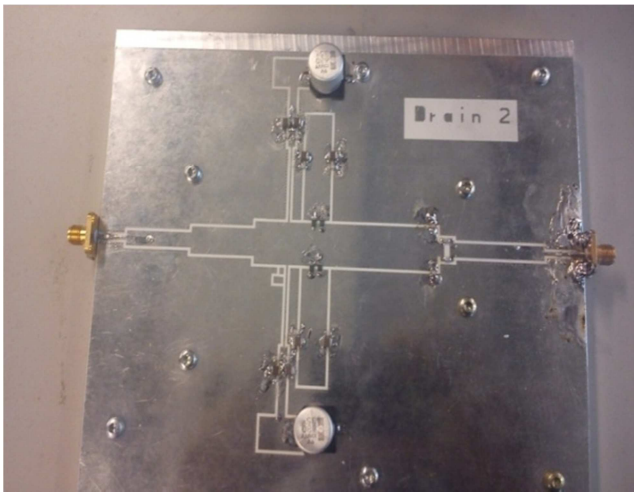


Figure 4.44 Drain impedance measurement board for the transistor with internal decoupling

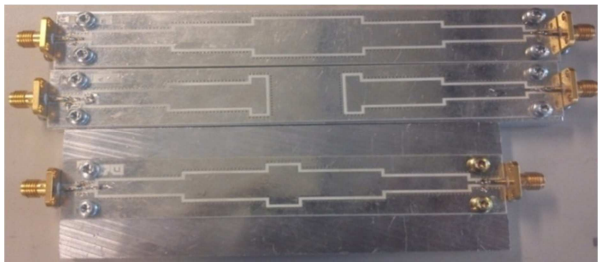


Figure 4.45 TRL structures

The simulation result for the tuned board capacitor values shows that the RF match impedances should be (2.082+j*1.114) at 1.8 GHz. For the measurement of impedance using VNA, a matlab written algorithm was used for de-embedding the transformer using the measurement results of the TRL structure. The obtained result comparing measurement and simulation over the whole simulation frequency is shown in figure 4.46

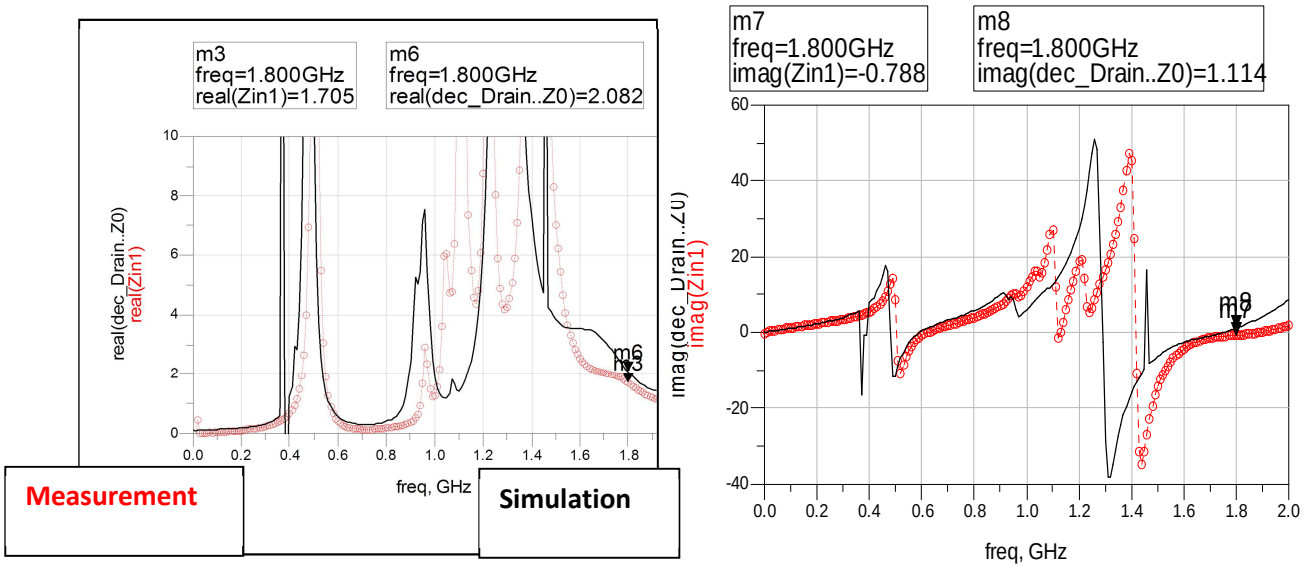


Figure 4.46.a Real and Imaginary drain impedance comparison between simulation and measurement results

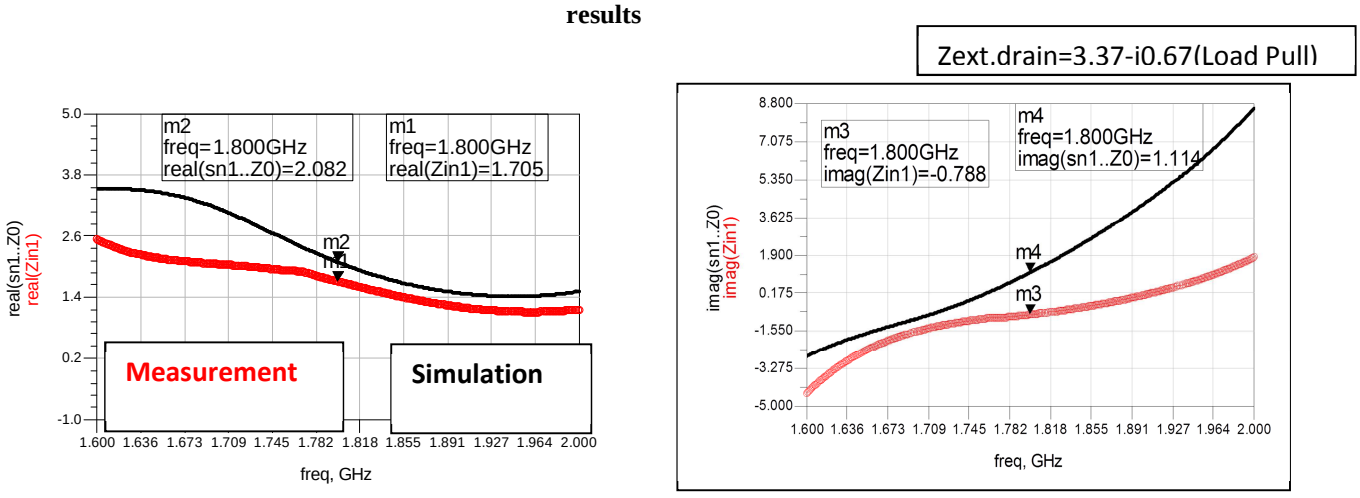


Figure 4.46.b Real and Imaginary drain impedance comparison between simulation and measurement results

From figure 4.46 it can be seen that the simulation model and the model board are rather similar at baseband and around RF frequencies, although there are significant differences between the exact values. For the frequencies in between they have the same overall shape but the resonances happen at different frequencies and large differences also in strengths. This might be one of the reasons why additional manual tuning was needed.

The picture of the drain impedance measurement board for the standard transistor is shown in figure 4.47

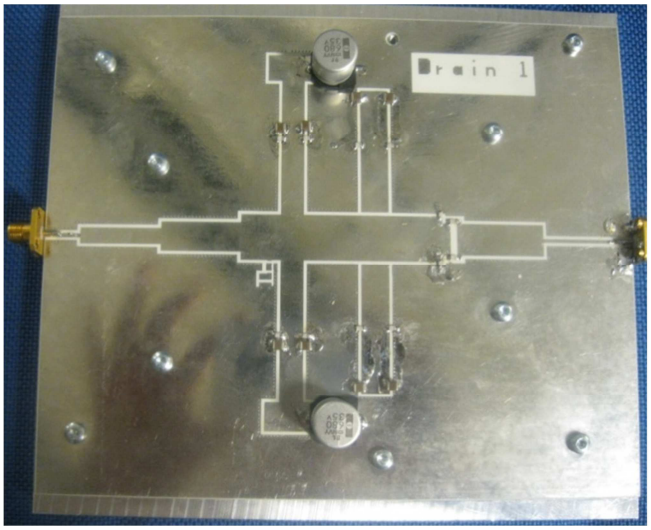


Figure 4.47 Drain impedance measurement board for the standard transistor

The obtained result comparing measurement and simulation for the tuned capacitor values over the whole simulation frequency is shown in figure 4.48

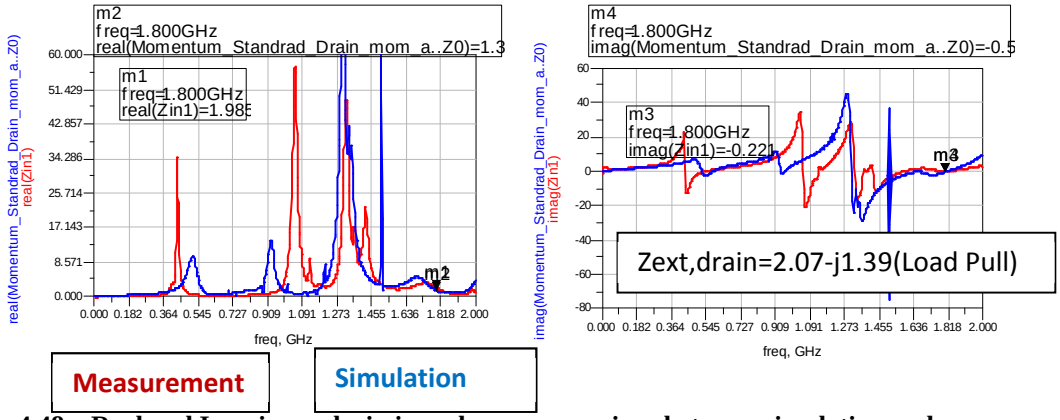


Figure 4.48.a Real and Imaginary drain impedance comparison between simulation and measurement results

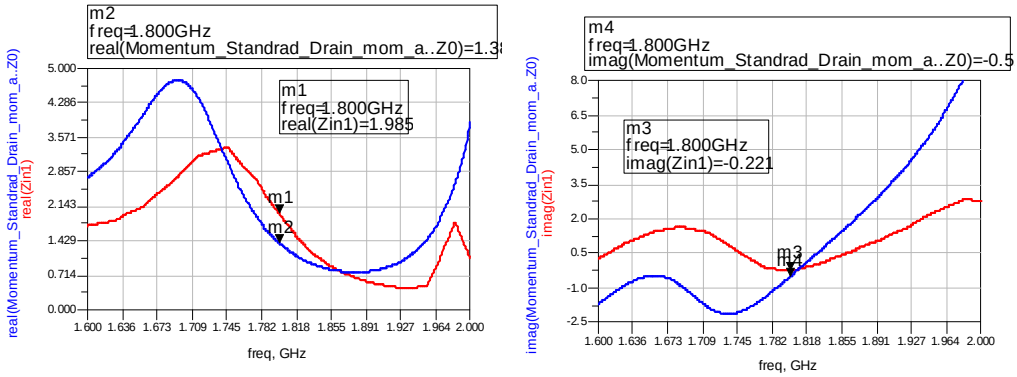


Figure 4.48.b Real and Imaginary drain impedance comparison between simulation and measurement results

From figure 4.48 it can be seen that the simulation model and the model board are quite similar at baseband and around RF frequencies as the transistor with internal decoupling case. For the frequencies in between they have overall the same shape but the resonances happen at somewhat different frequencies and somewhat different strengths. This might be one of the reasons why additional manual tuning was needed.

The picture of the gate impedance measurement board f of both transistors is shown in figure 4.49

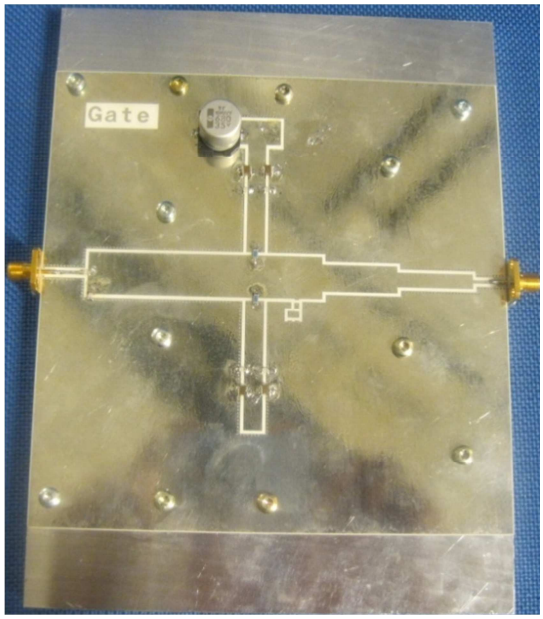


Figure 4.49 Gate impedance measurement board for the transistor with internal decoupling

The obtained result comparing measurement and simulation over the whole simulation frequency is shown in figure 4.50

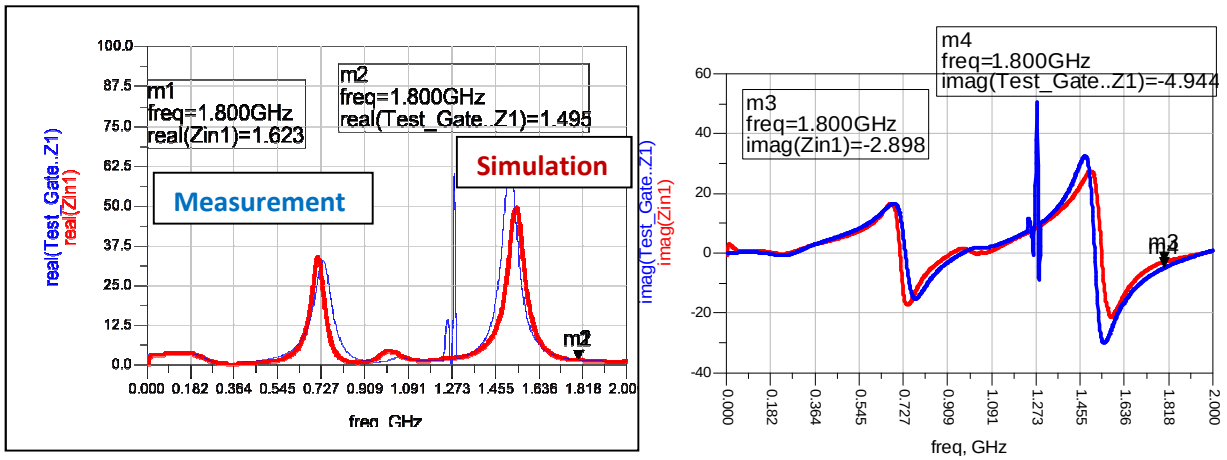


Figure 4.50.a Real and Imaginary gate impedance comparison between simulation and measurement results

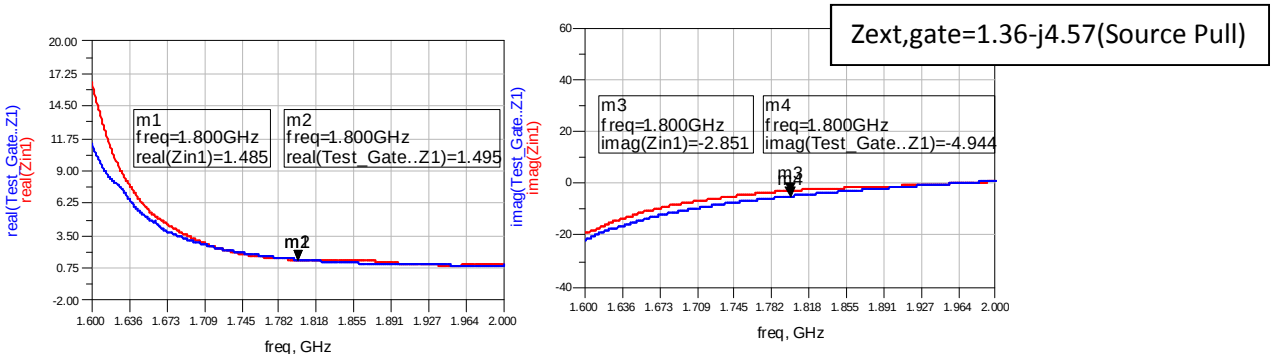


Figure 4.50.b Real and Imaginary gate impedance comparison between simulation and measurement results

From figure 4.50 it can be seen that the simulation model and the model board are quite similar at all frequencies except for that the measured resonance at approximately 1.05 GHz is much weaker than the corresponding simulated resonance at approximately 1.25 GHz. This shows that the input match was good which was also proved and discussed in section 4.22.

4.2.5.3 Other interesting simulations and measurements

Since the baseband impedance is so much different for the simulation and measurement other investigations were necessary to make sure where the difference is coming from. Also, it was necessary to check if the snubber resistors heat up to make sure if power is being dissipated in them

4.2.5.3.1 Investigating baseband impedance differences in measurement and simulation

For this investigation the procedure followed was first to measure the S-parameter of the drain/gate impedance board discussed in section 3.3.2.3 using VNA. After doing so, the transformer discussed in the same section was de-embedded using its characterized S-parameters. This process will move the reference plane to external drain/gate, which will give the whole part of the drain/gate circuit outside the drain/gate reference plane of the package. In principle if the transistor drain/gate package is approximated by a capacitance (which is the case when doing all the simulations), then

the simulation result when this S-parameter model is simulated should be quite similar to either the simulation result or the measurement result. The simulation setup is shown in figure 4.51

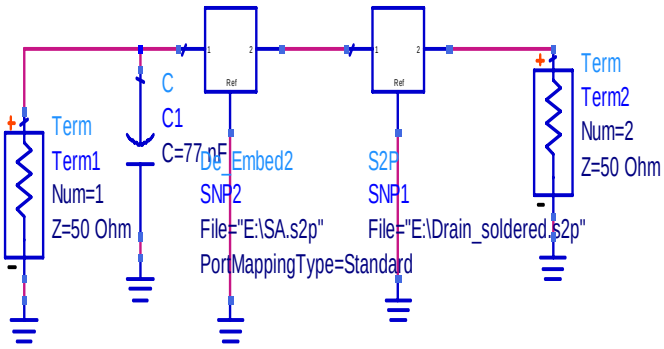


Figure 4.51 Simulation setup showing de-embedded transformer and drain S-parameter

In figure 4.51, SNP1 is a component in ADS which is used to read .s2p file for the two port S-parameter of the whole drain/gate impedance test board, SNP2 is a de-embedding component which is the inverse S-parameters of the transformer. Thus the cascade of SNP1 and SNP2 gives the measured S-parameters of the board part of the drain/gate circuit. The simulation results both for using S-parameter of the board together with transistor drain package capacitance and the original simulation results are shown below for both drains and for the gate

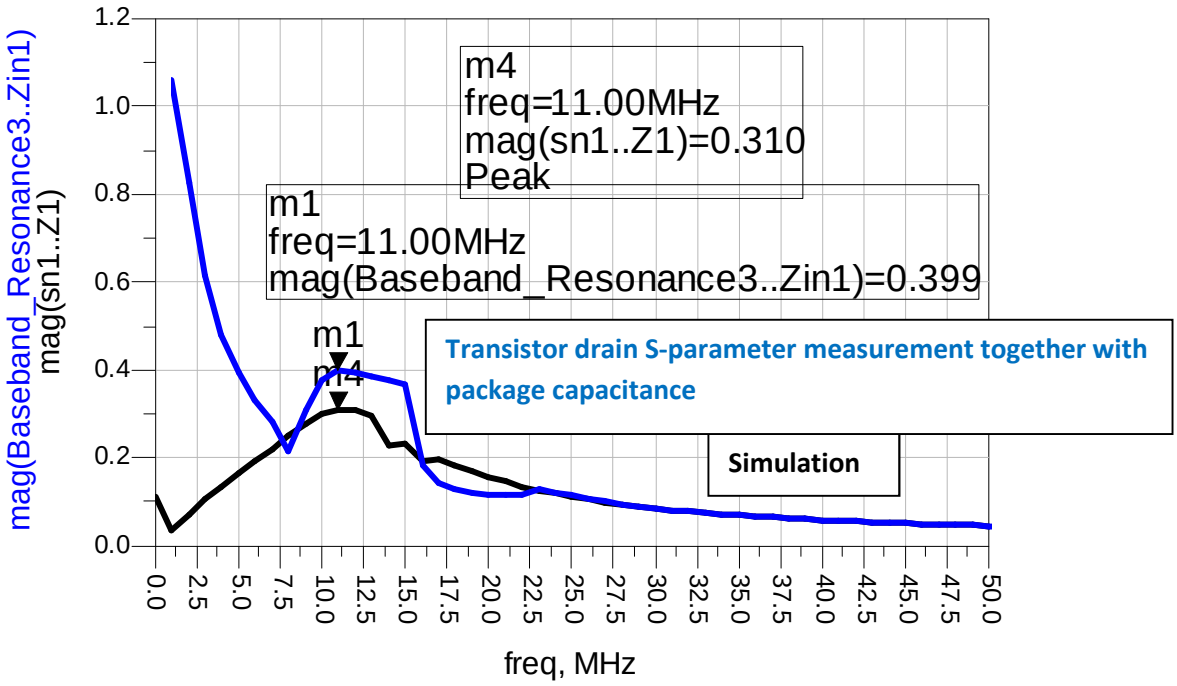


Figure 4.52.a Comparison between original simulation result and transistor drain s-parameter measurement together with approximated drain package capacitance for the transistor with decoupling

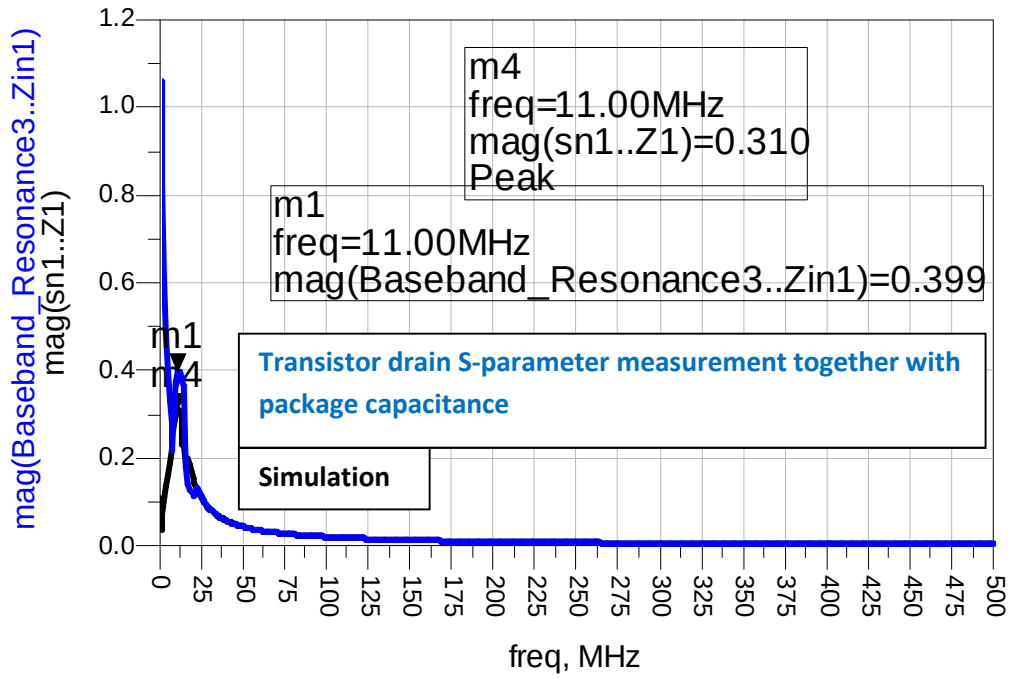


Figure 4.52.b Comparison between original simulation result and transistor drain s-parameter measurement together with approximated drain package capacitance for the transistor with decoupling

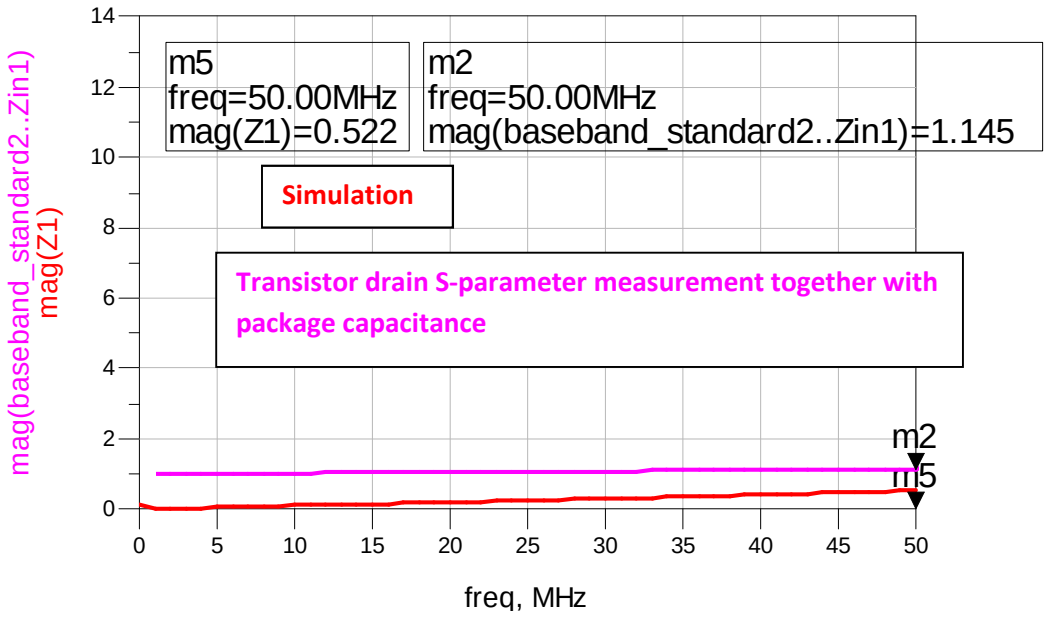


Figure 4.53.a Comparison between original simulation result and transistor drain s-parameter measurement together with approximated drain package capacitance for the standard transistor

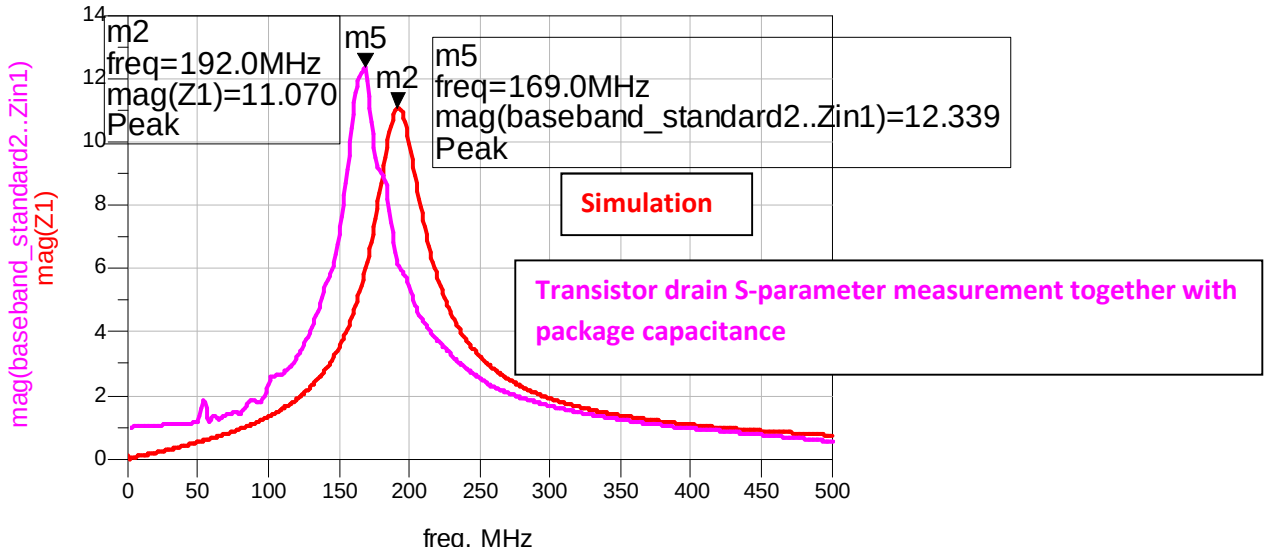


Figure 4.53.b Comparison between original simulation result and transistor drain s-parameter measurement together with approximated drain package capacitance for the standard transistor

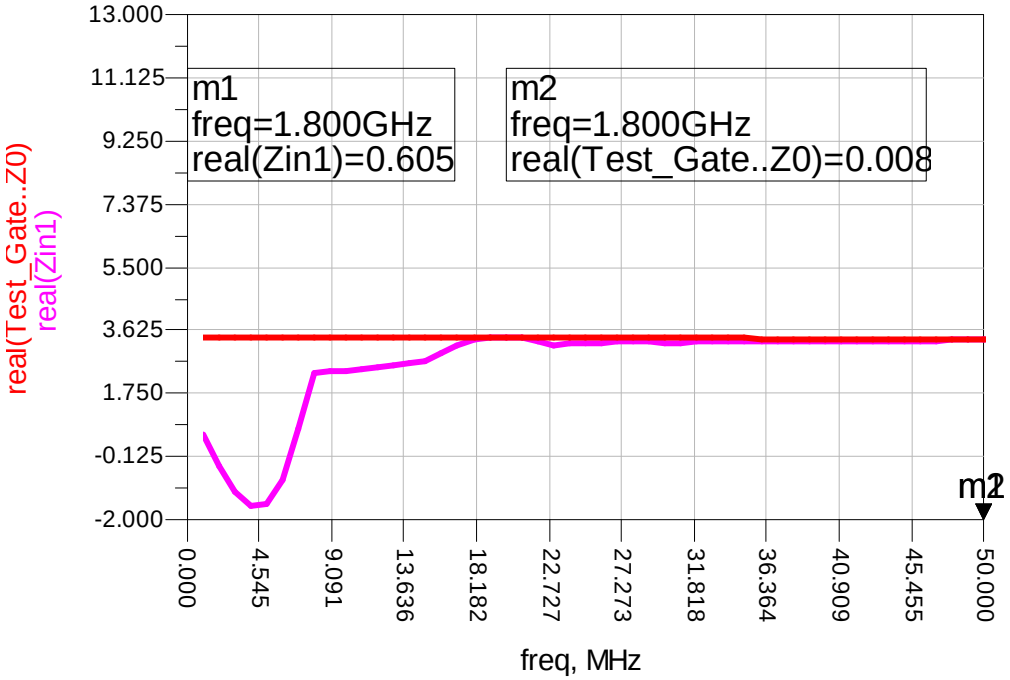


Figure 4.54.a Comparison between original simulation result, transistor gate s-parameter measurement together with approximated gate package capacitance for both transistors

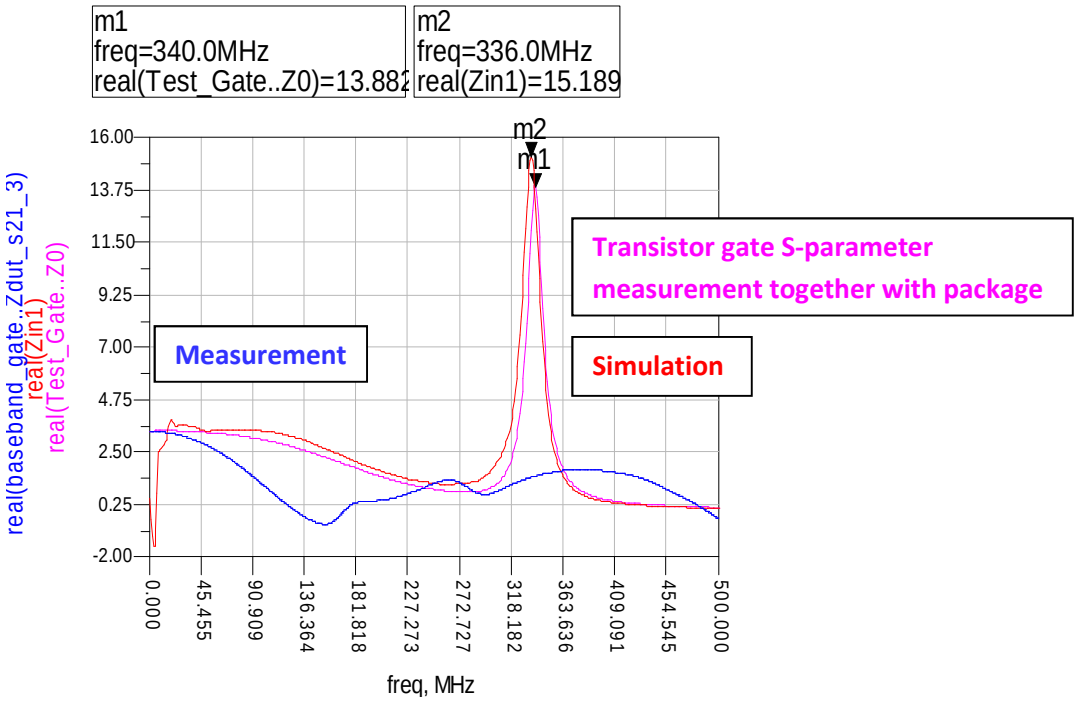


Figure 4.54.b Comparison between original simulation result, transistor gate s-parameter measurement together with approximated gate package capacitance for both transistors and measurement

From the above three figures (4.52,.53,.54), it can be seen that when the transistor package is approximated with a capacitance and simulated using the measured S-parameter of the board, it is quite similar to the simulation results. But the results are quite different for the very low frequencies. This difference is cause because the TRL algorithm frequencies start from 300 kHz and the next data point is 7 MHz, so ADS will interpolate the values in between which is not correct.

4.2.5.3.2 Infrared Camera Measurement

The snubber resistors used in the drain circuit of the two transistors should ideally have zero loss. This is due to the fact that the line with snubber resistor will be short circuited by the line without the snubber resistor for lower frequencies and both lines will be open circuit at the design RF frequency. This measurement was done by using infrared camera and checking if the resistor is heating up or not. The duty cycle for the CW measurement discussed in section 4.2.3 was 10 % but now the duty cycle was increased to heat up the PA and check if there is any dissipation in the snubber resistors. First the snubber resistors were coated with a black spray which has emissivity of 0.965 which is quite close to a black body emissivity which is 1. This coating will help in creating a uniform surface emissivity so that relative ability of the surface to emit energy by radiation is also uniform. The photo of the snubber resistors coated is shown in figure 4.55

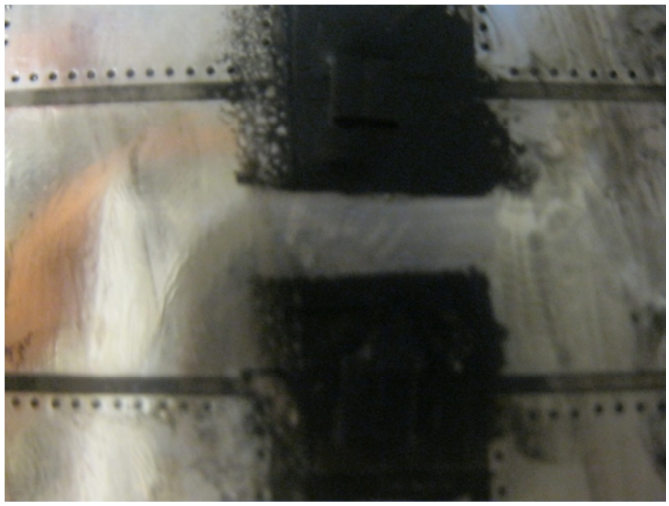


Figure 4.55 Snubber resistors coated with a black spray with emissivity of 0.965

The infrared camera pictures before the PA starts working and the plot of this picture is shown below

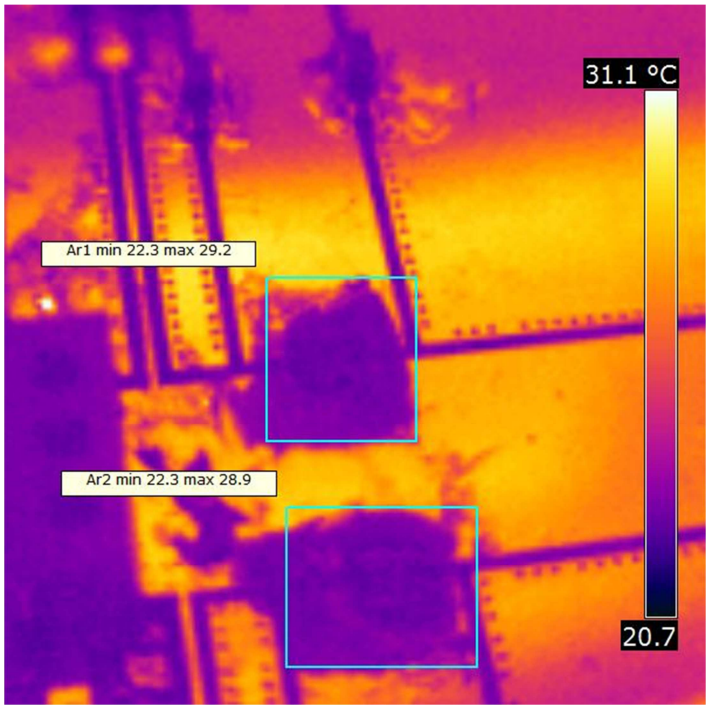


Figure 4.56 Infrared camera picture of the snubber resistors for the transistor with internal decoupling with the PA off

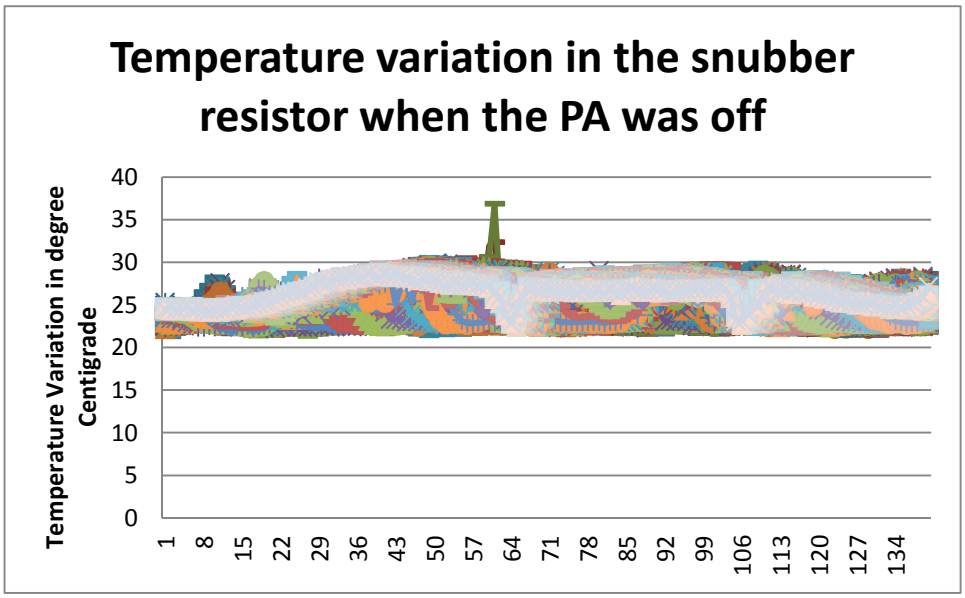


Figure 4.57 Plot of exported data from Figure 4.56(Temperature variation versus number of data)

From figure 4.57, it can be seen that the maximum temperature is around 30^0C and the minimum is around 20^0C . The same result was obtained for the standard transistor since both are at the same room temperature. Once the PA starts working with a higher duty cycle, again another picture was taken for both transistors. This is shown in figure 4.58

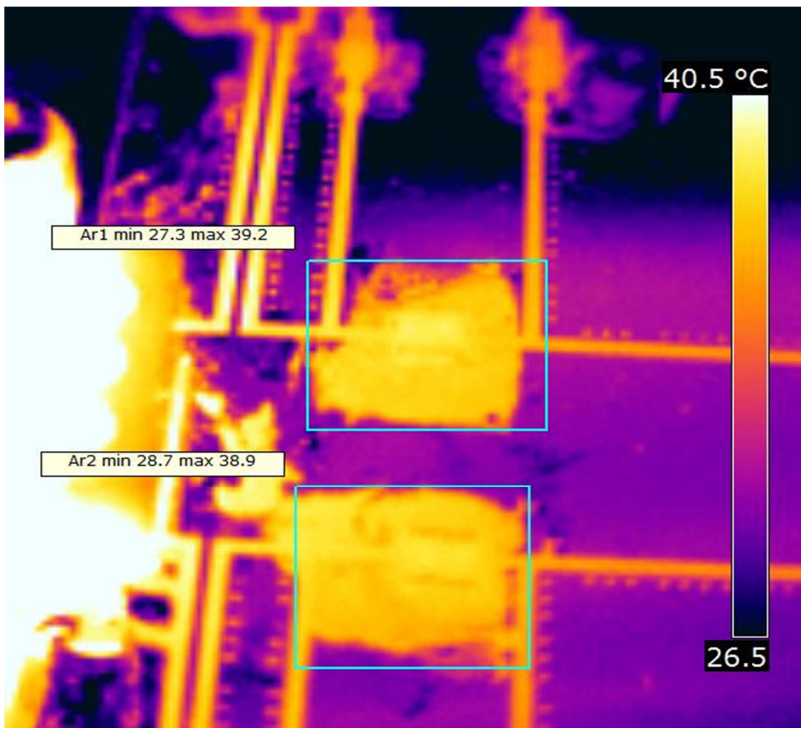


Figure 4.58 Infrared camera picture of the snubber resistors for the transistor with internal decoupling PA running with 30% duty cycle

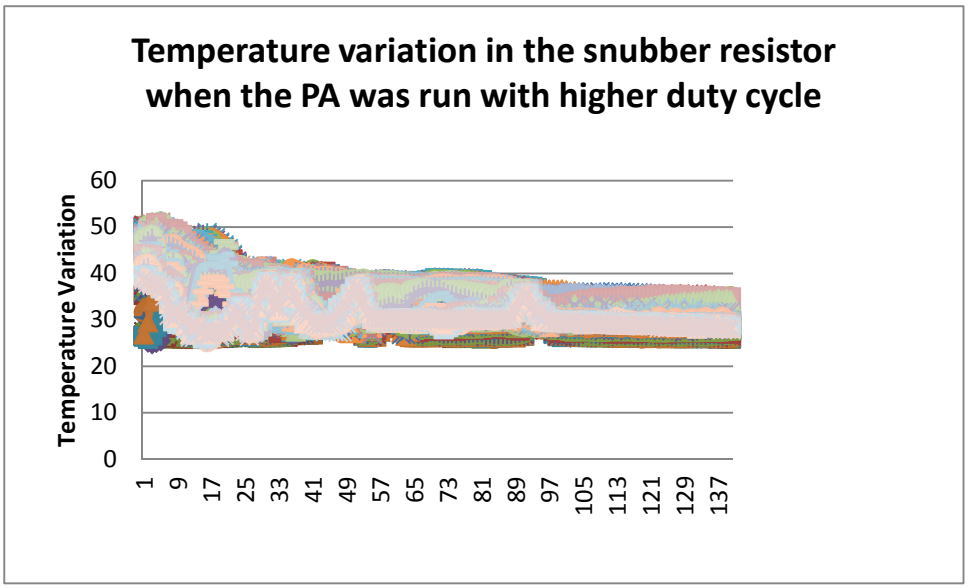


Figure 4.59 Plot of exported data from Figure 4.58 (Temperature variation versus number of data)

From figure 4.58 and 4.59 it can be seen that the temperature variation in the snubber resistors is between $\mathbf{26^0}\boldsymbol{C}$ and $\mathbf{40^0C}$. The same result was obtained for the standard transistor so it was not included in this section to avoid redundancy.

Chapter 5

5.1 Discussion and Conclusion

Bias circuits affect the performance of RF PA by causing variation in the baseband impedance which together with RF current varies the baseband voltage. The effects of different bias circuits were discussed. Two prototype transistors (without package information) were thoroughly and carefully studied including RF and baseband performance, with emphasis given to baseband performance. The first transistor was with drain internal decoupling and the other one was standard transistor. Snubber circuit was used to attenuate the resonance caused by the DC-Feed line together with the transistor gate or drain capacitance. This snubber circuit consists of a λ/4 DC-Feed line together with a resistor called a snubber resistor. In order for the bias circuit not to affect the RF match, the λ/4 DC-Feed line should be carefully designed. There is a specific optimal value of the snubber resistor which gives the smallest possible baseband impedance. From the design it was noticed that the optimized value of the characteristic impedance λ/4 DC-Feed line (without snubber resistor) is much higher for the transistor with internal decoupling than for the standard transistor.

Load Pull measurement RF impedance and the final tuned board RF impedance values were different for both transistors. This can be due to measurement error in load pull or TRL calibration error while characterizing the impedance transformer for the impedance measurement board. From load pull measurement it was proven that both transistors have the same RF performance. This performance was obtained for the CW measurement on test PA with internal decoupling transistor but for the standard transistor the RF match was not perfectly found. Due to lack of time and the scope of the project which is the baseband performance the results obtained were taken as final results. Even though much attention was given to base-band-width, from some preliminary analysis using load pull data and measurement results it was evident that the RF bandwidth of both transistors is package limited. From the two tone measurement, there was a voltage variation for both transistors but for the standard transistor the magnitude of voltage variation was more pronounced. At approximately same frequencies where baseband drain voltage variation occurred, there is also a variation in IM3 products for both transistors. This measurement result is fairly the same when other center frequency is also used which indicates the variation might be caused from baseband resonance.

For the baseband performance, as expected the transistor with internal decoupling exhibits lower impedance variation while the standard transistor shows a higher and narrow resonance peak which would be hard to pre-distort. These resonances for both transistors were also witnessed in causing baseband drain voltage variation at the same frequency as the baseband impedance resonance. This result shows consistency and proves the theory why studying baseband impedance is necessary. The simulation and the measurement results for the baseband impedance are significantly different except for very low baseband frequencies since for the simulation the transistor package was approximated only with drain/gate capacitance. Another study was performed by simulating the measured S-parameter of the drain/gate board and the same drain/gate capacitance. This result was quite similar with the simulation where the transistor package was approximated with capacitance. This can prove that a better transistor package model is needed to simulate base-band effects over the relevant frequency interval. So from this it is evident that approximating the transistor with only a capacitance is not a good enough approximation. To see the effect of the snubber resistors, there

was a test made by short circuiting the line with a piece of metal and by increasing the snubber resistor value from the optimum value found with optimization. The result shows that the resonance peak will increase for both cases. This indicates that despite the problem with accuracy of the transistor model (at relevantly high frequency) used to optimize snubber resistor value, the chosen values seen to be close to optimium. The snubber resistors ideally should not have any loss since at low frequency the snubber line (λ/4 line in series with snubber resistor) will be short circuited with the second non-snubber (λ/4 line only) line and at high frequency both lines are open circuit. Infrared camera was used to check if the snubber resistors are being heated up which indicates loss in the circuit. This measurement shows that there is 10^0C difference between the PA turned off and on with higher duty cycle.

5.2 Future Work

For future work, more emphasis can be given to study RF bandwidth together with base-band-width. Optimization can be done with emphasis given to RF bandwidth along with optimization goals discussed in this report

. During CW measurement, the power supply bias level was increased to compensate for cable losses. But in the future the best is to use a four-terminal power supply, two terminals for the power output (+ and -) and two for sensing the output voltage. And to connect the sensing terminals with separate cables directly at the PA big decoupling capacitors. Then the power supply will automatically compensate for the DC cable losses. Because to keep exactly that same drain bias at the PA with lossy DC cables the power supply has to output different voltages for different output RF amplitudes.

For Infrared camera measurement, the measurement was only taken at the center frequency but it would be good to have measurements for at least three frequencies: design centre frequency, low and high end of RF bandwidth. It would also be good to try to find out some way to calibrate the temperature increase to dissipated power. Also the size of the PA can be optimized more since both fabricated test PAs are large in size when compared to the traditional PA sizes.

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Appendix

I List of Figures

II List of Tables

III Glossary of Acronyms

AC	Alternating Current
A, mA	Amperes, milli-Amperes
ADS	Advanced Design System
C	Capacitance
Class F-1	Inverse Class-F
CW	Continuous Wave
DC	Direct Current
dB	Decibels
dBc	Decibels (reference to carrier power)
dBm	Decibels (reference to 1mW)
DC	Direct Current
DUT	Device-Under-Test
EM	Electro-magnetic
Freq., f	Frequency
Hz, GHz	Hertz, Giga-Hertz
I, i	Current
I_{dq}	Quiescent Drain Current
IM	Inter-modulation
L	Inductance
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LP	Load-Pull
m, mm,μm	metres, mili-meter,micro-metres
P	Power
PA	Power Amplifier
R	Resistance

RF	Radio Frequency
S-parameters	Scattering Parameters
SMA	Sub-Miniature version A
TRL	Thru, Reflect, Line
W	Watts
T	Dielectric Thickness
VNA	Vector Network Analyzer
X	Reactance
Z	Impedance
η	Efficiency
Ω	Ohms

IV List of Measurement equipments used

1. Rohde & Schwarz , FSG Spectrum Analyzer

2. Agilent Technologies, N5230A, PNA-Network Analyzer

3. MXG,N5182A, Vector Signal Generator

4. MIL MEGA, AS0102-8B, Pre-Amplifier

5. Narda, Model 3022,Bi-Directional Coaxial Coupler

6. Narda, Model 766-10, attenuator

7. Mini Circuits, 15542 ZAPD-21, Splitter

8. Hewlett Packard, 620088, Power Sensor

9. Weinschel Corp, 53-20-34, 500 W attenuator

10. Microlab/FXR , CK-18N, Directional Coupler

11. Huber+Suhner, 8687, Low Pass Filter

12. Hewlett Packard , G8250, Power Sensor

13. Fluke, 8842A, Multi-meter

14. Hewlett Packard, 6622A, System DC Power Supply

And Matlab GPIB program provided by Ericsson PA Department.