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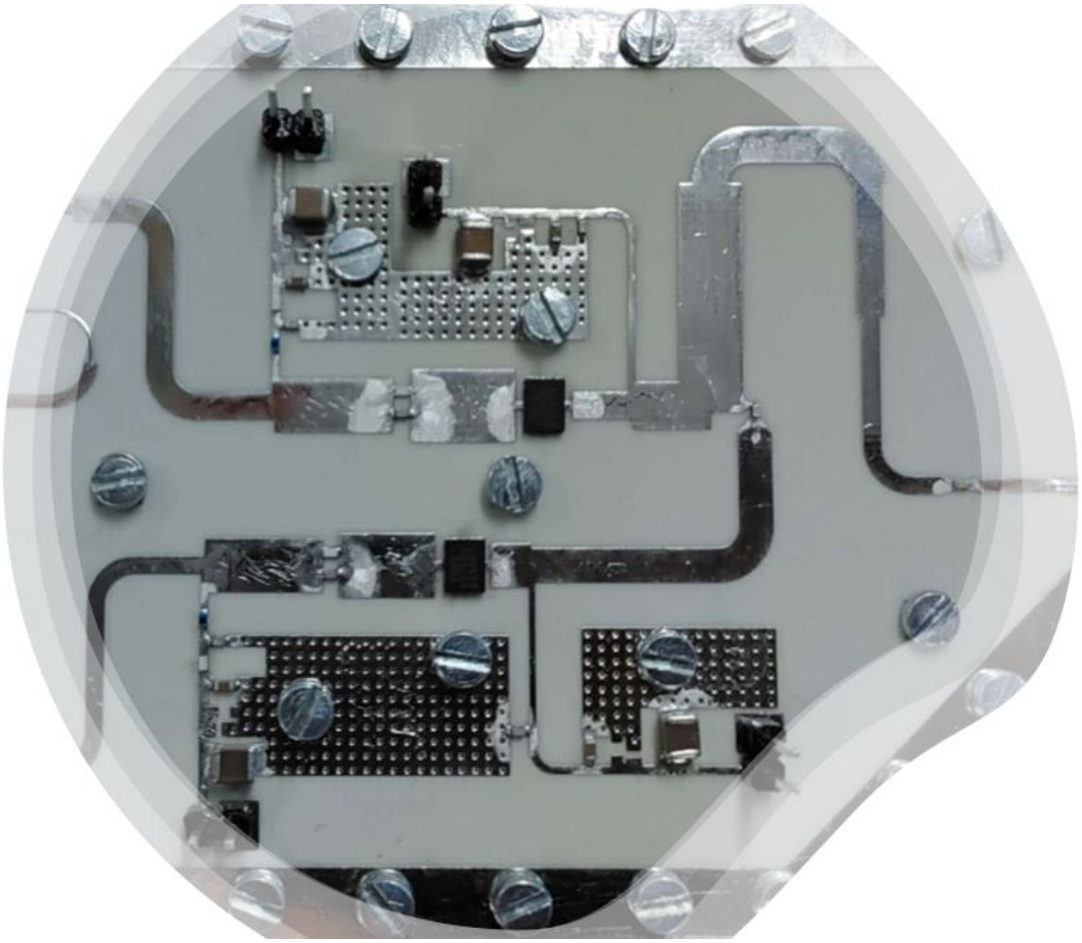

Design and Validation of a Concurrent Dual-Band GaN Doherty Power Amplifier

Master's thesis in Wireless, Photonics and Space Engineering

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DEPARTMENT OF MICROTECHNOLOGY AND NANOSCIENCE
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Abstract

In the current era characterized by rapid advancements in wireless communication, the demand for high data rates, multi-band operation and low power consumption in communication systems like mobile base stations, poses significant challenges. To address these challenges, it is imperative to explore and devise new power amplifier (PA) solutions that conform to these stringent requirements. This thesis presents a comprehensive solution in the form of a dual-band Doherty PA (DB-DPA) to meet these pressing requirements. DPAs have gained considerable popularity due to their ability to achieve high back-off efficiency across a wide range of output power levels. The primary objective of this research is to design and simulate a symmetrical DB-DPA using state-of-the-art GaN-HEMT technology, for the frequency bands of 1.85 and 2.65 GHz. The load modulation network comprises a wideband combiner followed by a Chebyshev transformer. Subsequently, the designed DB-DPA is fabricated, measured, and the obtained results are presented and analyzed in detail.

Through extensive measurements, this study demonstrates that the proposed DB-DPA design delivers satisfactory performance in terms of drain efficiency (DE) and power gain for both the lower and upper-frequency bands of 1.85/2.65 GHz with a bandwidth of 100 MHz each. At a peak power of 47.9/47.3 dBm, the DB-DPA achieves a DE of 55.6/54.5%. Furthermore, at a 6 dB back-off level, the DB-DPA exhibits a DE of 41.2/44.6% and a gain of 19.5/15 dB for the desired frequencies. These characteristics position this design as a promising candidate for communication applications. The findings presented in this research emphasize the potential of the proposed DB-DPA design and provide a viable solution that meets the growing requirements of the wireless industry. The comprehensive investigation conducted through simulations and measurements contributes to the body of knowledge in the field and provides valuable insights for further advancements in DB-DPA design.

Keywords: Doherty, Power Amplifier, GaN-HEMT, Efficiency, Dual-Band

Acknowledgements

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Finally, I am deeply grateful to my wife, Maryam, and my son, Zarrar, for bearing with my routine during this time frame.

Jamal Ur Rasool Haider, Gothenburg, June 2023

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis listed in alphabetical order:

PA	Power Amplifier
DPA	Doherty Power Amplifier
BER	Bit Error Rate
PAPR	Peak to Average Power Ratio
ACPR	Adjacent Channel Power Ratio
DSP	Digital Signal Processing
IMN	Input Matching Network
OMN	Output Matching Network
LMN	Load Modulation Network
LSSP	Large Signal Scattering Parameters
DSP	Digital Signal Processing
DE	Drain Efficiency
PAE	Power Added Efficiency
Pout	Output Power

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1

Introduction

1.1 Motivation

Radio Frequency (RF) Power Amplifiers (PAs) are one of the most important components in modern-day wireless systems like mobile phones, Wi-Fi, and satellite communication, etc. These amplifiers play a crucial role as they are responsible for boosting the signal power to cover larger distances, penetrate obstacles, and reach farther-located receivers.

PAs are the most dominant and power-consuming component within wireless transmitters. In an RF front end, PAs are located at the end of transmit chain as shown in Figure 1.1. Their non-linear characteristics have a profound impact on key performance metrics, including the adjacent-channel power ratio (ACPR) and the bit error rate (BER). As communication standards continue to evolve, more intricate signal modulation schemes have been introduced to meet the ever-increasing demand for data transmission capacity. Therefore, the design of RF PAs assumes growing importance due to the need to tackle these design challenges arising from wider bandwidth and higher peak-to-average power ratios (PAPR). It is essential to recognize that communication systems rarely operate at peak power levels but instead operate at various output power back-off (OBO) levels. As the back-off level increases, the efficiency of the PA experiences a significant decline, resulting in higher DC power consumption. Therefore, it becomes imperative to tackle these challenges and optimize PA efficiency to enhance the overall performance and power consumption of modern communication systems.

Various strategies have been proposed in the literature to address the issue of back-off efficiency in PAs. These strategies can be broadly categorized as Supply Modulation (SM) and Load Modulation (LM). LM entails the modulation of load impedance, while supply modulation involves controlling the supply voltage using an envelope amplifier. In SM, there are different sub-categories like Kahn Envelope Elimination and Restoration (EER), and Envelope Tracking (ET) [1]. EER utilizes a high-efficiency PA that is saturated by a driven switching current PA. The switches generate a constant envelope signal that carries both phase and amplitude information of the input signal. On the other hand, ET employs voltage supply tracking in a linear PA. However, these methods have limitations such as reduced efficiency in the modulator and difficulties in synchronizing the phase and envelope paths in the PA. These limitations can result in increased size and cost.

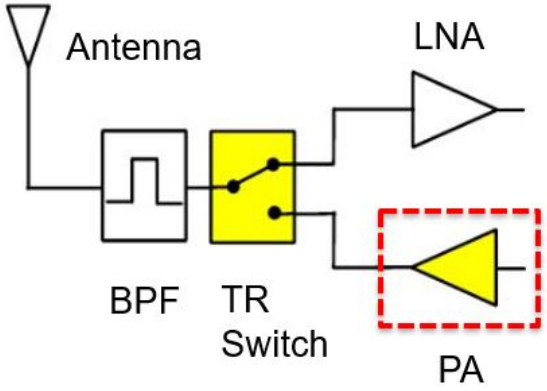


Figure 1.1: RF front end of a communication system

The other technique, known as LM, offers the ability to dynamically adjust the load seen by the amplifier in response to different input drive levels. This can be achieved by employing a varactor-based tunable matching network or by incorporating the principle of active load modulation (ALM) [2] which will be elaborated in detail in the subsequent chapters. In recent years, several new architectures employing LM have also been proposed, including the load-modulated balanced amplifier (LMBA)[3], the distributed efficient power amplifier [4], and the circulator load-modulated amplifier (CLMA)[5], [6], [7]. These techniques present potential solutions to enhance efficiency at reduced power levels.

1.2 Aim

The main goal of this thesis is to design a DB-DPA intended for radio links and mobile base stations. The desired frequency bands are 1805-1870 MHz and 2620-2690 MHz but the DB-DPA is designed for 1800-1900 MHz and 2600-2700 MHz to account for any process variation. The design is done in order to achieve the best possible efficiency at 6 dB output back-off (OBO) and maximum output power at saturation.

1.3 Constraints

The transistor used in the design process is Wolfspeed CGHV27030S which is a high-power device in Gallium Nitride technology capable of generating 30W of output power, shown in Figure 1.2. The substrate used for PCB fabrication is Rogers R4003c with a dielectric constant of 3.55 and a thickness of 0.508 mm. The DB-DPA is designed to generate nearly 47 dBm of output power with higher than 50% 6 dB OBO efficiency. Keysight Advanced Design System (ADS) is used for simulations while MATLAB is used for post-processing of measured data.

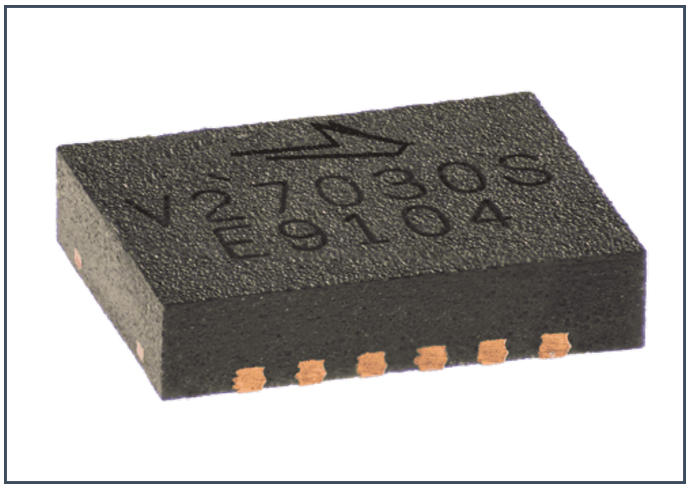


Figure 1.2: Wolfspeed CGHV27030S GaN HEMT

1.4 Outline

The thesis report is organized as follows: In Chapter 2, a detailed discussion is presented on PAs in general and DPA theory in particular. A complete step-by-step design flow is provided in Chapter 3 along with simulation results. Chapter 4 contains the complete measurement process description along-with detailed results and analysis. Finally, Chapter 5 concludes the thesis work.

2

Theory

This chapter discusses the theory of PAs in detail. First, the important design parameters required for PA design are discussed and elaborated. Subsequent to this, different classes of PAs are discussed followed by efficiency enhancement PA architectures. Finally, a detailed theory of DPAs is presented which concludes this discussion.

2.1 Power Amplifiers

RF PAs are used to amplify RF signals in wireless communication systems. The primary function of an RF PA is to receive a low-power RF signal and increase its power to a higher level that can be transmitted through the antenna to the receiver. This amplification process is essential in maintaining a high signal-to-noise ratio (SNR) and preventing signal degradation, which can lead to poor signal quality and reduced communication range.

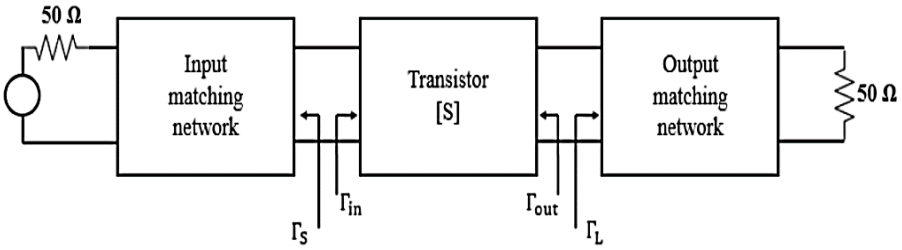


Figure 2.1: Block diagram of an ideal RF PA [8]

Figure 2.1 shows the block diagram of an ideal PA. In the heart of the PA lies the active device i.e., the transistor. Matching networks are required at both the input and output of the active device to transform the gate and drain impedances of the active device to a system impedance, usually 50 Ω. PAs are characterized by their output matching network (OMN) design as it requires power-matching in contrast to conjugate matching as in the case of max-gain amplifiers and low noise amplifiers (LNA). RF PAs come in various designs and configurations, each tailored for specific applications and frequencies. The selection of the right type of PA is critical for optimal system performance, as the PA's efficiency, linearity, and output power all affect the overall system performance. In this context, this introduction aims to provide a brief overview of the main figures of merit, classes of RF PAs, their basic operating principles, and some of the key factors that affect their performance.

2.2 Figures of Merit

A figure of merit (FOM) is a quantity or parameter used to characterize the performance of a device, system, or method, relative to its alternatives. In engineering, FOMs are often defined for particular materials or devices in order to determine their relative utility for an application. For the design of different components, different FOMs are considered. In the case of PAs, the most important FOMs are the output power, efficiency, and gain. These are elaborated in the following subsections [1].

2.2.1 Output Power

Output power is one of the most important considerations in the design of a PA as its basic purpose is to generate high power. For small-signal amplifiers, maximum gain is achieved with simultaneous conjugate matching at the input and output of the amplifier i.e., $\Gamma_S = \Gamma_{in}^*$ and $\Gamma_L = \Gamma_{out}^*$. However, simultaneous conjugate matching does not result in maximum output power and thus for PA design, a different design approach is required.

For small-signal amplifiers, the full utilization of both the current and voltage swings is less significant. However, in the case of PAs both the swings must be utilized to their full potential, to generate high output power. The optimum load that results in full utilization of both the voltage and current swings is called optimum load 'R_{opt}' or 'Cripps Load' given by the following relation [1]:

$$R_{opt} = \frac{V_{max} - V_{knee}}{I_{max}} \tag{2.1}$$

where V_{max} is the maximum breakdown voltage of the active device, V_{knee} is the knee voltage and I_{max} is the maximum drain current which can be obtained by plotting the IV-curves.

Compared to a small-signal amplifier, this load ensures that maximum power is extracted from the device. This phenomenon is illustrated in Figure 2.2 where it can be observed that for simultaneous conjugate matching, the load-line in blue color, is small resulting in smaller voltage and current utilization. With power matching, the load-line is large, giving higher current and voltage swings which result in higher output power. Figure 2.3 proves this where it is evident that a significant improvement in output power can be achieved using power matching. Output power is generally expressed in dBm.

2.2.2 Power Gain

The amplification of a PA is quantitatively expressed as the ratio between the output power and the input power. This ratio is often called the power gain of the amplifier, expressed in dB. As mentioned earlier, within communications systems, amplifiers serve the crucial purpose of increasing the signal level to meet the required

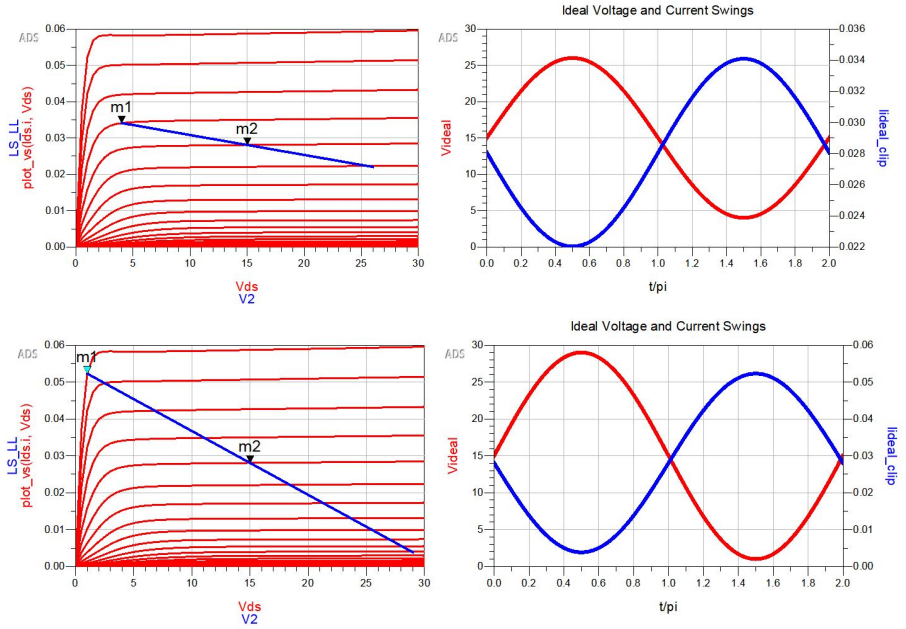


Figure 2.2: Load-line comparison of simultaneous conjugate-matched load with power-matched load

threshold in transmitters. However, the presence of inherent non-linearities in these devices introduces a phenomenon called gain compression. This compression effect occurs when a substantial signal is introduced to the amplifier, causing the gain to deviate from its linear behavior. As a result, careful consideration must be given to the design and optimization of amplifiers to ensure reliable and efficient signal amplification. The gain of an amplifier is expressed as:

$$Gain = \frac{P_{out}}{P_{in}} \tag{2.2}$$

2.2.3 Efficiency

In practical communications systems, PA is integrated as a subsystem and it consumes the highest amount of DC power from the supply. The efficiency of a PA is established in the literature as the ratio of output power to the DC power consumed. The efficiency of a PA is sometimes referred to as drain efficiency (DE) denoted by η, and is given as:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.3}$$

There is an alternative definition of efficiency that takes into account the RF drive power called power added efficiency (PAE). Generally, PA designers prefer to use PAE over DE to characterize the PA performance.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.4}$$

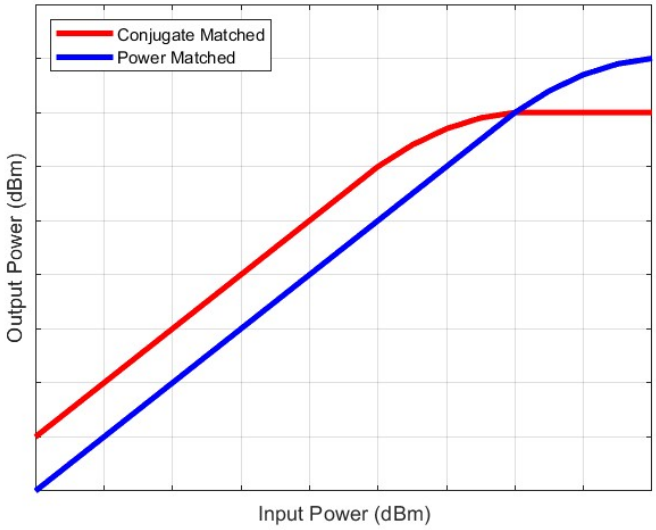


Figure 2.3: Output power comparison for maximum gain matching with power matching

The RF power and DE depend on the conduction angle of the current swing. The DE is around 50 % for a conduction angle of 2π and increases as the conduction angle is reduced. Conversely, the RF power increases with an increase in the conduction angle but the maximum power is achieved for an angle of 1.36π. The variation of RF power and DE with the conduction angle gives rise to different classes of PA which will be detailed in the following subsections.

2.3 Classes of Power Amplifiers

RF PAs operate in different modes depending on the design goal. These modes are known as 'classes' and are categorized based on whether the amplifier functions as a voltage controlled current source or a switch. Classes in which the active device works as a voltage-controlled current source are known as linear classes. These include Class-A, -AB, -B, and -C, which are classified based on their conduction angle. Among these classes, Class-A amplifiers are the most linear, while Class-C amplifiers are the most efficient.

The efficiency of the amplifier can be theoretically increased up to 100% by operating it in switch mode, but this mode is highly non-linear. Classes D, E, and F are examples of switch-mode PAs. In this context, linear RF PAs are particularly relevant to design. They operate as voltage controlled current sources and are intended to provide linear amplification of the input signal. The term 'linear' refers to the amplifier's ability to maintain the linearity of the input signal while amplifying it. The choice of amplifier class is crucial in achieving the desired level of linearity and efficiency in a specific application.

2.3.1 Class-A Power Amplifiers

Class-A amplifiers utilize the complete input signal as their conduction angle is 2π. This entails that the device is conducting at all times irrespective of any input RF signal. To operate in class-A, the biasing of the device is chosen in the center of the IV-curves. The class-A amplifiers are the most linear in their response till their compression point is reached. These amplifiers are linear but have lower efficiency as DC power is consumed even when there is no RF signal. The general expressions for DC and RF currents for a PA are given as [1]:

$$I_{RF} = \frac{I_{max}}{2\pi}.\frac{\alpha - sin(\alpha)}{1 - cos(\alpha/2)} \tag{2.5}$$

$$I_{DC} = \frac{I_{max}}{2\pi}.\frac{2sin(\alpha/2) - \alpha cos(\alpha/2)}{1 - cos(\alpha/2)} \tag{2.6}$$

The RF and DC powers for class-A operation can be calculated using the above relations. The conduction angle of 2π simplifies these relations and is given as:

$$P_{RF} = \frac{V_{RF}I_{RF}}{2} = \frac{I_{max}V_{max}}{8} \tag{2.7}$$

$$P_{DC} = V_{DC}I_{DC} = \frac{I_{max}V_{max}}{4} \tag{2.8}$$

From Equations (2.7) and (2.8), it is evident that the maximum theoretical DE that can be achieved in class-A operation is 50%. In practical design, this value will be even lower due to the non-ideal behaviour of the device.

2.3.2 Class-B Power Amplifiers

The amplifiers which operate in class-B have a conduction angle of π, implying that the active device conducts for only half of the time. To operate in class-B, the transistor is biased at the pinch-off resulting in a rectified current waveform having no negative swing. Furthermore, it is required to short-circuit the harmonics to achieve a class-B waveform. Class-B amplifiers are less linear compared to class-A but more efficient. For a class-B PA, the RF power remains the same as class-A, while the DC power at peak power level is given as:

$$P_{DC} = V_{DC}I_{DC} = \frac{I_{max}V_{max}}{2\pi} \tag{2.9}$$

Since the DC power consumption is lower in this case, the resultant efficiency is higher. The maximum theoretical drain efficiency for class-B operation is found to be 78.5%.

2.3.3 Class-AB Power Amplifiers

Class-AB amplifiers are the amplifiers that have a conduction angle between π and 2π. To achieve this, the device is biased between the class-A and class-B bias points resulting in a clipped negative current swing. These amplifiers are less efficient than class-B and less linear than class-A but the freedom of biasing provides the designer with the option to compromise either on linearity or efficiency, depending on the application.

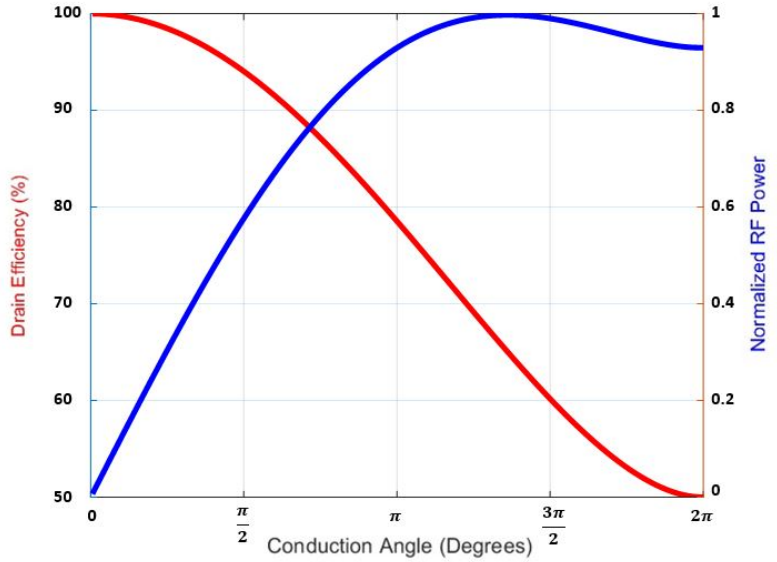


Figure 2.4: Variation of RF power and DE with current conduction angle.

Using equations (2.5) and (2.6), the RF and DC power consumption for class-AB operation can be calculated. The variation of RF output power and efficiency with respect to the conduction angle is illustrated in Figure 2.4. It is evident from Figure 2.4 that class-AB amplifiers can yield the highest output power compared to the other classes. The conduction angle which yields maximum output power can be calculated and is found to be 1.36π rad which corresponds to DE of 65%.

2.3.4 Class-C Power Amplifiers

A class-C amplifier is biased at a level below the pinch-off point, resulting in a reduced conduction angle of less than π. Consequently, the device conducts for less than half of the signal duration. This class of amplifiers demonstrates lower gain and output power with a higher presence of harmonic content, contributing to its highly nonlinear nature. The decreased gain necessitates driving the device with a larger input signal, which in turn diminishes the PAE. Similar to class-B, it is required to short-circuit the harmonics to achieve a class-C waveform. In theory,

class-C amplifiers exhibit 100% drain efficiency. The PA classes with their respective load-lines are illustrated in Figure 2.5.

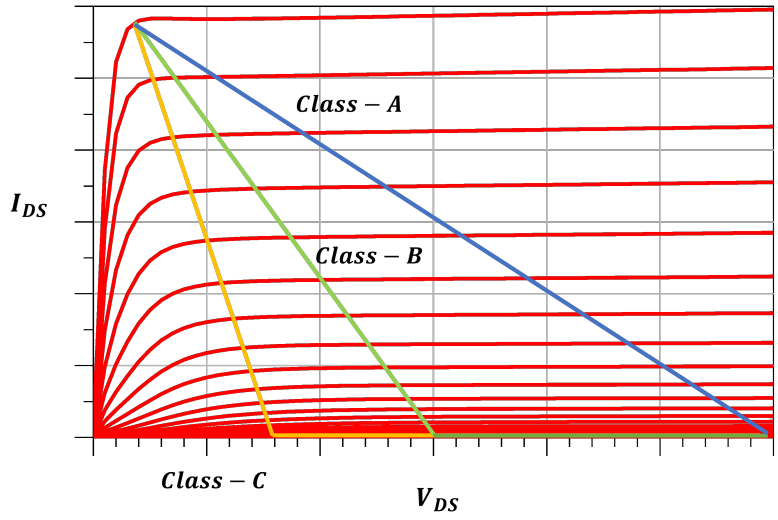


Figure 2.5: Loadlines corresponding to PA classes

2.4 Efficiency Enhancement Techniques

One of the major problems with PAs is that conventional PAs exhibit maximum efficiency at a single power level, which is typically near the maximum rated output power of the device. As the output power is reduced from this level, the efficiency drops sharply and heat dissipation increases resulting in a much lower efficiency. Efficiency enhancement techniques have been available for several years and can be effective in addressing this challenge [1]. Most of the efficiency enhancement techniques were invented in the early era of radio broadcasting. Three classical techniques that fall into this category are the Doherty PA, the Outphasing PA initially proposed by Chireix, and the EER technique demonstrated by Kahn. These techniques involve the usage of dynamic load modulation (DLM) and dynamic supply modulation (DSM).

DSM is an effective method employed to enhance efficiency by dynamically reducing the drain bias when the transistor drive level is backed-off. Similarly, DLM involves the dynamic adjustment of the load impedance when the transistor operates at a backed-off state. DLM comprises two principal categories, varactor-based modulation and active load modulation (ALM). The varactor-based method utilizes varactors to achieve precise load adjustments, whereas the ALM technique involves active current injection for LM in a transistor. An illustrative example of the ALM based technique is the well-known DPA, which will be comprehensively explained in subsequent sections. The concept of ALM can be effectively illustrated by modeling active devices as current sources, as depicted in Figure 2.6.

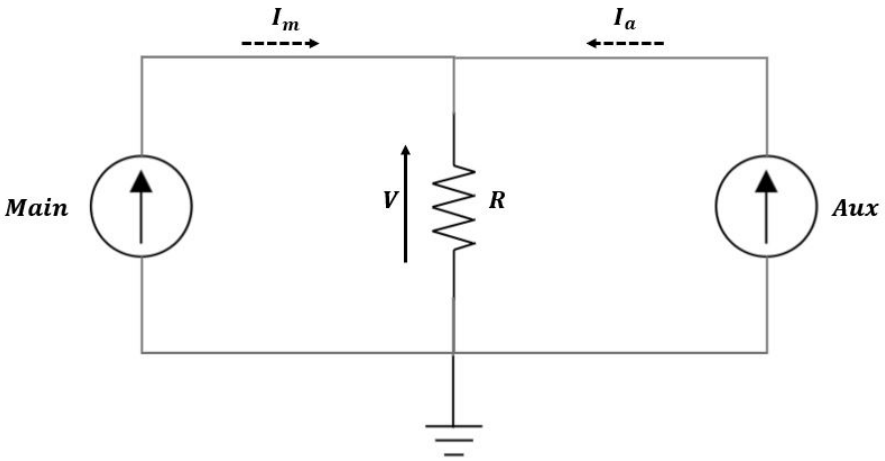


Figure 2.6: Active load modulation

Using Kirchoff's law, the voltage across the load resistor can be given as:

$$V = R(I_m + I_a) \tag{2.10}$$

The complex impedance at the two sources can be given as:

$$Z_m = R(\frac{I_m + I_a}{I_m}) = R(1 + \frac{I_a}{I_m}) \tag{2.11}$$

$$Z_a = R(\frac{I_m + I_a}{I_a}) = R(1 + \frac{I_m}{I_a}) \tag{2.12}$$

This means that the impedance seen by one of the sources can be transformed to a higher value if the currents are in-phase and a lower value if they are in anti-phase. This is the principle of ALM.

2.5 Doherty Power Amplifiers

One of the important methods used for ALM is DPA. The DPA was proposed in 1936 by William H. Doherty [2]. The original idea was concerned with tube-based PAs for broadcasting applications. The similarity between the modern-day wireless communication systems and the original idea is that modern-day transmitters are required to generate high data rates with low power consumption leading to a PAPR of around 6-9 dB. Conventional PAs have lower efficiency at average power levels which becomes a serious issue in modern RF applications. Hence, a solution is required to improve the average efficiency which can be solved by a DPA. Figure 2.7 illustrates a classical configuration of a DPA.

2.5.1 Doherty Theory

The main idea of DPA is to combine two devices in a way that one of the devices is switched on when the other device has reached saturation. The devices are referred

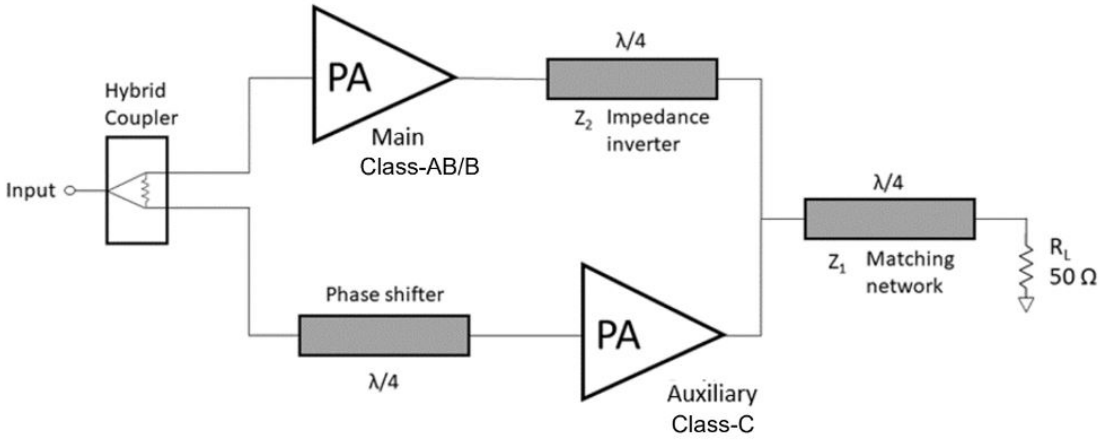


Figure 2.7: Classical DPA configuration [9]

as 'main' and 'auxiliary'. The output power of the complete DPA is the combined output of the two devices. However, as the input drive level is decreased, mainly around 6 dB from the maximum output power, the auxiliary amplifier is turned off. The auxiliary device modulates the load seen by the main device in a way that the desired efficiency is achieved at the back-off power level and maximum output power at saturation. There has been a lot of work done on DPAs due to their simple design with good back-off efficiency [9], [10], [11], [12].

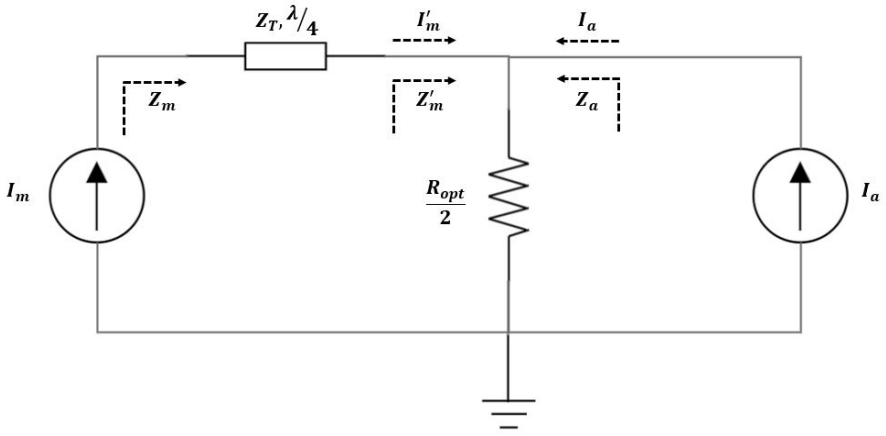
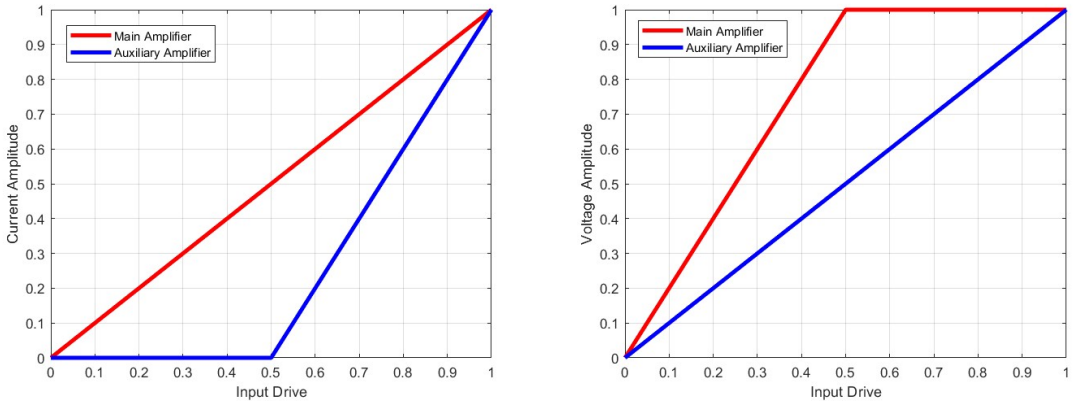


Figure 2.8: Current source representation of DPA

Figure 2.8 shows an operational diagram of a DPA. The difference from the previous representation in Figure 2.6 is the addition of the quarter-wave ($\lambda/4$) transformer between the load resistor and the main device output. This $\lambda/4$ transformer acts as an impedance inverter which helps in LM in a way that it makes the impedance seen by the main device go down as the auxiliary device current increases. The optimum matching impedance for both devices at peak power is R_{opt} but it becomes $2R_{opt}$ for the main device at back-off when the auxiliary device is off. The impedance inverter



(a) **(b)**

Figure 2.9: Doherty behavior (a) Current amplitude with an input drive voltage (b) Voltage amplitude with input drive voltage

has a characteristic impedance of Z_T which is a function of R_{opt} given as $Z_T = R_{opt}$. The load impedances seen by the main device before and after the $\lambda/4$ transformer are given as:

$$Z_m = \frac{R_{opt}^2}{Z'_m} = \frac{2R_{opt}}{1 + \frac{I_a}{I'_m}} \tag{2.13}$$

where

$$Z'_m = \frac{V_{opt}}{I'_m} = \frac{R_{opt}}{2}.(\frac{I'_m + I_a}{I'_m}) \tag{2.14}$$

From equation 2.13, it is evident that the impedance seen by the main amplifier is modulated by the auxiliary amplifier. The current I'_m is different from I_m due to the impedance change by the impedance inverter. Similarly, the impedance Z'_m is different from Z_m due to the $\lambda/4$ transformer. Generally, when two similar devices are used as main and auxiliary amplifiers, their current handling is similar at peak power level. When $I_m = I_a = I_{max}$, the impedance seen by the main device becomes $Z_m = R_{opt}$. However, it becomes $2R_{opt}$ at back-off due to the impedance transformation provided by the impedance inverter. The auxiliary amplifier presents an open-circuit condition to the main amplifier at the back-off level as the current I_a is 0. Once it is turned on, its impedance Z_a is load modulated and is given by:

$$Z_a = \frac{V_{opt}}{I'_a} = \frac{R_{opt}}{2}.(\frac{I'_m + I_a}{I_a}) \tag{2.15}$$

The LM behavior is illustrated in Figure 2.10. The main device impedance is modulated from $2R_{opt}$ to R_{opt} while the impedance of the auxiliary is modulated from open-circuit to R_{opt}. The change in current and voltage amplitude as a result of this LM is depicted in Figure 2.9. The current I_a is turned on at the midpoint of the input drive, which corresponds to the back-off level. To achieve this feat in a

practical design, the auxiliary amplifier is biased in class-C. The current I_m increases linearly from 0 input voltage to the maximum drive. The main amplifier is generally biased in class-AB or class-B.

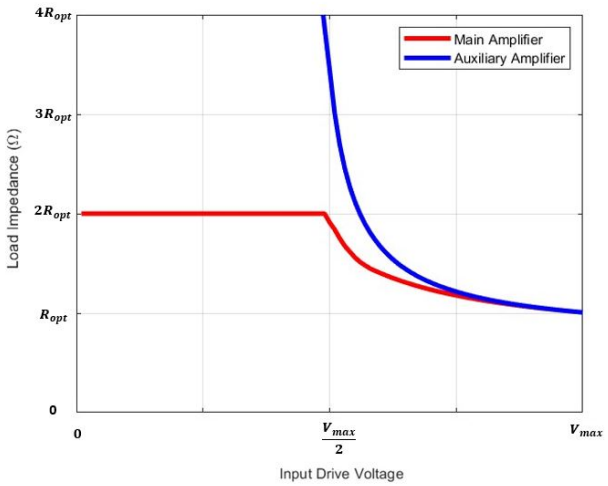


Figure 2.10: Change in impedance of main and auxiliary amplifier corresponding to input drive level

Based on the previous discussion and considering the case of an ideal class-B class-B DPA, it can be observed that the main device achieves a peak efficiency of 78.5% within the upper 6 dB power range. On the other hand, the auxiliary device experiences a linear decrease in RF voltage swing at the output, dropping to half of its maximum value at the 6 dB backoff point. As a result, the auxiliary amplifier's efficiency is not optimal within this range, but its contribution to the overall efficiency depends on the power it contributes. The overall efficiency of the DPA, as a function of the input drive can be given as [1]:

$$\eta = \frac{\pi}{2} \cdot \frac{(\frac{V_{in}}{V_{max}})^2}{3.(\frac{V_{in}}{V_{max}}) - 1} \tag{2.16}$$

where V_{in} is the input drive voltage and V_{max} is the maximum voltage corresponding to the maximum input drive. It can be observed that the relation yields $\pi/4$ for the maximum input drive, as well as for the 6 dB OBO condition. However, this configuration is for understanding and a real DPA will have an auxiliary device operating in class-C. The DE of the above-discussed ideal scenario is illustrated in Figure 2.11.

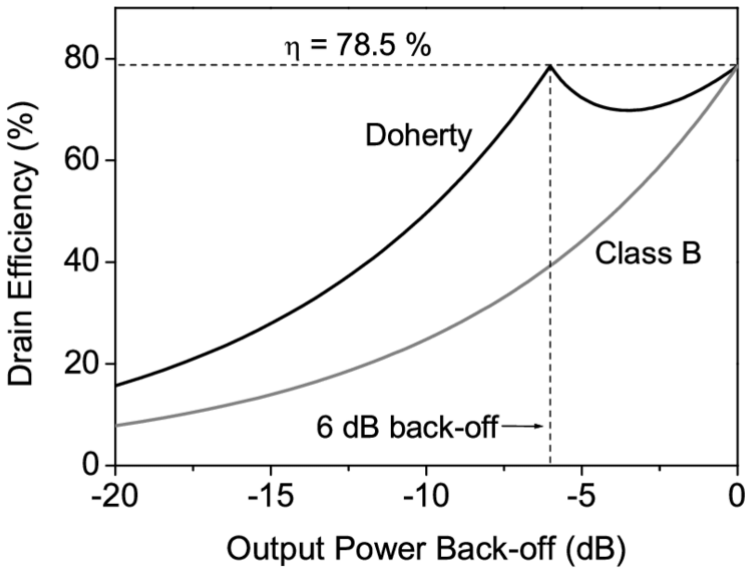


Figure 2.11: DE of an ideal class-B class-B DPA [14]

3

Doherty Power Amplifier Design

In the preceding chapter, the theoretical aspects of the DPAs have been elaborated. In this chapter, a comprehensive step-by-step design flow of the designed DB-DPA is presented. The amplifier is designed to operate in the frequency bands of 1800-1900 MHz and 2600-2700 MHz. The primary design objective is to achieve DE higher than 50% at 6 dB output back-off with output power higher than 47 dBM at saturation. The DPA is initially designed as a wideband amplifier, covering the entire bandwidth from 1800 MHz to 2700 MHz. After the initial design, further optimization is carried out for individual bands to achieve better performance.

3.1 Bandwidth Extension

As discussed in the previous chapter, the DPAs employ a $\lambda/4$ transformer as an impedance inverter network at the output of the main amplifier. However, the $\lambda/4$ transformer is inherently narrow-band, creating a significant challenge to its practical implementation for wideband systems [13]. The limitation stems from the dispersion effect of the impedance transformer, which results in an effective load impedance seen by the primary amplifier that matches the anticipated value only at the center frequency, f_c. As the operational frequency of the DPA deviates from f_c, the effective load impedance observed by the main amplifier deviates which leads to a reduction in back-off efficiency and limits the operational bandwidth. Therefore, it is critical to address this limitation to achieve optimal performance in a broader frequency range.

In the literature, several design strategies have been proposed for the purpose of extending the bandwidth of DPAs [15], [16], [17],[18]. One of these approaches is a transformer-less load-modulated architecture [19]. This design technique is highly effective in increasing the operational bandwidth of DPAs. Another topology that has been successfully employed to achieve up to 36.3% fractional bandwidth is based on the use of branch-line couplers [20].

In their study, Xia et al.[21] have introduced a broadband DPA configuration that incorporates an integrated compensating reactance (CR). This approach aims to analyze the influence of reactance on the back-off load impedance of the main amplifier during wideband operation. This task is accomplished by utilizing a $\lambda/4$ transmission line in the OMN of the auxiliary amplifier. This configuration produces an equivalent quasi-short-circuit, effectively mitigating the impedance fluctuations of

the main amplifier when operating at lower power levels with the auxiliary amplifier off. Additionally, a hybrid DPA topology that integrates a switching mode amplifier with a linear amplifier has been proposed, which is highly effective in achieving high efficiency and linearity simultaneously [22].

In conclusion, the literature proposes several design approaches to extend the bandwidth of DPAs, including the use of load-modulated architecture, branch-line couplers, compensating reactance. The DPA design presented here utilizes the approach presented by [21] which is sometimes referred to as the two-point matching technique as it involves matching the impedances at saturation and back-off levels.

3.2 Design Approach

PA design starts with the selection of bias points for the active devices by plotting the IV-curves. Subsequently, the individual amplifiers are designed, starting with the synthesis of OMNs in order to present the optimal load impedance to the transistors. Once the OMNs of both devices have been optimized, the devices are combined with a load modulation network. Finally, a post-matching network and the input matching networks for the amplifiers are designed to give the desired wideband response. All these steps are elaborated in the following sections. The transistors used in this design of DB-DPA are Wolfspeed CGHV27030S. The substrate used is Rogers4003c with a thickness and dielectric constant of 0.508 mm and 3.55 respectively.

3.3 Bias Selection

The DB-DPA consists of two devices, each designed with specific biasing characteristics. The main amplifier is biased near the pinch-off voltage, operating in deep class-AB, while the auxiliary amplifier is biased in class-C. To establish the appropriate bias points for both devices, the initial step involves plotting the IV-curves. These curves give the designer an idea about the device's gate voltages and the corresponding classes of operation. The IV-curves for the device in use are plotted in Figure 3.1a.

The blue line is the load line which signifies the current swing which can be observed in Figure 3.1a. The pinch-off voltage for this device is -3.1 V, therefore, for a class-AB operation, a gate bias of -2.85 V was selected. For the drain bias, 50 V was selected as per the data-sheet specifications. The auxiliary device was to be biased in class-C. It is possible to analytically calculate the bias point for the auxiliary amplifier and it was found to be -6 V. However, the auxiliary bias is generally considered an optimization parameter and it is tuned and optimized for better performance. Therefore, a gate voltage of -6.5 V and a drain voltage of 60 V was used for the auxiliary device. The reason for biasing the auxiliary device at a higher drain voltage is to increase its drain current at the peak input power. This is because, in symmetrical DPAs, the auxiliary amplifier does not reach its

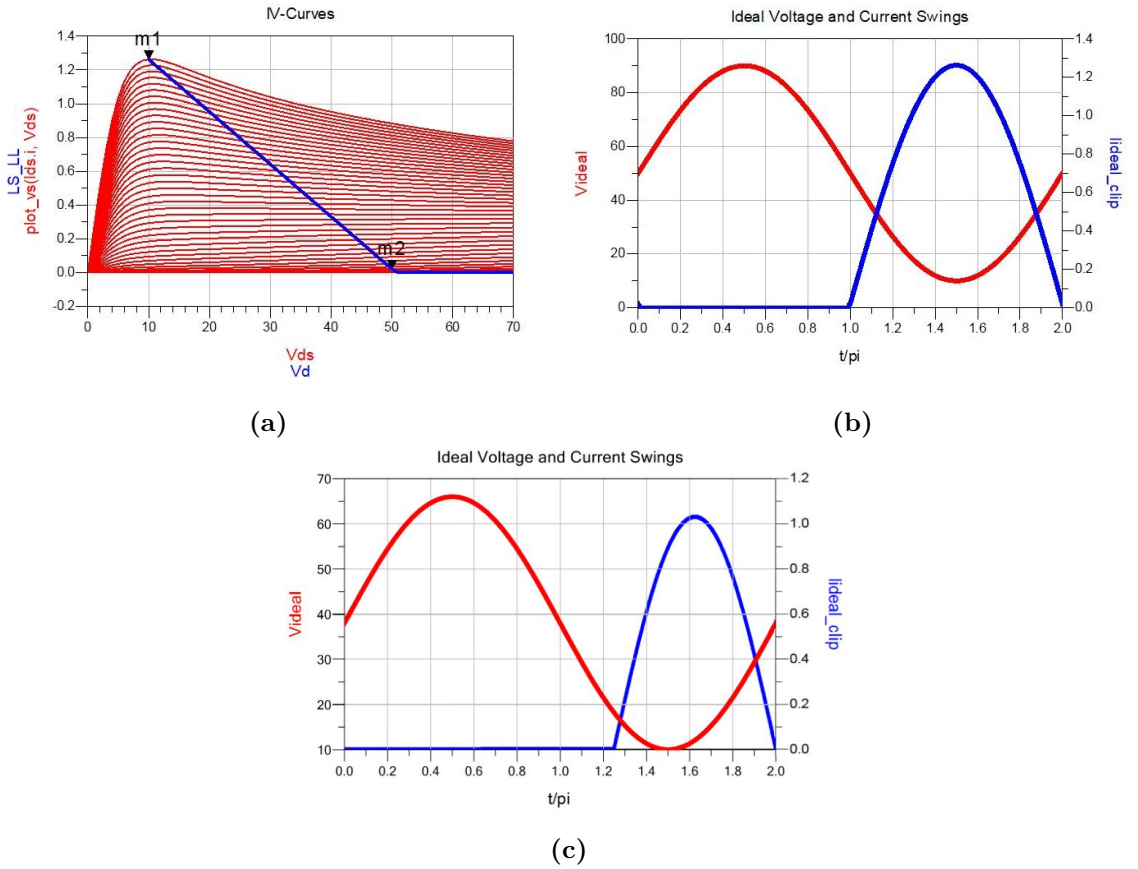


Figure 3.1: IV Curves. (a) IV Curve for drain current against drain voltage with load-line shown in blue. (b) Current and voltage swings corresponding to the load-line in (a). (c) Current and voltage swings corresponding to the bias point of class-C.

maximum current at peak input power [24]. To solve this, asymmetrical DPAs are designed by using either a larger transistor as an auxiliary amplifier or by using uneven power splitters at the input. Furthermore, it is possible to slightly increase the drain current by biasing the auxiliary at a higher drain voltage [21] which is also done in this design work.

3.4 Bias Network

A DC bias network is required for each amplifier in order to provide desired DC voltage and current to the PA. The design of a suitable bias network is extremely important as it might result in poor RF performance if not designed carefully. The bias network usually consists of multiple decoupling/bypass capacitors and an RF choke inductor. For the gate bias networks, a resistor is also added for low-frequency stability. Multiple bypass capacitors are required to minimize the supply ripple and noise which is unpredictable. For the RF choke, an inductor or a high impedance $\lambda/4$ transmission line can be used which presents an open circuit to the OMN transmission line. The incorporation of an RF choke within the bias network serves the

purpose of isolating RF signals originating from the device, preventing their interference with the DC supply. The network also consists of a series of capacitors at the gate and drain which are called DC-blocking capacitors. These are added in the design to decouple the DC source from the RF input and output.

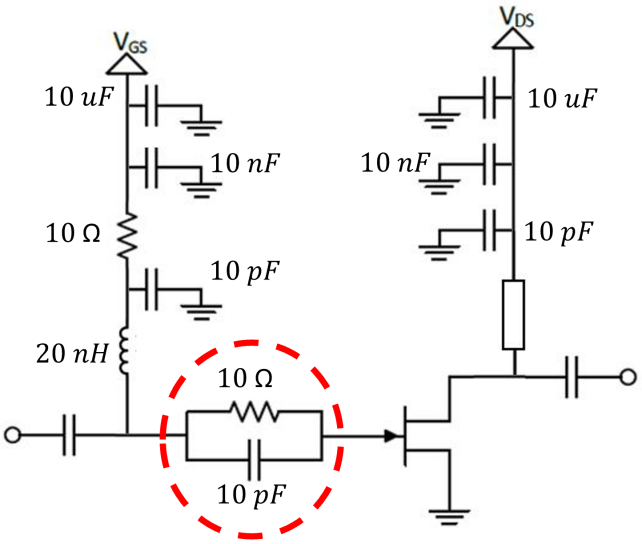


Figure 3.2: DC bias and stability networks for main and auxiliary amplifiers.

The finalized gate bias network for the DPA consists of a 20 nH RF choke inductor and three bypass capacitors of different values 10 uF, 0.01 uF, and 10 pF. A series resistor of 10 Ω is added with the inductor responsible for low frequency stability. In the drain bias network, a transmission line is used as an RF choke instead of inductor. Similar to gate bias, 3 bypass capacitors of the same values are added in the drain bias as well. The complete schematic of the finalized bias network is shown in Figure 3.2.

3.5 Stability Network and Analysis

Amplifier stability is one of the foremost design considerations, an unstable amplifier is in fact an oscillator. There are different techniques available in the literature for analyzing the stability of an amplifier. The most common is the Rollet's Stability Factor (K-factor) [32] which is a measure of the unconditional stability of an amplifier. Similarly the μ and $\mu'-$factors also provide information about the amplifier's stability status [33]. All these factors depend on the small-signal S-parameters and can be calculated in the following way.

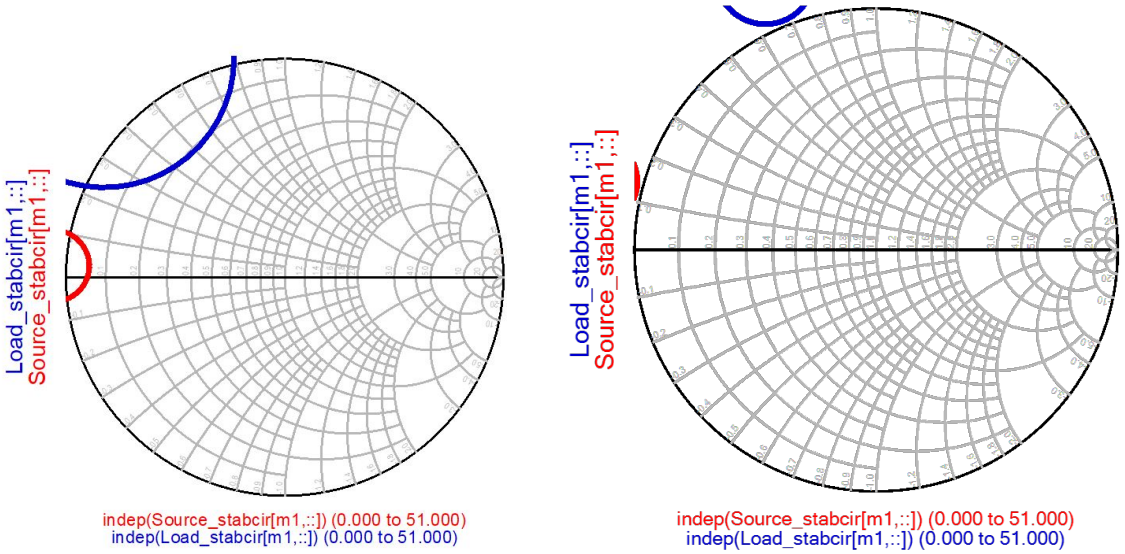
$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1 \tag{3.1}$$

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^{*}\Delta\| + |S_{21}S_{12}|} > 1 \tag{3.2}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \Delta\| + |S_{21} S_{12}|} > 1 \tag{3.3}$$

where

$$\Delta = S_{11} S_{22} - S_{21} S_{12} < 1 \tag{3.4}$$



(a) **(b)**

Figure 3.3: Stability analysis. (a) Source and load stability circles before the stability network was added. (b) Source and load stability circles after the stability network was added.

The K-factor greater than 1 means the amplifier is stable but it does not provide any detailed information as to how far outside the Smith chart, the stability circles are. Compared to this the μ and $\mu'-$factors give the distance from the center of the smith chart to the load and source stability circles. μ-factor measurement gives the distance from the center of the Smith chart to the nearest output (load) stability circle while the μ'-factor measurement gives the distance from the center of the Smith chart to the nearest unstable-input (source) stability circle. Thus a larger value implies the stability circles are further away from the smith chart center and vice versa.

To ascertain if the device is inherently stable or if it requires a stability network the load and source stability circles were plotted on the smith chart. When the simulation was done, it was found that the device was potentially unstable as the load and source stability circles were inside the Smith chart unit circle as shown in Figure 3.3. To make the device unconditionally stable, a stability network of a parallel resistor of 10 Ω and a capacitor of 10 pF was added at the gate of the device which is illustrated in Figure 3.2. The stability network is required to be added before performing the load-pull as it affects the optimal load for the device. After the

addition of a stability network, the device was found to be unconditionally stable as the source and load stability circles moved out of the Smith chart as shown in Figure 3.3. Figure 3.4 shows that the μ and $\mu'-$factors remain greater than 1 from DC to 10 GHz which means that the device is stable in this whole region.

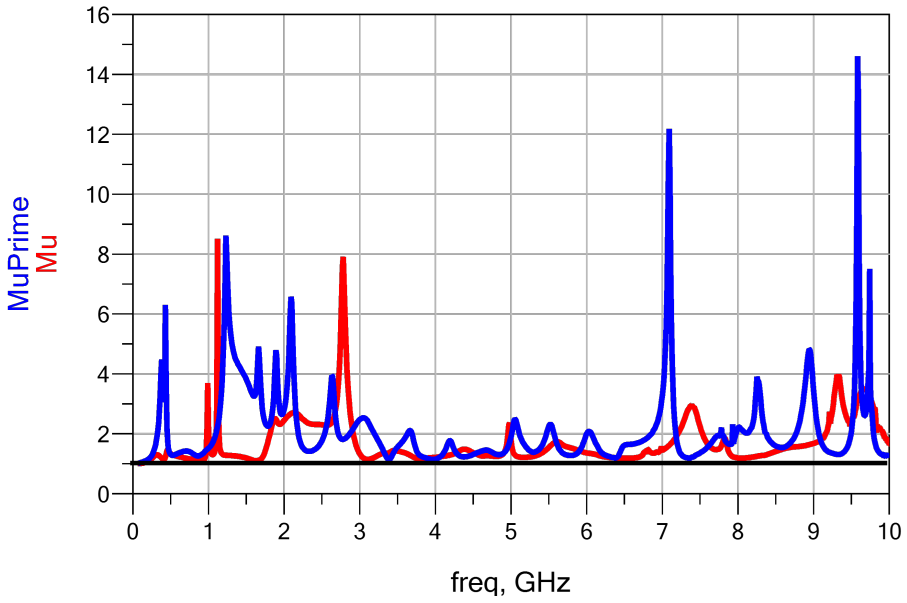


Figure 3.4: μ and $\mu'-$factor from DC to 10 GHz.

3.6 Load-Pull Analysis

As mentioned before, PAs are inherently nonlinear devices that produce high output power. However, due to their nonlinear behavior, traditional linear tools, such as the Smith chart, may not be adequate for designing impedance matching networks for PAs. This makes impedance pulling techniques, namely load-pull and source-pull, essential for determining the optimal load and source impedances to achieve desired design objectives, such as gain, efficiency, and output power.

Load-pull and source-pull techniques involve varying the fundamental and harmonic impedances of the input and output at the package reference plane, taking into account specific input levels, frequencies, and bias conditions. By doing so, these techniques ensure that the proper gain, efficiency, and output power are achieved for the given design objectives, considering the nonlinear behavior of the device. It is important to note that designing impedance matching networks for PAs using load-pull and source-pull techniques not only optimizes performance but also ensures the reliability of the amplifier by preventing unwanted signal reflections and maximizing power transfer. Therefore, the use of these techniques is widely accepted in modern communication systems, where PA performance plays a critical role in determining the overall system's performance.

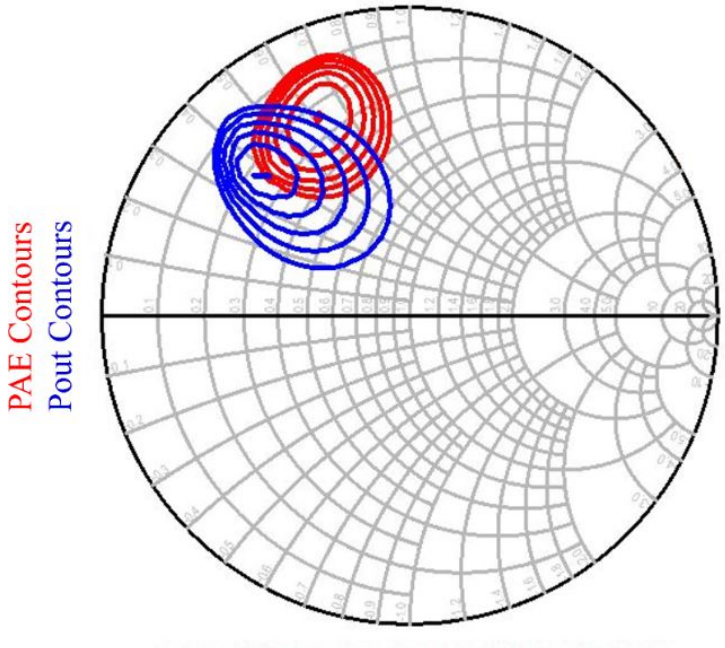


Figure 3.5: PAE and output power contours obtained through load-pull analysis for 2.25 GHz.

In designing PAs using load-pull and source-pull techniques, it is essential to have accurate models of the active device. These models provide a means to simulate the device's input-output characteristics and are often obtained from the device manufacturer. For the transistors used in this DB-DPA design, models were readily available and subsequently utilized in the design process. Additionally, in ADS, the load-pull analysis provides the source impedances corresponding to the optimal load impedances, thus making source-pull analysis redundant. In Figure 3.5 the PAE and output power contours for a frequency of 2.25 GHz are plotted on the Smith chart. The regions where the contours overlap are of more interest from a design perspective.

The load-pull simulations were performed at the centre frequencies of the desired upper and lower bands, and also for the frequency midway of these two frequencies i.e, 1.85 GHz, 2.25 GHz, and 2.65 GHz which are referred to as f_L, f_C, and f_U respectively in Figure 3.6. The optimal impedances for saturation and back-off level for these frequencies are plotted. At 6 dB OBO, the optimal load impedances were transformed to 15 Ω while the optimal load impedances at saturation were transformed to 30 Ω. The impedance at the common node was transformed to 50 Ω using an impedance transformer post-matching network (PMN) based on a Chebyshev transformer.

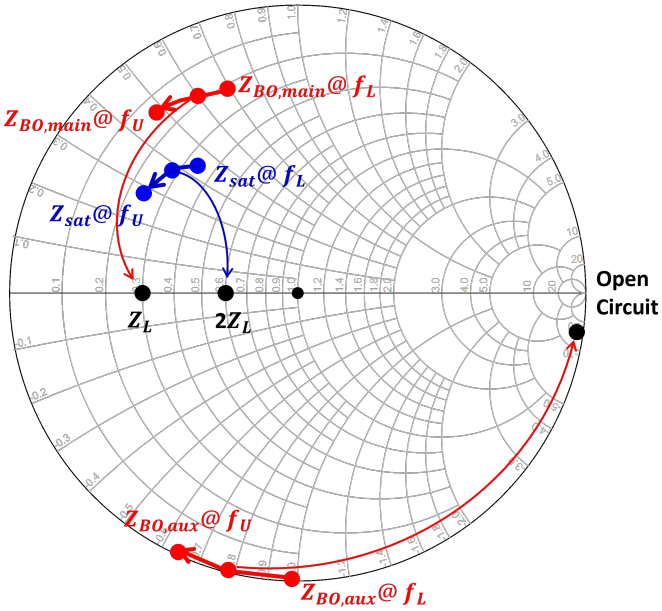


Figure 3.6: Impedance transformation at back-off and saturation for main and auxiliary amplifiers.

3.7 Output Matching Network

Once the optimal load impedances of the devices are known from load-pull analysis, the OMNs for both amplifiers can be designed. For the OMN of the main amplifier, it should present the impedance that corresponds to high efficiency at back-off level and provide maximum output power at saturation. Similarly, for the auxiliary amplifier, the OMN needs to exhibit a quasi-open circuit characteristic at the back-off and yield maximum output power at saturation. The OMN networks can be designed in the form of a complete three-port combiner [16]. However, in this design, the OMNs are first designed individually. Then these OMNs are combined and optimized to achieve the desired LM. In this section, the complete design process will be explained in a step-by-step manner.

The OMN can be modeled as a lossless, reciprocal, two-port network. The S-parameter matrix of such a network can be given as [21]:

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} -S_{22}^{*} e^{j2\theta_{21}} & \sqrt{1-|S_{22}|^2}\, e^{j\theta_{21}} \\ \sqrt{1-|S_{22}|^2}\, e^{j\theta_{21}} & S_{22} \end{bmatrix} \tag{3.5}$$

In this context, the symbol θ_{21} represents the phase of the S_{21}. The S-parameter matrix can be converted to ABCD parameters, which are as follows:

$$A = \frac{(1 - S_{22}^{*}e^{j2\theta_{21}})(1 - S_{22}) + (1 - |S_{22}|^2)e^{j2\theta_{21}}}{2\sqrt{1 - |S_{22}|^2}e^{j\theta_{21}}} \tag{3.6}$$

$$B = Z_0\frac{(1 - S_{22}^{*}e^{j2\theta_{21}})(1 + S_{22}) - (1 - |S_{22}|^2)e^{j2\theta_{21}}}{2\sqrt{1 - |S_{22}|^2}e^{j\theta_{21}}} \tag{3.7}$$

$$C = \frac{1}{Z_0}\frac{(1 + S_{22}^{*}e^{j2\theta_{21}})(1 - S_{22}) - (1 - |S_{22}|^2)e^{j2\theta_{21}}}{2\sqrt{1 - |S_{22}|^2}e^{j\theta_{21}}} \tag{3.8}$$

$$D = \frac{(1 + S_{22}^{*}e^{j2\theta_{21}})(1 + S_{22}) + (1 - |S_{22}|^2)e^{j2\theta_{21}}}{2\sqrt{1 - |S_{22}|^2}e^{j\theta_{21}}} \tag{3.9}$$

The OMN of the auxiliary amplifier will be discussed here in detail. The two-port representation of the OMN of the auxiliary amplifier is shown in Figure 3.7. During the low-power region, the OMN of the auxiliary device should effectively convert the impedance Z_{OUT_a1} to Z_{OUT_a} which corresponds to the quasi-open and drain impedance of the device respectively. Conversely, when the amplifier operates in saturation, the impedance Z_a which is obtained from load-pull should be transformed to Z_a1, which corresponds to some desired impedance value. Once these four impedances are known, the design parameters of the OMN i.e. S_{22} and θ_{21} can be obtained.

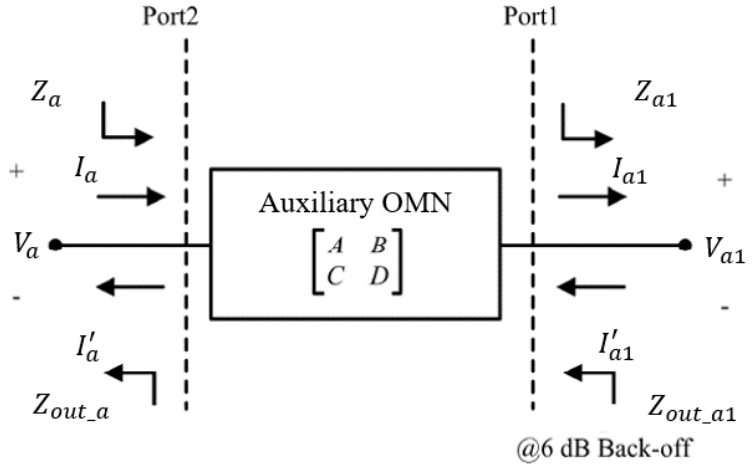


Figure 3.7: Auxiliary OMN modelled as a 2-port ABCD matrix.

The voltages and currents on both sides of the auxiliary OMN can be expressed in terms of ABDC parameters as:

$$\begin{bmatrix} V_{a1} \\ I'_{a1} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_a \\ -I_a \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_a \\ I'_{a1} \end{bmatrix} \tag{3.10}$$

At the back-off level, the auxiliary device is turned off and its output impedance is taken as Z_{out_a}. As $V_a = I'_a Z_{out\_a}$, the output impedance of the auxiliary amplifier becomes [21]:

$$Z_{out\_a1} = \frac{V_{a1}}{I'_{a1}} = \frac{Z_{out\_a}A + B}{Z_{out\_a}C + D} \tag{3.11}$$

At saturation, the same relationship is transformed to:

$$Z^*_{a1} = \frac{Z^*_a A + B}{Z^*_a C + D} \tag{3.12}$$

Table 3.1: Impedance values for main and auxiliary amplifiers.

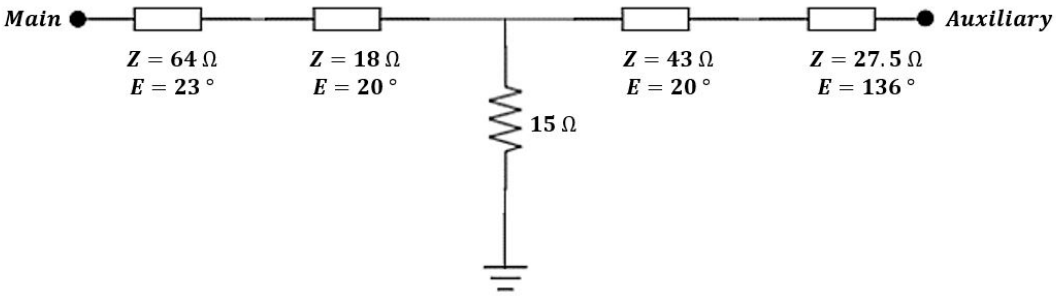
Frequency (GHz)	Z_m	Z_{m1}	$Z_{out,m}$	$Z_{out,m1}$
1.85	17 + j22 Ω	30 Ω	11 + j35 Ω	20.5 - j* 18.9 Ω
2.25	14 + j19 Ω	30 Ω	9 + j30 Ω	15 Ω
2.65	12 + j14 Ω	30 Ω	7 + j24 Ω	13 + j* 8.6 Ω

Frequency (GHz)	Z_a	Z_{a1}	$Z_{out,a}$	$Z_{out,a1}$
1.85	17 + j22 Ω	30 Ω	0.35 - j49 Ω	111 + j465 Ω
2.25	14 + j19 Ω	30 Ω	0.35 - j39 Ω	Quasi-Open
2.65	12 + j14 Ω	30 Ω	0.35 - j32 Ω	75 - j340 Ω

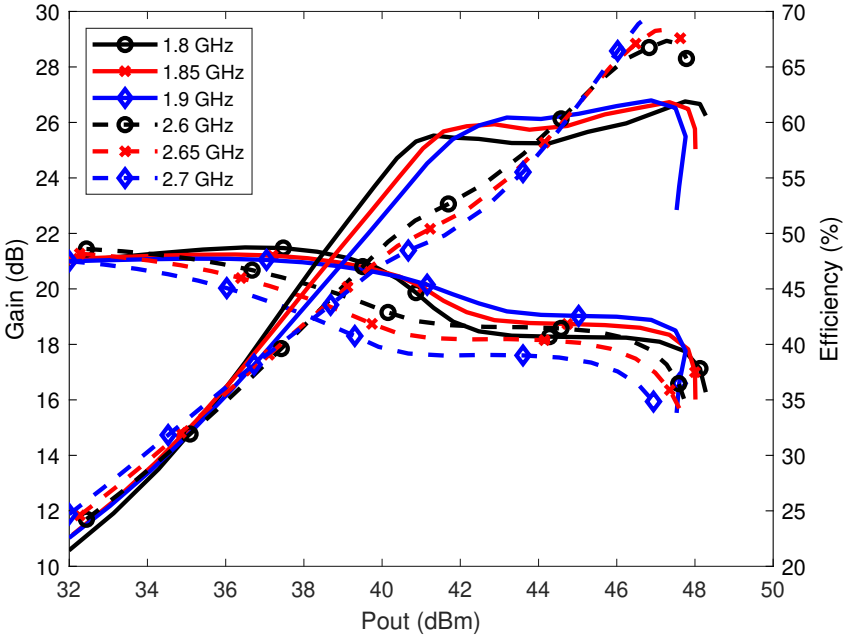
Taking the example of the center frequency 2.25 GHz, the optimum load impedance for the auxiliary amplifier is found from load-pull as Z_a = 14 + j19 Ω while Z_{a1} is chosen to be 30 Ω, as it gave a better response with a simpler network compared to 50 Ω . The output impedance of the auxiliary device is found to be Z_{out_a1} = 0.35 - j39 Ω. Using (3.12), the value of S_{22} is calculated. This obtained value is used in equation (3.11) and a set of impedances Z_{out_a1} can be plotted considering θ_{21} as a degree of freedom. To transform 0.35 - j39 Ω to a quasi-open condition, a value of $\theta_{21} = 95°$ is taken. Due to periodicity, multiple values of θ_{21} can be chosen but the smallest value provides the least frequency dispersion for a wideband design. The same can be done for the other frequency points as well and a complete two-port S-parameters representation can be obtained.

Once the two-port S-parameters of the desired OMN have been obtained, the OMN can be synthesized. There are different network synthesis techniques available in the literature which can be used [23]. However, the OMNs in this design were synthesized in ADS. The S-parameters matrix obtained as a result of the two-point matching technique was used as a starting point for the OMN design. A two-section impedance transformer was chosen for the OMNs of both the main and auxiliary amplifiers as it is a well established architecture known to provide wideband response [30] . The synthesized OMN was tuned and optimized in ADS for both back-off and saturation conditions. The combiner obtained as a result of optimization and its corresponding performance is shown in Figure 3.8. The performance of the ideal combiner is satisfactory with a 6 dB OBO DE of higher than 50% for both the bands.

For the main amplifier, the OMN is required to present optimal load impedance for high efficiency at the back-off level and optimal load impedance for maximum output power at saturation. Using a similar two-point matching technique for the main amplifier, the OMN for the main is designed. The impedances which were transformed using this two-point matching technique are tabulated in Table 3.1.



(a)



(b)

Figure 3.8: Ideal output combiner. (a) Schematic. (b) Simulated results.

3.8 Input Matching Network

To achieve wideband performance from the DPA, the design of an input matching network (IMN) can have a significant impact. The IMN is responsible to provide optimal source impedances to the active device, corresponding to the optimal load

impedances for each frequency point. Thus, to achieve an overall wideband response, a wideband IMN is required to be designed. There are several techniques available in the literature which can be used to design wideband IMNs. The technique used in this design is called the stepped impedance transformer [25],[27],[28],[29].

Initially, a 3-stage stepped impedance low pass filter with 6 reactive elements was designed by using the transformation tables available in [26]. The design constraints included a fractional bandwidth of 60% around the center frequency of 2.25 GHz. The optimal source impedance was found through the load-pull analysis in ADS where the real part was 5Ω. Therefore, in order to design a real-to-real impedance transformer to transform 5 Ω to 50 Ω, an impedance transformation ratio of 10:1 was selected.

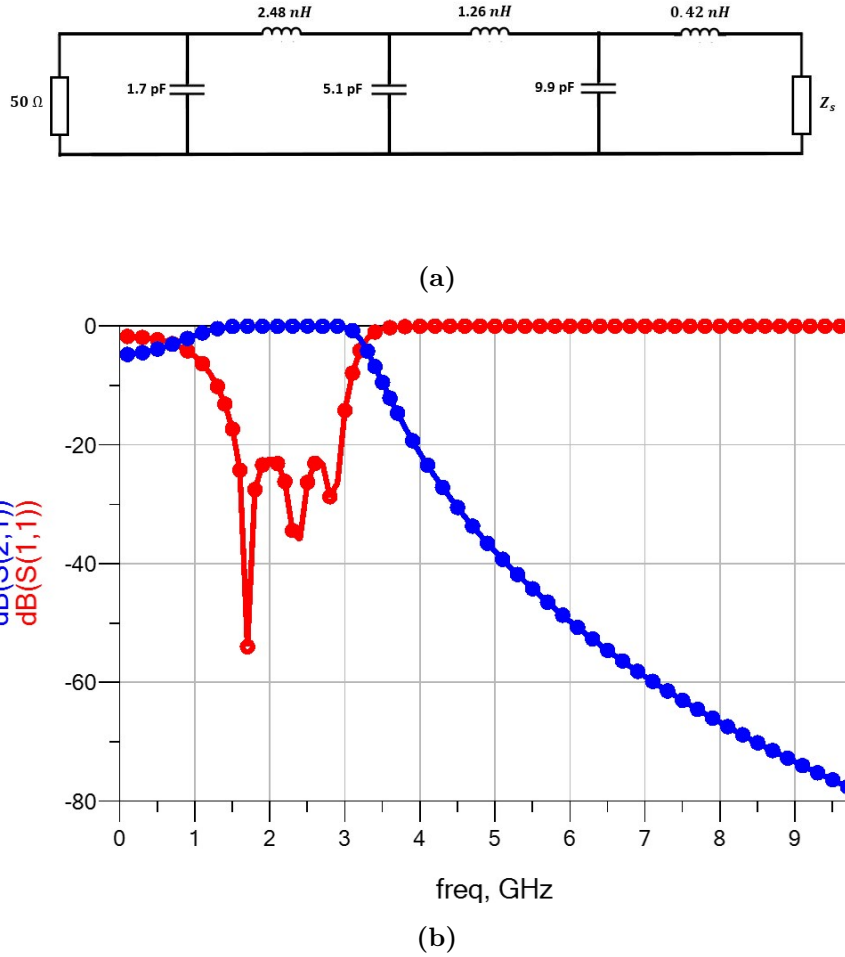


Figure 3.9: Simulated performance of the designed stepped impedance low pass filter. (a) Schematic with lumped components. (b) Simulated S-parameters.

First of all, a normalized design was selected for the stepped impedance low pass filter and the values of the reactive elements were obtained from tables available in [26] as per the considered design constraints. The normalized values of reactive

Table 3.2: Stepped Impedance Low Pass Filter Component Values

Element	Normalized Value	Scaled Value for Lumped Elements
g1	0.12	L1 = 2.48 nH
g2	7.01	C1 = 9.9 pF
g3	0.35	L2 = 1.26 nH
g4	3.57	C2 = 5.1 pF
g5	0.70	L3 = 2.48 nH
g6	1.12	C3 = 1.7 pF

elements are represented as g_1, g_1... g_n. Once the values have been determined, they were transformed into lumped element values of capacitors and inductors using the following equations [26]:

$$C_k = C_k^{'}(\frac{\omega_m^{'}}{\omega_m})(\frac{R^{'}}{R}) \tag{3.13}$$

$$L_k = L_k^{'}(\frac{\omega_m^{'}}{\omega_m})(\frac{R}{R^{'}}) \tag{3.14}$$

where C_k and L_k are the scaled values while $C_k^{'}$ and $L_k^{'}$ are the normalized values of the elements. $\omega_m^{'}$ is the normalized radian frequency which is taken as 1 while ω_m is the mean of the higher and lower frequency which corresponds to the scaled center frequency i.e., 2.25 GHz. The values of R and $R^{'}$ are taken as 50 and 1 as they are the impedance scaling factor. The finalized values of the lumped elements after the scaling are tabulated in 3.2. The schematic and response of the designed lumped element filter is shown in Figure 3.9.

The same technique was used to design the IMNs for the main and auxiliary amplifiers. However, the challenge here is that these types of impedance transformers are used to perform a real-to-real impedance transformation while the optimal source impedances are generally complex. So the synthesized real-to-real impedance transformer was taken as a starting point to design the IMNs. The network was converted to transform real-to-complex impedance transformation using tuning and optimization in ADS. Once the optimized real-to-complex impedance transformer was obtained, the lumped elements were converted to distribute elements i.e., transmission lines using Eqs. 3.8 and 3.9. The finalized IMNs for both the main and auxiliary amplifier can be observed in Figures 3.12 and 3.13. Here the high impedance lines act as series inductors while the low impedance lines act as shunt capacitors. These final IMN networks are obtained after rigorous optimization and tuning to achieve the best possible results for output power, gain, and efficiency for the desired frequency bands.

$$\beta l = \frac{Z_0 L}{Z_{high}} \tag{3.15}$$

$$\beta l = \frac{Z_{low} C}{Z_0} \tag{3.16}$$

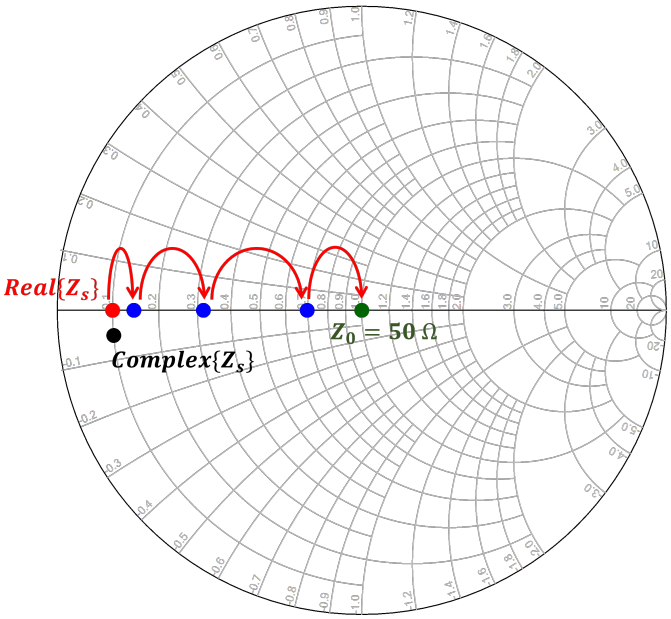


Figure 3.10: Illustration of the input impedance transformation.

At the input of the DPA, an off-the-shelf 90-degree hybrid (Anaren, X3C22E3-03S) is used to split the input into two paths with one having a leading phase. For the simulations, the S-parameters provided by the manufacturer were used. The phase shift introduced by the hybrid is compensated by the OMN in the auxiliary branch.

3.9 Post Matching Network

The OMN for both the main and auxiliary devices are designed to transform complex impedances to a real impedance of 15 and 30 Ω. At saturation, as both the devices are on and connected in a parallel configuration, the resultant impedance at the common node at saturation is also 15 Ω. To transform this impedance of 15 Ω at the common node to 50 Ohms impedance at the output, a four-section Chebyshev impedance transformer is designed using Table 5.2 in [31]. For the case of four sections, impedance transformation ratio of $\frac{Z_L}{Z_0} = 3$ and reflection coefficient magnitude of $\Gamma_M = 0.05$, the impedances of each of the section can be easily determined [31]. The lengths of the transmission lines were calculated for each section and then tuned in ADS to get the desired results.

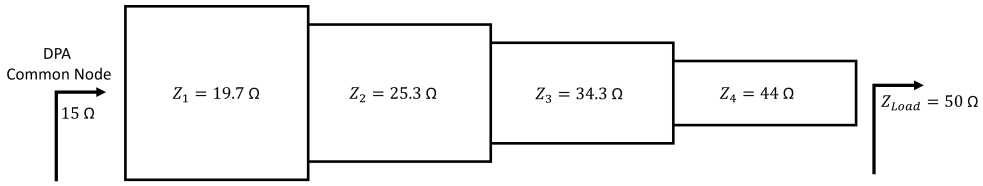


Figure 3.11: 4-section Chebyshev impedance transformer.

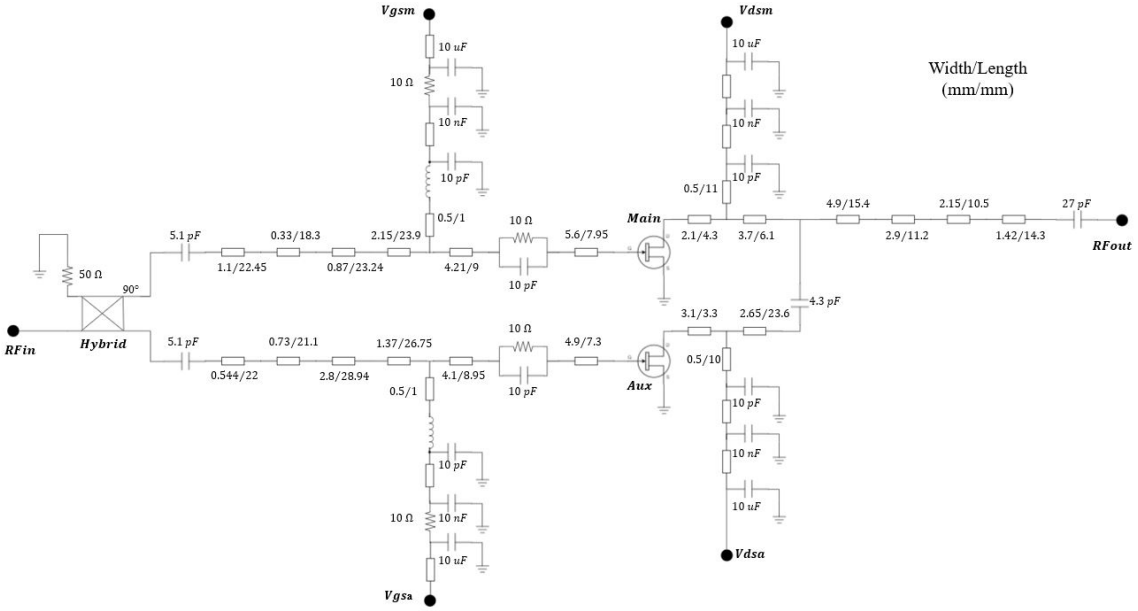


Figure 3.12: Schematic of the designed DB-DPA.

3.10 Simulation Results

The components of the DB-DPA like IMNs for main and auxiliary, OMNs, and the PMN were simulated individually as well as the complete DB-DPA, using Momentum RF simulations in ADS, in tandem with optimization at each step. The finalized schematic and layout of the designed DB-DPA are shown in Figures 3.12 and 3.13. Furthermore, in order to simulate a realistic scenario, Modelithics models of the capacitors, inductors, and resistors were used and subsequently, simulations were performed. The final simulation results obtained as a result are presented in Figure 3.14. The peak power, DE at 6 dB OBO, and DE at peak power are also tabulated in Table 3.3. DE higher than 49 % is observed at 6 dB OBO while it goes to higher than 60 % at peak power, for all the frequency points respectively. The peak power delivered to the load at the desired frequencies is above 47 dBm (50 Watts) for all frequencies except 2.7 GHz which is just slightly below this level i.e., 46.9 dBm. The gain ranges from 13 dB to 17 dB at the 6 dB OBO. These simulation results were deemed acceptable and the DB-DPA was sent for fabrication.

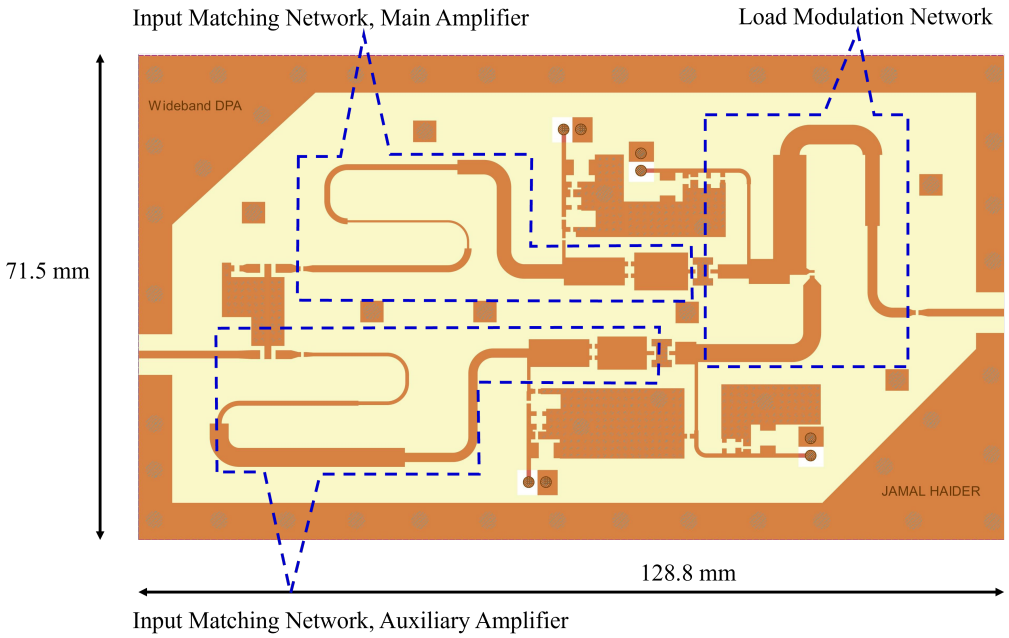
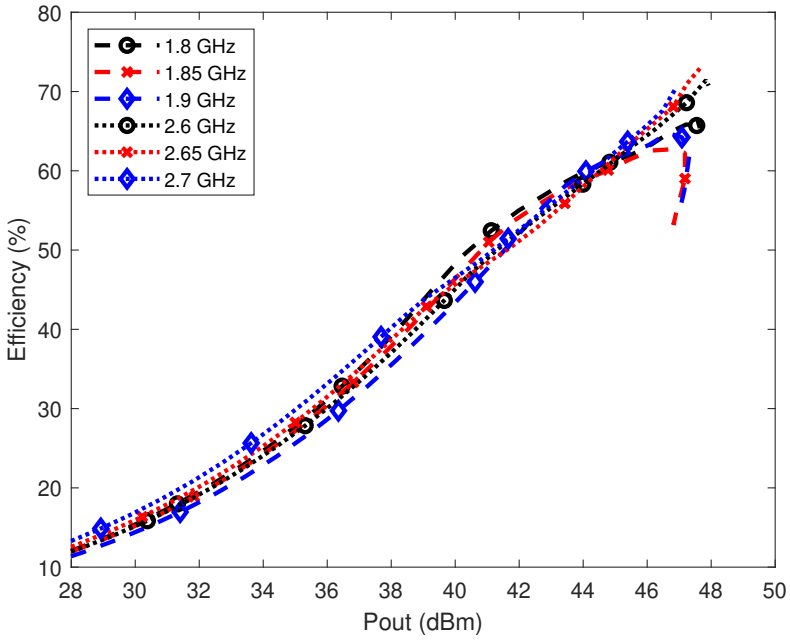


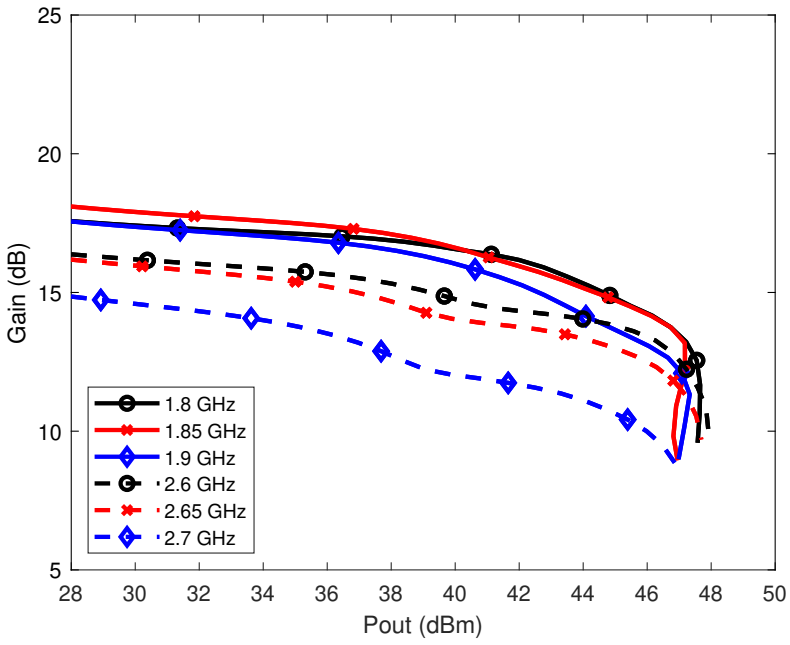
Figure 3.13: Finalized layout of the designed DB-DPA.

Table 3.3: Simulation Results

Frequency (GHz)	Efficiency (%) 6 dB OBO	Efficiency (%) Peak Power	Peak Power (dBm)
1.8	52.5	67.2	47.7
1.85	51.1	63.6	47.2
1.9	49.5	64.3	47.3
2.6	53.8	75.8	47.9
2.65	50.6	76.7	47.7
2.7	49.1	72.9	46.9



(a)



(b)

Figure 3.14: Simulated results. (a) DE vs output power. (b) Gain vs output power.

4

Measurement Results

In order to validate the performance of the designed DB-DPA, a thorough measurement scheme was adopted. PA measurements are challenging as they require the user to consider a number of factors while performing. These involve a number of different instruments which include Signal Generators (SG), oscilloscopes, vector network analyzers (VNA), spectrum analyzers (SA), and power meters, etc which must be used with a lot of care. In this chapter, all the steps undertaken to perform the measurements are elaborated in detail.

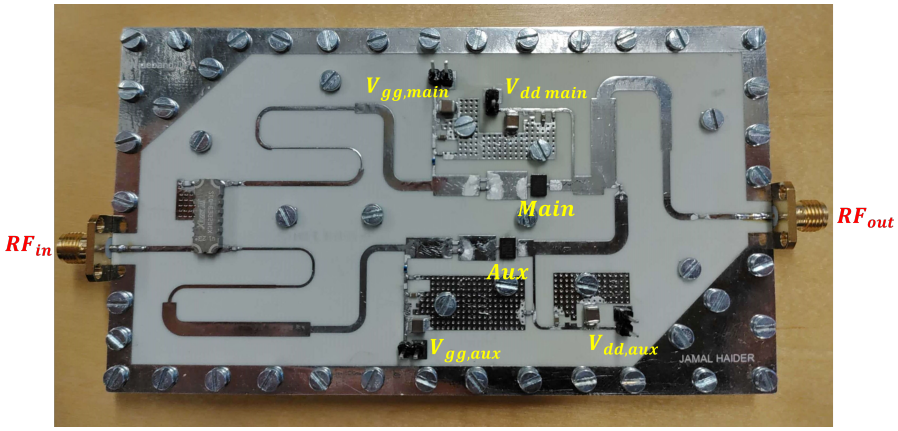


Figure 4.1: Photograph of the fabricated DB-DPA.

4.1 DC Analysis

The first step in PA measurements is the DC analysis in which the PA is connected to the power supplies which is referred to as biasing the device, and its response is observed. The fabricated DB-DPA is shown in Figure 2.7. The DB-DPA required multiple supplies as it involved two transistors which are required to be biased at the gate and drain. As the main amplifier operates in class-AB operation, it was biased at -2.85 V at the gate and 50 V at the drain. The auxiliary amplifier is biased at -6.5 V at the gate and 60 V at the drain and this same bias setup was used for all the results which are presented in the subsequent sections.

As the transistors used are GaN-HEMTs, therefore, the bias voltage used in the

simulations do not correspond exactly to the reality. This is an important consideration for biasing the DB-DPA. Thus once the gates and drains are supplied with DC voltages, the gate voltage of the main device is increased till the device is drawing the required amount of quiescent current (I_{dq}). The value of I_{dq} of 40 mA is taken from the simulations to make the comparison between the simulations and the actual DB-DPA valid.

After biasing the amplifier, its behavior is observed to see if there are any fluctuations in the drain current that are caused by instability of the PA. The designed DB-DPA was observed to be stable in this regard. The stability was further analyzed using an SA and it was observed to be stable with no oscillations. It is extremely important to ascertain the stability of the DB-DPA before proceeding with the small-signal measurements.

4.2 Small-Signal Measurements and Results

The next step in the measurement process is to perform the small-signal S-parameters measurement. The pre-requisite is a stable device that has cleared the DC analysis. The small-signal measurements are performed using a VNA and the setup is shown in Figure 4.2. The first and foremost step is to calibrate the VNA ports which include S-parameter and power-calibration. Once calibrated, the DB-DPA was connected to the VNA ports with some attenuation at the output. For this measurement, a 20 dB attenuator was connected to the output of the DB-DPA, and the S-parameters were measured.

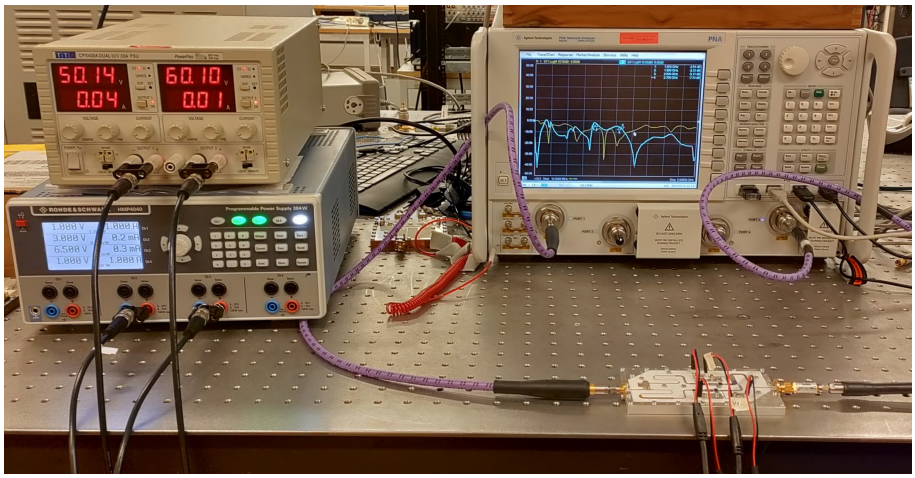
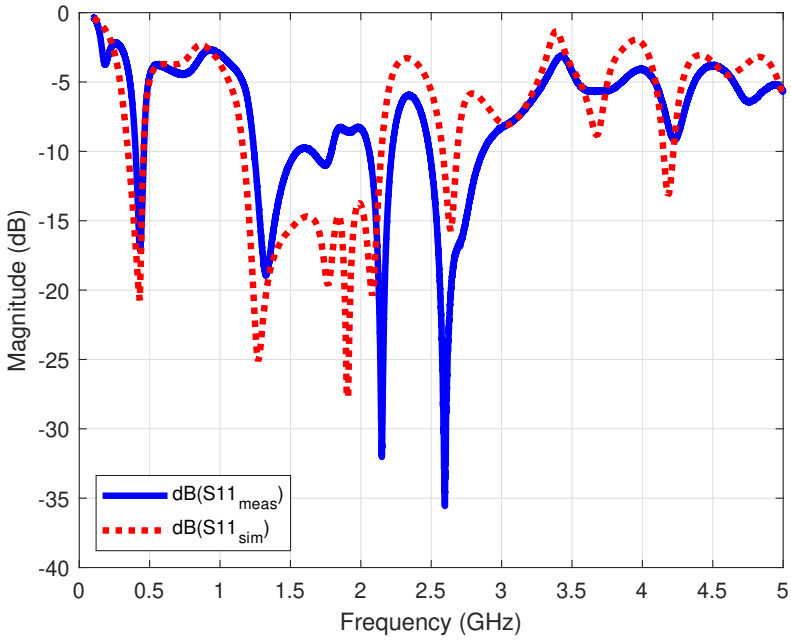


Figure 4.2: Small-Signal Measurement Setup.

The measured and simulated S_{11} and S_{21} are illustrated in Figure 4.3. From the figure, it can be observed that the measured results are approximately concurrent with the simulated results. The S_{11} in the lower band is higher than simulations but it is still acceptable. For the higher band, the measured results are better in contrast to the simulations. The S_{21} is slightly higher and shifted compared to the simulated results, especially in the lower band. This might be caused by some resonance in

the IMNs. This higher value of S_{21} in the lower band will translate to higher than expected gain which will be shown in the large signal measurements.



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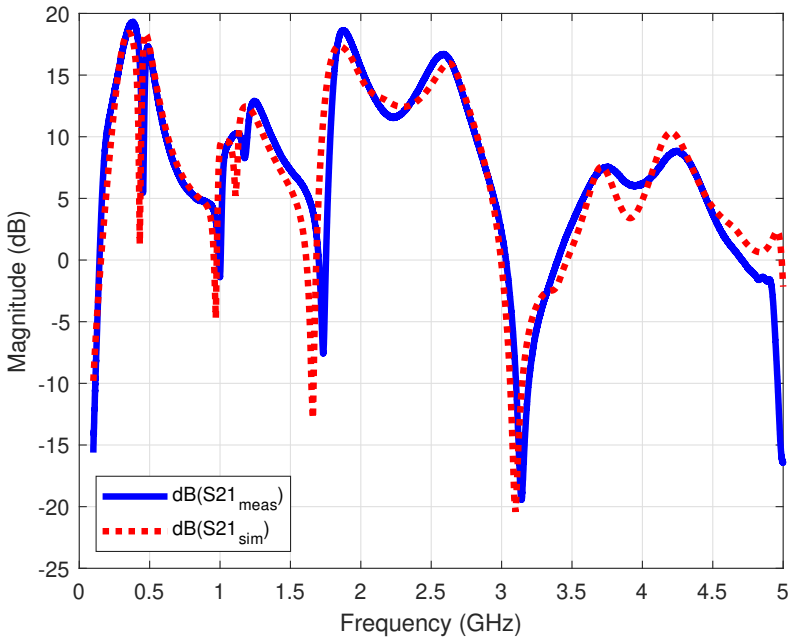


(b)

Figure 4.3: Measured and simulated S-parameters. (a) S_{11}. (b) S_{21}.

4.3 Large-Signal Measurements

The most important and critical measurements for a PA are the large-signal measurements which provide the complete extent of the PA's performance. Large-signal measurements are extremely challenging as they require an intricate measurement setup involving a number of instruments. The large-signal setup used for the measurement of the designed DB-DPA is shown in Figure 4.4. Different instruments are visible which include SG, oscilloscopes, and a power meter along with a driver amplifier and some passive components like a circulator, coupler, and attenuators. A filter with a cutoff frequency of 2.7 GHz was added to the output in order to measure the power of fundamental tone only excluding the harmonics. These attenuators, circulator and coupler were all categorized using a VNA in order to compensate for any added losses due to these components.

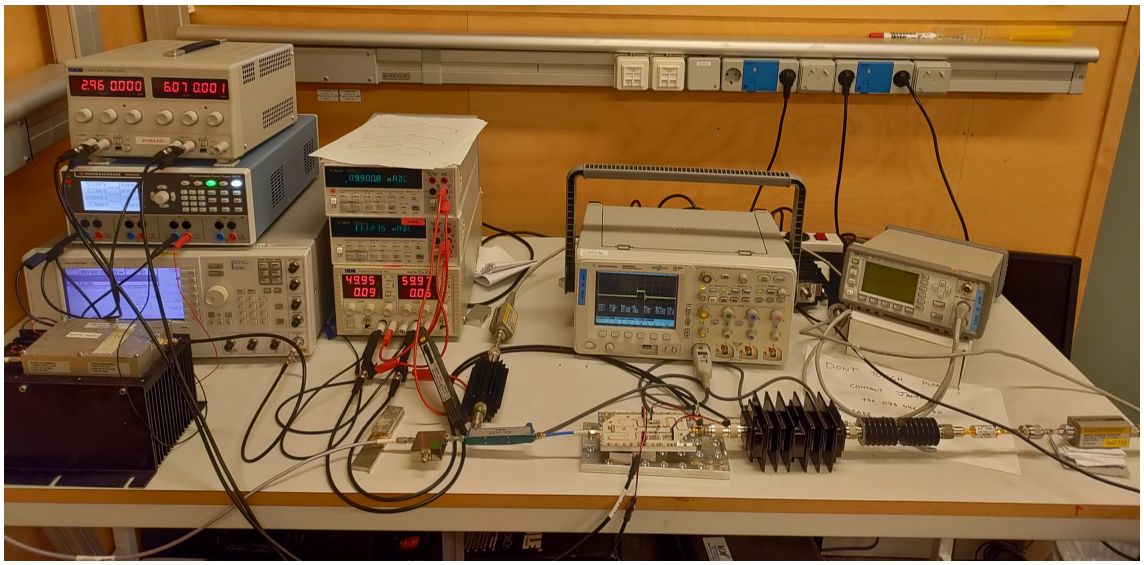


Figure 4.4: Large signal measurement setup actual.

Figure 4.5 illustrates how the measurement setup is connected. The SG provides the pulsed RF signal of a 10% duty cycle, which is fed into the driver PA for amplification. The driver PA output has a circulator in order to avoid strong reflections and ensure a one-way path for the RF signal. From the circulator, the RF signal enters a coupler which is a 3-port device. The output port of the coupler is connected to the input of the DB-DPA while the coupled port is connected to a power sensor through a 20 dB attenuator. This coupled port output is used to measure the RF power at the input stage. The output of the DB-DPA is also connected to a power sensor through an attenuator of 40 dB, to measure the DB-DPA output power.

The DC supply path of the DB-DPA is another important aspect of the measurement which is required to be measured accurately to calculate the efficiency of the DB-DPA. As mentioned earlier, there are DC supplies connected to the gates and drains of the two transistors to bias the DB-DPA. In order to calculate the DC power, the drain currents for the main and auxiliary amplifiers are required to be

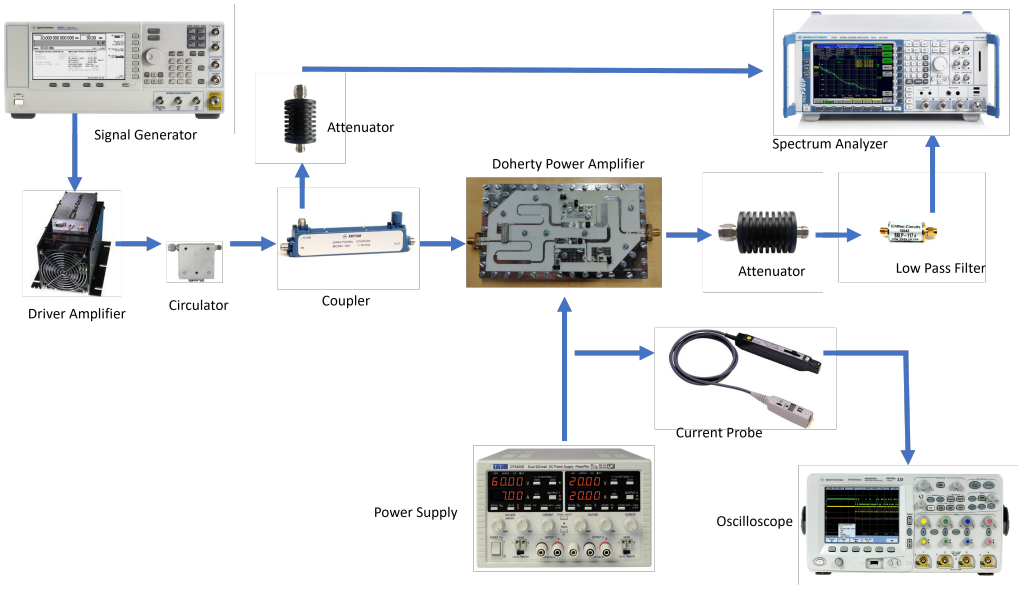


Figure 4.5: Large signal measurement setup connection diagram.

measured accurately. Initially, Digital Multi-Meters (DMMs) were used to measure the drain currents, but it was found that for a pulsed signal, DMMs are not accurate. Furthermore, the electron trapping effect in GaN devices also contributes to making a DMM measurement inaccurate. Instead, a current probe connected with an oscilloscope was used which provided an accurate output of the drawn current. An instance of the oscilloscope with current measurement is shown in Figure 4.6.

The measurement setup was automated and controlled using a MATLAB script. The large-signal measurements were initially performed using the power sensors and power meter, however, the results were deemed inaccurate due to the power sensors' overdue calibration as well as suspected inaccurate performance for pulsed operation. Consequently, the large-signal measurements were performed using an SA by calibrating it for each frequency point with a CW signal. The power sweeps were performed for the desired bands of operation and the final results are shown in Figures 4.7-4.9. The measured performance is also tabulated in Table 4.1. Figures 4.7 and 4.8 show the efficiency and gain response of all the frequencies in the band. Figure 4.10 illustrates the efficiency of the DB-DPA at saturation and 6 dB OBO for the complete frequency band along with the output power.

4.4 Analysis of the Measurement Results

From Table 4.1, it is clear that the DE obtained from the measurements is approximately 8-9% lower for all frequency points compared to simulations. The DE at 6 dB output back-off (OBO) for all frequency points is above 41%. For 1.85 GHz, the DE at 6 dB OBO is 41.2% while for 2.65 GHz, DE is 44.6%. At a peak power

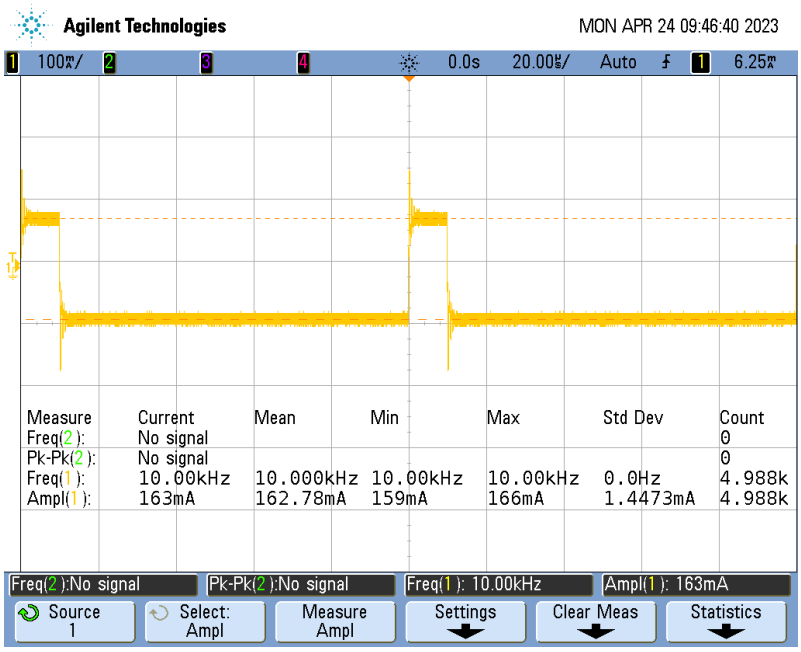


Figure 4.6: Oscilloscope display of the current measured using a current probe.

level of 48 dBm, the DE is 55.6% for 1.85 GHz while for 2.65 GHz, DE is 54.5% for a peak power of 47.4 dBm. Considering an OBO of 4.5 dB, the DE is higher than 45.6% while at peak power it is higher than 53.8% for all the frequency points. The peak power is approximately 48 dBm for the lower band while it ranges from 47.1 to 47.5 dBm for the upper band.

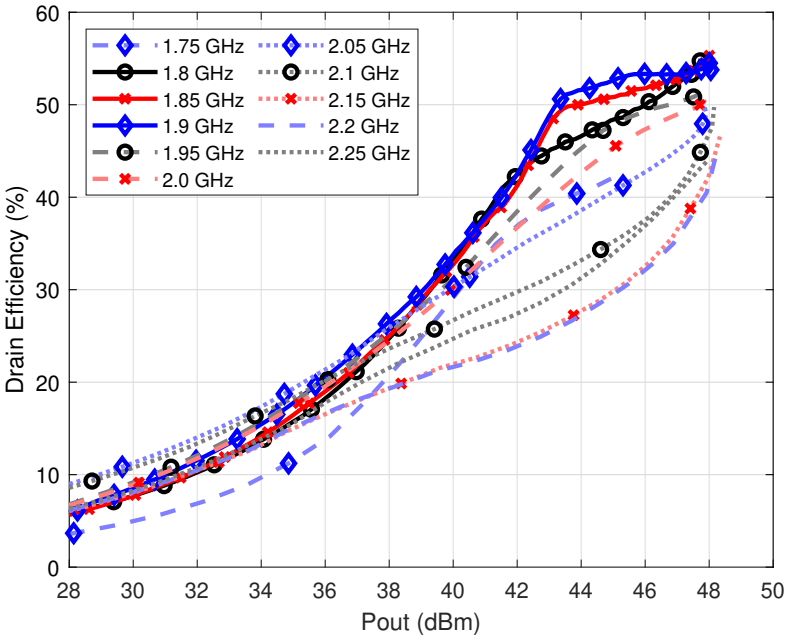
The gain curves have more deviation from the simulations than expected. The gain for 1.8 GHz is lower than simulations but higher for the two other frequencies of the lower band i.e., 1.85 GHz and 1.9 GHz. This correlates with the small-signal response of the DB-DPA as there is a higher-than-expected peak for both bands. Similarly, the upper band gain is also higher than the simulated values. Table 4.2 presents a comparison of the designed DB-DPA with previously published wide-band and dual-band DPAs. The designed DB-DPA offers a comparatively decent performance as it provides substantially higher gain and peak power. The efficiency response at 6 dB OBO is also satisfactory.

Table 4.1: Measured performance of the DB-DPA.

Frequency (GHz)	**Peak Power (dBm)**	**DE % 6 dB OBO**	**DE % 4.5 dB OBO**	**DE % Peak Power**
1.8	47.7	41.6	45.6	54.9
1.85	48.0	41.2	49.8	55.6
1.9	48.1	43.0	51.6	53.8
2.6	47.5	41.6	47.8	55.2
2.65	47.4	44.6	47.0	54.5
2.7	47.1	43.5	46.6	55.4

Table 4.2: Comparison of DB-DPA with already published literature.

Ref	**Freq (GHz)**	**Efficiency (%) 6 dB OBO**	**Efficiency (%) Peak Power**	**Peak Power (dBm)**	**Gain (dB)**
[13]	1.8/2.4	64/49	71/62	43/43	12/10
[17]	1.9/3.5	40/30	59/49	42.8/41.8	8/11.5
[35]	1.9/2.6	45/51	65/61	44.5/44.2	15/17
[36]	2.15/3.4	52/51	68/55	47.3/47	9/10.5
This work	1.85/2.65	41/44	50/47	48/47.4	14.5/20



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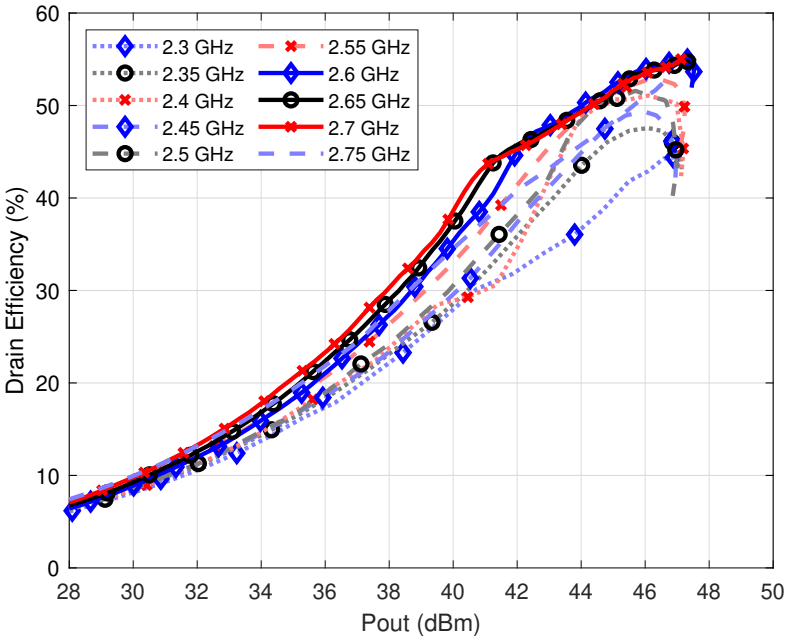
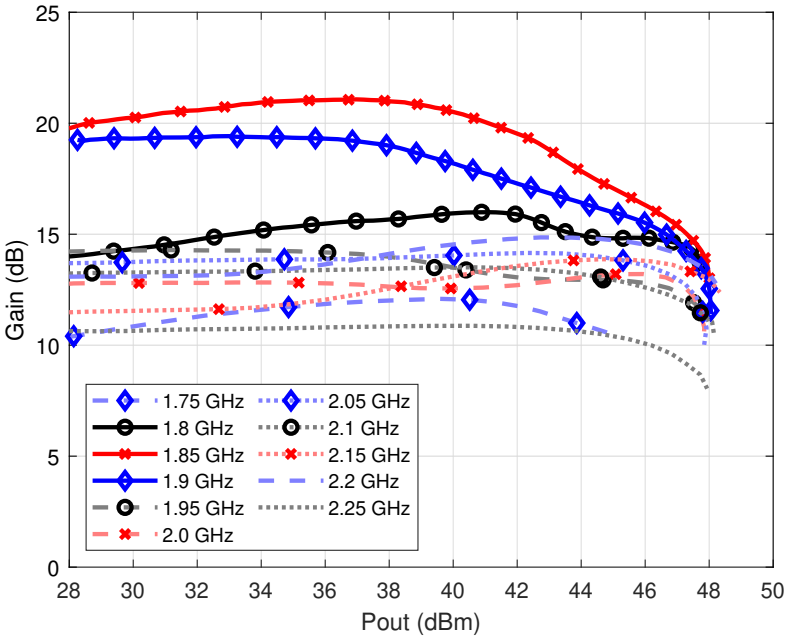


(b)

Figure 4.7: Measured DE. (a) Lower frequency band (1.75 - 2.25 GHz). (b) Upper frequency band (2.3 - 2.75 GHz).



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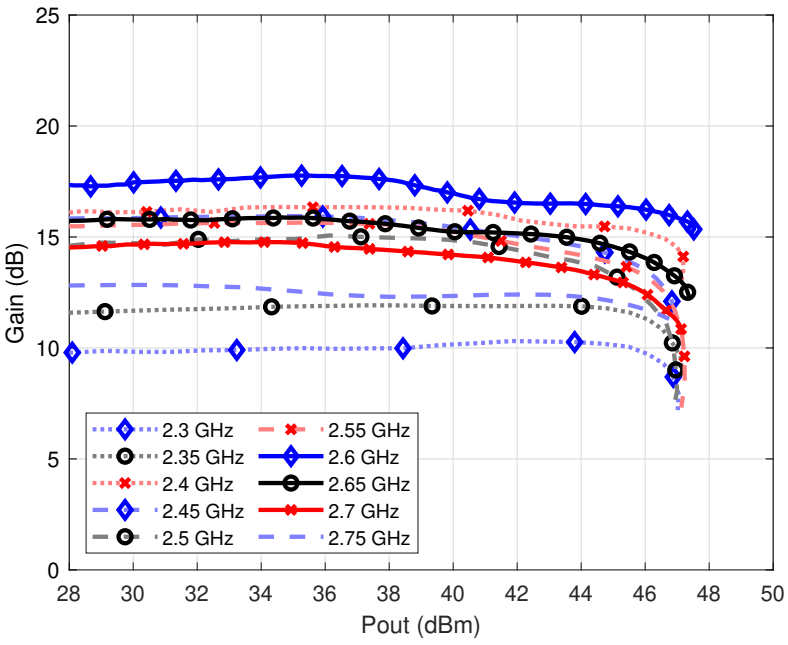

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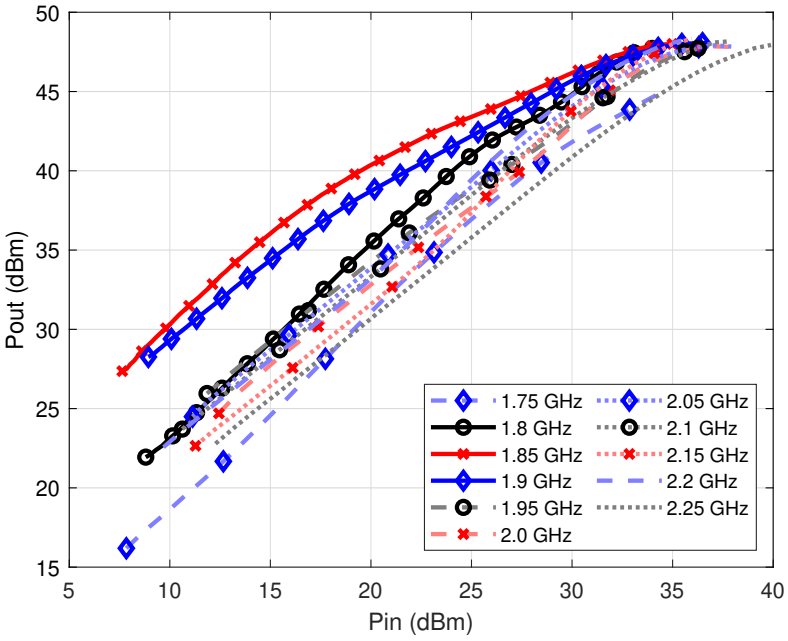
Figure 4.8: Measured power gain. (a) Lower frequency band (1.75 - 2.25 GHz). (b) Upper frequency band (2.3 - 2.75 GHz).



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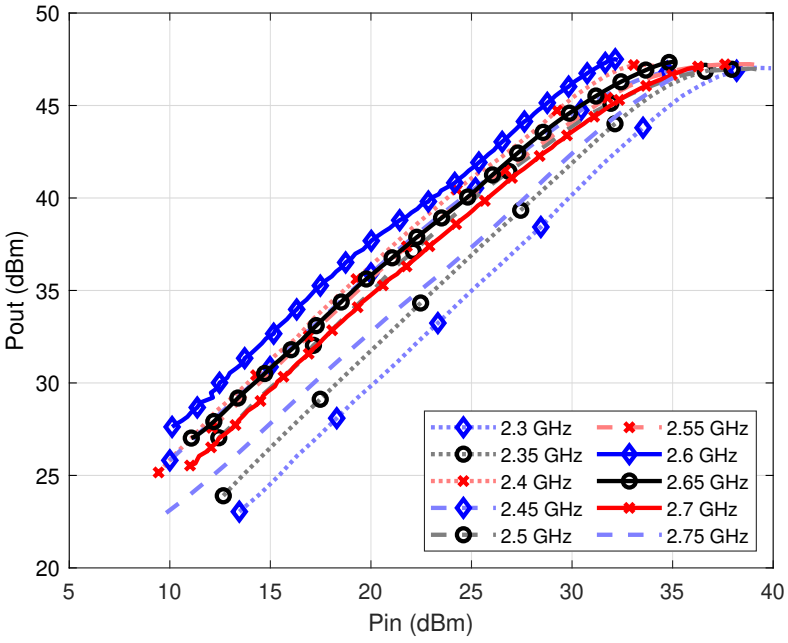

(b)

Figure 4.9: Measured output power. (a) Lower frequency band (1.75 - 2.25 GHz). (b) Upper frequency band (2.3 - 2.75 GHz).

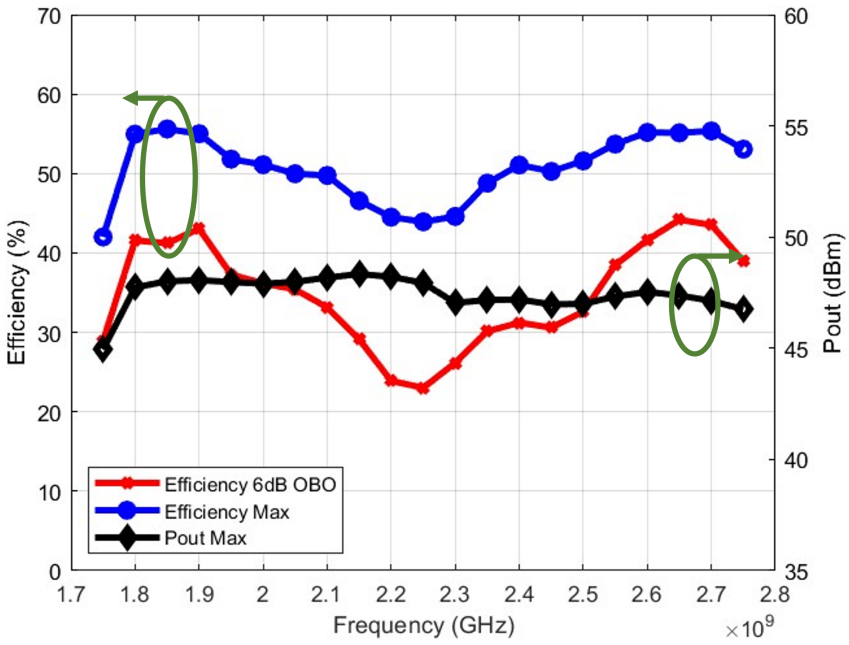

Figure 4.10: DE and output power with frequency sweep

5

Conclusion and Future Work

To summarize, this thesis work has presented a comprehensive design procedure for the design, implementation, and measurements of a concurrent DB-DPA operating at 1.85 and 2.65 GHz with a bandwidth of 100 MHz per band. The performance of the DPA has been extensively analyzed through simulations and measurements, providing detailed insights into its capabilities.

The measured results demonstrate satisfactory performance in terms of back-off DE, with a consistent DE exceeding 41% at a 6 dB back-off across all desired frequencies. Moreover, the DPA exhibits good performance with peak DE exceeding 50%, reaching a minimum of 47 dBm output power in the desired frequency bands.

This research makes a humble contribution to the field of concurrent DB-DPA design, showcasing promising results and setting the stage for further advancements and applications in high-efficiency RF power amplification systems. In the future, there are exciting prospects for the designed DB-DPA, including linearization and modulated measurements to enable concurrent operation in both frequency bands. Validating modulated measurements will pave the way for integrating the DB-DPA into a 4-way Doherty scheme, involving the incorporation of two additional main amplifiers. This enhancement of the DB-DPA architecture aims to further improve efficiency and output power in both bands, ultimately enhancing the overall performance of the DB-DPA.

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