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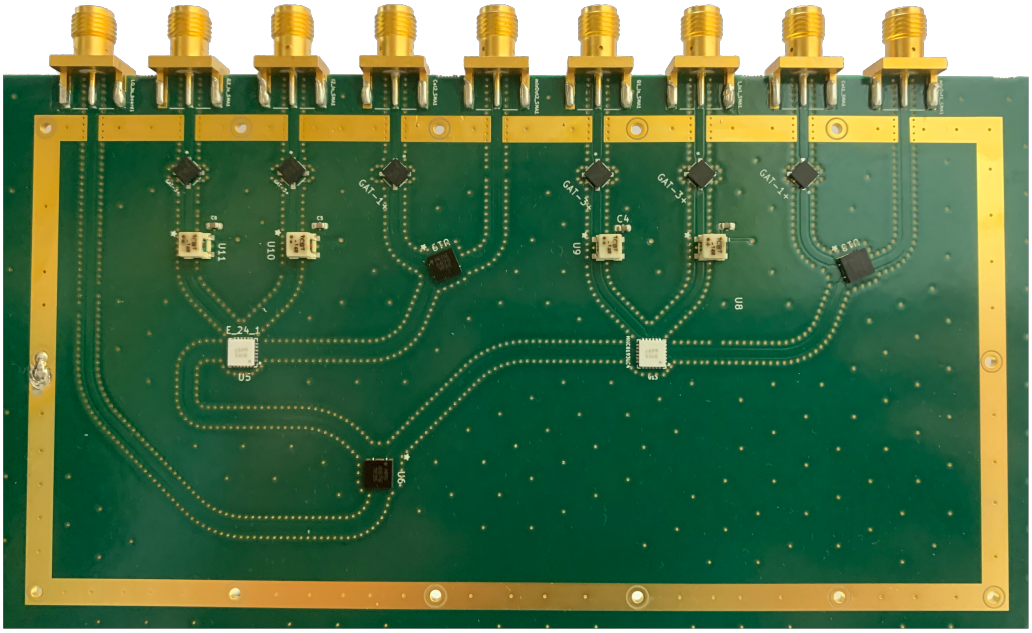

Scalable signal mixer stages in quantum processors

Development of a modular subrack instrument for quantum processor control

Bachelor's thesis in Electrical Engineering and Engineering Physics

Linus Andersson, Robin Folkesson
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DEPARTMENT OF MICROTECHNOLOGY AND NANOSCIENCE

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Cover: Printed circuit board containing two frequency upconverting mixer stages.

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Abstract

The development of cost-effective and compact quantum computers in the Quantum Technology Laboratory (QTL) at Chalmers University of Technology demands that the hardware of the control system can easily be scaled with the number of qubits. In this thesis the design and development of a rack instrument prototype is presented along with an evaluation of its performance. Three printed circuit boards were constructed and mounted in a subrack with the purpose of upconverting and downconverting the frequency of signals to and from the quantum processor with IQ mixers. Measurements performed at QTL confirmed image rejection and local oscillator signal supression between 49-51 dB and 86-85 dB respectively for the calibrated mixers. The instrument was not found to add any measurable phase noise beyond what was already present in the signal source. Possible future improvements include integrating amplifiers to both up- and downconverting mixer stages. Including amplifiers will also allow for an additional local oscillator signal distribution card to be added, which would improve the phase stability in the quantum computing system.

Keywords: quantum computing, IQ mixer, frequency upconversion, frequency downconversion, qubit readout, RF mixing modules, qubit control

Sammandrag

Utvecklingen av kostnadseffektiva och kompakta kvantprocessorer hos avdelningen för kvantteknologi (QTL) vid Chalmers Tekniska Högskola kräver att hårdvaran i kvantdatorns styrsystem enkelt kan skalas med antalet kvantbitar. I detta arbete presenteras konstruktionen av ett rackinstrument tillsammans med en utvärdering av dess funktion. Tre kretskort konstruerades och monterades i ett subrack med syftet att med IQ-mixrar kunna uppkonvertera och nedkonvertera frekvensen hos signalerna till och från kvantprocessorn. Mätningar utförda vid QTL visade en spegelfrekvensdämpning och en dämpning av lokaloscillator-läckage mellan 49-51 dB respektive 86-85 dB för de kalibrerade mixrarna. Vidare påvisades inte instrumentet addera något mätbart fasbrus utöver vad som redan fanns i signalkällan. Möjliga framtida förbättringar består exempelvis av att inkludera förstärkare i både upp- och nedkonverterande mixersteg. Förstärkarna kommer också möjliggöra att ett fördelningskort för lokaloscillatorsignalen kan läggas till, vilket skulle förbättra fasstabiliteten i kvantberäkningssystemet.

Nyckelord: kvantdator, IQ mixer, frekvenskonvertering, kvantbitsutläsning, mixermoduler, kvantbitstyrning

Acknowledgements

First of all, we want to thank our supervisors Simone Gasparinetti, Christian Križan and Giovanna Tancredi for your guidance. To Christan, thank you for going above and beyond supporting this thesis and for always appearing when we needed you the most. Thank you to Simone and Giovanna for your great advice and for trusting us in the lab with equipment way too expensive for undergraduate students. Simone, thanks for lending us your ”Tesla”. A huge thanks to Markus Enmark and Andreas Nylander at EMSL for allowing us to use your equipment. Without you, we would never have been able to successfully assemble our instrument in time. We also would like to thank Aamir Ali and Jiaying ”Claire” Yang at QTL for your support in the lab and for teaching us how to use your instruments. Last but not least, we want to thank Robert Rehammar at QTL. Thank you for sharing your knowledge within RF design and for helping us during frustrating times in the lab.

Linus Andersson, Robin Folkesson, Axel Jonasson, Sofia Reiner
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Part I

A Swedish Summary of the Thesis

Bakgrund

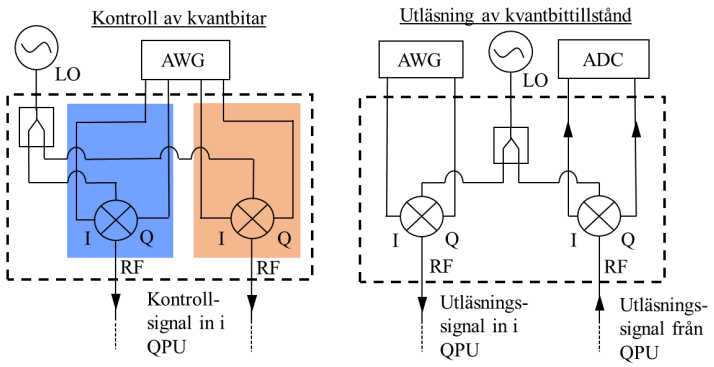
Kvantprocessorer har de senaste åren haft en brant utvecklingskurva. Till skillnad från digitala datorer där information representeras av *bitar* baseras en kvantprocessor på *kvantbitar* som tack vare kvantmekaniska fenomen kan befinna sig i superposition av två tillstånd. Idag utvecklar avdelningen för kvantteknologi (QTL) vid Chalmers tekniska högskola kvantprocessorer med målet att nå 40 kvantbitar innan 2024.

Flera utmaningar kvarstår, däribland kravet på en effektiv och skalbar kontrollenhet för styrning av signalerna till och från kvantprocessorn. Dagens lösningar är både kostsamma och tar upp mycket utrymme då de skalas med antalet kvantbitar. Det uppstår också fasskillnader när flera separata signalkällor och instrument används. Detta hämmar utvecklingen av en väl fungerade kvantdator. Med detta i åtanke redogör denna rapport för hur ett rackinstrument med kretskort har konstruerats som både uppkonverterar och nedkonverterar frekvenserna hos signalerna till och från processorn. Vidare har fokus legat på att bibehålla fasstabilitet för signalerna och minimera brus i kretsarna.

Styrning av kvantprocessorer

En kvantbit kan representeras av flertalet fysikaliska system som uppvisar kvanteffekter, exempelvis jonfällor, spin hos elektroner eller supraledande kretsar. Kvantprocessorerna hos QTL baseras på det sistnämnda. Denna teknik utnyttjar ickelinjära resonatorer vars energinivåer skapar ett tvånivåsystem. Kvantbitens tillstånd motsvarar energier mellan resonatorns två tillåtna energinivåer [5].

Genom att skicka in signaler som matchar resonatorns frekvens på 4-6 GHz kan kvantbitens tillstånd ändras. Genom att modifiera signalens amplitud och pulslängd kan önskad superposition nås och operationer i kvantprocessorn, eller *quantum processor unit* (QPU), utföras [3]. Utläsning av tillstånden sker med en linjär resonator som kopplar till kvantbitskretsen. Resonatorn kopplar i sin tur till en inskickad signal som efter att ha modulerats och återvänt kan analyseras med en analog-till-digital-omvandlare (ADC)[8].
Dock uppstår ett problem då frekvensen som behövs för att förändra kvantbittillstån-



Figur 0.1: Kretsdiagram över kontroll- och utläsningssignalerna till och från kvantprocessorn (QPU). Innehållet i de streckade lådorna har ersatts med de producerade kretskorten.

den ligger i det lägre GHz-området. Arbiträra vågformsgeneratorer (AWG) och ADC är för långsamma för att generera och läsa av sådana frekvenser på signalerna till och från processorn. Detta löses med hjälp av mixermodulering. En AWG genererar pulståg i MHz-området som sedan kombineras i mixern med en bärvåg i GHz-området. Utsignalen innehåller då informationen från bärvågen samtidigt som den matchar kvantprocessorns frekvens [3].

Implementering av IQ-mixrar i kvantprocessorer

En mixer är en elektronisk komponent som används i kretsar för att kombinera signaler med olika frekvenser. En vanlig mixer tar in en LO-signal (*lokal oscillator*) och en mellanfrekvenssignal eller IF-signal (*intermediate frequency*), där LO-signalen vanligtvis har betydligt högre frekvens än IF-signalen. Signalen ut från mixern har två frekvenskomponenter, så kallade *sidoband* där den ena är skillnaden mellan LO och IF och den andra summan enligt,

$$s_{RF} = \frac{1}{2}\left[\cos(2\pi(f_{LO} - f_{IF})t) + \cos(2\pi(f_{LO} + f_{IF})t)\right] \tag{0.1}$$

Dock är endast ett av dessa sidoband önskvärt då man tydligt vill kunna specifiera vilket tillstånd kvantbiten ska tillsättas. Därför används en IQ-mixer. Utöver LO-signalen har IQ-mixern istället två insignaler, I och Q, som hos en ideal IQ-mixer har en fasskillnad på 90°. Fasförskjutningen på 90° ger att ett av sidbanden i (0.1) helt undertrycks i utsignalen s_{RF}. I verkligheten krävs dock kalibrering av mixern för att endast få en signal. Vidare kan även signalläckage från LO-signalen förekomma i s_{RF}. Detta kalibreras genom att modulera DC spänningen på I- och Q-portarna till mixern [9].

Design av elektronik för radiofrekvenser

Då signalerna i kretsarna ligger i frekvensområdet 4-8 GHz har det varit viktigt att utforma kretskorten på sådant sätt att oönskade reflektioner och störningar reduceras. När våglängden hos en signal närmar sig storleken av kretsen gäller inte de fysikaliska modeller som används i lågfrekvent kretsanalys. Istället för att dela upp kretsen i komponenter med perfekta ledare mellan dem, ser man istället kretsens egenskaper som fördelade över hela kretsen och ledarna i kretsen som transmissionslinjer. Det finns många olika transmissionslinjer, men den som används i detta projekt kallas *Conductor-Backed Coplanar Waveguide* (CBCPW). Valet av vågledare baseras främst på att dimensionerna för en CBCPW enkelt går att justera så att önskad karakteristisk impedans uppnås [13].

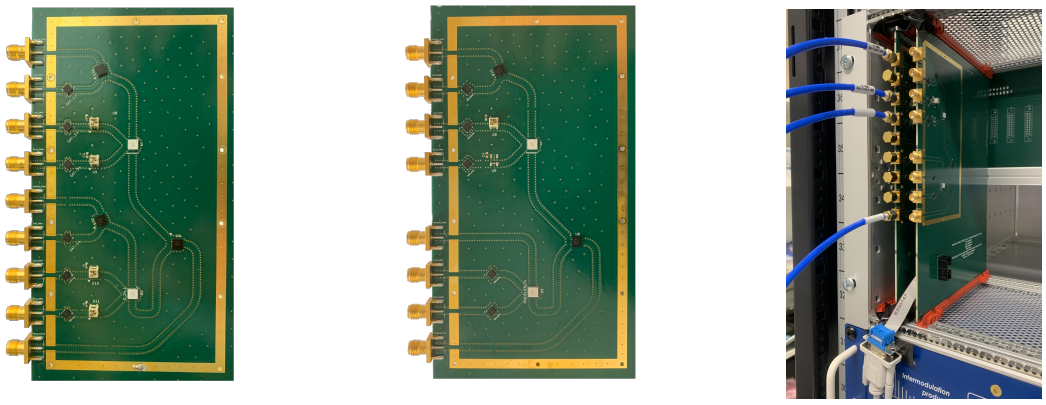
Det är nödvändigt att kunna matcha transmissionsledarnas impedans med resten av kretsen för att minimera reflektioner i kretsen som vidare leder till oönskade effektförluster hos signalen. Genom att öka avståndet mellan ledarna samt minska sträckan där de går parallellt, kan man minska interferensen mellan ledarna, även kallat *överhörning*. Vidare är det i vissa delar av kretsen viktigt att två ledare är av samma längd. Detta för att undvika större fasskillnader mellan signalerna i ledarna [14].

Designprocess och översikt av det färdiga instrumentet

Tre kretskort har konstruerats. Ett kontrollkort med två mixrar som uppkonverterar frekvensen i signalerna samt ett utläsningkort med två mixrar där en mixer uppkonverterar medan den andra nedkonverterar enligt Figur 0.1. Korten placerades sedan i ett 19-tums brett *subrack*, en rätblocksformad låda som håller kretskorten. Vidare konstruerades ett bakplan till subracket med möjligheten att strömförsörja samtliga kretskort. I detta instrument utnyttjades inte detta kretskort då förstärkaren som skulle drivas från bakplanet togs bort i designen. Med utgångspunkt i specifikationer och kretsdiagram från QTL valdes komponenter till kretskorten.

Design av korten skedde i KiCad och ritningarna skickades sedan till Eurocircuits för konstruktion. Lödning av korten gjordes av kandidatgruppen vid laboratoriet för Elektronikmaterial och system på Chalmers och på QTL. För att kunna välja rätt geometri på CBCPW och för att på så sätt undvika reflektioner i kretsen simulerades transmissionsledarna i KiCad och ADS för olika mått. Vidare gjordes testkort med en eller två komponenter för att testa deras funktioner innan den slutgiltiga designen fastslogs.

De slutgiltiga kortdesignerna kan ses i Figur 0.2a och 0.2b. Korten kantas av SMA-kontakter som leder LO-, I-, Q- och RF-signalerna till och från kortet. DC-signalerna till bias tees leds av ledningar i mellanlagret av korten från en fastlödd DC-kontakt. För att undvika överhörning mellan transmissionsledningarna är metallklädda hål, så kallade *vior*, borrade på korten och längs med ledningarna. Korten monterades i subracket för att sedan monteras i ett större rackskåp, en hylla som håller instrument. Detta kan ses i Figur 0.2c.



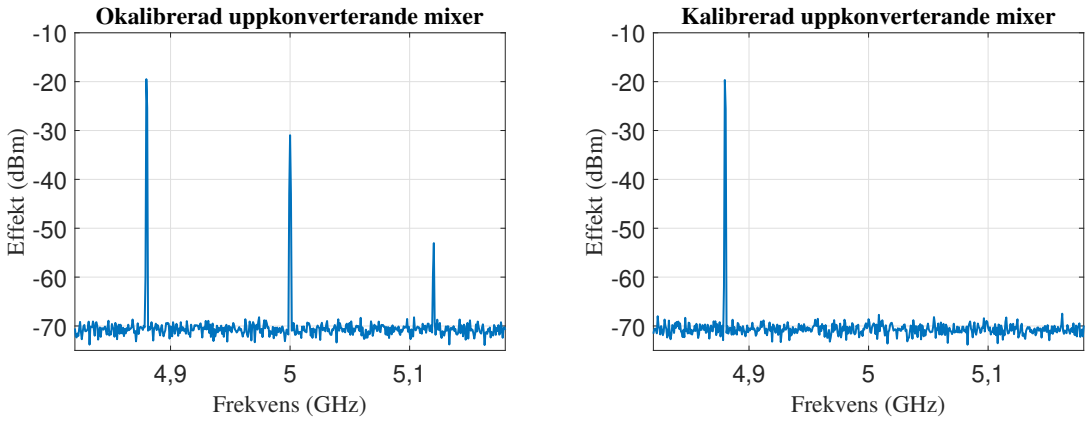
(a) **(b)** **(c)**

Figur 0.2: **(a)** Närbild på kontrollkortet med två mixrar som konverterar signalen till en högre frekvens. **(b)** Närbild på utläsningskortet där en mixer uppkonverterar och den andra nedkonverterar. **(c)** Korten monterade i racket. De blåa kablarna kopplade till de övre delarna av korten styr signalerna till och från mixrarna.

För att testa instrumentets funktioner och mäta relevanta parametrar kopplades korten till flera externa instrument. LO-signalen drevs av en signalgenerator och I, Q samt DC-spänningen genererades av en vågformsgenerator. Utsignaler undersöktes med en vektornätverksanalysator.

Test av monterat instrument och kalibrering av mixrar

Kalibrering av samtliga uppkonverteringsmixrar utfördes genom att undertrycka det övre sidobandet och LO-signalen genom att variera både fasförskjutningen och spänningsamplituden på Q-signalen. När topparna inte längre kunde urskiljas ur brusgolvet ansågs mixern vara kalibrerad. Detta kan ses i Figur 0.3. Vidare ses att det övre sidbandet kunde undertryckas mellan 49-51 dB. Ett urval av uppmätta värden för de tre mixrarna kan ses i Tabell 0.1. Utläsningskortet testades genom att jämföra dess utsignal med den från en färdigmonterad mixer från tillverkaren. Topparna i spektrat för instrumentet överensstämde till största del med evalueringskortets spektra. Anledningen till de andra frekvenstopparna som uppstår på båda korten skulle kunna vara att LO-signalens effekt var lägre än rekommenderat.



(a) **(b)**

Figur 0.3: **(a)** Spektrum från en av mixrarna innan kalibrering. **(b)** Spektrum från samma mixer efter kalibrering. Signalläckaget från LO-ingången vid 5 GHz och det högra sidbandet vid 5,12 GHz undertrycks genom justering av fas, amplitud och DC biasering på I och Q portarna.

Tabell 0.1: Mätvärden för de tre kalibrerade uppkonverterande mixrarna

Prestanda	Upkonv. mixer 1	Upkonv. mixer 2	Upkonv. mixer 3
Spegelfrekvensdämpning (dB)	49	49	51
LO-isolering (dB)	86	84	85

Diskussion och möjliga framtida förbättringar

Viss överhörning upptäcktes på kontrollkortet mellan två transmissionsledningar på den nedre mixerdelen i Figur 0.2a vilket kan åtgärdas genom större avstånd mellan ledarna på framtida kort. Vidare var ett förstärkarsteg också planerat på korten men uteblev då man ej fick det att fungera under testning. På grund av detta uteblev även ett planerat LO-fördelningskort som ej hade varit användbart utan förstärkaren. I framtiden rekommenderas det att försöka välja ett mindre rack för att göra instrumentet mer kompakt. På grund av för grunda SMA-kontakter gick det heller inte att montera den tänkta frontpanelen som skulle hålla korten på plats.

Part II

The Thesis

1 Introduction

In 2019, the Google AI Quantum team claimed to have devised an experiment that would begin to answer the questions: "will it [quantum computing] ever do something useful and is it worth investing in?" [1]. Their experiment supposedly showed their 53-qubit quantum processor *Sycamore* performing a target computation in 200 seconds, a computation they claim would take the fastest supercomputer at the time, *Summit* by IBM, 10,000 years to perform [2]. Today, the Quantum Technology Laboratory (QTL) at Chalmers is developing a quantum processor or quantum processing unit (QPU), that will reach 40 qubits by 2024. However, this demands an efficient and scalable solution for controlling the signals to and from the QPU. The current solution consisting of individual components mounted on separate boards is not well-suited for this increase in complexity and will ultimately limit the developments at QTL. With this in mind, a modular rack instrument was developed that not only facilitates linear scaling in the number of qubits, lowers the cost per channel and maintains phase stability between channels but also up- and downconverts the signals to and from the QPU, respectively.

1.1 Quantum processors

In digital computers, information is represented by the unit *bit* which only exists in two states, typically written as 0 and 1. In physical circuitry, this corresponds to an either high or low voltage applied to transistors in the central processing unit (CPU). Computations are performed with logical operators in the CPU and every input bit string gives a particular output bit string. A quantum processor works in the same way but instead implements quantum bits (*qubits*). The qubits differ from the regular bit in that they can exist in a combination of two different states at once due to superposition. In addition, contrary to the digital bits the qubits are controlled with analog signals. The different superposition states are initialized and changed by altering the amplitude, frequency and duration of the control signals [3]. These signal parameters are crucial for the performance of the quantum processor as perturbations in the signal can cause operations on the qubits to be inaccurate. *Qubit fidelity* is a measurement of how accurately the operations in the QPU are performed relative to what was intended. Well-functioning instruments in the control system of the QPU with low noise and high signal precision will result in high qubit fidelity, which is desired [4].

1.1.1 Superconducting circuits and the Transmon

There are several platforms for designing quantum processors since numerous physical phenomena can act as a qubit. Examples include but are not limited to trapped ions, electron spins and superconducting circuits [3]. QTL uses superconducting circuit technology in their quantum processors. The qubit is in this case a nonlinear microwave resonator called a *transmon*, whose state is controlled by microwave pulses sent to the quantum processor. The qubit states are represented by the two lowest energy states of the transmon [5]. A nonlinear *Josephson junction* consists of two superconductors with

insulating material between them which replaces the inductance in a normal LC-oscillator. Due to its nonlinear behaviour, the junction in the resonant circuit makes the distance between the transmon's energy levels uneven. This differs from the linear equivalent, the LC-oscillator, where the difference between energy states are multiples of $\hbar\omega$, which can be seen in Figure 1.1. When sending in a microwave pulse that matches the frequency $\hbar\omega_1$, the transmon is put in an excited state. The excitation of the transmon is restricted to only one energy level as the energy needed to climb one more energy level is not a multiple of $\hbar\omega_1$. This forces the transmon to only alternate between the ground state and the excited state or a superposition of the two, creating a nearly ideal two-level qubit [5]. The frequency of the pulses sent to the qubit in order to change the state is called the *qubit frequency* and for the transmon, energy levels typically lies in the 4-8 GHz range [3, 6]. This sets the required frequency of the signals to and from the QPU.

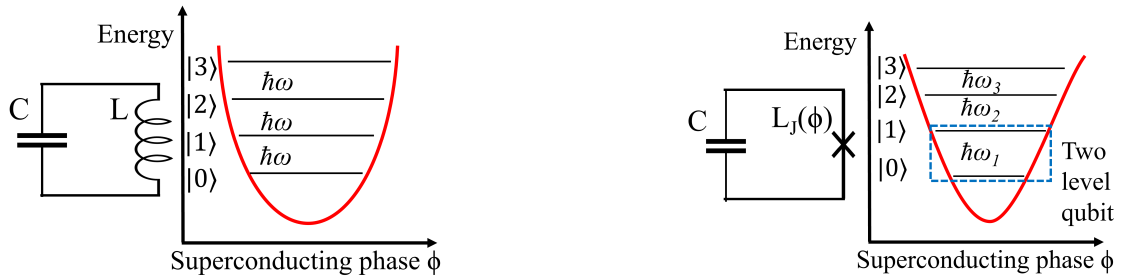


Figure 1.1: a Circuit and energy diagram of a linear LC-oscillator. The steps between energy levels are even. **(b)** Circuit and energy diagram of a transmon with a Josephson junction. Due to nonlinearity, the energy levels are unevenly spaced.

1.1.2 Qubit communication

In contrast to many other physical architectures of a qubit system, the size of the superconducting circuit is on the macroscopic scale, with the size of a transmon qubit measuring about 100 μm [5]. The circuit comprises a capacitor and a Josephson junction, printed on a microchip through photolithography and e-beam lithography and can be seen in Figure 1.2. In order to prevent unwanted excitation of the qubit states and for the circuit to be lossless, it is placed in a cryostat chamber which is cooled down to 10 mK [7].

The quantum processor needs to put the qubits in the desired state, operate on them with quantum gates, and read out the state. The circuit, and subsequently the transmon energy levels, are driven with microwave pulses. Capacitive coupling connect the qubit circuit with a waveguide which directs the pulses on the microchip [5]. It is the frequency, duration and amplitude of the pulse in combination with a well defined phase that dictates the change in qubit states. The pulses are sinusoidal in shape and are packed in pulse envelopes which are modulated to excite the transmon to the appropriate state [3].

Readout of the qubits is performed with a linear resonator circuit connected to the qubits with a capacitive coupling. A probing signal which matches the resonator frequency is sent into the QPU and will interact with the qubit. The qubit frequency will disturb the resonator frequency through the coupling and will induce a dispersive shift which is

dependent on the qubit state. The returned signal can then be measured and converted to the most likely qubit state [3, 8].

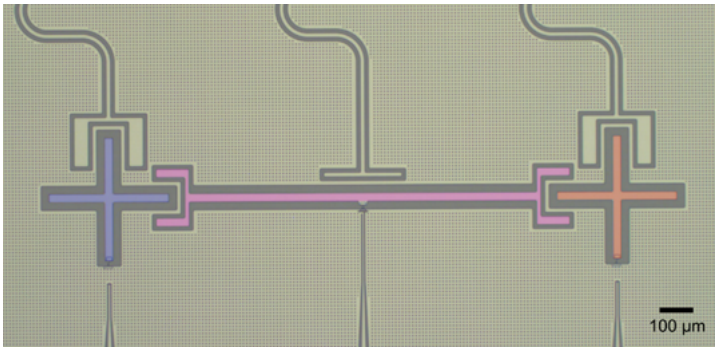


Figure 1.2: A coloured micrograph of two coupled qubits. Source:[8]. The plus-shaped qubits are capacitively coupled to their surroundings. The waveguides at the bottom control the qubits state. Three resonators are coupled at the top and the signals are subsequently used to read out the states.

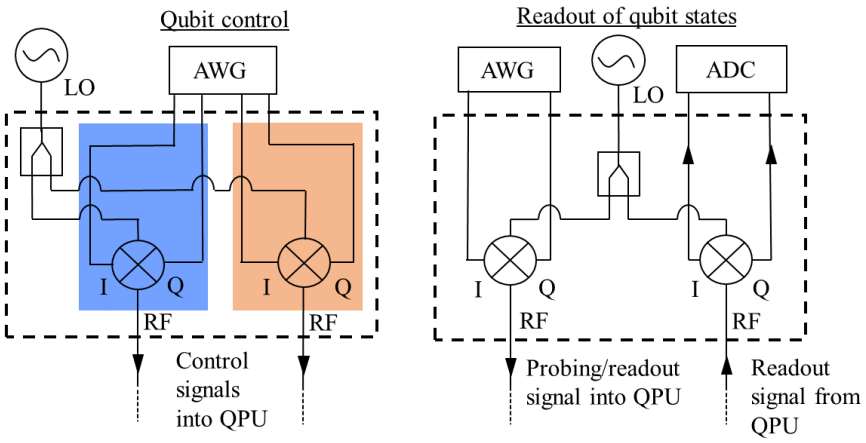


Figure 1.3: Wiring diagram over control and readout signals into the QPU. The colours match the qubits' in Figure 1.2. Contents of the dashed boxes are replaced by the produced control and readout cards. The signals are being attenuated before reaching the QPU.

A problem arises as the frequency needed to drive the state of the qubit is in the low GHz range. Arbitrary waveform generators (AWGs) are unable to generate pulse envelopes that contain the intended information to the qubits due to the frequency being too high. Likewise, the digitisers' analogue-to-digital-converters (ADC) can not sample the readout signals from the resonator circuit at a fast enough rate. This is solved through mixer modulation which consists of an upconversion and subsequently downconversion of the microwave pulse. The AWG generate the pulse envelope in the MHz range, which is then combined in the mixer with a carrier signal in the GHz range resulting in a frequency matching the qubit frequency range [3]. When the resonator signal, which is typically in

the 7-8 GHz range, returns from the qubit circuit the signal is downconverted to a lower frequency.

Furthermore, in order to be able to put the transmon in its intended state the phase between signals sent into the QPU must be precise. Phase noise and unwanted phase offset will affect the qubit fidelity negatively and the aim should be to reduce them as much as possible in instruments connected to the QPU.

1.2 Purpose statement

The purpose of this project is to design a scalable rack instrument to replace the current upconverting and downconverting stages in the quantum processor's control unit. In this thesis, the designs of two separate printed circuit boards (PCBs) will be presented, a *control* card consisting of two channels for frequency upconversion and a *readout* card consisting of one channel for upconversion and another for downconversion. By integrating passive IQ mixers, radio frequency (RF) mixing of the signals can be achieved while keeping a modular design better suited for further development. Two of the cards will be fitted into a 19-inch wide subrack unit with spare slots for later addition of cards. A third card, a backplane, will be fitted into the subrack and provide power distribution in future revisions. Furthermore this thesis presents performance data of the rack instrument, followed by a discussion of possible improvements for future iterations of the PCBs. The instrument will serve as a prototype for QTL to further develop.

2 Theory

This chapter addresses the underlying theory regarding implementation of a mixer in a high frequency electronic circuit. Starting with the ideal mixer, the chapter explains the fundamentals of mixing theory, leading to IQ-mixing and the necessity of calibrating an actual mixer. Furthermore, important aspects of high frequency circuit design are discussed regarding transmission lines and distributed-element circuits, dielectrics and impedance matching of transmission lines. Lastly, relevant theory behind attenuation and reflections in waveguides is presented.

2.1 Implementation of mixers in quantum processors

Mixers are the most central aspect of the instrument and the thesis. Implementing them in the signal-chain to and from quantum processors allows for modular design and scalability. In the following section the basics of the IQ mixer are explained. How and why calibration is needed is also covered in this section.

2.1.1 The ideal mixer

A mixer is an electronic device that can convert frequencies and is used in several high frequency applications such as transmitters and receivers for communication and radar systems. Typically, a mixer has three ports. Two inputs which consist of the local oscillator (LO) signal and the intermediate frequency (IF) signal . The LO signal frequency is usually much higher than the IF signal frequency. These signals are mixed inside of the mixer, producing the resulting RF signal, which is a combination of both the LO and IF frequencies. This arrangement of inputs is used to upconvert the signal frequency. By instead using the RF port as the input, the mixer can also be used to perform downconversion of the signal frequency.

The operation of a mixer can simply be explained. Imagine two input signals

$$s_{LO} = \cos(2\pi f_{LO} t) \tag{2.1}$$

$$s_{IF} = \cos(2\pi f_{IF} t) \tag{2.2}$$

where f_{LO} is the LO signal frequency and f_{IF} is the IF signal frequency. The output of an ideal mixer

$$s_{RF} = \cos(2\pi f_{LO} t) \cdot \cos(2\pi f_{IF} t) \tag{2.3}$$

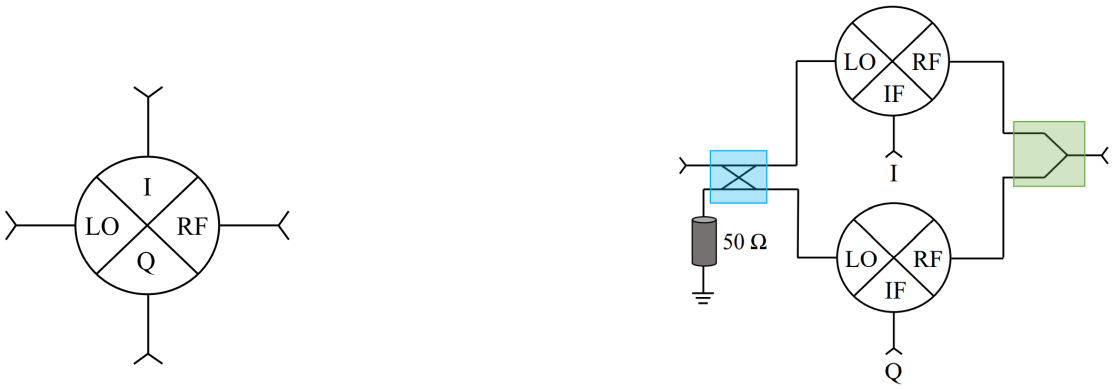
will be the product of the two input signals. Using trigonometric identities the output signal can be rewritten as

$$s_{RF} = \frac{1}{2}\Big[\cos(2\pi(f_{LO} - f_{IF})t) + \cos(2\pi(f_{LO} + f_{IF})t)\Big] \tag{2.4}$$

clarifying the conversion properties of the mixer [9, p. 637-638]. These up-converted signals are often referred to as upper and lower *sidebands*, consisting of the $f_{LO} + f_{IF}$ and $f_{LO} - f_{IF}$ frequency components respectively.

2.1.2 Basics of the IQ mixer

In quantum computing applications it is desirable for the mixer output to only contain one of the sidebands. The reason for this is to be able to target only the qubit frequency. Minimizing LO signal leakage is also important for the same reason. Otherwise, unwanted frequencies can lead to unintended phase-shift which could subsequently reduce qubit fidelity [3]. This can be done if an In-phase/Quadrature-phase mixer (IQ mixer) is used. An IQ mixer is built by using two regular mixers: one of them is fed with an in-phase signal, the I signal, and the other with a 90° out of phase signal, the Q signal. The I and the Q signals represent the IF signal for each mixer. The LO signal is generated from one single source, and is split inside of the mixer component with a so-called *quadrature hybrid*, which is a directional coupler where the two outputs are 90° out-of-phase of each other, see Figure 2.1b. A schematic symbol of an IQ mixer can be seen in Figure 2.1a.



(a) **(b)**

Figure 2.1: **(a)** Schematic symbol of an IQ mixer. **(b)** Internals of an IQ mixer. Quadrature hybrid in blue and power combiner in green.

Modifying (2.2), the I- and Q-signals are given by

$$s_{IF}^{I} = \cos(2\pi f_{IF} t) \quad \text{and} \quad s_{IF}^{Q} = \cos(2\pi f_{IF} t + \frac{\pi}{2}) \tag{2.5}$$

and the LO signals are

$$s_{LO}^{I} = \cos(2\pi f_{LO} t) \quad \text{and} \quad s_{LO}^{Q} = \cos(2\pi f_{LO} t - \frac{\pi}{2}) \tag{2.6}$$

Both of the RF outputs from the mixers are then combined using an in-phase power combiner which forms one single RF output $s_{RF} = s_{RF}^{I} + s_{RF}^{Q}$. Using the same principles as before, this sum will be $s_{RF} = s_{LO}^{I} \cdot s_{IF}^{I} + s_{LO}^{Q} \cdot s_{IF}^{Q}$. Applying (2.4), while choosing $+\frac{\pi}{2}$ for the phase of s_{IF}^{Q}, gives

$$s_{RF} = \frac{1}{2}\Big[\cos(2\pi f_{+} t) + \cos(2\pi f_{-} t) + \cos(2\pi f_{-} t - \pi) + \cos(2\pi f_{+} t)\Big] = \cos(2\pi f_{+} t)$$

Hence, the output signal s_{RF} consist of only the upper sideband. Choosing $-\frac{\pi}{2}$ for the phase of the Q-signal will produce only the lower sideband [10].

2.1.3 IQ mixer imbalances

The case described in section 2.1.2 is ideal. In reality, it is necessary to calibrate the mixer to maintain its performance. There are three main ways by which the mixer is calibrated: phase, amplitude and DC-offset modulation [11]. To achieve a more realistic view of the signals, amplitude offset Δk and phase offset $\Delta\phi$ are added to (2.6)

$$s_{LO}^{I} = (1+\Delta k_1)\cos(2\pi f_{LO}t + \Delta\phi_1) \quad \text{and} \quad s_{LO}^{Q} = (1+\Delta k_2)\cos(2\pi f_{LO}t + \Delta\phi_2)$$

Assuming that the IF signals in (2.5) have an amplitude of A_1 and A_2 respectively, the resulting RF signal is

$$\begin{aligned} s_{RF} = A_1(1+\Delta k_1)\frac{\cos(2\pi f_+ t + \Delta\phi_1) + \cos(2\pi f_- t - \Delta\phi_1)}{2} \\ + A_2(1+\Delta k_2)\frac{\cos(2\pi f_+ t + \Delta\phi_2) + \cos(2\pi f_- t - \Delta\phi_2 - \pi)}{2} \end{aligned}$$

It can be seen that to eliminate one of the sidebands the amplitude and phase of the IF signal must satisfy

$$A_1 = A_2\frac{(1+\Delta k_2)}{(1+\Delta k_1)} \quad \text{and} \quad \Delta\phi_1 - \Delta\phi_2 = 0 \tag{2.7}$$

By choosing appropriate values for A_1 and A_2 the amplitude difference will disappear. Since the phase condition in (2.7) is generally not satisfied, phase offsets on s_{IF}^{I} and s_{IF}^{Q} can be added accordingly.

Minimising the LO signal leakage is done by applying DC-offsets to s_{IF}^{I} and s_{IF}^{Q}. In an ideal mixer, there is no LO leakage, but when the signal runs through the quadrature hybrid the phase difference between the LO signals may not be exactly $\frac{\pi}{2}$ in reality. The same goes for the splitting, as it may not exactly be an even split. Consider a single LO signal provided to the IQ mixer. If two DC voltages, V_1 and V_2, are applied on the I and Q port, the resulting RF output will be

$$s_{RF} = V_1\cos(2\pi f_{LO}t) + V_2\sin(2\pi f_{LO}t) + L_I\cos(2\pi f_{LO}t) + L_Q\sin(2\pi f_{LO}t)$$

where $L_I\cos(2\pi f_{LO}t)$ and $L_Q\sin(2\pi f_{LO}t)$ is the LO leakage. This can be rewritten as

$$s_{RF} = \sqrt{V_1^2 + L_Q^2}\cos(2\pi f_{LO}t + \arctan\frac{V_1}{L_Q}) + \sqrt{V_2^2 + L_I^2}\cos(2\pi f_{LO}t + \arctan\frac{L_I}{V_2})$$

Hence, for $s_{RF} = 0$ the following conditions must be satisfied

$$\sqrt{V_1^2 + L_Q^2} = \sqrt{V_2^2 + L_I^2} \quad \text{and} \quad \arctan\frac{L_I}{V_2} - \arctan\frac{V_1}{L_Q} = \pi \tag{2.8}$$

2.2 Design of radio-frequency electronics

In this section, the necessary theory needed for the design of RF electronic circuits used in this project is presented. The section begins with a brief overview of why transmission line theory is important when designing RF systems, followed by a more detailed explanation of how coplanar waveguides can be designed to reach a specific characteristic impedance. The importance of impedance matching and coupling effects are also discussed. At the end of this section, a short explanation is given about how scattering parameters can be used to analyse RF circuits.

2.2.1 Transmission lines and distributed-element circuits

When designing a PCB for use in RF applications there are a number of effects that need to be addressed. These effects are negligible for lower frequencies [12]. As the frequency of an AC signal increases, the corresponding wavelength decreases proportionally. When this wavelength approaches the length of the conductor carrying the signal, the lumped-element model commonly used when doing circuit analysis no longer adequately describes the behaviour of the signal propagating through the circuit. The reason for this is that because of the relative size of the signal wavelength compared to the length of the conductor, the voltage and current will be a function of not only time but also position along the length of the conductor as the signal propagates through it. Therefore, the conductors are for these higher frequencies modelled as transmission lines that are part of a distributed-element circuit [9, p. 48-51]

2.2.2 The conductor-backed coplanar waveguide

There are many different types of transmission lines used in RF electronics. One of the commonly used ones is a type of waveguide called a conductor-backed coplanar waveguide (CBCPW). It is easy to use with surface-mount devices (SMDs) and provides good isolation from other parts of the circuit by placing a ground plane between them [13, p. 1-10], [14, p. 44]. The geometry of a CBCPW is shown in Figure 2.2. It consists of a signal conducting strip of width S, ground planes on each sides of the strip separated by a gap of width W, as well as an additional ground plane on the bottom. Between the two conducting planes there is a dielectric material with height h.

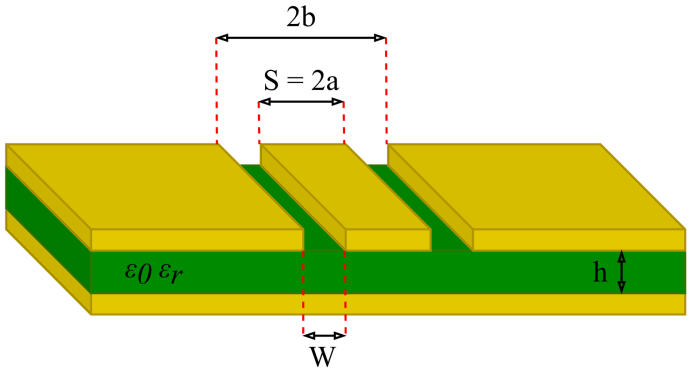


Figure 2.2: The conductor-backed coplanar waveguide (CBCPW).

The bottom ground plane visible in Figure 2.2 is what "conductor-backed" in CBCPW refers to. The bottom ground plane is not present in the conventional coplanar waveguide (CPW) [15]. By adjusting the parameters S, W, h, and ε_{r} shown in Figure 2.2, where ε_{r} is the relative permittivity of the dielectric substrate, the effective dielectric constant $\varepsilon_{\mathrm{eff}}$ and characteristic impedance Z_0 can be accurately selected [13, p. 11, 87-89]. The effective dielectric constant $\varepsilon_{\mathrm{eff}}$ and characteristic impedance Z_0 are calculated as

$$\varepsilon_{\mathrm{eff}} = \frac{1+\varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_3)}{K(k_3')}}{1+\frac{K(k')}{K(k)} \frac{K(k_3)}{K(k_3')}}, \quad Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{\mathrm{eff}}}} \frac{1}{\frac{K(k)}{K(k')} + \frac{K(k_3)}{K(k_3')}} \tag{2.9}$$

where

$$k = \frac{a}{b}, \quad k_3 = \frac{\tanh(\frac{\pi a}{2h})}{\tanh(\frac{\pi b}{2h})}, \quad k' = \sqrt{1-k^2}, \quad k_3' = \sqrt{1-k_3^2} \tag{2.10}$$

and K(k) is the complete elliptic integral of the first order [13, p. 87-89]. Since (2.9) depends on the relative sizes of the parameters a and b in (2.10), it is possible to achieve the same characteristic impedance for different track widths S by simply adjusting the gap width W (shown in Figure 2.2) accordingly.

The guided wavelength in the CBCPW can then be calculated using

$$\lambda_G = \frac{1}{f\sqrt{\varepsilon_{eff}\varepsilon_0\mu_0}} \tag{2.11}$$

2.2.3 Impedance matching and dielectric losses

Matching the characteristic impedance of the transmission line is necessary in order to minimise signal reflection [9, p. 56-59]. The reflection coefficient between two interfaces is generally represented by Γ. For the interface between a transmission line and the load, the reflection coefficient is

$$\Gamma_{\mathrm{L}} = \frac{Z_{\mathrm{L}} - Z_0}{Z_{\mathrm{L}} + Z_0} \tag{2.12}$$

where Z_{L} is the load impedance and Z_0 is the characteristic impedance of the line [9, p. 76-77]. If the transmission line is properly matched, Γ_{L} will be zero; the transmission line will have no reflection and the maximum amount of power will be delivered to the load. An impedance mismatch will give rise to reflections in the circuit and thereby result in so-called mismatch loss, which is a measure of the power that is wasted in the system [16]. A mismatched transmission line is thus a source of attenuation.

Another source of attenuation is dielectric loss, which can be minimised by limiting the length of the transmission line [9, p. 83].

2.2.4 Coupling between transmission lines

When designing a PCB with multiple transmission lines, the spacing between transmission lines as well as the distance that they run in parallel will affect the coupling effects between them. In order to minimise unwanted coupling effects, the transmission lines should be as distantly placed as possible, and the distance for which they are in parallel should be as small as possible [14, p. 44]. One advantage of using CPWs is that there is always a ground plane between transmission lines, which reduces unwanted coupling [13, p. 1].

2.2.5 S-parameters and VSWR

When characterizing a RF circuit it is common to measure the scattering parameters, often referred to as S-parameters. Measuring S-parameters can be done in any N-port system, but explaining it in terms of a 2-port system is the most straightforward approach. S-parameters are ratios between incoming and outgoing electromagnetic waves at the systems ports. This is often represented as a linear equation

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{21} \\ S_{12} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}$$

where the minus and plus signs represent the incoming and outgoing waves respectively on either port 1 or 2. These parameters give information of the performance of the system. The variable $S_{11} = \frac{V_1^-}{V_1^+}$ is the reflection coefficient equivalent to (2.12) and $S_{21} = \frac{V_2^-}{V_1^+}$ is the attenuation, or gain in an active system. A typical measure of the mismatch of a transmission line is *Voltage Standing Wave Ratio*, VSWR, which is given by

$$VSWR = \frac{|V_{max}|}{|V_{min}|} = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{2.13}$$

which is a real number $1 \leq VSWR \leq \infty$. For a perfectly matched line $VSWR = 1$.

2.2.6 Phase noise

An ideal sinusoidal signal has a single peak in the frequency spectrum. In practice, the peak will be accompanied by some phase noise caused by the signal generator and possibly by the device under test. Phase noise will cause the signal to spread out over the frequency spectrum, which is not desirable in quantum computing since this can cause unintended phase shifts on the qubits.

3 Development of the rack instrument for QPU control

The purpose of this section is to describe the steps of the development process, from initial specifications to the finished rack instrument. An overview of the system is presented, followed by a description of the components chosen during the design process. Lastly, the finished rack instrument is presented.

3.1 System overview and initial specifications

Specifications received from QTL mainly concerned the frequency operating ranges for the LO and IF signals respectively, which can be seen in Table 3.1. Additional requirements states that the frequency upconverted signal is at least 50 dB higher than the LO leakage and image sideband after calibration. Considerations when choosing PCB material and components were price and availability. These choices were made while still meeting the specification of the project.

Table 3.1: Instrument specification.

Instrument specifications	RF/LO freq. range [GHz]	IF freq. range [MHz]	LO/Image suppression [dB]
Mixer	4-8	0-1000	50

The aim is to design three PCBs, consisting of one upconverting control PCB, one downconverting readout PCB and a backplane PCB which will provide power to future integration of amplifiers and microcontrollers. A block diagram depicting the control and readout circuits can be seen in Figure 3.1 and 3.2. Note that on the upconverting portions of each card is followed by a directional coupler with a calibration port attached to it. This means that it is possible to calibrate the mixers without swapping cables from the QPU. Applying DC biases on the IQ-signals is done through bias tees which allows the use of a separate DC-source.

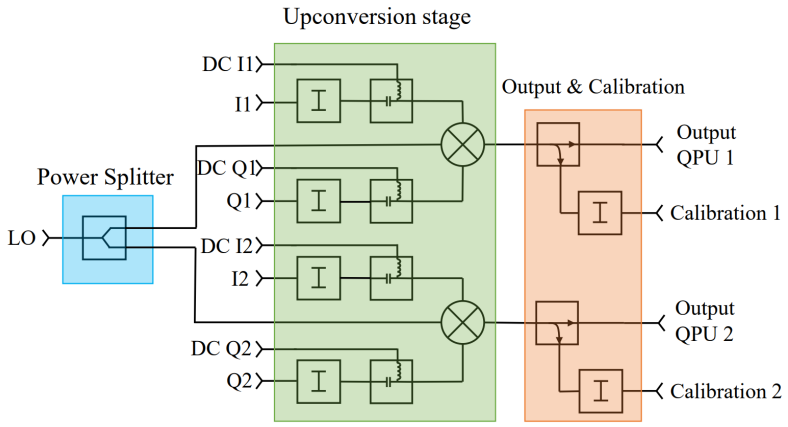


Figure 3.1: Block diagram of the control card. The upconversion stages are used for upconverting the qubit control signal.

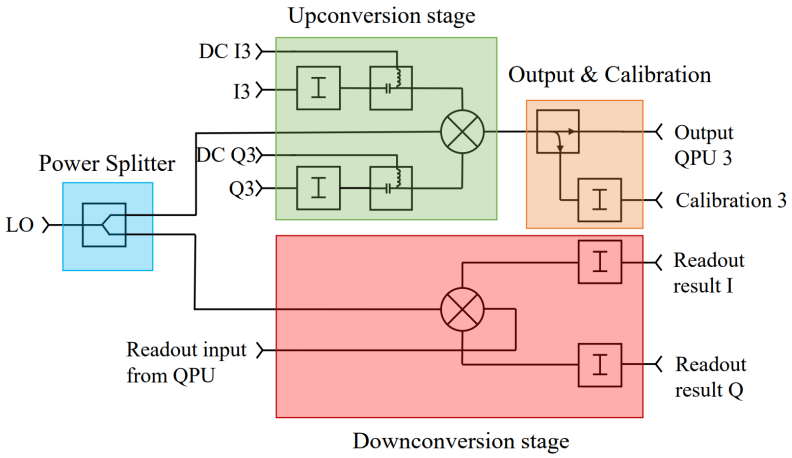


Figure 3.2: Block diagram of the readout card. The upconversion stage on the top is identical to the one on the control card, while the bottom mixer is performing the down-converting operation of the readout signal from the QPU.

3.1.1 Components

The mixer is the core of the project and the whole system is designed accordingly. Since the quantum processor used in QTL are operating between 4-8 GHz, the SMD IQ mixer HMC8193 from Analog Devices fits the specification. The IQ mixer has an operating range for RF and LO ports between 2.5-8.5 GHz and DC-4 GHz for the IF ports [17]. Some of the most important parameter values can be seen in Table 3.2. All the components mentioned in this section are listed in Appendix A.

Table 3.2: HMC8193 data.

HMC8193	RF/LO (GHz)	IF (GHz)	Image reject. (dB)	Isolation LO/RF (dB)
	2.5-8.5	DC-4	25	48

Bias tees were used to apply DC biases for LO suppression on the I and Q signals as described in Section 2.1.3. A bias tee consists of an inductor and a capacitor which combines DC and RF signals while still keeping the DC and RF parts of a system separate. This can be seen in Figure 3.1 and 3.2. For this purpose, the SMD bias tee TCBT-14R+ from Mini-Circuits was chosen. The component is matched to 50 Ω, requiring no external matching, and operates between 10 MHz-10 GHz [18]. All IF signals are specified to provide frequencies between 100-1000 MHz which is satisfied by using the TCBT-14R+. The insertion loss of the component is specified to 0.6 dB in the datasheet.

Since two mixers are used in both the control and readout designs, the LO signal needs to be split. The splitting is done with the power splitter MPD-0226SM from Marki Microwave. It is specified between 2-26.5 GHz, with a splitting loss of -3 dB and additional insertion loss of -1.5 dB [19].

At the mixer output, a directional coupler is used for the purpose of calibrating the mixer. This is done with the directional coupler MC16-0222SM, also from Marki Microwave, which operates between 2-22 GHz and provides a coupled output of -16 dB [20]. The direct line loss is specified to -1.5 dB.

Attenuators are used to decrease VSWR on the transmission lines. They are used on all IQ lines as well as the coupled output of the mixer. In this design, the attenuators GAT-X from Mini-Circuits are used. They exist in different varieties when it comes to the amount of attenuation. For the IQ-lines, GAT-3+ is used, providing -3 dB of attenuation. For the coupled output, GAT-1+ is used [21, 22]. The different varieties all come in the same SMD package which allows for trimming the attenuation level.

Connecting to the instrument is done via SMA connectors. In this design the edge-mounted Rosenberger 32K145-400L5 SMA connector is used. The connector is rated from DC to 18 GHz [23].

3.2 Design process

In order to be able to test individual parts of the PCBs and to assure both components and transmission lines worked as intended, several smaller evaluation boards were manufactured. The small boards were then tested and improvements implemented on the final boards. All schematic and PCB design was performed in the Electronic Design Automation (EDA) software KiCAD and the designs were sent to the PCB manufacturer Eurocircuits. This section will further specify which simulations and tests were made before the final cards were designed.

3.2.1 Simulation of characteristic impedance

The transmission lines used in this application consists of CBCPW. Since the characteristic impedance is heavily dependent on geometry, the dimensions can be adjusted according to the dielectric material and PCB build-up to reach the desired value. For the evaluation boards a 2-layer build-up with h=1.55 mm dielectric thickness was used. The dielectric material used was IS400 from Isola. IS400 is a fibreglass material with relative permittivity $\varepsilon_r = 4.45$ at 5 GHz [24]. Since the height of the dielectric is fixed, the track

width and gaps can be altered to reach a characteristic impedance close to 50 Ω. Unfortunately, the minimal track clearance available from Eurocircuits for this particular build-up was 0.2 mm, resulting in a characteristic impedance of $Z_0 = 51.015$ Ω according to the impedance calculation tool built into KiCad.

The 4-layer PCB build-up used in the final design of the circuits can be seen in Figure 3.3. To minimise the dielectric losses, the dielectric material I-Tera was chosen which is a high-performance RF material [25]. Simulations of the characteristic impedance were done in the simulation software ADS and the resulting values can be seen in Table 3.3. The CPW model presented in section 2.2.2 gives similar values of $Z_0 = 49.588$ Ω and $\varepsilon_{eff} = 2.577$. In Table 3.3, $\tan(\delta)$ is the dissipation factor and t is the thickness of the copper layer on the top.

Table 3.3: Simulated values of Z_0 and ε_{eff} together with the geometry of the CBCPW.

$Z_0[\Omega]$	$\tan(\delta)$	ε_r	ε_{eff}	t [μm]	h [mm]	W [mm]	S [mm]
49.905	0.0031	3.45	2.501	18	0.508	0.36	1

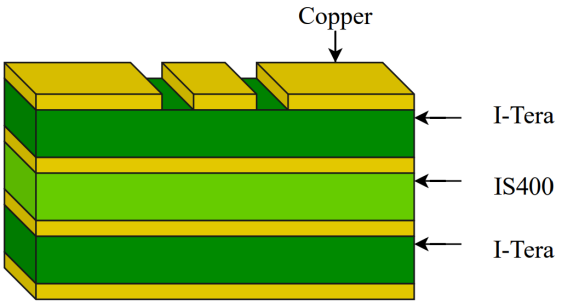


Figure 3.3: PCB material build-up for the final board design. The signal layer is on top and the power layer is on the third copper plane viewed from the top.

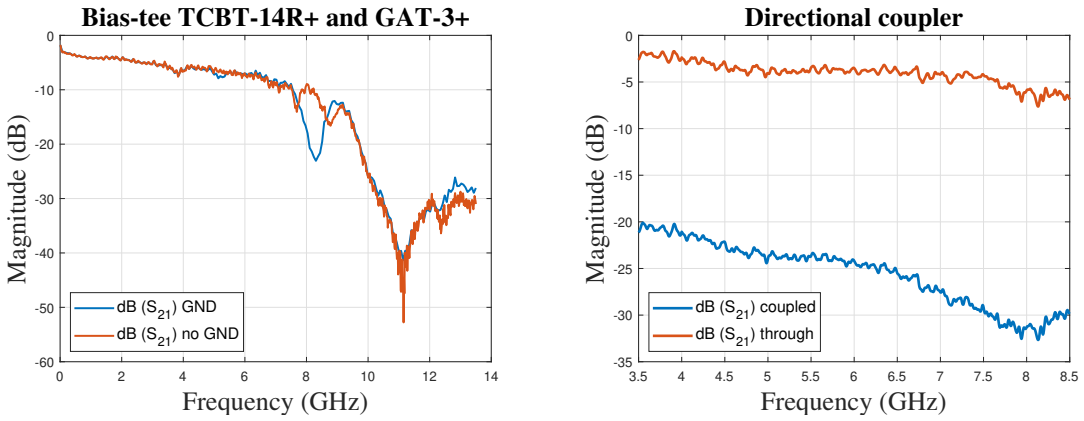
3.2.2 Assembly of PCBs

The assembly of the boards was done by the group at Chalmers University of Technology, at the Electronics Materials and Systems Laboratory and at the QTL. To apply solder paste to the component footprints, a solder paste dispenser was used. A manual pick-and-place tool was then used to place the components onto the board. Finally, the boards were put in a reflow oven which fixed the components in place. Soldering of the SMA-connectors was performed by hand at QTL as well as soldering the Eurocard connectors on the backplane.

3.2.3 Testing of evaluation boards

To verify the design, evaluation boards with either one or two discrete components were made. The parts tested were the mixer, the coupler and bias tee. When testing the PCB with the bias tee and attenuator, a unexpected drop in transmission occurred, which can be seen at around 8.3 GHz of S_{21} in Figure 3.4a. After comparing the design with evaluation boards made by the manufacturer of the bias tee, it was discovered that pin 3 was not

connected to ground. The pin is marked as "not connected" in the datasheet, which was incorrectly interpreted as meaning that the pin was not internally connected to the rest of the component. After discussing the issue with the component manufacturer, the connection between this pin and the ground plane was manually removed. As can be seen in figure 3.4a, disconnecting the pin resulted in the unexpected dip disappearing. However, the dip occurred far beyond the operating range of DC-1 GHz for the I and Q signals, which means it would not have negatively affected the performance even if had not been corrected.



(a) **(b)**

Figure 3.4: **(a)** S_{21} for the bias tee and attenuator board when connected to ground in blue versus not connected to ground in orange. **(b)** S_{21} for the directional coupler board with an attenuator of -1 dB at the coupled output.

It was also found that the evaluation board for the directional coupler had transmission lines with incorrect dimensions, which was a design error. Note that the loss is greater than the expected 1.5 dB, see Figure 3.4b. Impedance mismatching is expected to be the reason for this increase in loss.

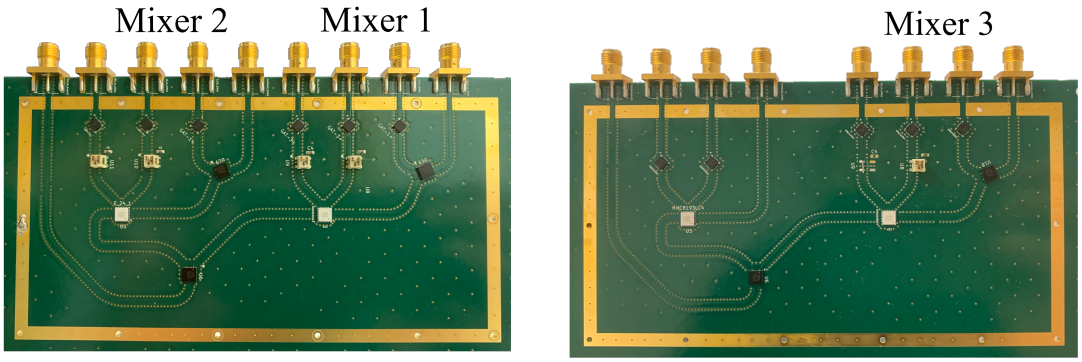
3.3 Final design of the rack instrument

This section presents the final instrument and how the specifications in section 3.1 have been realised. The section is divided into three subsections, the first one showing the layout of the plugin cards which are the PCBs with the upconverting and downconverting stages. The second section describes how the PCBs fit into the subrack and how power is supplied to them through DC connectors. Lastly, the third present which external instruments the rack is connected to.

3.3.1 RF plugin cards

After simulating the impedance of the transmission lines and testing of the individual parts of the circuit, the design was updated and the final boards constructed. Figure 3.5a and 3.5b show a close-up of the control card and readout card respectively. The layout follows the block schematics of Figure 3.1 and 3.2.

The transmission lines are designed to minimise reflections in the circuit and the geometry of the CBCPW is according to subsection 3.2.1. In order to avoid coupling effects, metal plated holes through the board called *vias* are scattered around the boards and along the transmission lines. The vias connect ground planes in the boards with each other. The length of the transmission lines between the LO signal input and the I and Q output were measured and designed to be as similar as possible to avoid unwanted phase offset. The tracks carrying the DC bias to the mixers are routed on the third layer of the PCB buildup and are therefore not visible except for near the bias tee where the component connects to the third layer through a via. The DC biasing tracks are connected to a DC connector on the board.



(a) **(b)**

Figure 3.5: **(a)** Close up of the two upconverting sections on the control card. **(b)** Close up of the upconverting and downconverting sections of the readout card. Edge-mounted SMA-connectors are soldered to the top of the board. The leftmost SMA-connector on both boards is the input for the LO signal which is split into two mixer stages. DC signals, supplied by a non-depicted pin header, run through the third layer of the board and are not visible.

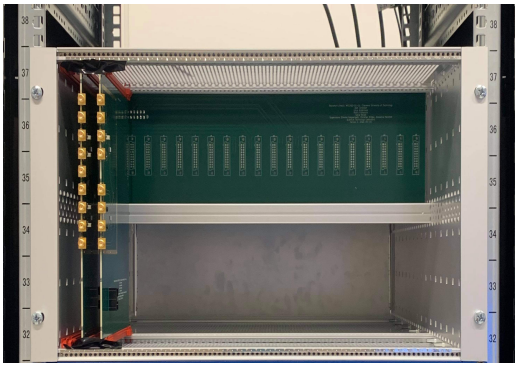
A rectangular area without green solder mask can be seen in Figure 3.5 which allows electromagnetic shielding to be attached. Using the mounting holes drilled into the board along the rectangular area, a metal box can be mounted to the boards in order to further shield the RF circuitry. No shielding was added in this project due to time constraints but is an option in future board revisions.

As of now the mixer stages are referred to by numbers as per Figure 3.5. When inspecting the boards when they were received it was discovered that the power line to the bias tee on Mixer 3 was accidentally routed too close to a via, which shorted the bias tee to the ground planes. Subsequently the decision was made to not solder the bias tee and instead bypass the component with a metal pin which can be seen in Figure 3.5b.

3.3.2 Subrack, backplane and power supply

The plugin cards along with the backplane and power supply are housed in a 6U/84HP (1 U= 44.45 mm, ”Horizontal Pitch” 1 HP= 5.08 mm) subrack by the manufacturer nVent

Schroff, made to fit a 19-inch (48 cm) standard rack cabinet, see Figure 3.6a.



(a)

(b)

Figure 3.6: **(a)** The subrack inside the rack cabinet with the control- and readout cards inserted. The backplane is mounted inside the subrack. **(b)** DC power distribution to the bias tees. A ribbon cable connects to a DE 9 connector and the DC is supplied by an AWG.

The power supply is a 180 W four-channel embedded switch mode power supply that is enclosed and medical approved from TDK-Lambda with manufacturer article number NV1-4G5TT-C. It is connected to the 2-layer backplane which then distributes the four channels to the plugin cards. The plugin RF cards are connected to the backplane via DIN 41612 Eurocard connectors by Harting, on the rear of the cards. A maximum of 21 plugin cards can be connected simultaneously.

Table 3.4: **(a)** The pin configuration of the Eurocard connector on the backplane. NC = Not connected. **(b)** The power supply specifications according to the manufacturer.

(a)

Pin row	Pin columns 1 and 2
1	+24VDC
2	+12VDC
3	+5VDC
4	GND
5	-12VDC
6	NC
7	NC
8	NC
9	NC
10	NC

(b)

Channel	Voltage [V DC]	Maximum current [A]
1	24	7.5
2	5	8
3	12	5
4	-12	1

As can be seen in Table 3.4a the number of pins available on the Eurocard connector is greater than the ones currently used. This was done at the request of the project supervisor

in order to make room for future iterations of the backplane to include digital electronics that can be used to control the plugin cards.

The DC for the bias tees on the I and Q ports is not supplied by the backplane but from a DC connector on the board as stated in section 3.3. A ribbon cable connect the board to a DE 9 connector which can be seen in Figure 3.6b.

3.3.3 Connection to external instruments

The rack instrument was fitted into a rack cabinet at QTL which can be seen in Figure 3.6a. To be able to test the functions of the rack instrument and measure image rejection and LO signal isolation; the spectrum analyser Keysight M9803A was used. The LO signal was generated using an Anapico APMS20G-4 signal generator, and the IF signals together with the DC biases were generated by the AWG Keysight M3202A. The block schematic can be seen in Figure 3.7. To ensure the instruments were synced, a rubidium frequency standard atomic clock FS725 from Stanford Research Systems was used as a frequency reference. RF cables 141-XXSM+ from Mini-Circuits in various lengths were used to connect both the SMA-connectors to the external instruments and the DE 9 connector to the AWG. Since phase is an important factor when sending or receiving signals to and from the I and Q ports, cables of equal length were used when connecting I and Q to the AWG. For Mixer 3, where the bias tee was bypassed, the DC bias was supplied along with the RF signal from the AWG instead.

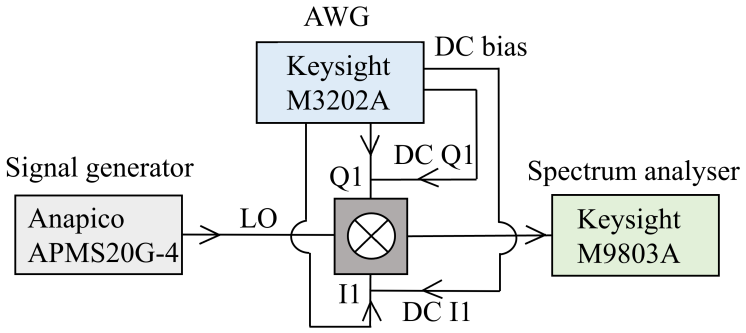


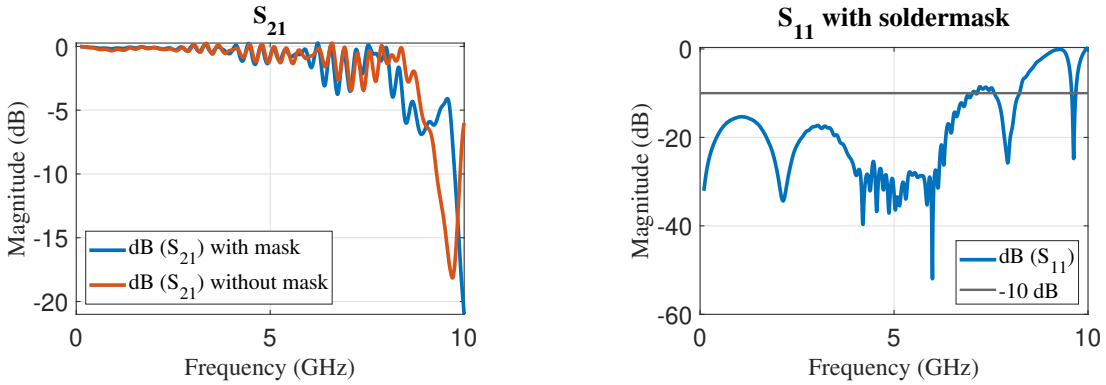
Figure 3.7: Block schematic of the measurement setup at QTL with a PCB mixer stage in the middle. Both RF signals and DC bias to the mixer stage on the board are supplied by the AWG. A network analyser was used to measure the output spectrum. A connected non-depicted rubidium atomic clock ensures the instruments are synchronised.

4 Performance measurements of the final boards

In this section, measurement results covering the performance of the instrument are presented. Beginning with an evaluation of the transmission line performance, the section continues with a demonstration of IQ mixer calibration for the upconversion mixers. The readout ability is tested and compared to the readout performance of an evaluation board provided by the component manufacturer. Lastly, the phase noise characteristics during upconversion are evaluated.

4.1 Attenuation and impedance matching of the CBCPW

In order to determine how the solder mask affects the performance of the transmission lines, two additional test boards were manufactured. These test boards consist of a straight CBCPW between two SMA connectors and are identical except that one of them does not have any soldermask or silkscreen. Their performance was evaluated by S-parameter measurements using the Keysight P5024A vector network analyser (VNA) with input power set to -10 dBm. Figure 4.1 shows the measured S-parameter performance of the CBCPW test boards with and without solder mask. From Figure 4.1a it is evident that the difference in attenuation greatly increases above approximately 8 GHz.



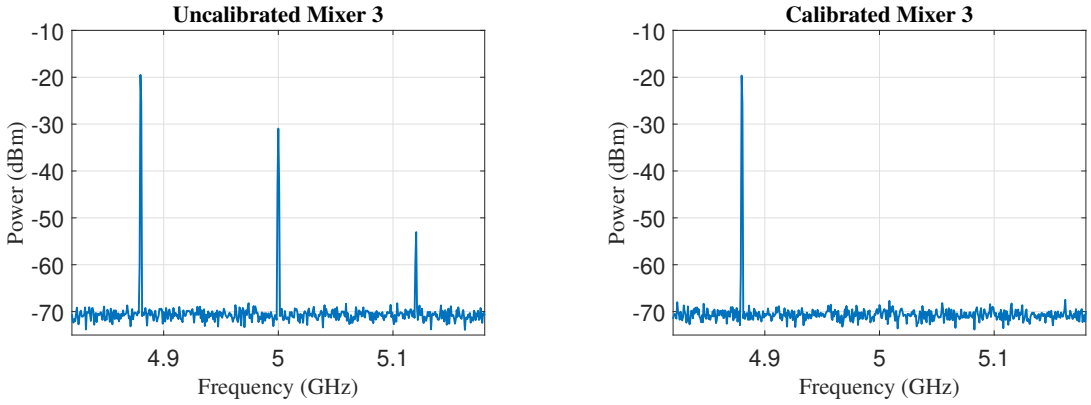
(a) **(b)**

Figure 4.1: S-parameter measurements of the CBCPW test boards. **(a)** S_{21} of the CBCPW test boards. **(b)** S_{11} of the CBCPW test board with solder mask.

As can be seen in Figure 4.1b, the magnitude of S_{11} is below -10 dB for almost the entire frequency range of 100 MHz to 8 GHz, except for around 7 GHz. The frequency difference between two minima in the wide ripple in S_{11} is around 1.69 GHz. By using (2.11), the frequency difference corresponds to a distance between discontinuities of around 5.5 cm. From S_{21} in Figure 4.1a a high frequent ripple can be seen. The frequency difference between two minima is about 340 MHz which corresponds to a distance of around 27 cm.

4.2 Suppression of upper sideband and LO leakage through mixer calibration

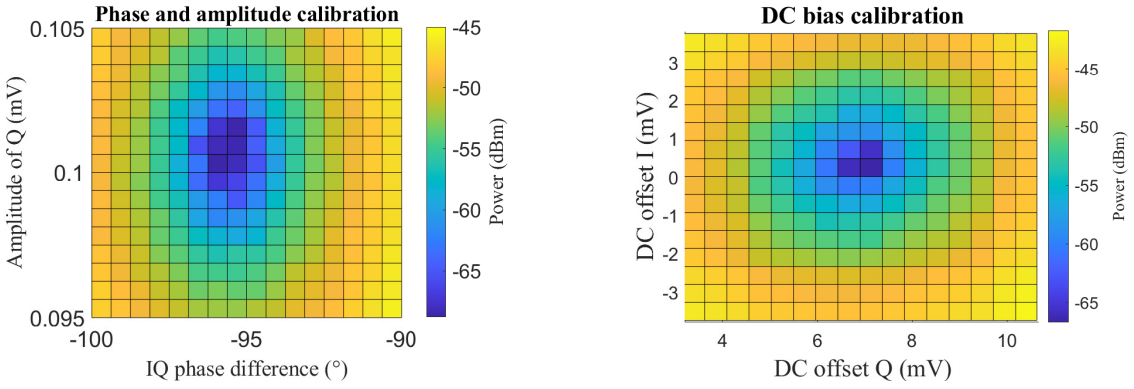
The mixer calibration was performed as outlined in Section 2.1.3 to suppress both the upper sideband and the LO leakage.



(a) **(b)**

Figure 4.2: **(a)** The output spectrum from mixer 3 before calibration. **(b)** The output spectrum from mixer 3 after calibration. Note that the peaks at 5 GHz and 5.12 GHz have disappeared into the noise floor.

The suppression of the upper sideband at 5.12 GHz shown in Figure 4.2a was done by measuring the power of the sideband for different combinations of IQ phase and amplitude differences. The sideband power measurements were plotted as shown in Figure 4.3a.



(a) **(b)**

Figure 4.3: Surface plots of amplitude, phase and DC calibration. **(a)** Optimal phase and amplitude biases for suppressing the upper sideband are found in the blue area. **(b)** Optimal DC biases for suppressing the LO signal are found in the blue area.

The sideband power measurements were repeated using a progressively smaller span of input parameters until a combination of parameters resulting in the upper sideband being

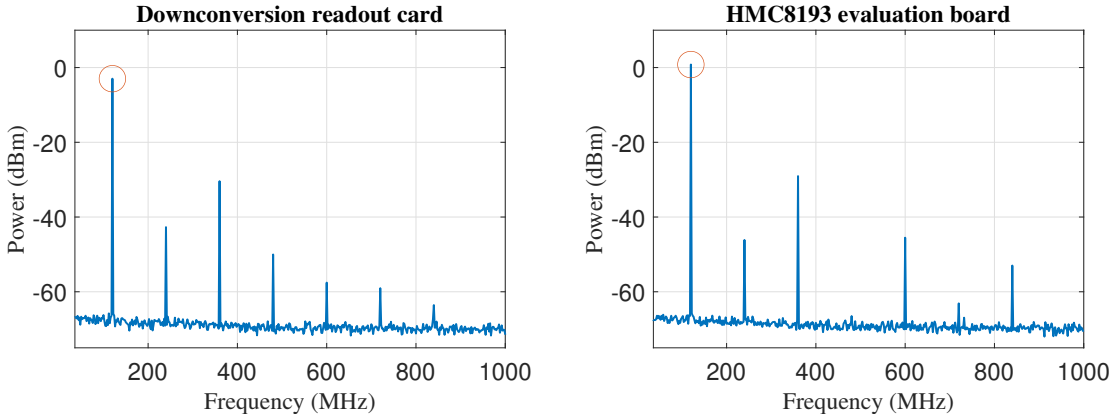
indistinguishable from the noise floor was found. The spectrum of the calibrated mixer obtained in the measurements is shown in Figure 4.3a. Final combinations of phase and amplitude deemed to give an optimal upper sideband suppression is presented in Table 4.1. The calibration process continued in order to suppress the LO signal at 5 GHz shown in Figure 4.2a. The LO power for different combinations of IQ DC offsets is shown in Figure 4.3b. As was the case for upper sideband suppression, the DC bias calibration was repeated with progressively smaller spans of input parameters until a combination which sufficiently suppressed the LO was found. As is evident in Figure 4.2b, the calibration process resulted in the acquisition of parameters that can suppress both the upper sideband and the LO signal until they are indistinguishable from the noise floor. The calibrated parameters along with the measured image rejection and LO isolation are shown in Table 4.1.

Table 4.1: Measurement conditions, calibration parameters and performance of calibrated up-conversion mixers.

Measurement conditions	**Upconv. mixer 1**	**Upconv. mixer 2**	**Upconv. mixer 3**
LO Drive level (dBm)	16.5	16.5	16.5
LO freq. (GHz)	5	5	5
IF freq. (MHz)	120	120	120
Calibrated parameters			
Phase I (°)	0	0	0
Amplitude I (mV)	100	100	100
Phase Q (°)	83.8*	-95.8	-94.4
Amplitude Q (mV)	101.3	100.3	100
DC bias I (mV)	-1.2	0.1	-3.6
DC bias Q (mV)	8.8	6.6	12.2
Performance			
Image rejection (dB)	49	49	51
LO Isolation (dB)	86	84	85

Due to issues with the measurement equipment, the measured value for the phase offset of Q for mixer 1, marked with *, is likely incorrect. These issues are discussed further in Section 5.1.

To demonstrate the readout functionality of the readout card, downconversion of a 4.88 GHz signal was performed. To do this, port 1 of the Anapico APMS20G-4 was used to provide a 16.5 dBm, 4.88 GHz signal to the RF input of the readout card. Port 2 of the same instrument was connected to the LO port of the readout card, providing the LO signal at 21 dBm at 5 GHz. The result can be seen in Figure 4.4 where the same settings used for the readout card was applied to an evaluation board of HMC8193, provided by the manufacturer. In both cases, the output of the I port was measured.



(a) **(b)**

Figure 4.4: A demonstration of the readout capability of the instrument, where the downconverted signal at 120 MHz is marked with a circle in both graphs. **(a)** The readout spectrum for a 4.88GHz RF signal of downconversion mixer on the readout card. **(b)** Same settings, but attached to the evaluation board of HMC8193 IQ mixer.

As can be seen Figure 4.4a and 4.4b, higher order mixing products appear in the spectrum. The most prominent, higher order peak is at 360 MHz. Relative to the downconverted signal of the readout card the difference between the 120 MHz and 360 MHz peak is around 27 dB. For the evaluation board, the difference is around 30 dB.

The phase noise for the lower sideband of mixer 1 was measured using the spectrum analyser USB-SA124B from Signal Hound. In Figure 4.5 the phase noise was measured up to 1 MHz offset from 4.88 GHz. Firstly, the output from port 2 of the Anapico APMS20G-4 was measured when directly connected to the spectrum analyser. In the next step, the same port was connected to the LO input of the control card. This time, the LO was driven at 5 GHz and at a power level of 21 dBm. After calibration, the phase noise was measured up to 1 MHz offset to the 4.88 GHz lower sideband of the calibrated mixer. The mixer stage does not seem to add noticeable phase noise to the the signal.

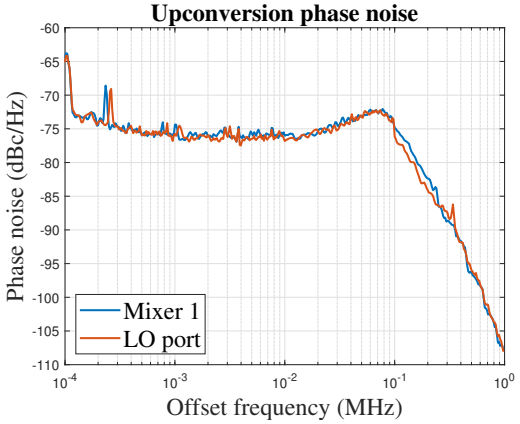


Figure 4.5: Phase noise at 4.88 GHz measured at the LO source and at the output of the upconverting mixer 1.

5 Discussion and conclusion

In this section, the results presented in Section 4 are discussed and is subsequently paired with suggestions of possible improvements to the instrument. This part contains a number of aspects that could be improved or otherwise further investigated for future iterations of scalable signal mixer stages in quantum processors.

5.1 Evaluation of the mixer stages

The performance of the transmission lines designed in this project can be seen in Figure 4.1a and 4.1b. As can be seen, the transmission in the S_{21} plot is dropping slightly until the frequency reaches above 8 GHz, where a big drop can be seen. The reflection is larger than expected compared to simulations. In the datasheet of the SMA connector (Rosenberger 32K145-400L5) used in this project, the VSWR no longer linearly increases with frequency when above 8 GHz according to the datasheet. Therefore, it is suggested to try another SMA connector with the same transmission line dimensions. It should be noted that the parameters of the calibration kit used were not pre-programmed in the VNA. This means that the nonidealities of the calibration kit were not accounted for when calibrating.

As is evident from Figure 4.2, the upconverting mixer stages can be calibrated to suppress both the upper sideband and the LO leakage. Looking at Table 4.1, there is a significant difference in phase of Q for upconverting mixer 1 compared to mixer 2 and 3, 83.75°compared to -95.8°and -94.4 °. The first mixers to be calibrated were mixer 2 and 3 because an attenuator on mixer stage 1 had not been properly soldered. By the time mixer stage 1 had been properly soldered and was ready for calibration, there had been some maintenance and other testing in the lab at QTL. When attempting to calibrate mixer 1, it was discovered that the phase difference between I and Q needed to be significantly different when compared to mixers 2 and 3. In order to verify that this unexpected parameter value was not simply due to a design or assembly issue of the mixer stage, the previously calibrated mixers were tested again, and it was found that their calibration parameters had changed significantly more than had previously been experienced when doing calibrations. An obvious explanation would have been that the I and Q connections had been mixed up, which was investigated and found not to be the case. Since the theory discussed in Section 2.1.2 suggests that the parameters initially determined for mixers 2 and 3 are correct, one possible explanation is that some setting in the computer program used for calibration was changed when another group did measurements during the time between calibration of mixers 2 and 3, and mixer 1. Except for the issues regarding the phase and possible crosstalk, all four mixers seemed to be functioning correctly.

The calibration ports for mixer 1 and 3 show the same characteristics as the output ports of the mixers. However, when suppressing the LO signal on the output of mixer 2, it appears on the calibration port. This is likely due to the fact that this mixer is too close to the LO port of the PCB. Due to this, the coupling is different on the output and calibration port, which makes the interference behave differently between the ports. Nonetheless,

the upper sideband suppression for all the mixers is maintained on the calibration ports. To solve this problem, the best solution would be to try and isolate the LO port and the transmission line carrying the signal with EMI shielding. In addition, designing a PCB with two transmission lines and measure the coupling between these can also be done to investigate the coupling effects.

The downconversion of the readout card shows similar performance as the evaluation board of HMC8193. As can be seen in Figure 4.4a and 4.4b, several higher order mixing products appear in the spectrum of both mixers. The mixers are fed with a LO signal with an estimated power of 16.5 dBm, which is below the recommended level of 18 dBm given in the datasheet. Therefore, the prominence of higher order peaks may be different if another power level of the LO signal is used. To see if this is the case, one could measure how these peaks vary in power when sweeping the power of the LO signal. In addition, studying the spectrum of Figure 4.4a closely, one can see a peak at 480 MHz which does not appear on the evaluation board. If higher order mixing products on the output depends heavily on the LO power, one explanation to why the 480 MHz peak shows up could be because the LO power is slightly less than 16.5 dB. It can be seen that the power of the downconverted peak at 120 MHz is slightly different on both boards. On the evaluation board, the peak is around 0.8 dBm while on the readout card it is around -3 dBm. However, this difference in power is more likely to be caused by the attenuators of -3 dB at the I and Q ports on the readout card.

The circuits designed in this project do not seem to add any additional phase noise compared to the phase noise of the signal source. However, the phase noise measured in Figure 4.5 is significantly higher than what is stated in the datasheet of Anapico APMS20G-4. The phase noise of the Anapico was also measured with the Keysight P5024A VNA which gave the same result. More measurements of the phase noise should be done in order to properly understand why the measured phase noise from the Anapico APMS20G-4 was not what was expected.

5.2 Improvements

Tapers were used in the design of the RF plugin cards when transitioning from one CBCPW track width to another. The gap width of the tapers were however not appropriately adjusted in order to retain the characteristic impedance as specified in Section 2.2.2. This means that the characteristic impedance will not remain constant through the taper which could lead to signal reflections as discussed in Section 2.2.3. In order to more accurately match the characteristic impedance of the transmission lines, tapers with correctly varying gap widths should therefore be used.

Originally, the design of the control card contained an amplifier with the purpose of driving the LO signal before it entered the mixer. The amplifier was also supposed to be driven in saturation mode, ensuring a constant power level was delivered to the mixer. An evaluation board was developed for this purpose, containing the amplifier HMC8412 from Analog Devices [26]. To increase power integrity, the amplifier was powered via the low drop out, low noise voltage regulator LP38798 from Texas Instrument [27]. However, a suspected damage to the amplifier occurred during measurement. Therefore, it was im-

possible to determine the performance of the amplifier in the scope of this thesis, which resulted in it being excluded from the final design. In a future version, it is strongly recommended to revisit the design suggested in this thesis in order to examine the possibility of integrating an amplifier.

An LO distribution card was also requested in the project specification, and it was designed as shown in Figure B.1 in Appendix B. Because the distribution card would split the input signal between the eight output ports, the resulting loss in signal strength was deemed to be too high to be useful without an accompanying amplifier. Since there were some issues regarding the amplifier as previously discussed in this section, it was decided that the LO card would not be manufactured along with the control and readout cards. For future designs, a properly functioning amplifier would therefore enable the use of a plugin card to distribute the LO signal.

As can be seen in Figure 3.6a, the Eurocard connector on the rear of the plugin cards does not line up with the corresponding connector on the backplane. This mistake in design was a result of a misinterpretation of the subrack design guide. Since the only purpose of the backplane for this iteration of plugin cards was to power the amplifiers, and there were no amplifiers for this iteration, the inability to connect the plugin cards to the backplane does not negatively affect the usability of the plugin cards. It should nonetheless be corrected in future iterations.

When attempting to attach a front panel to the plugin cards, it became evident that the chosen model of SMA connector was not compatible with the front panel. The front panel would in fact prevent the SMA cables from being properly screwed in. The front panels were therefore not attached to the plugin cards. As such, the plugin cards can be placed on the guide rails inside the subrack but not otherwise locked in place. Additionally, the backplane may need to be moved slightly horizontally in order for the front panels to properly line up with the front of the subrack. Subrack rails capable of this horizontal movement were purchased but not installed during assembly of the subrack. For future iterations, compatibility between front panel and SMA connectors should be properly investigated.

5.3 Conclusion

The purpose of this thesis was to design and demonstrate the performance of scalable signal mixer stages in quantum processors. A rack instrument that is capable of performing both frequency upconversion and downconversion of signals was successfully developed. The instrument is now integrated in the Quantum Technology Laboratory (QTL) at Chalmers University of Technology and can be used in experiments for quantum processor control and readout. The rack instrument presented in this thesis promises scalability in terms of the modular design, but needs further development in order to integrate the ability to amplify and distribute LO signals. Lastly, the project has resulted in a prototype instrument that will be further developed by the research groups at QTL.

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A Complete List of Components

Table A.1: List of components.

Items	Model	Vendor
Mixer	HMC8193	Analog Devices
Power Splitter	MPD-0226SM	Marki Microwave
Directional Coupler	MC16-0222SM	Marki Microwave
Bias-tee	TCBT-14R+	Mini-Circuits
SMA connector	32K145-400L5	Rosenberger
Attenuators	GAT-3+	Mini-Circuits
	GAT-1+	Mini-Circuits

B Design of LO distribution card

A LO distribution card was also designed but was not manufactured due to problems that occurred when testing the amplifier HMC8412 from Analog Devices on an evaluation board. The function of the PCB is to split a single input LO signal into eight signals which would then drive the control and readout cards. A two-way power splitter and a four-way power splitter divide the signals.

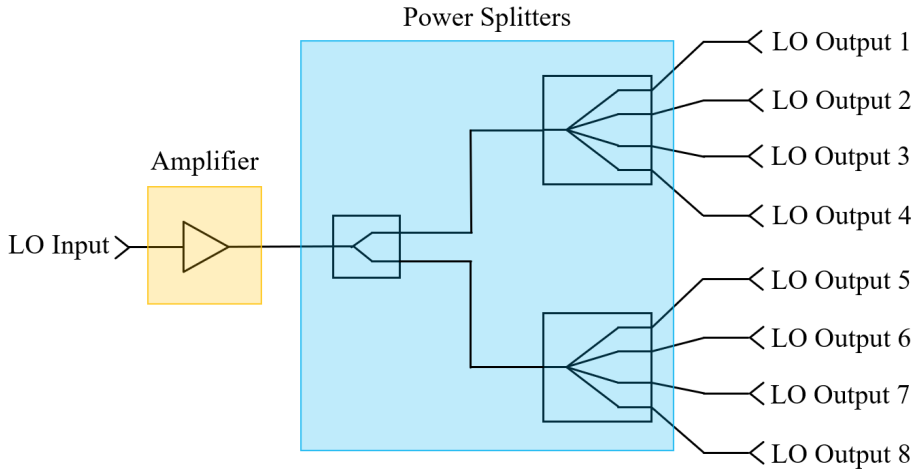

Figure B.1: Block diagram of the LO distribution card.

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