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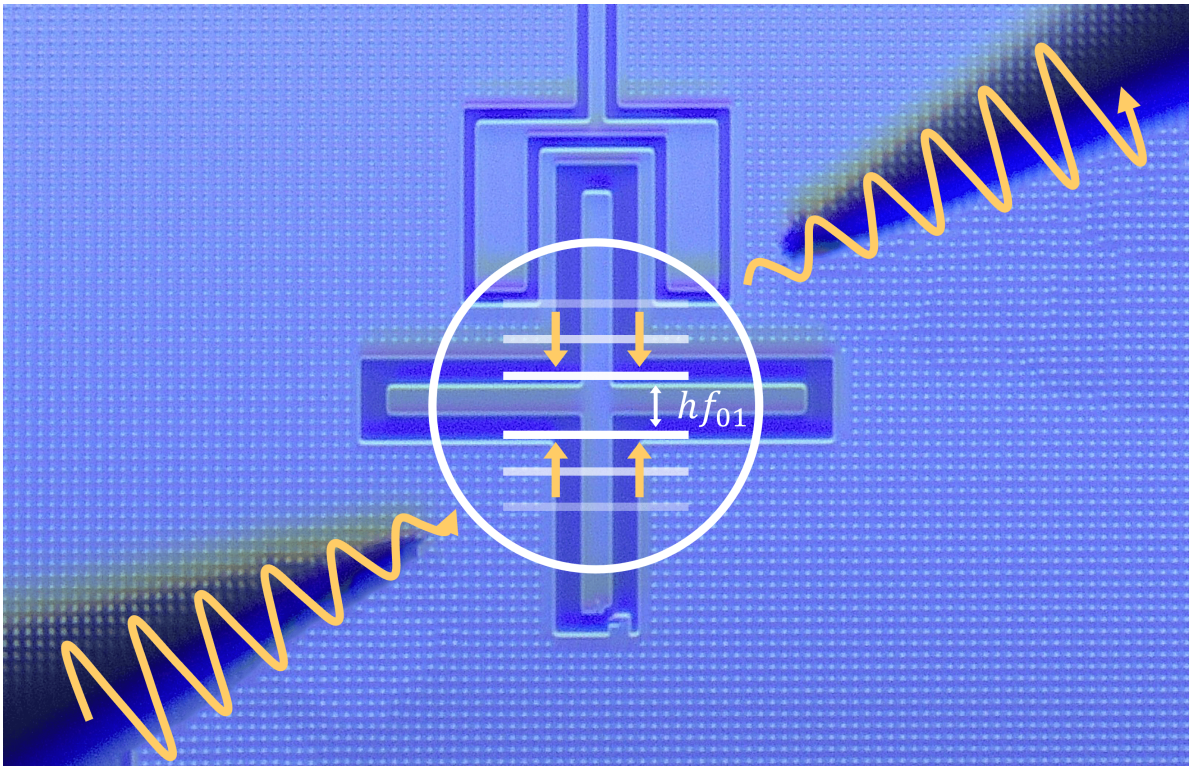

Post-fabrication Frequency Tuning in Superconducting Transmon Qubits

- To Mitigate the Effects of Fabrication Uncertainty

Master's thesis for the Erasmus Mundus Master of Science in Nanoscience and Nanotechnology

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CHALMERS UNIVERSITY OF TECHNOLOGY
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Cover: Illustration of the frequency tuning of a superconducting transmon qubit.

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Abstract

This thesis presents a study on the manipulation of the normal state resistance R_N of Al/AlOx/Al Josephson junctions using electrical DC signals. The goal is to develop a post-fabrication method for tuning the frequency of transmon qubits in superconducting quantum processors. This method aims to correct initial fabrication uncertainties and mitigate frequency collisions to scale up the number of qubits. The project initially focused on a precise, non-intrusive technique to measure R_N at room temperature, which is directly related to the qubit plasma frequency f_{01} through the Ambegaokar-Baratoff relation. Subsequently, the natural aging of two types of devices, thin-oxide and thick-oxide junctions, was studied. Thin-oxide junctions proved less stable, exhibiting a resistance increase of more than 30% within the first two weeks after fabrication, compared to the 3% to 4% observed in thick-oxide junctions. A procedure was then developed to deliberately increase R_N at room temperature using high DC voltage biases, achieving increases of nearly 20% for thin-oxide devices and about 10% for thick-oxide ones. This demonstrates the potential for correcting fabrication variations on a wafer-level scale. An essential finding was the delayed resistance increase after manipulation, suggesting the need for further studies to better understand and control this effect. Theoretical modeling and simulations also revealed that the applied voltage plays a crucial role beyond simply delivering localized heat to the junction. Finally, a technology demonstration performed with a new experimental setup specifically designed to address individual qubits validated this method on a working quantum processor, providing a proof of concept. The results showed frequency shifts of several hundred megahertz after manipulation, without compromising qubit lifetimes. Despite a systematic overestimation of the final frequencies, likely due to the delayed resistance increase, this thesis successfully demonstrates a promising frequency tuning method and suggests future optimization and implementation directions.

Keywords: frequency tuning method, transmon qubit, Josephson junction, superconducting quantum computing, electrical measurements, junction aging.

Acknowledgements

Before delving into the technical aspects of my master's thesis, I would like to take this opportunity to acknowledge and thank all the people who have shared a part of this incredible journey with me.

I would like to start from the beginning, when five years ago I decided to enroll in the Bachelor's program in Engineering Physics at the Polytechnic University of Turin. It was there that my passion for physics was born and truly developed, thanks in no small part to the incredible fellow students I met along the way. To the "biutiful grup", my deepest gratitude. I will always cherish the countless hours spent together.

The second stage of this journey took me to the stunning city of Leuven through the Erasmus Mundus Master in Nanoscience and Nanotechnology. I couldn't be more grateful for the decision that led me there. I want to express my deepest thanks to my amazing housemates at STUDAX and all my EMM colleagues. Thank you all for an incredible year that enriched me both as a student and as a person.

The final stop on this journey brought me to Gothenburg, specifically to the Quantum Technology Laboratory at Chalmers University of Technology, where I carried out this master's thesis project. In this stimulating and welcoming environment, I had the privilege of working with so many wonderful people. Without your support, this work wouldn't have been possible. Thank you Chris, Janka, François, Marcus, Christian, Anuj and Amr for your invaluable time and assistance. A special thanks also goes to the professors who guided and supported me throughout this project: Per, Clement and Jonas. To Filip, Halldór, Emil, Stefan and Hervé, thank you for the valuable time we spent together - both the productive and the not-so-productive moments! Most importantly, I am deeply grateful to my supervisors, Andreas and Giovanna. It's difficult to express how much I appreciated your time, guidance, patience and expertise. I truly couldn't have done this without you.

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Maurizio Toselli, Peveragno, August 2024

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1
Introduction

The idea of using the principles of quantum mechanics like superposition and entanglement to address specific computational problems which cannot be efficiently solved by classical computers traces back to the early 1980s. Pioneering scientists like Paul Benioff, Yuri Manin, and Richard Feynman [1] were among the first to propose this concept. Over the following decades, this idea gained popularity, leading to the establishment of the field nowadays known as quantum computing.

The theoretical foundations of this discipline were relatively quickly laid, accompanied by the development of various algorithms and possible applications to demonstrate the potential of these quantum machines. However, experimental validations were slower in coming. Even now, more than 40 years since the inception of quantum computing, building a quantum computer that can outperform classical ones in solving practical and useful problems remains an ongoing and ambitious challenge.

During the initial years, many platforms were proposed to physically implement a quantum computer. Among the different options, superconducting circuits have emerged as one of the leading candidates for a scalable quantum processor architecture. The first example in this direction dates back to 1999, when Y. Nakamura et al. [2] first developed a qubit based on a superconducting circuit called single-Cooper-pair box. Since then the field has rapidly grown, culminating in 2019 with the achievement of the milestone known as quantum supremacy [3] by a group of researchers from Google on their 53-qubit processor called Sycamore [4]. It is indeed not a coincidence that many of the big technology companies that are nowadays leading the quantum computing effort, such as Amazon, Microsoft, Google, and IBM, have decided to bet on the superconducting circuits platform.

1.1 Motivation

One of the many scientific and engineering challenges in building a quantum computer is implementing scalable and well characterized qubits, as specified in the first of DiVincenzo's criteria [5]. Among the various superconducting qubit realizations, fixed-frequency transmons are particularly attractive for their long coherence times (T_1 and T_2) approaching 500 µs [6, 7] and their high single-qubit and two-qubit gate fidelities (above 99.99% [8] and 99.5% [9] respectively). Currently, the dimension of state-of-the-art superconducting based systems already exceeds 1000 qubits [10], but in order to achieve fault-tolerant quantum computing much more is needed [11].

A big challenge for scaling fixed-frequency transmon architectures is mitigating the errors coming from the frequency collisions between the first and higher order transitions of neighbouring qubits. It is easy to imagine that the need of scaling up the number of qubits in a quantum processor, combined with the limited bandwidth (typically 3 to 6 GHz [12]) available for qubit plasma frequencies, can lead to unwanted interactions between similar energy transitions of neighbouring qubits. This phenomenon is usually referred to as frequency crowding [13]. To avoid these collisions, it is therefore crucial that the qubit frequencies of a newly fabricated quantum processor are aligned with the designed ones.

In a realistic situation however, precisely addressing the designed frequencies for all the qubits in a device is not a simple task. As it will be explained in detail in Chapter 2, the plasma frequency of a transmon qubit is related to the normal state resistance R_N of the Josephson junction by the Ambegaokar-Baratoff relation (see Equation (2.8)). Given the nanometer scale dimensions of the junctions employed, the current level of fabrication technology results in a variation in tunneling resistance on a wafer-scale ranging from 5% to 10% [14, 15]. This contribution usually dominates the variation in the plasma frequency of transmon qubits, leading to a frequency variation for the as-fabricated transmon qubits on the order of 2.5% to 5%. This is currently not enough to reliably produce processors with a number of qubits that can scale above hundreds of units [16].

For this reason, in the last couple of years, many post-fabrication methods and techniques for individually tuning the normal state resistance of Josephson junctions have been developed [17–21]. Most of these methods are based on the observation that the resistance of a tunnel junction can be increased and eventually stabilized against what is commonly known as aging by a thermal treatment as shown in previous works [22–24]. The common idea of these methods is to compensate for fabrication uncertainties by individually addressing single qubits inside a quantum processor and tuning the resistance of their Josephson junction to the target value. By using different physical means to locally manipulate or deliver heat to specific qubits, these methods promise to correct for fabrication uncertainties and increase the production yield of quantum processors, enabling further scaling of the number of qubits.

In this scenario of practical necessity for a post-fabrication method to individually tune the frequencies of transmon qubits in a quantum processor, a discovery made by some researchers at the Quantum Technology Laboratory (QTL) division at Chalmers immediately appeared promising. They observed some correlation between the routine resistance measurements of Josephson junctions and their aging process, suggesting that the resistance value of the junctions might have been affected by the electrical signals applied during the measurement procedure. This observation is the starting point that led to this master's thesis project.

1.2 Aim

The aim of this master's thesis project is to develop a post-fabrication method to individually tune the resistance of the Josephson junctions inside a quantum processor, with the purpose of adjusting the frequency of the transmon qubits and correct for fabrication uncertainties. To enable the manipulation of the normal state resistance of the junctions, the investigated physical mean is the application of electrical signals in the form of voltage or current DC biases.

For the purpose of this project, the intended method can be delineated into a series of steps or tasks that need to be accomplished and demonstrated independently. This approach allows for the evaluation of the method's applicability and utility. The different steps can be understood as follows:

- **Resistance measurement.** The first step of the method consists of assessing the initial qubits' frequencies. This involves measuring the normal state resistance of each Josephson junction (JJ) and estimating the plasma frequency of each qubit using Equation (2.8), which is derived from the Ambegaokar-Baratoff relation. It is crucial for this step that the measurement remains non-intrusive and does not alter the resistance value of the junction. Otherwise, the method's reliability would be compromised. A demonstration of this step necessitates showcasing a measurement procedure that is sufficiently precise in terms of standard deviation of the outcome and that does not induce significant alterations in the measured resistance value.

- **Resistance manipulation.** The second step involves precisely and independently manipulating the resistance of each individual qubit's Josephson junction. These resistances must be adjusted and aligned with the designed values to mitigate the undesired effects of fabrication uncertainty. Key aspects to consider in this process are manipulation range, precision and yield. The range refers to the maximum resistance manipulation achievable, which indicates the extent to which initial resistance variations can be corrected. Precision indicates how closely the manipulated resistance matches the target value. Finally, yield describes the consistency and repeatability of the manipulation process. To demonstrate the feasibility of this approach, it is crucial to show that the resistance can be accurately controlled over a wide range and across a substantial number of samples.

- **Proof of concept.** The last step consists in providing a proof of concept to showcase the potential of this frequency tuning method. The main goal is to demonstrate that the plasma frequencies of the qubits within a quantum processor unit (QPU) can indeed be individually modified. Furthermore, to validate the method's effectiveness and practicality, it is crucial to ensure that its implementation does not compromise other properties of the qubits. The primary metric for assessing the "quality" of a qubit is the relaxation time T_1 [25]. If manipulating the resistance significantly reduces this relaxation time, the benefit of the frequency adjustment provided by the method would be overcome by this

drawback, rendering the method inconvenient. Demonstrating the capability to individually manipulate the resistance of the qubits without significantly affecting their lifetime would be the ideal validation of the method's applicability and potential.

The aim of the project can thus be summarized in the achievement and demonstration of these three steps.

2

Theoretical background

2.1 Transmon qubit

One of the simplest, yet most used, superconducting qubit realization is the fixed-frequency transmon qubit. A fixed-frequency transmon qubit is made by a shunt capacitor C_S in parallel with a nonlinear superconducting element called Josephson junction (JJ), which will be analyzed in detail in Section 2.2. The contribution of the JJ to the circuit can be expressed in terms of an additional self-capacitance term C_J and a nonlinear inductance

$$L_J = \frac{\Phi_0}{2\pi I_c \cos\left(2\pi \frac{\Phi(t)}{\Phi_0}\right)}, \tag{2.1}$$

where I_c is the critical current of the junction, $2\pi\Phi(t)/\Phi_0 \equiv \varphi(t)$ is the difference in phase between the two superconducting islands and $\Phi_0 = h/(2e)$ is the magnetic flux quantum. The electrical circuit diagram of a fixed-frequency transmon is shown in Figure 2.1a.

Following the derivation from reference [26], the quantum Hamiltonian of this circuit is given by

$$\hat{H} = \frac{\hat{Q}^2}{2C_\Sigma} + E_J[1 - \cos\left(\frac{2\pi}{\Phi_0}\hat{\Phi}\right)], \tag{2.2}$$

where $C_\Sigma = C_S + C_J$ is the total capacitance and $E_J = I_c(\Phi_0/2\pi)$ is the Josephson energy. The operators $\hat{\Phi}$ and $\hat{Q}$ are obtained by promoting the classical conjugate variables Φ and Q to operators which satisfy the commutation relation $[\hat{\Phi}, \hat{Q}] = i\hbar\hat{\mathbb{I}}$. This Hamiltonian is then usually simplified by discarding the constant energy term $+E_J$ and introducing the rescaled flux $\hat{\phi} = (2\pi/\Phi_0)\hat{\Phi}$ and charge $\hat{q} = \hat{Q}/2e$ operators. This results in

$$\hat{H} = 4E_C\hat{q}^2 - E_J\cos\hat{\phi}, \tag{2.3}$$

where $E_C = e^2/2C_\Sigma$ is the charging energy required to add an additional electron to the superconducting island. The obtained Hamiltonian is similar to the LC harmonic oscillator's one (Equation (2.20) in [26]), but in this case the cosinusoidal potential introduces a nonlinearity into the system. By diagonalizing this Hamiltonian, an anharmonic energy spectrum is obtained, which means that the transition energies between the levels are different ($\hbar\omega_{01} \neq \hbar\omega_{12} \neq \hbar\omega_{23} \neq ...$) as shown in Figure 2.1b. This allows to define a computational two-dimensional subspace $\{|0\rangle, |1\rangle\}$

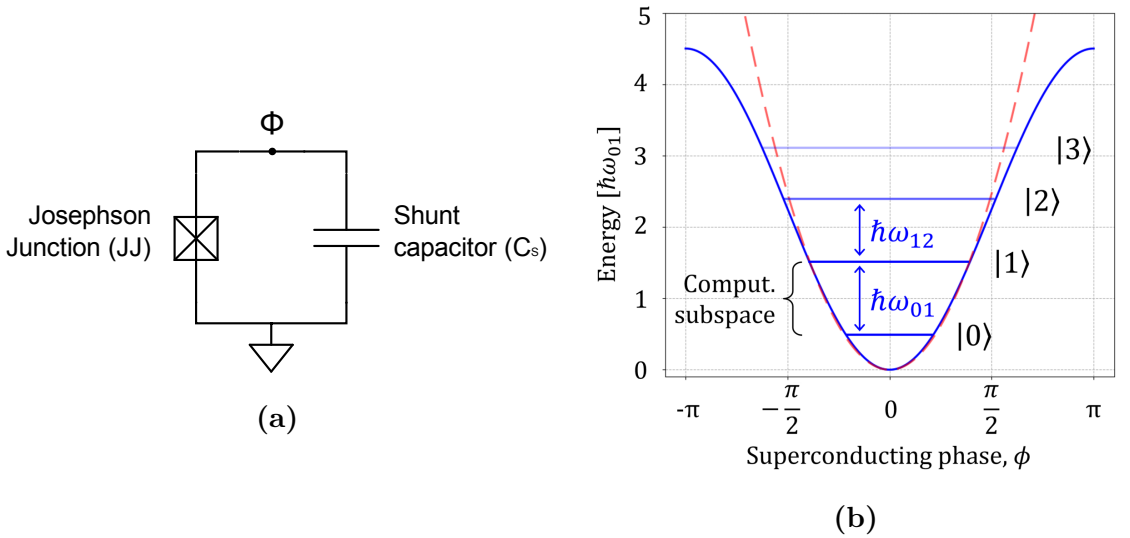


Figure 2.1: **(a)** Circuit diagram of a fixed-frequency transmon qubit. The two superconducting islands of the transmon are represented by the two nodes of the circuit. Φ is the upper node flux, while the lower one is took as reference (ground). The nodes are connected by a shunt capacitor C_S in parallel with a Josephson junction. **(b)** Anharmonic energy spectrum of a transmon qubit. The cosinusoidal potential energy of the transmon circuit (blue line) is compared with the quadratic one of the LC harmonic oscillator (dashed red line). The former results in an anharmonic energy spectrum.

made by the two-lowest energy eigenstates of the system and therefore approximate the multi-level transmon to a quantum two-level system.

In literature, this system is usually referred to as Cooper-pair box [2] and can be highly sensitive to charge noise in the case when $E_J \leq E_C$. For this reason, the superconducting qubit community moved towards what is commonly known as transmon regime, where $E_J \gg E_C$. This can be accessed by shunting the junction with a large capacitor ($C_S \gg C_J$), resulting in a small E_C and a qubit which is less sensitive to charge noise [25]. In this regime, the qubit plasma frequency can be approximated by performing a Taylor expansion and using the harmonic oscillator basis with

$$f_{01} \simeq \frac{\sqrt{8E_C E_J} - E_C}{h}. \tag{2.4}$$

For a more accurate formula to calculate the qubit plasma frequency, refer to Section 2.3 in reference [27].

2.2 Josephson junction

The Josephson junction is a fundamental element in superconducting electrical circuits and takes its name from the british physicist Brian Josephson, who predicted in 1962 the mathematical relationships between the voltage and current across this device [28]. In general, a JJ consists of two closely spaced superconductors coupled by a weak link. This link can be implemented by dividing the two superconductors by a thin insulating layer. The resulting structure is referred to as a superconductor-insulator-superconductor (S-I-S) junction. In the superconducting quantum circuits field, JJs are usually made by two superconducting aluminium layers divided by an oxide layer. This oxide layer is grown by a controlled oxidation process, resulting in an $Al/AlO_x/Al$ structure.

In such a structure, if the wave functions of the Cooper pairs in the two superconductors Ψ_1 and Ψ_2 overlap, there is a finite probability for Cooper pair tunneling, which results in an effective supercurrent through the device. A schematic of a S-I-S Josephson junction is shown in Figure 2.2a.

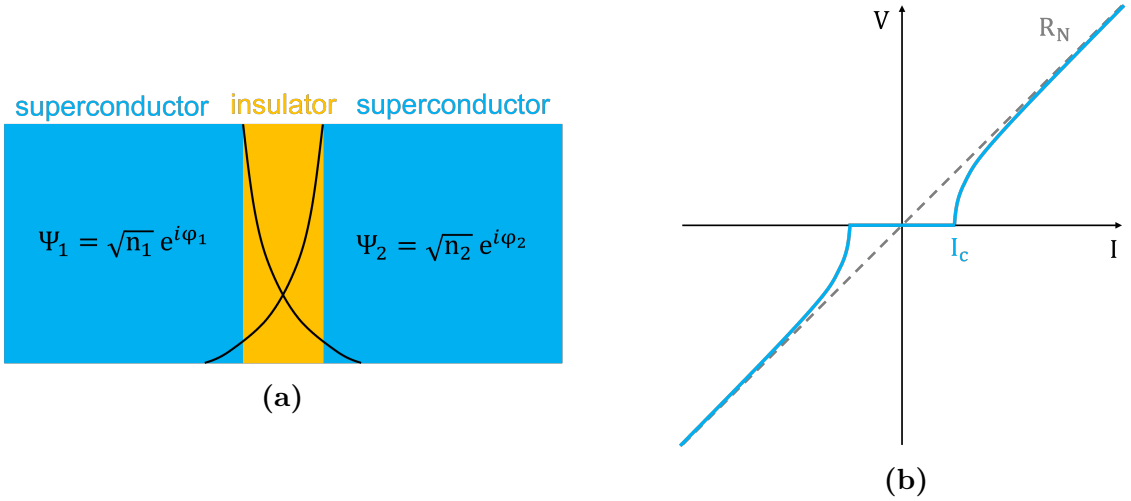


Figure 2.2: **(a)** S-I-S Josephson junction structure. The overlap of the superconducting wave functions ψ_1 and ψ_2 (black lines) of the two superconductors allows the tunneling of Cooper pairs. **(b)** IV characteristic of a superconducting Josephson junction. For $I < I_c$ the voltage drop across the junction is $V = 0$, meaning that only the supercurrent is flowing through the device. For larger current biases dissipation occurs and the device behaves similarly to a resistor of normal state resistance R_N (dashed gray line).

At sufficiently low temperature, the behaviour of this device is described by the so called DC (2.5) and AC (2.6) Josephson effects [29]

$$I = I_c \sin(\varphi), \tag{2.5}$$

$$\frac{d\varphi}{dt} = \frac{2eV}{\hbar}, \tag{2.6}$$

where $\varphi = \varphi_2 - \varphi_1$ is the difference in phase between the two superconducting islands as in Equation (2.1), V is the voltage drop across the junction and I_c the critical current. The latter is a crucial parameter that represent the maximum supercurrent that the junction can support before switching to the dissipative state where a quasiparticle current starts flowing. Under this condition, the device will behave similarly to a resistor of normal state resistance R_N. The complete nonlinear IV characteristic of a superconducting Josephson junction is shown in Figure 2.2b.

The normal state resistance R_N of a Josephson junction is the tunneling resistance of the insulator potential barrier felt by the quasiparticles in the superconducting islands. It is related to the critical current at zero magnetic field of the device by the Ambegaokar-Baratoff relation [30]

$$I_c = \frac{\pi\Delta(T)}{2eR_N} \tanh\left(\frac{\Delta(T)}{2K_BT}\right), \tag{2.7}$$

where $\Delta(T)$ is the superconducting gap from the BCS theory [31]. The normal state resistance of a junction strongly depends on the insulating layer and other material properties and can be extracted by the IV characteristic of the Josephson junction for large biases as shown in Figure 2.2b.

In Section 2.1, an approximation of the plasma frequency of a transmon qubit was given by Equation (2.4). Using Equation (2.7), it is possible to relate the qubit plasma frequency f_{01} directly to the normal state resistance R_N of its Josephson junction, obtaining

$$f_{01} \sim \frac{\sqrt{2E_C\frac{\pi\hbar\Delta(T)}{e^2R_N}} - E_C}{h}, \tag{2.8}$$

where $\tanh\left(\Delta(T)/2K_BT\right) \sim 1$ since $\Delta(T) \sim 176\ \mu$eV for aluminium thin layers and these devices typically operate at temperatures in the order of 10 mK.

2.3 Tunnel junction

When the S-I-S Josephson junctions are not in their superconducting state, for example at room temperature, they behave like metal-insulator-metal (M-I-M) tunnel junctions. In general, a tunnel junction consists of a potential energy barrier between two electrically conducting materials. According to quantum mechanics, if the potential barrier is thin enough, there is a finite probability for the electrons (or quasiparticles) to pass through the barrier even if their energy is lower than the potential energy of the barrier. This phenomenon, which is not allowed in classical mechanics, is known as quantum tunneling.

By solving the Schrödinger equation for an electron in a 1D potential barrier using the Wentzel-Kramers-Brillouin (WKB) approximation [32], it is possible to calculate the transmission coefficient across the barrier as

$$T(E) = e^{-2\int_0^d dx\sqrt{\frac{2m}{\hbar^2}[V(x)-E]}}, \tag{2.9}$$

where d is the thickness of the barrier and $V(x)$ is the potential energy profile. For the simple case of a rectangular barrier ($V(x) = V_0$ for $0 \leq x \leq d$), this expression simplifies to

$$T(E) = e^{-2d\sqrt{\frac{2m}{\hbar^2}[V_0-E]}}. \tag{2.10}$$

Since the current density produced by an electron with energy E flowing through a tunnel junction is proportional to the transmission coefficient $T(E)$, Equation (2.10) implies that the current across the tunnel junction exponentially decreases with the thickness d of the insulating barrier. For this reason, the thickness of the insulating layer must be very thin, typically in the order of few nanometers.

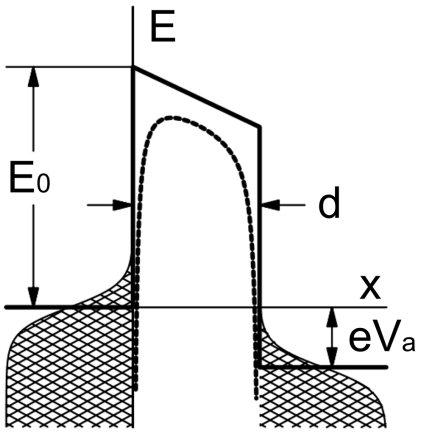


Figure 2.3: Rectangular tunnel barrier of width d and height E_0 after applying a bias voltage V_a. The real potential barrier profile (dashed line) is changed due to image forces. The shaded areas represent populated electron states at finite temperature. Figure adapted from [33].

When a voltage difference V_a is applied to the two electrodes of the junction, an ideal rectangular barrier changes into a trapezoidal shape. For a real junction however, the effective potential energy distribution $V(x)$ gets also distorted by the image forces acting on the tunneling electron. This can be described by the standard Simmons model [34] and is shown as a dashed line in Figure 2.3.

The dependence of this potential barrier profile on the voltage drop across the junction, together with the different tunneling regimes involved, imply that the complete IV characteristic of the device is not linear. The resistance in fact decreases when the voltage bias increases as shown in Figure 2.4. Because of this nonlinearity, a resistance value is usually extracted by linearizing the IV characteristic in a small interval around zero to compare different devices.

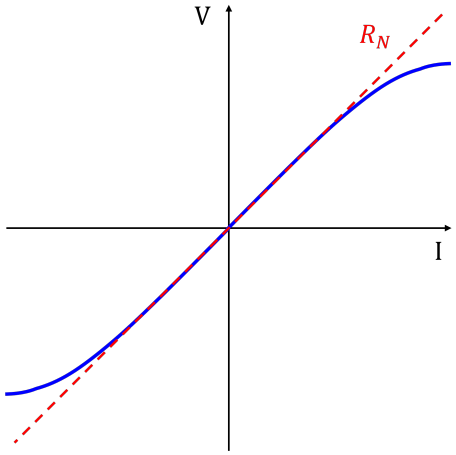


Figure 2.4: Nonlinear IV characteristic of M-I-M tunnel junction (blue curve). In the case of a room temperature $Al/AlO_x/Al$ Josephson junction, an approximate value of the normal state resistance R_N is obtained by linearizing the curve in a small interval around zero (dashed red line).

In the case of $Al/AlO_x/Al$ Josephson junctions at room temperature, an experimental measurement of the total resistance of the junction can be used to estimate the normal state resistance R_N of the device. This for example can be used to infer the plasma frequency f_{01} of the transmon qubit through Equation (2.8).

2.4 Insulating oxide layer

The devices described in Sections 2.2 and 2.3, are based on the quantum mechanical tunneling of charge carriers (Cooper pairs and electrons respectively) across a thin insulating layer. The geometrical and material properties of this layer therefore play a crucial role in defining the properties of these devices. As already mentioned in this chapter, in superconducting electrical circuits the insulating layer of the S-I-S Josephson junctions typically consist of a thin metal oxide layer which in most of the cases is aluminium oxide (AlO_x) [35]. This amorphous oxide is very convenient for the fabrication of a few nanometers thick insulating layers, as it can be easily grown on the surface of the aluminium by controlling the oxidation parameters such as temperature, partial oxygen pressure and oxidation time [36, 37].

2.4.1 Cabrera-Mott metal oxidation theory

In 1949, N. Mott and N. Cabrera proposed a model to describe the low-temperature oxidation of metal, which represents still today a landmark in this field [38]. According to this model, during the oxidation process, the oxygen molecules O_2 that adsorb at the oxide/gas interface get ionized by the electrons coming from the metal. These electrons can easily pass through the forming oxide layer and occupy the empty energy levels of the adsorbed oxygens, which lie at lower energies than the Fermi level of the metal. This leads to the establishment of a strong electric field between the oxygen anions at the surface and the metal cations deeper in the metal.

The core idea of the theory is that this electric field can flatten the potential profile felt by the ions inside the oxide layer and drive the migration of the metal cations (e.g. Al^{3+}) towards the surface and the oxygen anions (O^{2-}) in the opposite direction. Therefore, according to the model, this electric field is the main responsible for the oxide formation. The oxide layer growth and the change of the potential profile due to the electric field in the oxide region are illustrated in Figure 2.5.

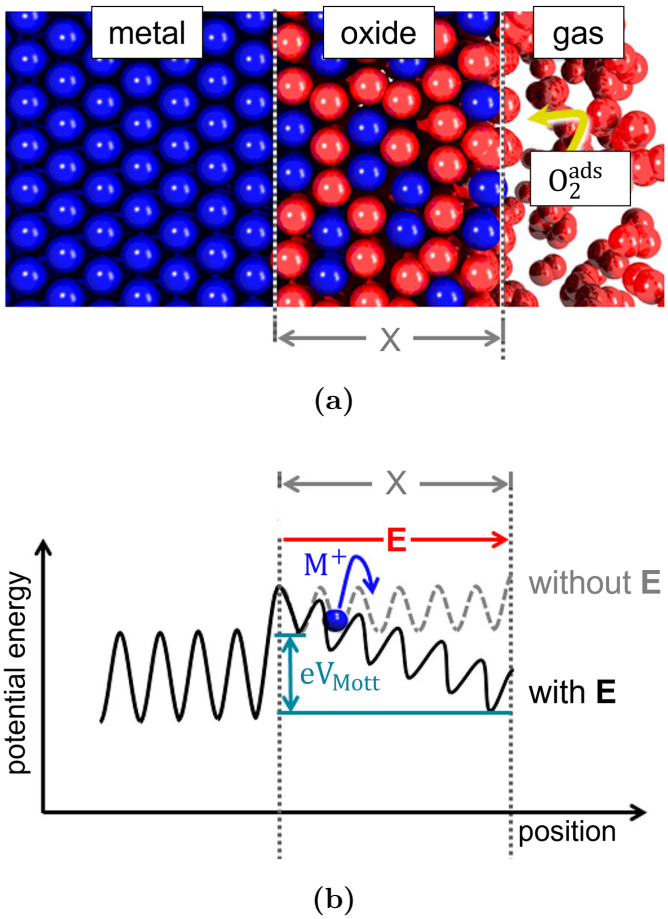


Figure 2.5: **(a)** Metal/oxide/gaseous O_2 system during the oxide formation. **(b)** Potential energy of a migrating metal cation in the presence of an electric field **E** according to the Cabrera-Mott oxidation theory. Figures adapted from [39].

The strong electric field that is formed inside the oxide layer and drives the oxide growth can be thought as the electric field inside a parallel plate capacitor with dielectric layer thickness d and voltage bias V_{Mott}

$$|\mathbf{E}| = \frac{qV_{Mott}}{d}, \tag{2.11}$$

where the so called Mott voltage V_{Mott} is the voltage difference that develops between the metal cations and oxygen anions during the oxide growth. For aluminium oxide barriers, typical values of Mott voltages are $V_{\text{Mott}} \sim 0.5 - 1$ V [40].

2.4.2 Aging and "annealing" methods in literature

As with any other type of device, reliability is a crucial aspect of $Al/AlO_x/Al$ Josephson junctions and the subject of many studies and concerns. In literature, a process known as aging is widely reported to affect these devices. The term aging usually refers to an instability in the properties of the junctions under room temperature and air conditions. This instability manifests as a slow, creeping increase in the junction tunneling resistance over time [22]. Various factors are often indicated as possible causes of aging, including (i) relaxation of the oxide structure towards a more stable and lower energy configuration, (ii) absorption of unwanted molecules into the insulating barrier and (iii) resist residuals on the substrate prior to electrode deposition. It has been demonstrated that factors (ii) and (iii) can indeed contribute to junction aging, as storing devices in vacuum conditions and performing plasma cleaning of surfaces before Al deposition have been shown to reduce aging significantly [22]. However, the main contribution to aging in $Al/AlO_x/Al$ junctions is generally attributed to factor (i), which is extensively studied in [41] and described as a glass-like relaxation affecting defects at the top electrode Al/AlO_x interface.

As anticipated in Section 1.1, previous studies [22–24] have shown that the tunneling resistance of similar junctions can be increased through a high-temperature exposure which is usually referred to as "thermal annealing". In general, the idea behind annealing involves increasing a sample's temperature above a specific threshold for a certain period of time, followed by a controlled cooling process. From the perspective of aging, this "annealing" process is believed to accelerate the relaxation process and help the oxide structure to find a more stable, lower energy configuration. This thermal treatment therefore advances the junction along its aging trajectory, resulting in a greater stability against the drift in resistance. Conversely, cooling the junction can retard or stop this relaxation process, highlighting its thermally activated nature [41].

In the case of the $Al/AlO_x/Al$ tunnel junctions described in Section 2.3, the physical effect of this "annealing" is believed to be an increase in the effective thickness and height of the potential barrier [22], which translates in the observed increase in tunneling resistance according to Equation (2.9).

In the past few years, many studies have been proposed where this idea of "annealing" is implemented by targeting specific junctions in a superconducting quantum circuit, using different physical means to locally deliver heat. So far, this has been done by exploiting the power of a laser focused in proximity of a single junction at the time [17] or the electron beam of a standard electron beam lithography system used for the fabrication of the junctions themselves [19].

A slightly different approach was also recently presented [20], demonstrating an increase in the resistance of the junctions over a wide range. This was achieved through the combined effect of wafer-scale temperature exposure and the local application of alternating voltage biases to a single junction at a time. This method was called alternating-bias assisted annealing (ABAA) technique. In this case, the

purpose of applying the voltage bias is to emulate the presence of the electric field during the oxide formation process, as described by the Cabrera-Mott oxidation theory presented in Subsection 2.4.1. According to the authors, the applied voltage bias is expected to flatten the potential profile experienced by the Al^{3+} and O^{2-} ions within the oxide layer, facilitating their migration and reconfiguration into a more stable and lower energy configuration.

Noticeably, also in reference [41] it was demonstrated that applying a voltage drop across the tunnel junction affects the effective barrier height of the insulator, in addition to the natural increase observed due to aging. In particular, the polarity of the voltage alters the asymmetric shape of the barrier described by the Simmons model [34] due to a redistribution of ionic charges.

3
Methods

3.1 Measurement setups

In this section, the two experimental setups used throughout the project to measure and manipulate the $Al/AlO_x/Al$ tunnel junctions at room temperature are presented and explained.

3.1.1 Automatic probe station

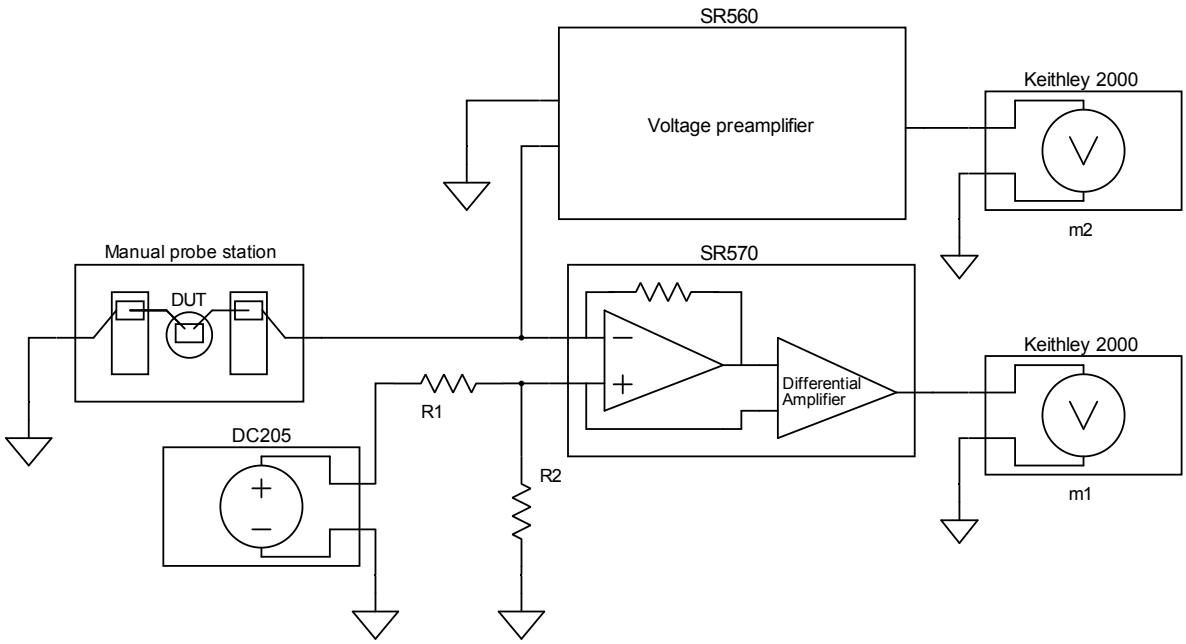
The first setup used is the automatic probe station MPI TS200 [42], equipped with the source measurement unit (SMU) Keithley 2612B [43]. With this setup it is possible to measure the resistance of the device under test (DUT) using a 4-point probes method. This technique allows to accurately measure the resistance of the device by neglecting the resistance contribution of the cables [44].

In particular, this setup is equipped with a probe card consisting of 40 fixed probes. The spatial configuration of these probes allows to measure simultaneously two rows of five junctions each. However, the junctions need to be disposed in a specific fixed pattern, with 2 contact pads per junction of equal dimensions. It is also important to mention the noise limitation of this setup for the typical devices employed in the project. In fact, the noise of the setup becomes noticeable when attempting to measure resistances by driving currents on the order of a few nA, leading to inaccurate measurements.

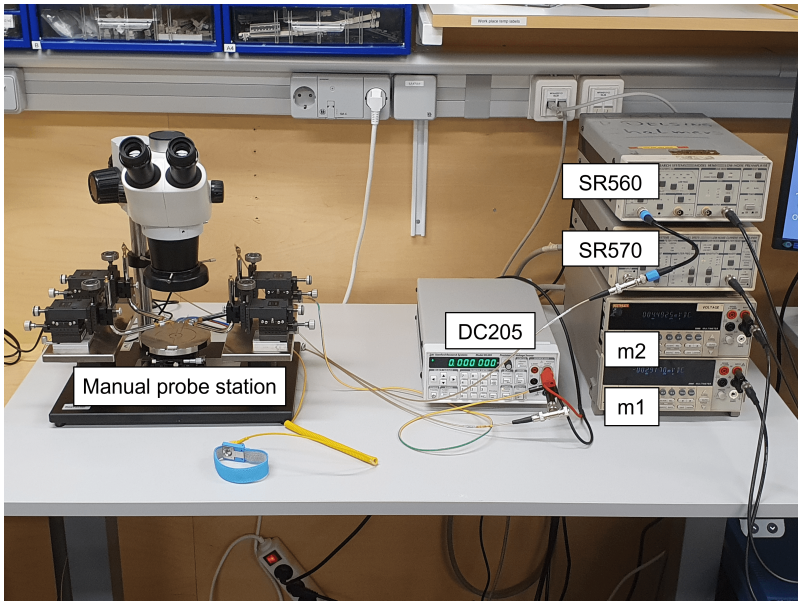
This setup is ideal for large scale measurements of test-junctions arranged in a specific pattern within a chip, but it is absolutely not flexible and incapable to individually address a specific junction inside a quantum processor.

3.1.2 Manual probe station

To individually address one specific junction at a time inside a quantum processor, a manual probe station was specifically designed and implemented. It allows to apply and measure low levels of current and voltage. This is a crucial requirement, as the only difference between the measurement and manipulation processes lies in the levels of applied voltage biases. Detailed explanations of these processes are provided in Sections 3.2 and 3.3 respectively.



(a)



(b)

Figure 3.1: **(a)** Simplified circuit diagram of the manual probe station setup. The interior of the bench instruments used in the setup is only sketched. **(b)** Picture of the manual probe station setup built in the laboratory.

The simplified circuit diagram of the setup is shown in Figure 3.1a and the idea behind its design is the following: To measure the resistance of the DUT, various voltage biases V_s are provided by the voltage source SRS DC205 [45]. The voltage from the source is then divided by 100 using the voltage divider formed by R_1 and

R_2. This divider reduces the voltage difference applied to the DUT, allowing for measurements with small voltage biases. Consequently, a voltage of approximately $V_s/100$ is applied to the DUT, given that the two terminals of the current preamplifier SR570 [46] are virtually at the same potential. The current preamplifier amplifies the low currents (even in the order of nA or pA) flowing through the DUT into a higher voltage level that can be easily read by the Keithley 2000 multimeter (m1) [47], which operates as a voltmeter. With the known current and the approximate voltage drop across the device, the resistance value of the DUT could, in principle, already be estimated.

However, to account for the non-idealities of the current preamplifier, such as current input offsets and a non-zero voltage drop between the two input terminals, as well as the series input resistance of the instrument, an additional component is added to the circuit. A voltage preamplifier SR560 [48] is used to amplify the exact voltage drop across the DUT and a second Keithley 2000 multimeter (m2) is used to read the output of this amplifier. At this point, the normal state resistance of the junction is more precisely calculated as explained in Section 3.2.

It is immediately noticeable from the schematic that this setup uses "only" two terminals to measure the resistance of the DUT, indicating that the resistance contribution of the cables cannot be neglected. Apart from this detail, which is not particularly relevant for the typical resistance values of the analyzed devices, this second setup offers numerous advantages for the purpose of this project. Firstly, the probe station consists of two independent, manually controllable probes. These probes allow for probing a single device on a chip with arbitrary geometry, as long as there is sufficient space for the needles (each tip is approximately 2 µm in size) to access the DUT. Secondly, the two current and voltage preamplifiers enable reliable measurements of the device with extremely low levels of current and voltage. These can be read using standard bench multimeters such as the Keithley 2000. This feature is crucial as it was observed that the measurement process itself can actively change the resistance value of the device.

3.2 Resistance measurement

In the following sections of this report, many plots illustrate the variation in the resistance of a specific junction under various conditions, each of which is presented in detail. The resistance is consistently depicted on the y-axis, with individual measurement values typically represented as dots. This section explains the process of extracting these measured values from electrical measurements of the devices in both the setups presented in Section 3.1.

The resistance of a linear electronic device can be calculated according to Ohm's law as

$$R = \frac{V}{I}. \tag{3.1}$$

Experimentally, this is achieved by applying a fixed current (or voltage) to the device and measuring the resulting voltage (or current) through it. However, obtaining a precise measurement of the resistance typically requires collecting data across multiple points. Therefore, the voltage (or current) is recorded for many different values of current (or voltage) applied and these data points are used to plot the IV characteristic of the device. The measured resistance value is then determined by fitting a straight line to these points, with the slope representing the resistance. Often in this report, additional information about the measurement procedure is provided by specifying a current value. This value represents the maximum amount of current applied to the device during the measurement. Typically, the current difference between data points is one-tenth of this maximum value.

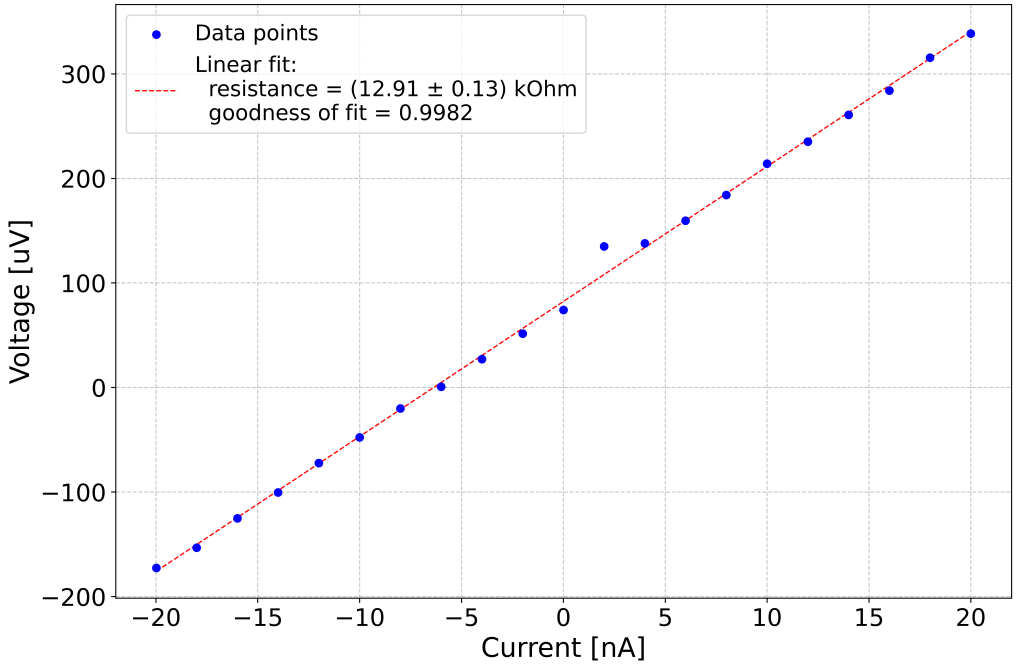


Figure 3.2: Typical resistance measurement. The IV characteristic of a device is measured at 21 current points (blue dots), with a maximum current of 20 nA in this case. These data points are fitted to a straight line (dashed red line), whose slope represents the resistance of the device. The uncertainty value provided is the mean-square error of the fit.

An example of IV characteristic of a real Al/AlO_x/Al tunnel junction is shown in Figure 3.2. The plot displays the measured resistance value, which is 12.91 kΩ in this case, along with the goodness of fit R^2 for the specific measurement. R^2 is a well-known parameter in statistics that describes how well a statistical model fits a set of data. In this project, only measurements with $R^2 > 0.99$ were considered valid and used. Measurements with lower R^2 values were discarded as indicator of potentially faulty devices.

It is crucial to remember that, as discussed in the theoretical Section 2.3, a tunnel junction is not strictly a linear device. Due to the dielectric nature of the AlO_x

layer, there are specific voltage values $\pm V_{\mathrm{BREAK}}$ at which the electric field exceeds the dielectric strength of the material, leading to breakdown [49]. When breakdown occurs, the resistance of the tunnel junction immediately drops, causing the device to behave similarly to a short circuit. In such cases, the device is considered "broken" and unusable for the purpose of the project.

However, even between the bias voltage values of $\pm V_{\mathrm{BREAK}}$, the IV characteristic does not exhibit complete linearity throughout the entire interval. A real example illustrating the IV characteristic of a typical Josephson junction at room temperature is shown in Figure 3.3. From this example, it is evident that the conductance of the junction increases with the bias voltage at the two extremes of the plot, in agreement with the standard Simmons model [33, 34]. Therefore, to determine the normal state resistance for these devices, it is necessary to conduct a linear fit of the data points within a small interval centered around the 0 V bias point as done in Figure 3.2.

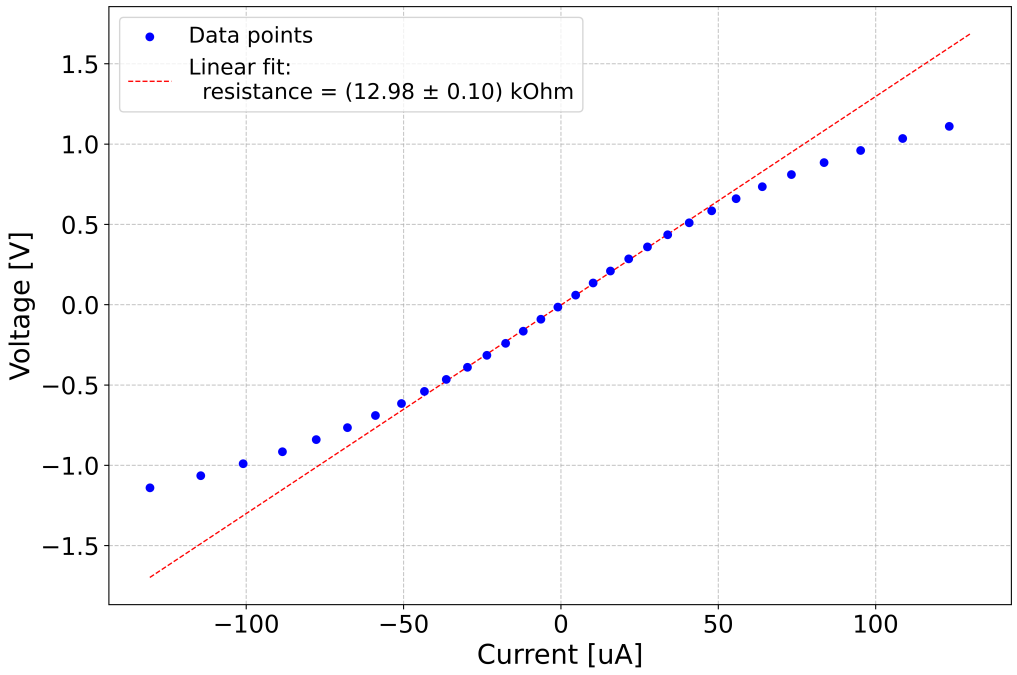


Figure 3.3: Nonlinear IV characteristic of an Al/AlO_x/Al tunnel junction. The blue dots represent the data points. A linear fit performed within the interval [−12.5 mV, 12.5 mV] is shown as a dashed red line, which determines the resistance value and its error. The plot follows the theoretical prediction illustrated in Figure 2.4.

In this project, a critical consideration regarding the measurement procedure is its non-invasiveness. As reported in Section 1.2, there seems to be a potential correlation between the increase in tunneling resistance of the junctions and the electrical signals applied during the measurements. For the sake of convenience, in this report the term "measurement backaction" is borrowed from the vocabulary of quantum mechanics to denote this unwanted effect in measurements. Therefore, it

is imperative to devise a method that allows to accurately measure the junction resistance without inducing significant "backaction". This feature is essential for safely monitoring the resistance manipulation process.

3.3 Resistance manipulation

This section presents the typical procedure used to manipulate the normal state resistance of Josephson junctions at room temperature. Practical limitations, precautions taken and parameters involved in the process are discussed here.

The success of this project relies on the ability to manipulate the resistance of a junction over a broad range, with high control and precision. As anticipated in Section 1.2, the physical mean investigated for achieving this manipulation involves the application of electrical signals. Typically these signals consist of "high" DC voltage biases applied for a duration on the order of a few minutes. It is important to clarify what high indicates in this context.

The $Al/AlO_x/Al$ junctions used in the Quantum Technology Laboratory at Chalmers for superconducting quantum circuits typically exhibit a breakdown voltage V_{BREAK} between 1.05 and 1.25 V (see Section 3.4 for more details). If a voltage exceeding this value is applied to the two electrodes of the junction, the dielectric layer would experience electrical breakdown, causing the device to break and behave similarly to a short circuit. Therefore, to safely manipulate the resistance of a junction without damaging the device, the applied voltage should remain below this limit. On the other hand, if the voltage applied is too low, there will be no significant effect on the resistance. As explained in Subsection 2.4.1 and suggested by reference [20], the applied voltage should be in the order of or greater than the Mott voltage ($V_{\mathrm{Mott}} \approx 0.5 - 1\ V$ for these AlO_x layers) to induce an observable increase in the normal state resistance of the junction.

An important aspect of the manipulation studies conducted in this project concerns the experimental setup used. Most of the room temperature studies on the manipulation procedure were conducted on purposely designed test structures using the automatic probe station described in Section 3.1.1. This choice was made to enable faster measurements compared to the manual probe station described in Section 3.1.2, and to allow for pipelining measurements on junctions at different positions on the chip. This significantly facilitated and accelerated data collection over extended periods. However, this setup has the drawback of limited flexibility in the types of signals that can be applied. This was one of the reasons why all manipulation experiments aimed at gaining insights into the mechanism behind the resistance increase were performed using a simple constant DC bias.

On the other hand, the manual probe station used for the technology demonstration described in Section 3.5 offers greater flexibility in terms of the signals that can be applied. In that case, a variation of the manipulation process was utilized, as specified in Subsection 3.5.2.

To better understand how DC electrical signals can be used in the context of a frequency manipulation method, it is crucial to anticipate a key observation regarding this approach: the normal state resistance of $Al/AlO_x/Al$ tunnel junctions can only be increased. This is essential to consider when designing a chip that will undergo this post-fabrication method. In such a case, the Josephson junctions should be designed with a slightly lower resistance than the target value. This ensures that after fabrication, even accounting for the fabrication uncertainty, there will be sufficient margin to increase the resistance of these junctions to match the target value.

Considering this, a wide resistance manipulation range is essential to accommodate the still significant fabrication uncertainty inherent in these devices, typically ranging from 5% to 10% on a wafer-level scale [14, 15]. As a rule of thumb, this range should be at least $2\sigma_{R_N}$, where σ_{R_N} denotes the fabrication uncertainty of the normal state resistance of the junctions. This ensures the capability to adjust any resistance value falling within one standard deviation from the mean designed value to the same target value [18]. This concept is illustrated in Figure 3.4. The rule of thumb provides a lower bound for the experimental manipulation range based on the typical uncertainty of the fabrication process employed. A larger manipulation range would allow an even bigger design flexibility and the ability to correct more outlier results effectively.

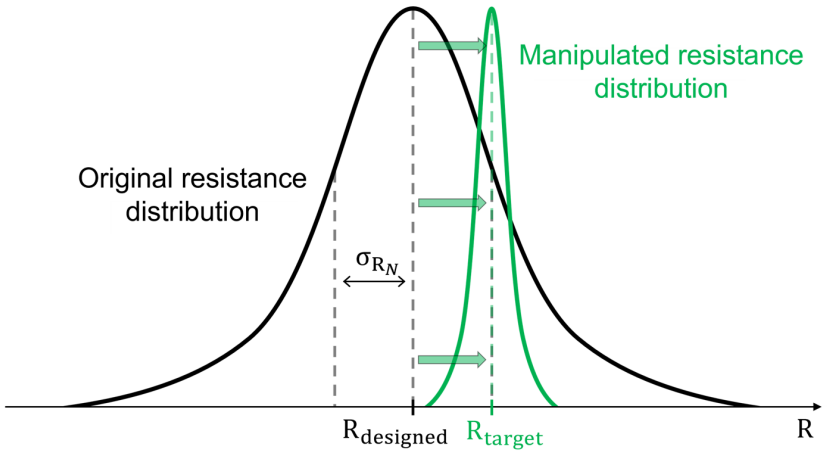


Figure 3.4: Intended usage of the resistance manipulation to mitigate fabrication uncertainties in $Al/AlO_x/Al$ Josephson junctions. After fabrication, the typical resistance distribution for a designed resistance R_{designed} has a standard deviation σ_{R_N} given by the fabrication uncertainty. After manipulation (bold green arrows), the mean value of the distribution can be increased and adjusted to the target value R_{target}. The width of the resulting distribution (green Gaussian) reflects the precision of the manipulation.

The control and precision of the manipulation procedure are also important, as they determine the position and the spread of the newly manipulated resistance distribution depicted by the green curve in Figure 3.4.

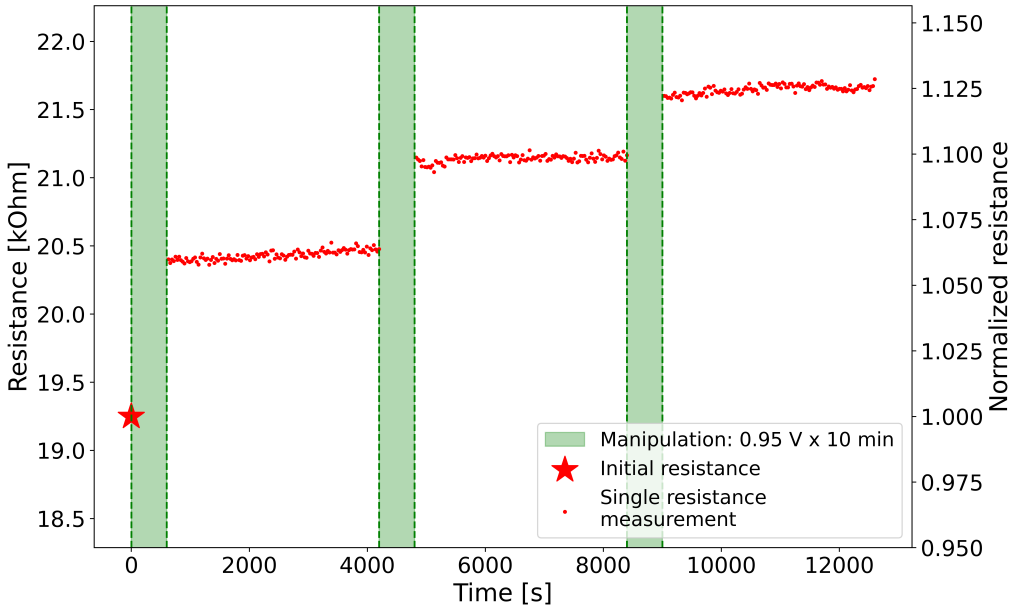


Figure 3.5: Typical resistance manipulation experiment. The resistance of the device is initially measured and depicted with a red star. Subsequently, a series of identical manipulation steps are applied to the junction, illustrated as green areas. The time and the DC voltage applied in these manipulation steps are shown in the legend. In this case, a DC voltage of 0.95 V was applied for 10 minutes for a total of 3 times. After each manipulation step, the resistance is monitored for a certain period of time and depicted with red dots.

In Figure 3.5, the evolution of the tunneling resistance of a single junction subjected to a manipulation procedure in multiple steps is shown. In the plot, the red star marks the pre-manipulation initial resistance, while the dots represent subsequent measurements. Each of these measurements is obtained from a linear fit of the device's IV characteristic as described in Section 3.2. The green regions indicate intervals during which "high" DC voltages are applied for a specified duration, resulting in the observed step-like increases in resistance.

Notably, the resistance change over time within these green regions is not shown. This omission is a natural consequence of the nonlinear IV characteristic of these devices, which requires the resistance to be measured around the 0 V bias, precluding simultaneous measurements and manipulation. For this reason, each manipulation step is followed by a series of "low" current measurements. In Section 4.1, it will be shown that the effect of these measurements on the resistance of the device is negligible, allowing for safe monitoring of the resistance change.

With this type of step-like manipulation, the main adjustable parameters for precisely tuning the resistance to the target value are the number of manipulation steps, their duration, the applied voltage and its polarity. The impact of varying these parameters on the resistance increase is discussed in Section 4.2.

3.4 AlO_x layer thickness

During the course of the project, many different $Al/AlO_x/Al$ junctions have been measured and analyzed. The main parameter of interest for these devices in the context of this project is the normal state resistance R_N. Many factors contribute to the normal state resistance of these junctions, including both material properties and the geometry of the junction itself. The latter can be reduced to two main variables: the thickness of the oxide layer and the junction's size. According to Equation (2.10), the tunneling resistance of these devices exponentially increases with the thickness of the insulating layer. On the other side, the dependence on the junction size follows the trend [16]

$$R_N \propto \frac{1}{d^2}, \tag{3.2}$$

where d is the width of each of the two aluminium electrodes forming the junction, which has a square footprint. Typically, when building a superconducting circuit, to achieve different normal state resistance values for different Josephson junctions inside the circuit, the oxide layer thickness is kept constant and the junction size is varied. This is a consequence of the typical fabrication procedure, where all the junctions in a wafer are individually patterned with electron beam lithography and then oxidized together in a single step [50]. This ensures a uniform oxide thickness across the wafer with minimal variations [36].

In this project, two types of junctions with different oxide thicknesses have been studied. These two types of junctions are the same described in [16] and named for simplicity thin-oxide and thick-oxide junctions. The difference between these junctions lies in the oxidation parameters during the fabrication process: the thin-oxide ones are oxidized in pure oxygen with a pressure of 2 mbar for 10 min, whereas the thick-oxide ones undergo oxidation at a pressure of 10 mbar for 60 min. These distinct oxidation processes are estimated to result in an average variation in the oxide thickness of a couple of Ångstrom.

The different thicknesses of the oxides in the two types of junctions influence many properties of the devices, including the unit-area resistance [16] and the breakdown voltage V_{BREAK}. The latter is particularly important for this project, as it determines the maximum voltage that can be applied to the junction during manipulation. To understand why different oxide barrier thicknesses result in different V_{BREAK}, it is important to remember that the breakdown mechanism of a dielectric is triggered when the electric field in the material exceeds its dielectric strength [49]. According to the definition of the electric field as the negative gradient of the electric potential, a thicker oxide reaches the same electric field in the material when a higher voltage is applied, resulting in a higher breakdown voltage. For the thin-oxide and thick-oxide devices used in this project, the measured average V_{BREAK} values are approximately 1.05 V and 1.25 V respectively.

For the remaining of this report, a consistent color scheme is used across all plots to facilitate the recognition of the junction type. Thin-oxide junctions have their resistance measurements represented by cool colors, such as blue, while thick-oxide junctions are depicted using warm colors like red. This color coding will help to quickly distinguish between the two types of junctions.

3.5 Proof of concept

To demonstrate the principles and the ideas behind this frequency tuning method, it is essential to carry out a technology demonstration on an actual quantum processor as a proof of concept. While resistance measurement and manipulation studies can be conducted at room temperature on specifically designed test chips containing only $Al/AlO_x/Al$ Josephson junctions, validating the method requires testing it on the qubits in a quantum chip inside a dilution refrigerator. For this test it is fundamental to verify that the theoretical relationship given in Equation (2.8) between the normal state resistance of the Josephson junction and the plasma frequency of the qubit remains valid after manipulation. Not only, it is very important to assess whether the qubits subjected to this method experience any performance degradation. This last point is critical: even if the manipulation successfully changes the qubits' plasma frequencies according to the theoretical relation, the method would be impractical if the qubits' performance would degrade substantially. Therefore, to monitor the performance of the tuned qubits, the relaxation time T_1 is chosen as the main metric.

3.5.1 Device

In this section, the step-by-step process required to prepare the quantum chip for the technology demonstration is outlined, from the initial design to the assembly in the dilution refrigerator. This procedure is standard for any generic quantum chip, but the specific details and considerations taken for this particular project are presented and explained in the following list:

- **Design.** The design of the chip has been carried out using the KLayout software and builds upon the standard qubit design commonly used in the Quantum Technology Laboratory (QTL) group. The chip layout is shown in Figure 3.6 and consist of 8 fixed frequency transmon/Xmon-type qubits [51], each of which is capacitively coupled to a readout $\lambda/4$ coplanar waveguide resonator (CPWR). All the resonators are then inductively coupled to a single feedthrough transmission line, which can be used to control and read out the qubits with standard microwave electronics equipment [52].

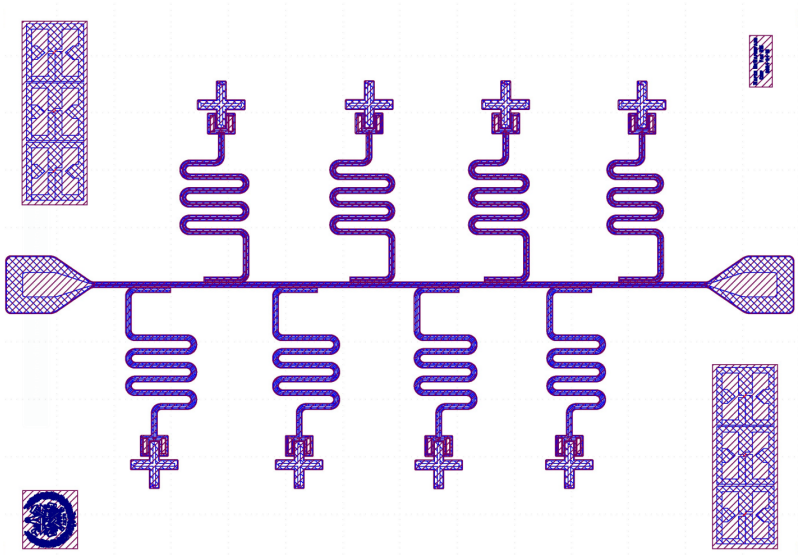


Figure 3.6: Chip design in the KLayout software. The 7×5 mm chip contains 8 transmon/Xmon-type qubits (cross shapes) capacitively coupled to their readout resonators (serpentine-shaped coplanar waveguides). The resonators are inductively coupled to the central feedthrough transmission line, which terminates on both sides of the chip with contact pads for wire bonding with the sample holder. The patterns at the corners of the chip are standard test structures and labels for identifying the specific chip.

All the qubits are designed to be detuned by $\Delta_{\text{res-qub}} = f_{\text{res}} - f_{01} = 1.9$ GHz from their respective readout resonators, where f_{01} is the plasma frequency of the specific qubit. The designed frequencies of the resonators are reported in the first line of Table 3.1. To achieve this detuning value, considering that all capacitors are identically designed to have $E_C/h = 195$ MHz, the width of the junctions is varied accordingly. This dimension is calculated according to Equation (2.8), with $\Delta = 176$ µeV. The normal state resistance of the junctions is determined based on their dimensions using a calibration curve extracted from the latest Josephson junction fabrication batch performed in the QTL group. This is the same methodology explained in [16], resulting in

$$R_N(d) = \frac{254\ \Omega\mu\text{m}^2}{(d + 0.014\ \mu\text{m})^2}. \tag{3.3}$$

Furthermore, since the tunneling resistance of a M-I-M barrier measured at room temperature is smaller than the tunneling resistance at "low temperatures" [53] considered in Equation (2.8), an empirical increase factor of +14% is considered. The junction dimensions calculated in this way for each qubit are reported in the second row of Table 3.1.

	q1	**q2**	**q3**	**q4**	**q5**	**q6**	**q7**	**q8**
$\boldsymbol{f}_{\text{res}}$ **[GHz]**	5.880	6.011	6.131	6.259	6.380	6.529	6.669	6.825
JJ width [nm]	139	144	149	153	158	163	169	174

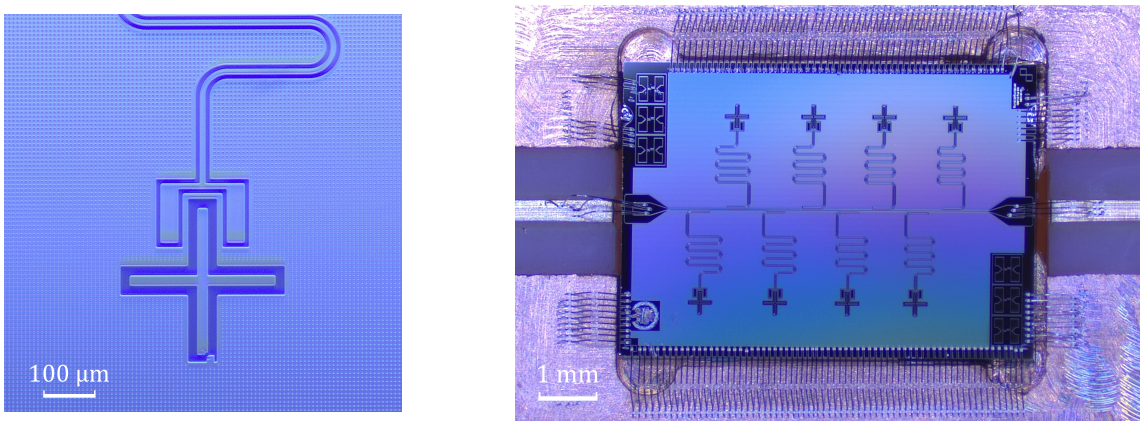
Table 3.1: Relevant design parameters for the quantum chip used in the technology demonstration. The resonant frequencies of the readout resonators f_{res} and the widths of the Josephson junctions are listed.

Other important and necessary design considerations are the dimensions and connectivity of the selected qubits, specifically the "grounded" Xmons. This choice was not casual: grounded Xmons were preferred over other floating transmon qubit types due to their practical advantages when using the manual probe station described in Section 3.1.2. In fact, with one probe already at the same potential of the Xmon's ground island upon contact and ensuring no voltage differential between the probes, the second probe can safely contact the other conducting island, minimizing the risk of electrostatic discharge (ESD) events. These ESD events can easily cause the breakdown of the oxide layer, irreversibly breaking the device. Additionally, the size of the x-shaped island is also important, as it must be large enough for the needles to make contact. The needle tips of the manual probe station, approximately 2 µm in diameter, are sufficient to contact the Xmon's central conductive island, which has a width of 24 µm.

- **Fabrication.** When the chip design is finalized, it can be incorporated into a wafer-level design and fabricated in the cleanroom. The fabrication followed the standard procedures and recipes typically used in the QTL group and detailed in Chapter 3 in reference [50]. A significant aspect of the fabrication was the decision to use thin-oxide junctions, chosen for their demonstrated potential to be manipulated over a broader range as it will be discussed in Section 4.2. It is also worth mentioning that the fabricated junctions are of the PICT type described in [37]. In Figure 3.7a, a micrograph depicting a qubit capacitively coupled to its readout resonator is shown. Once the wafer is completed, it can be diced and the individual chips extracted.

- **Wire bonding.** After being diced, the chip is ready to leave the cleanroom. It is then carefully glued into the dedicated cavity within a copper sample holder. Once the chip is correctly fixed, electrical connections are established with the sample holder through Al wire bonding. For this particular chip design and sample holder, there is no need for an intermediate printed circuit board (PCB) to connect them. Therefore, the device's ground plane is directly connected to the copper case of the sample holder box, while the feedthrough transmission line's ends are connected to the inner conducting part of the SMA connectors. A picture of the wire bonded chip inside the open sample holder box is shown Figure 3.7b. Subsequently, the sample holder can be sealed and secured to the bottom plate of a dilution refrigerator. Finally, the room temperature electronic instru-

mentation is connected to the device using coaxial cables with an appropriate series of microwave filters, attenuators and amplifiers as explained in [52]. Once the cooldown of the dilution refrigerator starts, it takes approximately $36 - 48$ hours for the mixing chamber to reach a temperature of ≈ 10 mK, at which point the device becomes operational and ready for measurements.



(a) **(b)**

Figure 3.7: **(a)** Optical microscope image of a qubit within the quantum chip. The aluminium (light blue) is deposited on the silicon substrate (gray) and patterned according to design using photolithographic techniques. The holes present in the superconducting ground plane serve to trap the Abrikosov magnetic flux vortices. At the bottom of the Xmon, the x-shaped central conductive island is connected to the ground plane through the Josephson junction (not visible due to the nanometer-scale dimension). **(b)** Optical microscope image of the chip connected to the sample holder box through Al wire bonds. The ground plane is directly connected to the copper case of the sample holder box, while the ends of the feedthrough transmission line are connected to the inner parts of two SMA connectors.

3.5.2 Plan

To provide a proof of concept for the frequency tuning method, the technology demonstration has been planned following the example described in [17], and can be summarized in the following key points:

- **First cooldown.** Once the newly fabricated chip reaches the temperature of approximately 10 mK inside the dilution refrigerator, it is possible measure and perform the characterization of the qubits within it. The main parameters of interest for this project are the plasma frequency f_{01} and the relaxation time T_1 of the qubits. These parameters are characterized through a series of standard experiments, which are listed in Appendix A.

- **Warm up: resistance measurement.** After characterizing the qubits at low temperatures, the dilution refrigerator is warmed up and the device extracted. The Josephson junctions within each qubit are then measured using the manual probe station described in Section 3.1.2. At this point, the plasma frequency f_{01} and normal state resistance R_N of each qubits are known. According to Equation (2.4), the relationship between these two quantities should follow a power law with an exponent of $-\frac{1}{2}$. Therefore, it is possible to plot these quantities and perform a fit according to this relation.

- **Warm up: resistance manipulation.** Now the Josephson junctions on the chip can be manipulated. The greater flexibility in the signals that can be applied during manipulation with the manual probe station, compared to the automatic probe station, allows for a variation in the manipulation process described in Section 3.3. Specifically, the manipulation used in this technology demonstration consisted of a series of 1 second long alternating bias pulses. This approach was inspired by the ABAA technique [20], but was conducted at room temperature. This technique was preferred because it showed greater potential for increasing the resistance in a shorter amount of time compared to a constant DC bias. As suggested in reference [41], this increased effectiveness is believed to result from the varying polarizations of the bias affecting both interfaces of the junction.

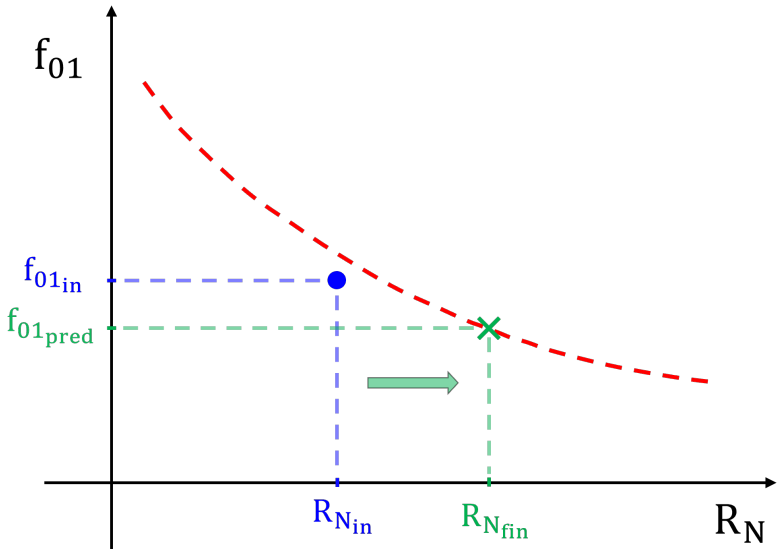


Figure 3.8: Theoretical illustration of the frequency manipulation process for one qubit. After fitting the Ambegaokar-Baratoff relation (dashed red curve) to the initial data points (only one blue dot is shown here), the resistance of the junction is manipulated at room temperature (green arrow) up to the final value $R_{N_{\text{fin}}}$. Using the previously obtained fit, the final qubit plasma frequency can be predicted from the final resistance value.

Since this is the first attempt to provide a proof of concept for the method under development, it is sufficient to demonstrate that the plasma frequency of the qubits can indeed be changed by increasing the resistance of the junctions, in accordance with the previously fitted Ambegaokar-Baratoff relation. Therefore, in this project, the junctions have been manipulated without targeting a precise frequency value. Instead, the aim was to induce a significant change in frequency that exceeds the normal fluctuations typically observed between different cooldowns [54, 55]. The final resistance obtained after the manipulation is used to predict the expected final plasma frequency of the qubits. This is achieved by projecting the final resistance value onto the fitted curve and extrapolating the corresponding frequency, as illustrated in Figure 3.8.

- **Second cooldown.** Finally, the sample holder is mounted again in the dilution refrigerator and the device is cooled down for the second time. The final plasma frequency of each qubit is measured and compared with the predicted value from the fit. The qubits' coherence times are also measured to investigate whether the manipulation has a significant effect on the performance of the device.

Additionally, an identically designed copy of the chip was fabricated to provide a reference for comparison with the device subjected to the frequency tuning method. This reference device was mounted alongside the main chip in the same dilution refrigerator and characterized at low temperatures. During the warm-up of the refrigerator, the reference chip was left untouched and then re-characterized during the second cooldown to assess the natural fluctuations affecting the qubit frequency f_{01} and coherence time T_1.

4

Results and discussion

In this chapter, the results of the room temperature experiments on the normal state resistance of Josephson junctions are presented, analyzed and discussed in the context of developing a complete and practical method for tuning the frequency of superconducting transmon qubits. Additionally, a qualitative theoretical model based on the available literature is proposed to explain these observations. Finally, a proof of concept for this method is presented and discussed, alongside considerations regarding its limitations and potential improvements.

4.1 Resistance measurement

Initially, the primary focus of the project was to find a reliable method for measuring the resistance of the junctions with high precision and minimal "backaction" (term introduced in Section 3.2). Therefore, various experiments were conducted to determine the optimal measurement parameters to achieve this goal.

To further emphasize the importance of this section, one of the very first noticeable evidences of the correlation between the electrical measurements of the junction and the increase in its tunneling resistance is shown in Figure 4.1. The plot depicts the result of 1000 consecutive measurements of a single Josephson junction performed with the automatic probe station described in Section 3.1.1. The intended current level for these measurement was 100 µA. However, to prevent the breakdown of the device, the instrument allows to set a limit on the effective voltage drop across the junction. This limit was set to 0.9 V, resulting in a maximum current for each data point being closer to $70 - 80$ µA, rather than the intended 100 µA.

During the 1000 measurements, the device clearly exhibited a gradual increase in its tunneling resistance, up to approximately +20% of its initial value. The same trend was not observed in similar junctions measured with lower current levels and cannot be explained by the natural aging described in Section 2.4.2, since the device was fabricated more than one year before the experiment and its natural aging process was fully saturated. Therefore, the increase in resistance must be a consequence of the measurements performed.

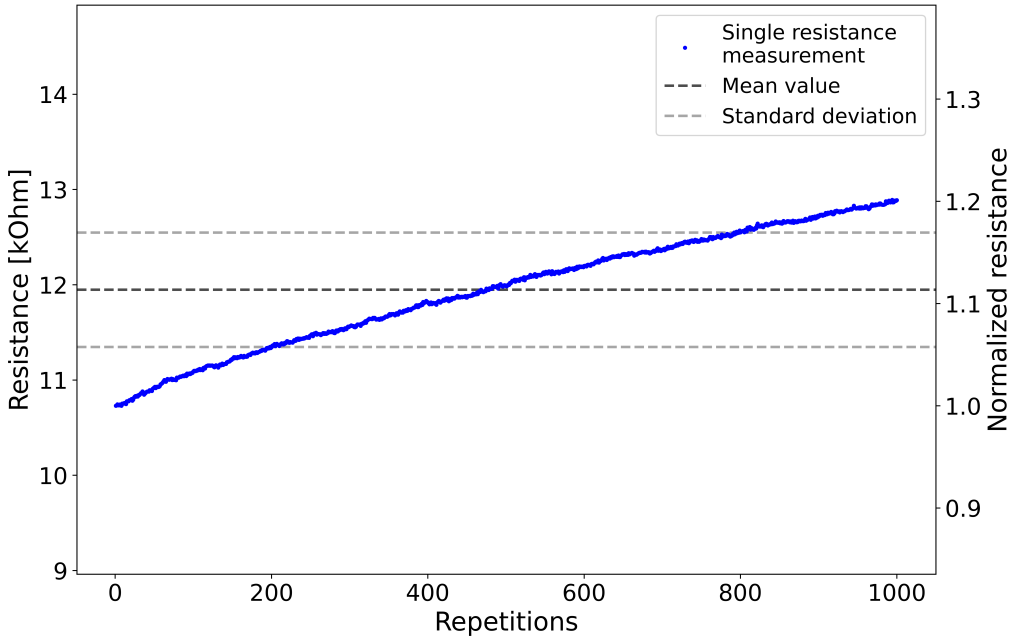


Figure 4.1: Repeated resistance measurements with the automatic probe station on a single thin-oxide Josephson junction. The device is measured 1000 times with a maximum current set to 100 µA and a voltage limit of 0.9 V. The measurement outcomes are represented by blue dots, with a time interval of 5 seconds between two consecutive measurements. The mean value and standard deviation of the measurements are shown by the dashed black and gray lines respectively. These indicators, which are typically used to provide a better estimation of the measured quantity and its uncertainty according to statistical principles, lose their significance due to the continuous resistance increase observed between individual measurements.

The significance of presenting this preliminary result obtained during the initial months of the project is twofold. Firstly, it confirms the feasibility of effectively increasing the normal state resistance of a Josephson junction through the application of DC electrical signals, holding the promise for applications in tuning the frequencies of superconducting transmon qubits. Secondly, it highlights the criticality of the resistance measurements within the framework of the project, which are clearly susceptible to the so called "measurement backaction".

4.1.1 Precision trade-off

Following the observation of the "backaction" effect in the "high current" measurements depicted in Figure 4.1, the logical next step is to attempt to minimize this effect by using lower current levels for the measurements. However, every measuring instrument has its own limitations and intrinsic noise floor. As a result, using excessively low currents can become challenging to detect precisely and consistently, or even infeasible with the available instruments.

For this reason, an experiment was performed to assess the precision and the built-in noise of the automatic probe station described in Section 3.1.1 for measuring these tunnel junctions. In this experiment, multiple thin-oxide devices of different dimensions were measured at various current levels. Each junction was measured 50 times to try to limit the "backaction" of the measurements. The experiment was conducted exclusively on thin-oxide junctions, as the precision of the measurement is influenced by the resistance value of the device rather than other specific properties like the thickness of the oxide layer. The results are reported in Table 4.1 and show no significant "measurement backaction".

The value used in the table to compare the precision of the different measurement conditions is the coefficient of variation (CV). The coefficient of variation is defined as

$$\mathrm{CV} = \frac{\sigma}{\mu}, \tag{4.1}$$

where σ is the standard deviation of the distribution of multiple measurements for the same device and μ is the mean. This quantity provides a metric for the repeatability of the measurement outcomes, which can be used to compare the precision of different measurement conditions.

	100 nm	**150 nm**	**200 nm**	**250 nm**	**300 nm**	**350 nm**
20 nA	0.32%	0.39%	0.51%	0.85%	1.06%	1.24%
40 nA	0.17%	0.22%	0.38%	0.43%	0.54%	0.63%
80 nA	0.13%	0.17%	0.21%	0.27%	0.27%	0.46%
160 nA	0.11%	0.09%	0.11%	0.12%	0.17%	0.15%
320 nA	0.09%	0.09%	0.08%	0.09%	0.10%	0.10%

Table 4.1: Coefficient of variation for junctions of different dimensions (columns) measured at different current levels (rows). Each entry is extracted from 50 measurements on different thin-oxide devices.

The results presented in Table 4.1 clearly exhibit two distinct trends: firstly, an increase in CV as the current level of the measurements decreases; and secondly, an increase in CV for larger junction dimensions. The latter trend can be explained recalling Equation (3.2), which indicates an inverse relationship between resistance and the square of the junction width. Therefore, larger junctions have lower resistance, resulting in a smaller voltage drop for the same current applied during the measurement. A reduced voltage drop leads to a lower signal-to-noise ratio (SNR), which result in less precise measurements. However, this trend becomes less pronounced for the 160 and 320 nA cases, suggesting that the precision is approaching the limit imposed by the intrinsic noise of the measuring instrument.

In the context of developing a method to tune the plasma frequency of the transmon qubits within a quantum processor, the choice of the optimal measurement conditions depends on the precision required for the final frequency of the tuned qubits. A practical and effective method requires a measurement precision that matches or exceeds the precision necessary to avoid frequency collision issues. Reference [16] suggests that achieving a precision of ±10 MHz in the qubit plasma frequencies is necessary to scale the number of qubits in the processor above 100 while minimizing the problem of frequency collisions for a given connectivity. As discussed in the reference, the standard deviation in the plasma frequency under the assumption that the normal state resistance is the only source of uncertainty can be calculated as

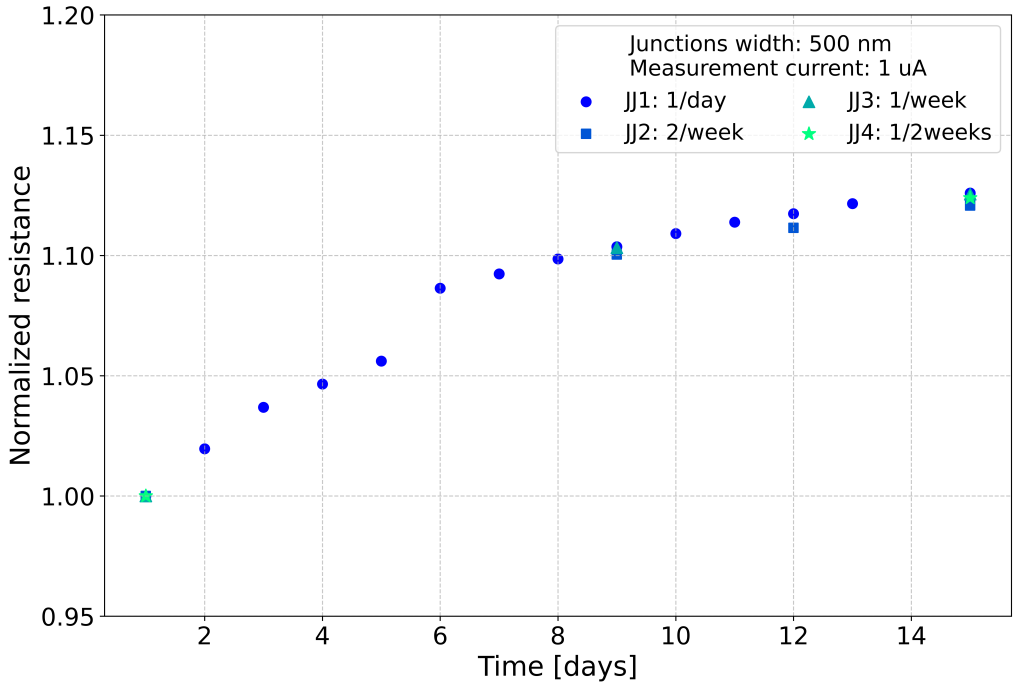
$$\sigma_{f_{01}} = \frac{1}{2}\mathrm{CV}_{R_N} f_{01}. \tag{4.2}$$

To provide context, for a qubit with $f_{01} = 4$ GHz and a desired frequency uncertainty of 10 MHz, according to Equation (4.2), a coefficient of variation equal to or smaller than 0.5% is required for the resistance measurement. Considering typical dimensions of thin-oxide junctions ranging between 100 nm and 250 nm, a measuring current equal to or greater than 40 nA ensures sufficiently high precision. For this reason, throughout this project, the standard maximum current used for measurements on the automatic probe station has been set to 50 nA, unless otherwise specified.

4.1.2 Natural aging

Another crucial consideration to keep in mind when dealing with $\mathrm{Al/AlO_x/Al}$ tunnel junctions is the phenomenon of aging. As discussed in Section 2.4.2, in these devices aging manifests as a slow increase in the tunneling resistance over the initial months following fabrication. However, reference [41] reveals that aging is particularly pronounced in the first few hours post-fabrication, exhibiting a stretched exponential behavior. Therefore, aging must be taken into account in the context of developing a methodology to precisely asses the resistance of these junctions.

A natural question arising from the observation at the beginning of this chapter about the "backaction" of the measurement (see Figure 4.1), is whether the aging of the junctions is influenced by the repeated measurements performed to observe it. To address this question, an experiment was conducted involving multiple newly fabricated junctions of various dimensions. These junctions were subjected to repeated measurements on the automatic probe station with different time intervals over a span of two weeks, varying the current level used in the measurements. This experiment was repeated for both thin-oxide and thick-oxide devices. The results for some selected samples are illustrated in Figures 4.2 and 4.3.



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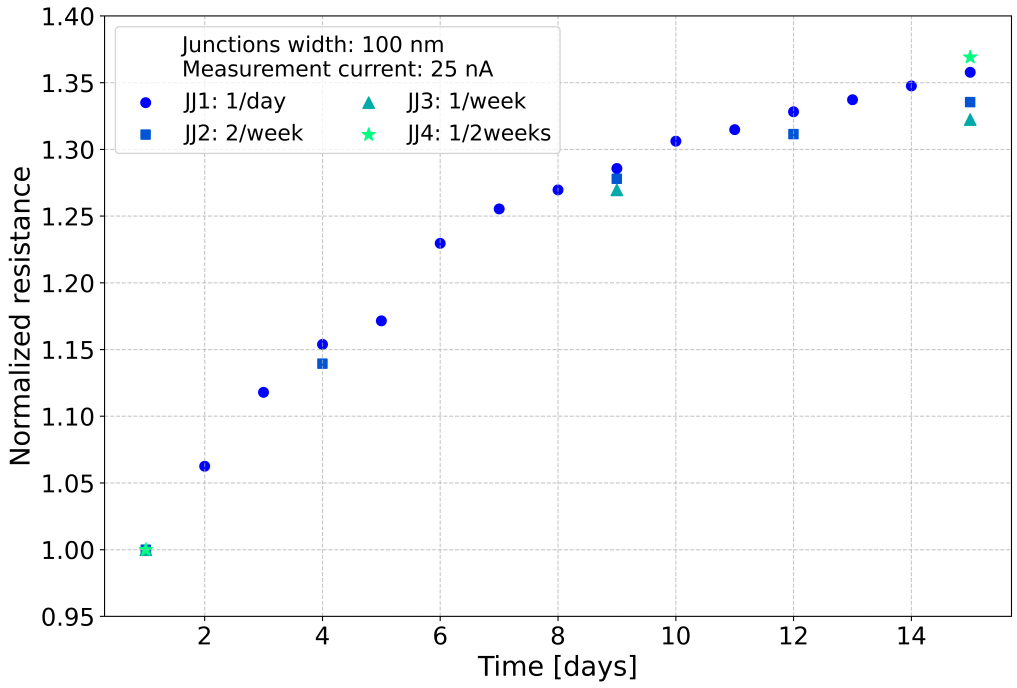
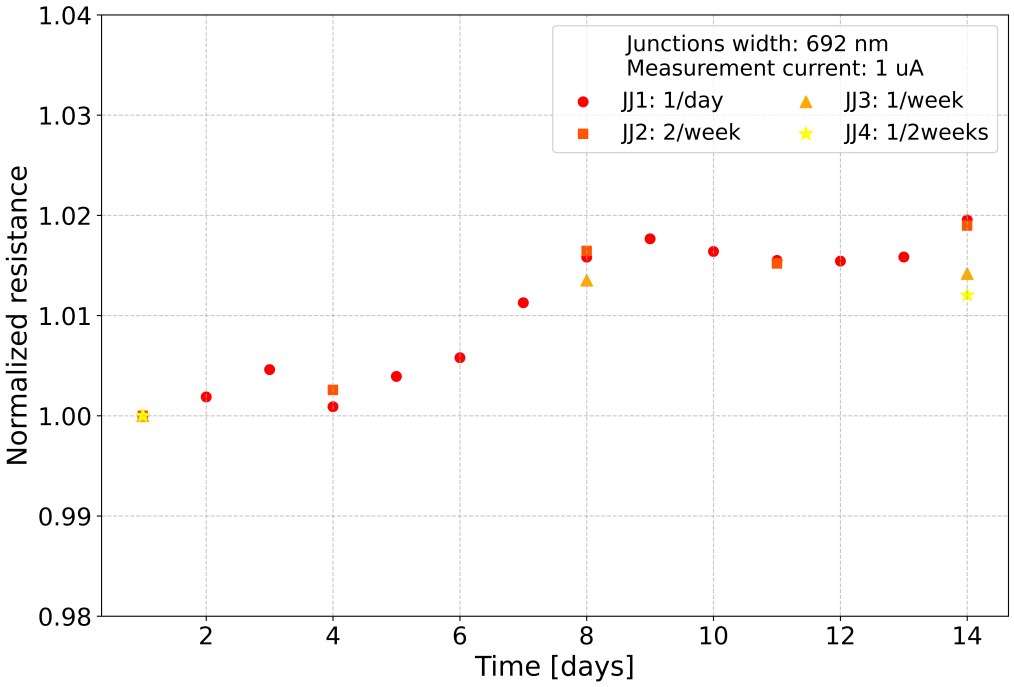


(b)

Figure 4.2: Aging measurements on thin-oxide junctions. Nominally identical, newly fabricated devices are measured over two weeks at different time intervals. In the plot, data points from different devices are distinguished by color and shape. **(a)** Four 500 nm width junctions are measured with a maximum current of 1 µA. **(b)** Four 100 nm width junctions are measured with a maximum current of 25 nA.



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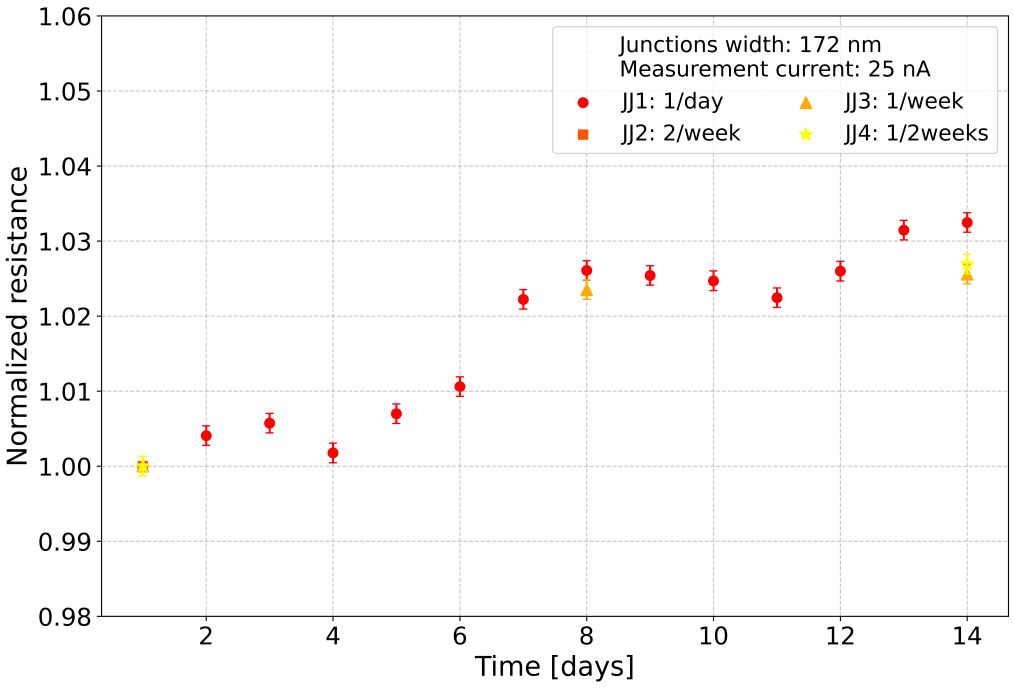


(b)

Figure 4.3: Aging measurements on thick-oxide junctions. Nominally identical, newly fabricated devices are measured over two weeks at different time intervals. In the plot, data points from different devices are distinguished by color and shape. **(a)** Four 692 nm width junctions are measured with a maximum current of 1 µA. **(b)** Four 172 nm width junctions are measured with a maximum current of 25 nA. The error bars indicate the uncertainty relative to the specific measurement conditions, which is appreciable only in this case and thus plotted.

The few examples presented in Figures 4.2 and 4.3 adequately capture and illustrate the general trend observed in all the experiments and allow to effectively address the initial question. In fact, across all the analyzed samples, which differ for junction dimensions and current levels, no significant influence of the number of performed measurements on the relative resistance increase was observed. This trend holds true across all levels of applied current, ranging from 25 nA to 10 µA (see Appendix B). The small variations in the relative resistance increase that can be observed in certain cases between nominally identical junctions, are attributed to the slight differences in the actual devices, which are a direct consequence of the inherent fabrication uncertainty [14, 15].

For these reasons, it is possible to conclude that the observed increase in resistance must be entirely attributed to the natural aging mechanism discussed in Section 2.4.2, discarding the possibility of any significant contribution from the measurements themselves. Consequently, this allows for a comparison between different devices measured with various current levels and facilitates the analysis of their aging behavior on an average level. The collected data are plotted in Figure 4.4.

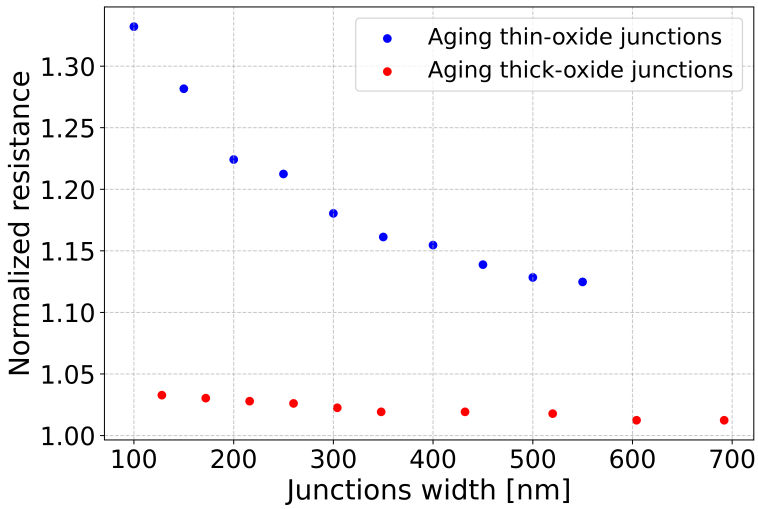


Figure 4.4: Relative normal state resistance increase in Josephson junctions due to natural aging, measured two weeks after fabrication. Thin-oxide (blue dots) and thick-oxide (red dots) junctions of various dimensions are compared.

From Figure 4.4 the correlation between the junction's geometry and aging is clearly visible. The effect of aging is significantly more pronounced for the thin-oxide junctions. In this case, the relative increase in tunneling resistance within the first two weeks after fabrication ranges from around 12% for the larger junctions to more than 30% for the smaller ones. A similar trend of dependence on junction width is also observed in the thick-oxide devices, although in this case these do not exhibit more than 3% to 4% relative resistance increase in the smallest dimension cases. This result aligns with reference [16], where this type of thick-oxide junctions where first introduced.

This significant increase in resistance highlights the importance of considering aging effects when designing junctions for quantum chips. Furthermore, understanding the differences between thin-oxide and thick-oxides junctions can guide in the selection of the devices for a specific application, ensuring the optimal combination of practicality and performance.

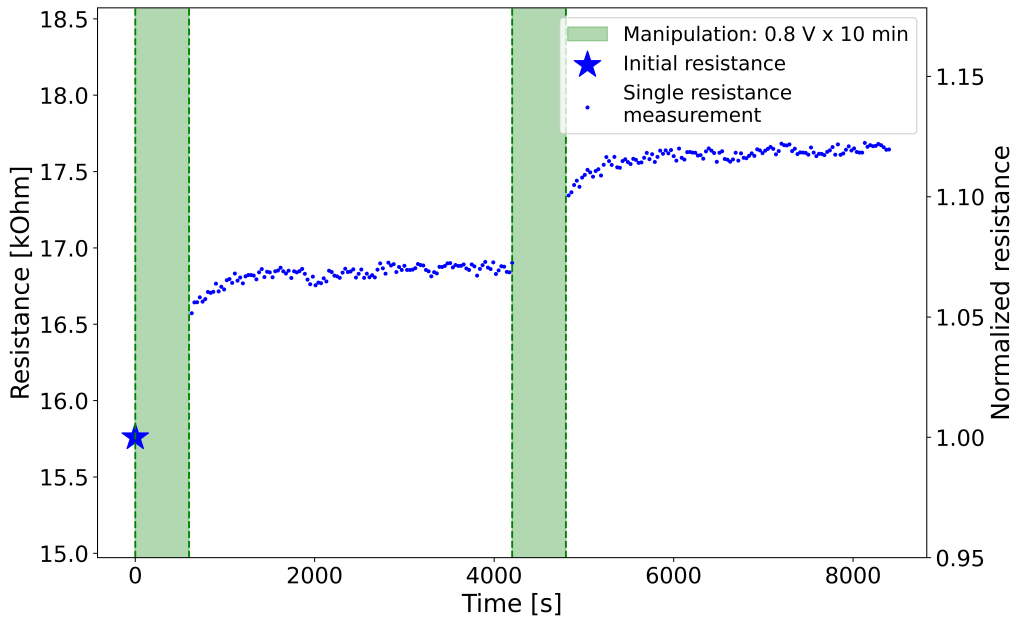
Finally, in the context of developing a post-fabrication frequency tuning method, the results of this experiment ensure that newly fabricated junctions can be measured a relatively small number of times with these current levels without significantly affecting the natural aging process. This understanding is crucial, as it allows for the reliable assessment of the normal state resistance both before and during the manipulation procedure. In the next section, the developed technique for measuring the resistance of the junctions will be implemented alongside the active manipulation procedure of these devices.

4.2 Resistance manipulation

After establishing a reliable method to measure the normal state resistance of Josephson junctions at room temperature with negligible "backaction", the next step is to manipulate the resistance of these devices in a controlled and precise manner. With the results from Section 4.1, it is possible to integrate that measurement process into the manipulation procedure. This allows for continuous assessment and control of the resistance change during manipulation, ensuring that the measurement process itself does not contribute to these changes.

Before presenting the results of the experiments, it is important to highlight and clarify the purpose and intended implementation of the resistance manipulation step within the frequency tuning method. As explained in Section 3.3 with Figure 3.4, the goal of the manipulation is to correct for the fabrication uncertainties of these devices. It must be kept in mind that the electrical DC signals investigated in this project can only increase the initial resistance of the device, not decrease it. Therefore, before evaluating the precision of the manipulation, it is essential to determine whether the range over which the resistance can be increased is sufficient to correct for these initial uncertainties.

In this project, to gain insight into the magnitude of resistance increase that can be achieved and the parameters that can be adjusted to control it, manipulation experiments were conducted on hundreds of Josephson junctions of various dimensions using the automatic probe station described in Section 3.1.1. In Figures 4.5, 4.6 and 4.7, some relevant results from these experiments are illustrated. A detailed description of these plots can be found in Section 3.5. These examples effectively capture the main trends observed among all the analyzed cases. Thus, some qualitative considerations regarding the relationship between the manipulation conditions and the observed resistance increase are discussed in the following paragraphs.



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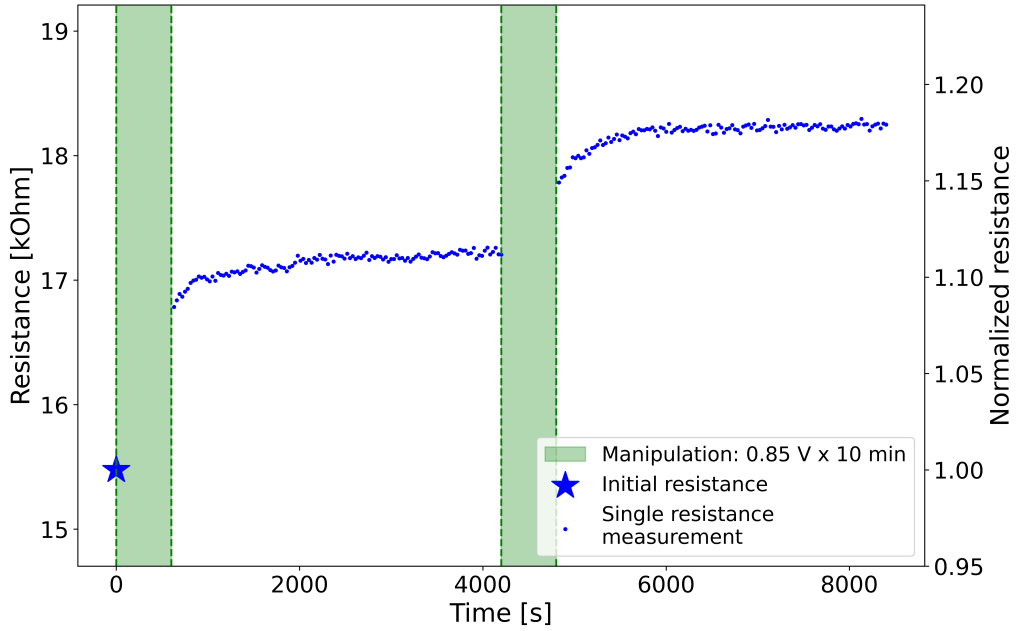
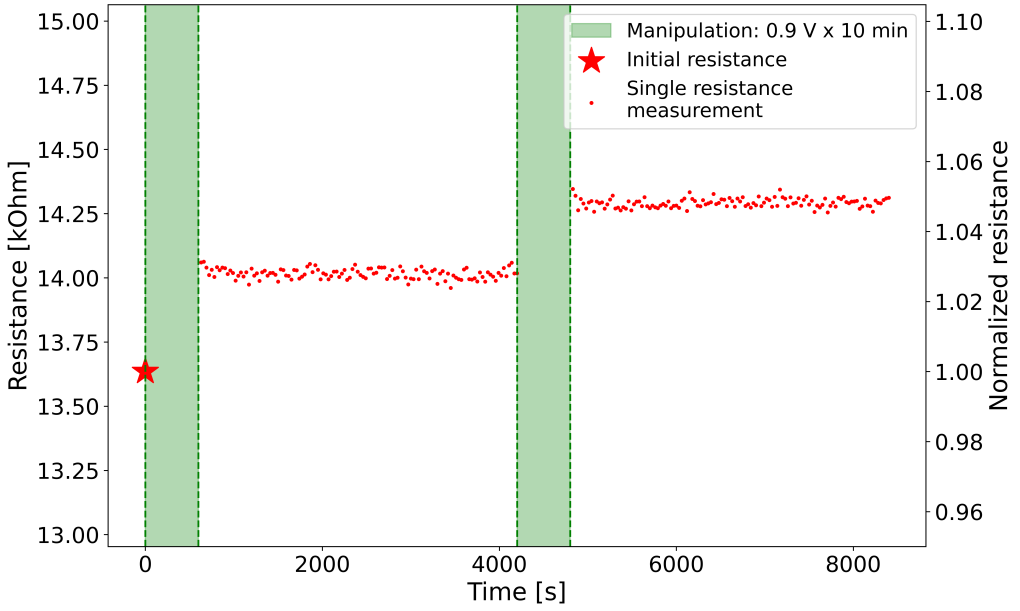


(b)

Figure 4.5: Manipulation experiments on thin-oxide junctions. **(a)** The initial resistance of the device is measured (blue star), followed by two manipulation steps where a constant voltage bias of 0.8 V is applied for 10 minutes each (green areas). After each manipulation step, the resistance is measured every 30 seconds for one hour (blue dots). **(b)** In a similar experiment, the device is subjected to two manipulation steps with a constant voltage bias of 0.85 V for 10 minutes each.



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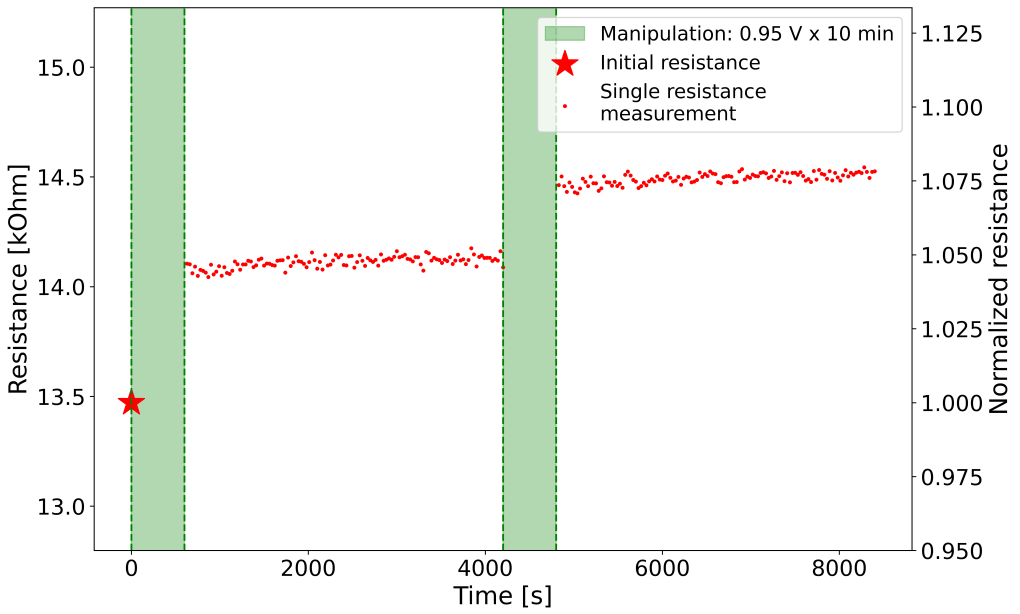
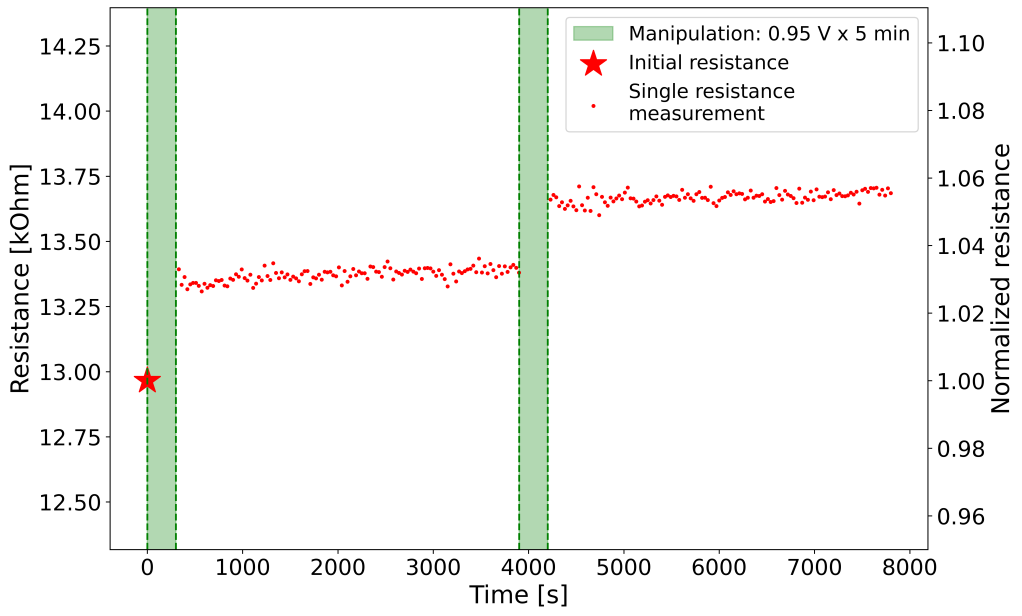


(b)

Figure 4.6: Manipulation experiments on thick-oxide junctions. **(a)** The initial resistance of the device is measured (red star), followed by two manipulation steps where a constant voltage bias of 0.9 V is applied for 10 minutes each (green areas). After each manipulation step, the resistance is measured every 30 seconds for one hour (red dots). **(b)** In a similar experiment, the device is subjected to two manipulation steps with a constant voltage bias of 0.95 V for 10 minutes each.



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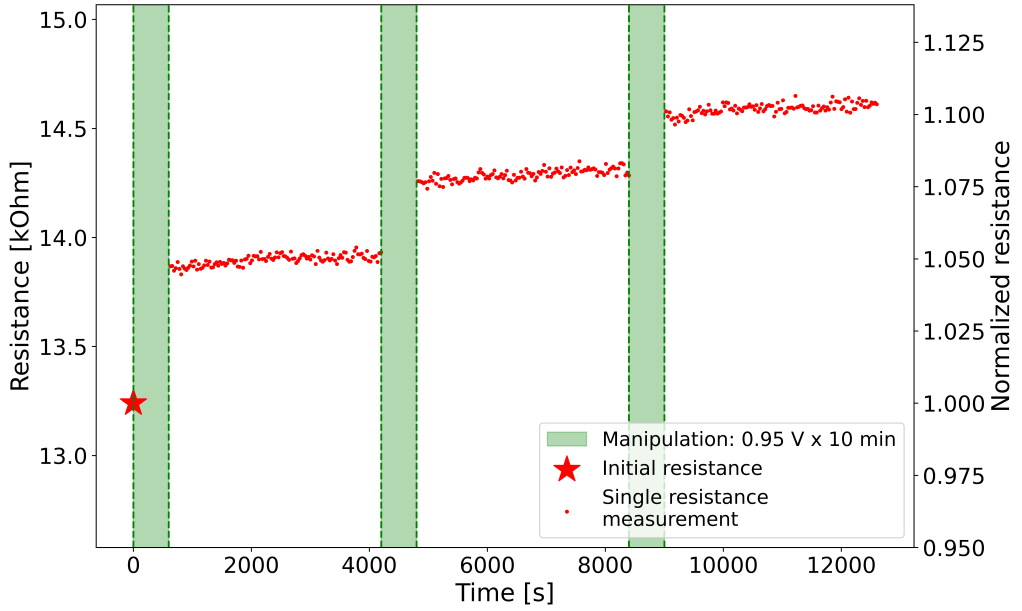


(b)

Figure 4.7: Manipulation experiments on thick-oxide junctions. **(a)** The initial resistance of the device is measured (red star), followed by two manipulation steps where a constant voltage bias of 0.95 V is applied for 5 minutes each (green areas). After each manipulation step, the resistance is measured every 30 seconds for one hour (blue dots). **(b)** In a similar experiment, the device is subjected to three manipulation steps with a constant voltage bias of 0.95 V for 10 minutes each.

To asses the contribution of different parameters, the manipulation experiments were performed varying the DC voltage bias, the duration of the manipulation and the number of manipulation steps. Between each step, the resistance was measured with

a current of 50 nA every 30 seconds for one hour to monitor and evaluate the effect of the manipulation. Interestingly, this monitoring revealed a characteristic behaviour suggesting that the resistance increase does not stabilize immediately after the voltage application ceases, but slowly continues to evolve over time afterward. This sort of delayed effect will be discussed further in Section 4.2.1.

The first prominent trend observed across all the examples is the relationship between the amplitude of the applied DC signal and the total increase in resistance. Specifically, for an equivalent total manipulation time, a significantly greater final resistance increase was noted when a higher voltage bias was applied during the manipulation. This effect is clearly illustrated by comparing Figures 4.5a with 4.5b and 4.6a with 4.6b. The second significant observation relates to the total manipulation time, which can be achieved either by increasing the duration of each manipulation step or by increasing their number, and its effect on the resistance increase. As expected, a longer manipulation time results in a larger relative increase in resistance. This trend is evident when comparing Figures 4.7a, 4.6b and 4.7b.

Noticeably, a clear feature emerges from dividing the total manipulation time into separate steps. A closer look at Figure 4.7b shows how the initial manipulation step results in the largest "jump" in resistance value, while each subsequent step leads to progressively smaller increases. This pattern suggests a form of saturation in the manipulation process, effectively limiting the maximum resistance that can be achieved. However, there are also limitations on the duration and voltage levels that can be applied to increase the resistance without causing the breakdown of the oxide layer in the junction. Once breakdown occurs, as detailed in Section 3.2, the device breaks and start behaving similarly to a short circuit. During the measurements of hundreds of Josephson junctions for this project, many devices experienced breakdown, although not shown here. A key lesson learned is that exposing the junction to voltage biases close to the V_{BREAK} of the specific oxide layer already carries a non negligible risk of breakdown. Therefore, prolonged exposure to such biases will lead to device failure. For this reason, the manipulation procedure must be carefully designed for each specific device to ensure optimal results with a high success rate.

Finally, another important noticeable trend is the dependence of the relative resistance increase on the oxide thickness, as evidenced by comparing Figures 4.5 and 4.6. Despite these experiments being conducted under different conditions to adapt to the varied V_{BREAK} for thin-oxide and thick-oxide devices (see Section 3.4), the trend is evident. Thin-oxide junctions demonstrate a more significant resistance increase, approaching nearly +20% of the initial value. In contrast, thick-oxide junctions exhibit greater resistance to changes, with observed relative increases typically not exceeding 10%. This suggest a relative ease in manipulating thin-oxide junctions compared to the other type of devices. This is another important factor to consider when selecting the type of junctions for a specific application.

To summarize, the results from the manipulation experiments presented in this section demonstrate a promising capability to deliberately increase the normal state

resistance R_N of the Al/AlO_x/Al Josephson junctions. As noted in Section 3.3, achieving a manipulation range at least twice the fabrication uncertainty is essential to correct for the initial spread in resistance. Therefore, the observed resistance increase of nearly 20% for the thin-oxide junctions indicates that this technology can in principle compensate for the fabrication variations on a wafer-level scale of this type of devices [14, 15, 37]. For the thick-oxide junctions, given their intrinsic lower fabrication uncertainty due to the larger junction area [16], the demonstrated manipulation range suggests that this method can still adjust for the initial uncertainties. These results highlight the potential of this resistance manipulation technique to enhance the precision and reliability of qubit fabrication. However, to rigorously demonstrate the capability to precisely and completely correct for the fabrication variations, further systematic studies on assessing the initial uncertainty and optimizing the technique to improve the manipulation range are needed.

4.2.1 Delayed effect

This section is dedicated to exploring the slow continuous resistance evolution observed after the application of a high DC voltage during a manipulation procedure. To observe this delayed effect more closely, some thick-oxide devices were subjected to a single manipulation step and monitored for the subsequent 24 hours. During the manipulation procedure, a DC voltage of 0.95 V was applied for 10 minutes. The result of this experiment for one of the devices is depicted in Figure 4.8.

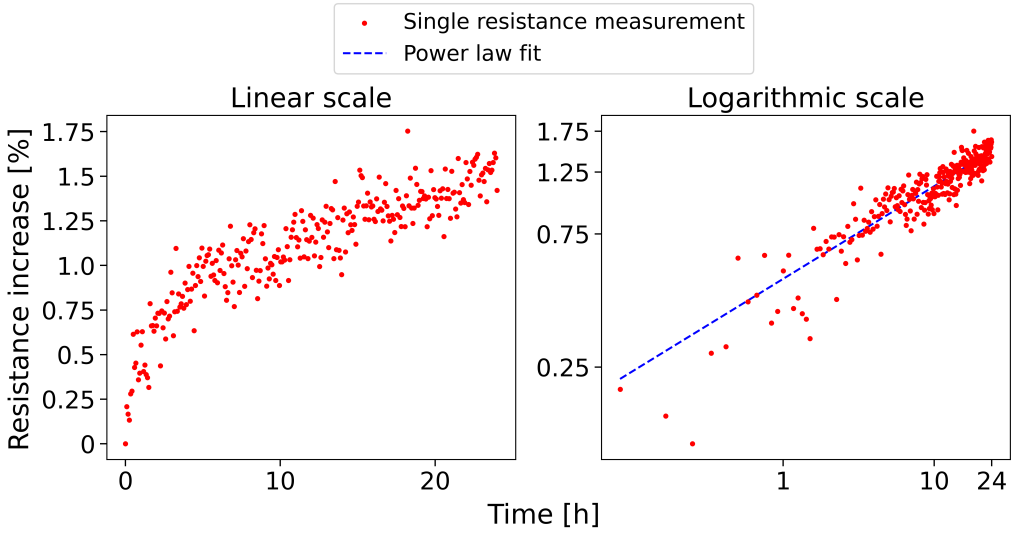


Figure 4.8: Delayed resistance increase after manipulation of a thick-oxide junction. Following a manipulation procedure where a constant voltage bias of 0.95 V was applied for 10 minutes (not shown), the device's resistance was measured every 5 minutes over the subsequent 24 hours, represented by the red dots. The y-axis shows the percentage increase in resistance relative to the first measurement after the manipulation step. The results are displayed in both linear (left panel) and logarithmic (right panel) scales. In the logarithmic axes plot, the blue dashed line represents the fitted power law $y = \alpha \cdot x^{\beta}$, with $\beta = 0.33 \pm 0.01$.

The resistance of the thick-oxide junction, as shown in Figure 4.8, continued to increase over the 24 hours following the manipulation step, showing an additional increase of nearly 2% relative to the first resistance measurement taken immediately after the manipulation. This increase is on top of the more rapid and larger step-like increase of about 6% (not shown in the plots) that occurred during the manipulation itself. This observed additional increase cannot be attributed to natural aging for two reasons: first, the junction had already undergone weeks of natural aging before the experiment; second, even in the initial days after fabrication, when aging effects are more pronounced, such an increase was never observed in thick-oxide devices. For these reasons, this resistance increase must be considered a delayed effect of the manipulation procedure.

In Figure 4.8, the plot in the right panel shows the delayed resistance increase on a logarithmic scale, revealing a linear behavior that suggests the delayed effect of the manipulation follows a power law. This hypothesis is also supported by the very recent follow-up publication on the alternating-bias assisted annealing (ABAA) technique [21]. Noticeably, the fitted exponent values obtained in this project are consistent with those reported in that study.

Throughout the course of the project, this observed delayed effect was not the main focus of the study. However, the results from the technology demonstration on actual qubits, supported by the recent follow-up publication on the ABAA technique [21], suggest that the delayed resistance increase caused by the manipulation procedure plays a crucial role in the development of a controllable and precise frequency tuning method. The discussion of these considerations is postponed to Section 4.4.

4.3 Theoretical model

This section explores a potential explanation for the physical mechanism behind the increase in normal state resistance observed after applying a voltage drop to the $Al/AlO_x/Al$ tunnel junction. The model presented, however, has to be considered solely as an intuitive empirical attempt to explain some of the experimental results obtained and to draw connections with current literature examples.

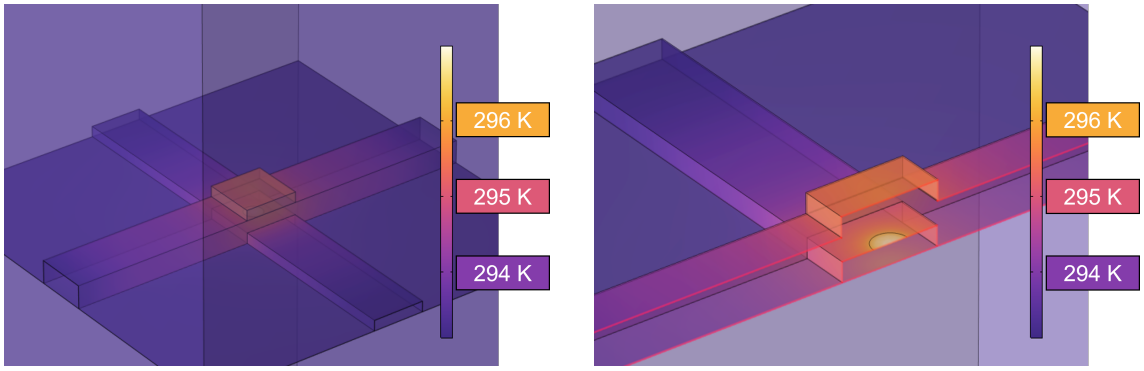
4.3.1 Heat transfer simulation

As previously discussed in Section 2.4.2, the literature contains numerous examples of increases in the normal state resistance of tunnel junctions with AlO_x barriers following various heat treatments and exposure methods [17, 19, 20, 22–24]. Initially, the resistance increase observed during this master's thesis project suggested that extremely localized Joule heating at the insulator/metal interface of the junction could be the responsible. This phenomenon, even in the case of a tunnel junction [56], can be described by the simple relation

$$P = VI, \tag{4.3}$$

where P is the electric power dissipated due to the voltage drop V and the flowing current I. To validate this hypothesis, a very basic heat transfer simulation of a standard device was performed to estimate the temperature range reached during a typical manipulation process. This was carried out using the Heat Transfer Module of the COMSOL Multiphysics software. For the simulation, a typical $Al/AlO_x/Al$ cross-type Josephson junction [57] was chosen, with dimensions 0.25 µm × 0.25 µm = 0.0625 µm^2. The simulation replicated the heat generated during a manipulation procedure where a constant DC voltage of 0.9 V was applied for 10 minutes. Given the typical resistance values and behavior of junctions of this size, an average tunnel current of about 120 µA was measured. According to Equation (4.3), this results in a power dissipation of approximately 110 µW at the junction interface.

However, an important consideration on the actual junction interface involved in the tunneling current must be done. Recalling Equation (2.10) in Section 2.3, the exponentially decaying dependence of the tunneling current on the thickness of the insulating barrier means that small variations in the barrier thickness ($\sim$ 1 Å) can change the tunneling current by an order of magnitude. In the junctions used in this study, typical variations in the oxide barrier thickness are in the order of several angstroms. It is also estimated that less than 10% of the total barrier area is responsible for the entire tunneling process [36]. Therefore, for the purpose of the simulation, only 10% of the total upper surface of the junction was considered responsible for dissipating power.



(a) **(b)**

Figure 4.9: Temperature profile of an $Al/AlO_x/Al$ tunnel junction after a typical manipulation procedure, simulated on COMSOL Multiphysics software with the Heat Transfer Module. The junction dimensions are 0.25 µm × 0.25 µm = 0.0625 µm^2. During the manipulation, a power of approximately 110 µW is uniformly dissipated from the inner circular part of the bottom electrode Al/AlO_x interface, which represents 10% of the junction area. The temperature profile shown is a snapshot of the simulation after 10 minutes of applied power. **(a)** 3D view of the temperature profile. **(b)** Cross-sectional view highlighting the internal temperature distribution.

The result of the simulation of the manipulation process is presented as a 3D temper-

ature profile in Figure 4.9. According to the simulation, the increase in temperature at the hottest spot inside the junction is in the order of 3 K to 4 K. This result seems in contrast with the initial hypothesis that local Joule heating is solely responsible for the increase in R_N, since, as discussed in Section 2.4.2, other documented examples of "thermal annealing" of AlO_x insulating barriers require temperatures greater than 200° C to observe a significant increase in resistance [22, 23].

A new insight into the interpretation of this result comes from the Cabrera-Mott theory of metal oxidation, discussed in Section 2.4.1. In alignment with the interpretation given by D. Pappas et al. (2024) [20] regarding their similar observations, it can be inferred that the voltage drop across the junction (or the resulting electric field) indeed plays a critical role in the observed resistance increase. In their study, the application of a voltage difference across the junction aimed to replicate the conditions similar to those present during the formation of the oxide layer. The idea is that the applied voltage modifies the potential profile experienced by the oxygen ions already present within the oxide. In fact, another study [23] has shown that the resistance of similar devices can still be increased by "thermal annealing" even in a nitrogen gas environment, suggesting that the changes in oxide the properties result from migration of pre-existing oxygen ions within the oxide. However, the physical mechanism driving this migration may have varied origins. D. Pappas et al. (2024) [20] proposed that the resistance increase could be a thermally activated effect, which is in general explained by an Arrhenius law

$$k = Ae^{\frac{-E_a}{k_B T}}, \tag{4.4}$$

where in this case k is the rate constant of the resistance change and E_a the activation energy of the process. However, the voltage dependence of the observed resistance increase, discussed in Section 4.2, needs to be considered in this model to adequately explain the experimental observations. One possible approach, inspired by the growth rate of oxide layers in the low-temperature oxidation regime as described by the Cabrera-Mott oxidation theory [58], is to introduce a modification to the Arrhenius law. This modification accounts for the effect of the voltage applied V_a on lowering the activation energy E_a of the process. This adjustment leads to

$$k = Ae^{\frac{-E_a+|qV_a|}{k_B T}}, \tag{4.5}$$

where q is the ion charge and its product with V_a is taken in absolute value because the different polarizations affect each of the two metal/oxide interfaces as demonstrated in [41], resulting in a similar effect. With this addition to the conventional Arrhenius law describing thermally activated processes, Equation (4.5) can qualitatively account for most of the experimental observations discussed in Section 4.2. Specifically, the larger relative increase in resistance observed with higher DC voltages applied for longer times can be explained by such a relationship. Furthermore, it is conceivable that the thickness of the oxide may influence the activation energy E_a of the process, resulting in the observed relative ease in manipulating the thin-oxide devices.

However, it is essential to clarify that the primary objective of this project is not to formulate and rigorously demonstrate a comprehensive theoretical model explaining the physical mechanisms underlying the observed resistance increase in these junctions. Instead, the project aims to develop a practical and effective post-fabrication method for individually tuning the qubit frequencies within a quantum processor. Therefore, the hypotheses and conclusions presented in this section must be considered solely at the qualitative and heuristic level. To substantiate and verify these hypotheses, a meticulous theoretical investigation at the atomic level of the materials and additional experimental data collection are necessary to verify the agreement with the proposed relationship.

4.4 Proof of concept

Finally, this section presents the proof of concept for the post-fabrication frequency tuning method. The technology demonstration was performed on the device introduced in Section 3.5.1, utilizing the purposely designed manual setup described in Section 3.1.2. Following the detailed plan outlined in Section 3.5.2, the device was initially measured in the dilution refrigerator to characterize the initial frequencies and relaxation times of the qubits. Then, the cryostat was warmed up and the chip was extracted. At room temperature, the normal state resistance of the Josephson junctions for each qubit was measured before and after the manipulation procedure. Finally, the device was placed back inside the refrigerator, and the qubits were characterized again to compare the results with the initial measurements.

In Table 4.2, all the relevant parameters for characterizing the qubits before and after manipulation are presented.

	q1	**q2**	**q3**	**q4**	**q5**	**q6**	**q8**
$f_{01_{\text{des}}}$ **[GHz]**	3.980	4.111	4.231	4.359	4.480	4.629	4.925
$f_{01_{\text{in}}}$ **[GHz]**	3.7503	3.8149	4.0628	4.0912	4.2354	4.4623	4.6995
$T_{1_{\text{in}}}$ **[µs]**	68 ± 18	81 ± 28	87 ± 21	89 ± 19	84 ± 22	78 ± 21	61 ± 15
$R_{N_{\text{in}}}$ **[kΩ]**	13.152	12.022	10.966	10.631	10.059	9.028	8.156
$f_{01_{\text{fin}}}$ **[GHz]**	3.3296	3.3836	3.6798	3.5486	3.7680	4.0202	4.0468
$T_{1_{\text{fin}}}$ **[µs]**	69 ± 15	112 ± 21	32 ± 12	90 ± 16	48 ± 14	107 ± 14	74 ± 18
$R_{N_{\text{fin}}}$ **[kΩ]**	15.127	14.107	12.360	12.994	11.888	10.495	9.998
Δ_f **[MHz]**	−420.7	−413.3	−383	−542.6	−467.4	−442.1	−652.7

Table 4.2: Relevant qubit characterization parameters for the manipulated quantum chip. $f_{01_{\text{des}}}$ denotes the designed initial target plasma frequency. Quantities with the subscript $_{\text{in}}$ were measured before the manipulation process, while those with the subscript $_{\text{fin}}$ were measured after. The reported values for T_1 are $\mu \pm \sigma$, where μ and σ represent respectively the mean and the standard deviation of the relaxation times distribution obtained from 60 experiments (see Appendix A). $\Delta_f = f_{01_{\text{fin}}} - f_{01_{\text{in}}}$ indicates the frequency change induced by the manipulation process.

To provide a comparison for the variations induced by manipulating the normal state resistance of the qubits, a second chip of identical design was also characterized in two consecutive cooldowns without any manipulation in between. As expected, most qubits showed only minor variations in frequency, typically within a few MHz. However, one isolated case exhibited a more significant change of ≈ -24 MHz. These data are reported in the last row of Table 4.3. In contrast, the relaxation times of certain untreated qubits fluctuated more significantly. The measured lifetimes for

each qubit in the reference chip during both cooldowns are listed in Table 4.3 and plotted in the right panel of Figure 4.11 for a better comparison with the manipulated chip.

	q1	**q2**	**q3**	**q4**	**q5**	**q6**	**q8**
$\boldsymbol{T_{1_{\text{in}}}}$ **[µs]**	72 ± 15	68 ± 18	78 ± 16	42 ± 17	69 ± 16	65 ± 13	61 ± 13
$\boldsymbol{T_{1_{\text{fin}}}}$ **[µs]**	75 ± 18	67 ± 12	38 ± 13	35 ± 6	52 ± 9	12 ± 4	55 ± 11
$\boldsymbol{\Delta_f}$ **[MHz]**	+5.8	−24.4	+5.0	0	+6.4	+6.2	+3.8

Table 4.3: Relevant qubit characterization parameters for the reference chip. $\Delta_f = f_{01_{\text{fin}}} - f_{01_{\text{in}}}$ represents the frequency fluctuation between consecutive cooldowns without any manipulation in between. $T_{1_{\text{in}}}$ and $T_{1_{\text{fin}}}$ indicate the average relaxation times measured during the first and second cooldowns respectively.

It is important to note that, due to a defect in the readout resonator coupled to qubit q7, it was impossible to perform the full characterization of that qubit in both chips. Therefore, it is excluded from Tables 4.2 and 4.3 and Figures 4.10 and 4.11.

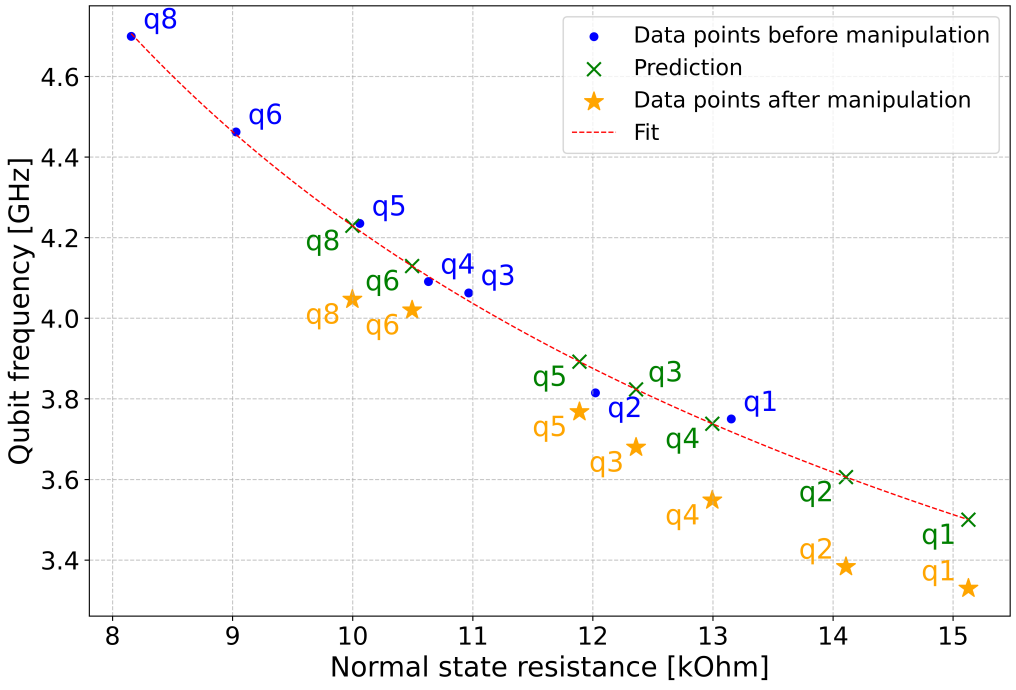


Figure 4.10: Results of the technology demonstration. Initially, the qubits are characterized (blue dots) and the Ambegaokar-Baratoff relation is fitted to these data points (red dashed line). After manipulating R_N of the qubits, predictions of the final qubit plasma frequencies are made (green crosses). Finally, the qubits are characterized again in a second cooldown of the dilution refrigerator and plotted (orange stars).

The most significant result, evident from the last row of Table 4.2 and Figure 4.10, is the notable change in qubit plasma frequency after manipulating the Josephson junctions' normal state resistance. This change, ranging approximately between −350 MHz and −650 MHz across the manipulated qubits, must be attributed to the manipulation procedure, as the fluctuations in the reference chip were only on the order of a few to tens of MHz during the same period. This marks the primary achievement of this experiment, demonstrating the ability to decrease the qubit plasma frequency by applying DC voltage signals to the Josephson junction.

Furthermore, examining the fluctuations in the relaxation time distributions before and after the manipulation reveals no clear evidence that the electrical signals applied to the junctions to increase their normal state resistance directly degrade the qubits' lifetimes. For instance, as highlighted in Figure 4.11, while qubits q3 and q5 showed a significant decrease in their average measured T_1, qubits q2 and q6 exhibited a notable increase. Similar fluctuations in relaxation times are also observed in the reference chip, which didn't undergo the same manipulation procedure as the main device. Also in literature there are many examples describing fluctuations in T_1 [54, 55], usually attributed to the coupling between the qubit and unwanted two-level systems (TLS) arising from defects in the device materials or other intrinsic mechanism. For these reasons, it is reasonable to conclude that the manipulation of the Josephson junctions' normal state resistance does not induce a degradation of the qubit's lifetime on its own, and multiple other factors likely contribute to determining the final relaxation time T_1. Therefore, the applicability of the method is demonstrated.

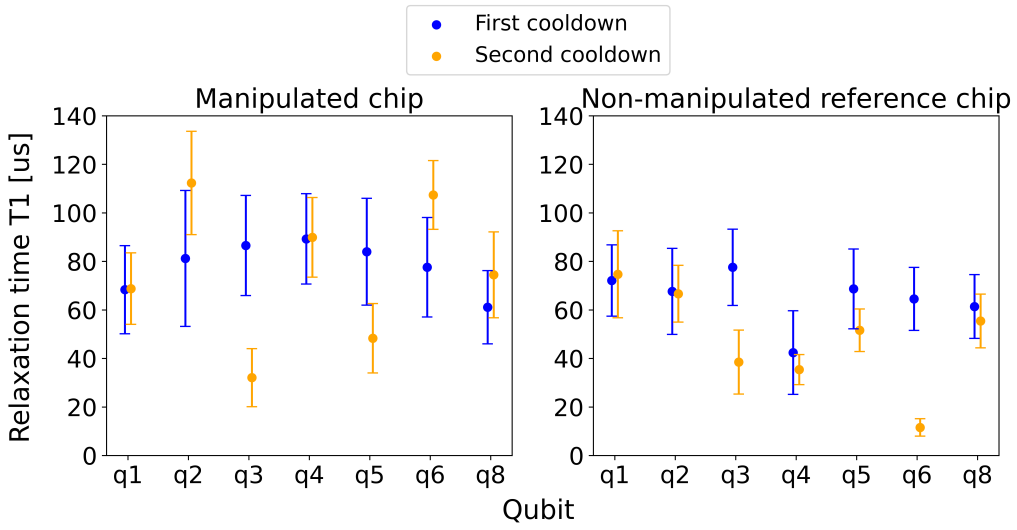


Figure 4.11: Qubit relaxation times T_1 measured for both chips during two consecutive cooldowns. The left panel illustrates the T_1 values for the manipulated chip before (blue dots) and after (orange dots) manipulation. The right panel displays the values for the non-manipulated reference chip. Mean values and standard deviations plotted here are also reported in Tables 4.2 and 4.3.

On the other hand, a critical aspect of this method emerges from Figure 4.10. The plot shows with blue dots the initial characterization of the qubits before manipulating the junctions' normal state resistance R_N versus the qubit plasma frequency f_{01}. The Ambegaokar-Baratoff relation is fitted to these points and depicted as a red dashed line. After the manipulation, the final resistances are measured, allowing to predict the final frequencies using the fitted relation, as explained in Section 3.5.2 and illustrated in Figure 3.8. These are represented by green crosses. Finally, after the second cooldown, the effective final manipulated qubit frequencies are measured. These, along with the presumed final resistance values, are represented by orange stars.

However, the plot clearly indicates that for each manipulated qubit, the predicted final frequency is constantly higher than the actual frequency measured during the second cooldown. This systematic error is in the order of hundreds of MHz, whereas, as discussed earlier in this report, a realistic target for the precision of a practical and useful method should be around 10 MHz [16]. Nevertheless, the systematic nature of the frequency overestimation error suggests that there may still be potential for this method to succeed with appropriate adjustments. In fact, identifying and understanding the source of this systematic error could potentially lead to corrections or adjustments that would still enable the development of a practical and effective frequency tuning method. Therefore, the following paragraphs in this section explore the potential reasons behind this systematic error, propose possible explanations and suggest the steps to verify and address these issues.

Comparing the fluctuations in qubit frequency of the reference chip with the more significant systematic error observed in the frequency prediction, it becomes evident that the error is not attributable to the natural aging of the junctions. Instead, it appears to be a consequence of the manipulation procedure applied to the qubits. From the insights gained from the room temperature studies conducted on similar junctions, a potential explanation for this frequency overestimation error can be found in what was discussed in Section 4.2.1 as the delayed effect.

In fact, to perform this technology demonstration, each qubit within the quantum processor was manipulated and immediately measured to assess the final resistance R_{fin} before moving to the next one. After manipulating all the qubits, the chip was remounted in the dilution refrigeretor, and the R_{fin} values were used to predict the final frequencies of the qubits. For this specific cooldown, approximately two and a half days have passed before the mixing chamber reached the target temperature of $\approx$ 10 mK. However, considering the observations of delayed resistance increase discussed in Section 4.2.1, it is plausible that the resistance of the manipulated junctions continued to change during this period. If this were the case, it could result in an overestimation of the final frequencies of the qubits.

It can be inferred that the critical period during which the resistance of a manipulated junction may continue to drift must end at some point before the device reaches the approximate temperature of 10 mK under vacuum conditions in the di-

lution refrigerator. This conclusion is supported by the observation that, although the frequency of a qubit inside a functioning dilution refrigerator can randomly fluctuate [59], it has never been observed to decrease monotonically in an aging-like manner. Furthermore, during the second cooldown of this technology demonstration, the qubit frequencies did not show any drift towards lower values while the chip was inside the dilution refrigerator.

Additional evidence supporting the criticality of the period between the end of the resistance manipulation and the point when the chip inside the dilution refrigerator reaches approximately 10 mK can be found in the recent follow-up study on the ABAA technique [21]. This study shows that the resistance continues to increase in the 11 days following the manipulation of the qubits. This increase is on the order of more than a few percent relative to the initial resistance, which is significant for the intended application of a precise method to correct for fabrication uncertainties. The authors suggest stopping the manipulation of the junctions before their resistance reaches the target value. By reserving a "global aging budget" (X. Wang et al., 2024) [21] of around 2%, the target qubit frequency can be achieved with higher precision.

5

Conclusion and outlook

In this thesis, a study on the manipulation of the normal state resistance R_N of $Al/AlO_x/Al$ Josephson junctions using electrical DC signals was conducted, with a specific focus on the development of a post-fabrication frequency tuning method. This method aims to enhance the precision of addressing specific qubit frequencies in superconducting quantum processors, mitigating the frequency collision problem by correcting for the high fabrication uncertainties inherent in these devices [14, 15].

The initial phase of the project involved assessing a precise and reliable technique to measure the normal state resistance of these junctions at room temperature. This quantity is directly linked to the plasma frequency f_{01} of the transmon qubit by the Ambegaokar-Baratoff relation (see Equation (2.8)). During this phase, the "back-action" (term introduced in Section 3.2) of the measurement was observed, which manifested as an increase in the resistance value caused by the measurement process itself. To mitigate this unwanted effect, optimal measurement conditions and parameters were determined for the typical automatic probe station setup used in the Quantum Technology Laboratory. It was demonstrated that a measurement current of 40 nA is sufficiently low to have a negligible effect on the resistance value while ensuring the high precision needed for developing a frequency tuning method that allows scaling the number of qubits beyond hundreds of units.

Additionally, the natural aging of these devices was studied for two types of junctions that differ in the thickness of the AlO_x layer due to different fabrication processes. It was observed that thin-oxide junctions are less stable, exhibiting more than 30% increase in resistance within the first two weeks after fabrication. In contrast, thick-oxide junctions proved to be more stable, with an aging-induced resistance increase of only a few percent. It is clear that accounting for aging is important for achieving high frequency precision in superconducting transmon qubits, and the choice of junction type can play a crucial role in this.

The next step involved the development of a manipulation technique to deliberately increase the tunnel resistance of these junctions in a controlled and significant manner. By applying high DC voltage biases at room temperature, substantial changes in the resistance were achieved, with observed increases up to nearly 20% for thin-oxide junctions. This manipulation window demonstrates the potential to correct for fabrication-induced variations on a wafer-level scale [14, 15, 37]. For thick-oxide junctions, which inherently exhibit lower fabrication uncertainties due to their larger junction area [16], the manipulation range achieved also proved sufficient.

An essential finding of this study is the delayed effect in the resistance increase following the manipulation procedure. Observations indicate that the resistance continues to rise over an extended period of time, well beyond the immediate application of the voltage bias. This delayed increase appears to follow a power law, as suggested by both experimental data and recent literature [21]. Although this delayed effect was not extensively studied during this project, the results from the technology demonstration highlight the importance of understanding and controlling this effect to achieve the desired qubit final frequency with precision.

In addition to the experimental work, which was the primary focus of this project, this thesis also explores a theoretical model to understand the mechanisms behind the resistance increase in $Al/AlO_x/Al$ Josephson junctions. A heat transfer simulation using COMSOL Multiphysics estimated the temperature variations during a typical manipulation process, showing an increase of approximately 3 K to 4 K at the hottest point within the junction. This temperature is significantly lower than the hundreds of degrees Celsius required for a notable resistance increase through what is commonly referred to as "thermal annealing" [22, 23]. Thus, localized Joule heating alone cannot explain the observed resistance increase, suggesting that the applied voltage or the resulting electric field play a crucial role in this effect.

Finally, the technology demonstration on actual qubits in a quantum processor further validated the potential of this technology, providing a proof of concept for this frequency tuning method. Since the standard automatic probe station is unable to address individual qubits within a quantum circuit, a new manual setup was specifically designed and implemented. This enabled to individually address a single qubit within an arbitrary quantum circuit, allowing for room temperature measurement and manipulation. The results from the technology demonstration fulfilled the promises by demonstrating the capability to effectively change the qubit frequencies by several hundred megahertz, without directly compromising the lifetimes. This important outcome establishes the success of the experiment and provides a solid proof of concept for the frequency tuning method.

However, the frequency predictions based on the final resistances measured immediately after the manipulation resulted in a systematic overestimation of the final qubit frequencies. This error could undermine the effectiveness of the manipulation for frequency adjustment purposes. Given the observations of the delayed resistance increase, it is plausible that the resistance continued to rise immediately after the manipulation until the chip reached low enough temperatures inside the dilution refrigerator. To confirm this hypothesis and improve the accuracy of the tuning method, further studies on the delayed resistance increase are needed.

In conclusion, this thesis demonstrates a promising method for fine-tuning the frequencies of superconducting transmon qubits by manipulating the normal state resistance of their Josephson junctions. The induced frequency shift of several hundreds of megahertz demonstrates the capability to correct for typical fabrication uncer-

tainties on a wafer-level scale [14, 15]. This makes the method's target frequency precision the only limiting factor for accurately targeting frequencies in superconducting quantum processors, holding the promises to scale the number of qubits by addressing the frequency collision problem.

Future work should prioritize achieving high precision in the frequency manipulation. In fact, in this project, the precision assessment of the manipulation was not the primary focus. This initial study aimed to establish a fundamental understanding of how control parameters influence the resistance increase and to demonstrate a sufficiently large manipulation range to correct for typical fabrication uncertainties [14, 15]. This was accomplished through a step-like manipulation procedure. However, for a practical and precise frequency tuning method, a different approach is needed. Moving towards DC pulses with alternating polarization, similar to the ABAA technique, has already proven promising by providing a wider manipulation range during the technology demonstration. Additionally, this technique allows for continuous monitoring the resistance evolution between these pulses, enabling the interruption of the manipulation once the resistance reaches the target value. This could significantly improve the precision of the manipulation technique.

Another related critical aspect to address is the delayed resistance increase after manipulation. Systematic studies are required to better understand the magnitude and time scale of this effect for the specific type of junctions. Adjusting the manipulation procedure to account for this delayed effect is crucial. One potential approach is to incorporate a "global aging budget" (X. Wang et al., 2024) [21] calculated based on the junction type and the estimated time before cooldown. This adjustment would help mitigate the delayed resistance increase and further improve the accuracy of the frequency predictions.

By addressing these aspects, future research can refine and optimize the frequency tuning method developed in this thesis, making it a fundamental step in the production of superconducting quantum processors with more than hundreds of qubits. This will effectively mitigate frequency collision problems and advance the scalability and reliability of superconducting quantum computers.

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A

Appendix A

A.1 Qubit characterization procedure

In this Appendix, the procedure followed to characterize the qubits for the technology demonstration is outlined. The aim is not to detail the various experiments and calibrations performed, but rather to list them and briefly explain their purposes. For a comprehensive description of the typical characterization procedure of these superconducting quantum devices, along with the necessary theoretical background, the interested reader is referred to Chapter 3 in reference [60]. Additionally, for the scope of this master's thesis project, the characterization was limited to assess the qubit plasma frequency f_{01} and the relaxation time T_1.

To perform the characterization, the device described in Section 3.5.1 is mounted in a sample holder that is attached to the mixing chamber of a dilution refrigerator and connected to room temperature electronics for control and measurements. A simplified schematic of the cryogenic measurement setup is illustrated in Figure A.1.

The list of experiments performed to characterize the qubits is the following:

1. **Resonator spectroscopy.** The first step of qubit characterization involves performing resonator spectroscopy at various power levels to observe the resonator "punch-out" effect [60]. Observing this effect ensures that the resonator is coupled to a two-level system and confirms whether the qubit is "alive" or not. Additionally, this experiment is used to calibrate the optimal readout signal amplitude. By choosing the maximum amplitude that still allows the measurement of the resonance at the "dressed" resonator frequency $f_{\text{res}_{\text{"dressed"}}}$ in the dispersive regime [12], the signal-to-noise ratio (SNR) of the qubit readout is maximized.

2. **Qubit (two-tone) spectroscopy.** The next step involves performing qubit spectroscopy to estimate the qubit plasma frequency f_{01}^*. This experiment requires simultaneously applying a signal with a varying frequency to excite the qubit and a second signal at $f_{\text{res}_{\text{"dressed"}}}$ to read out the resonator. The second signal is applied with the amplitude that was previously calibrated to ensure high SNR.

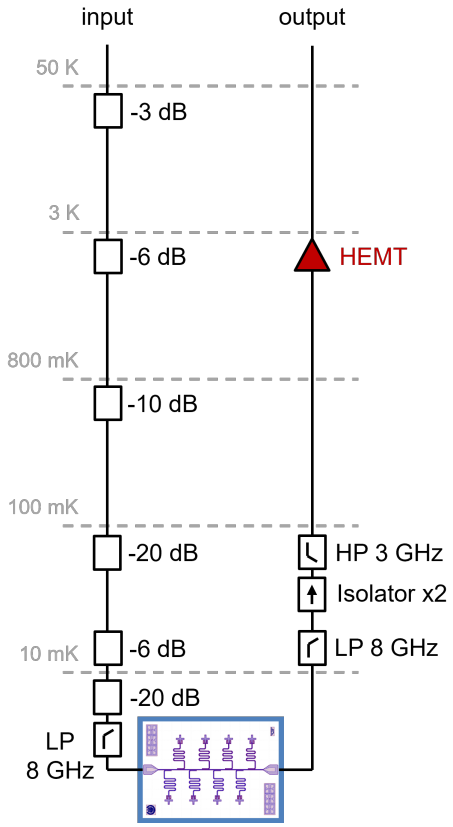


Figure A.1: Simplified schematic of a typical wiring diagram for a dilution refrigerator used to measure a superconducting quantum processor. For a more detailed description of the setup and electronic components, refer to Chapter 3 in reference [60].

3. **Rabi experiment.** The Rabi experiment is then conducted to roughly calibrate the π-pulse. The qubit is excited with a pulse at f_{01}^{*} of fixed duration $t = 100$ ns and is immediately read out through the resonator. This sequence is repeated while incrementally increasing the amplitude of the signal to excite the qubit. This process allows to reconstruct the typical Rabi oscillation pattern [52] and helps estimate the signal amplitude needed to perform a π-pulse on the qubit.

4. **Ramsey interferometry .** With the π-pulse roughly calibrated in the previous step, the Ramsey interferometry experiment is performed to measure the qubit plasma frequency with higher precision. The pulse sequence for this experiment is illustrated in Figure A.2.

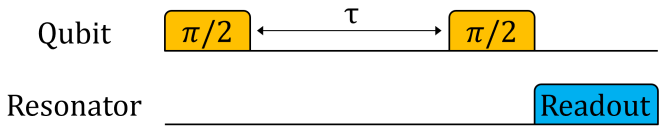


Figure A.2: Pulse sequence for the Ramsey interferometry experiment. First, a $\pi/2$-pulse is applied to the qubit to place its Bloch vector on the equator of the Bloch sphere. The qubit is then allowed to "freely" evolve for a variable time τ, followed by the application of another $\pi/2$-pulse. Finally, a readout pulse on the resonator measures the qubit's final state. The qubit population is obtained by repeating this sequence 500 times and averaging the results.

To obtain a more accurate estimation of the qubit plasma frequency, two Ramsey experiments are performed using $\pi/2$-pulses detuned by $\pm$ 1 MHz from the f_{01}^* value estimated with the two-tone spectroscopy. The characteristic Ramsey fringes [52] obtained from these experiments oscillate at a frequency that reflects the relative detuning Δ between the pulses' frequency and the true qubit plasma frequency. Knowing the two reference frequencies used in the Ramsey experiments and the relative detuning Δ from the actual f_{01}, this value can be determined with much greater precision. The f_{01} values reported in this thesis have been measured using this technique.

5. **π-pulse calibration.** Once the plasma frequency is more precisely determined, the amplitude of the π-pulse can be finely adjusted to accurately calibrate the gate. This is achieved by conducting Rabi experiments varying the pulse amplitude for 1, 3, 5, and 7 concatenated π-pulses. Repeating the π-pulse an odd number of times should bring the qubit state back to the excited state. Therefore, with this error amplification technique, the amplitude value at which the different Rabi oscillations show a common peak in qubit population represents the finest calibrated π-pulse amplitude.

6. **T_1 measurement.** Finally, the relaxation time T_1 is measured using the pulse sequence illustrated in Figure A.3. A typical result obtained from a T_1 measurement is shown in Figure A.4. The relaxation time T_1 is extracted by fitting the data to an exponential decay curve, with the inverse of the decay constant representing the T_1 value. The T_1 values reported in this thesis have been obtained by repeating this experiment 60 times and calculating the average and standard deviation of the resulting distribution.

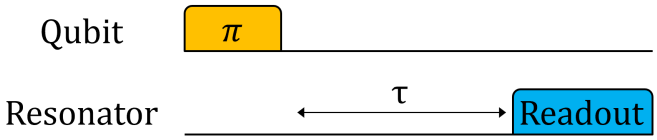


Figure A.3: Pulse sequence for the T_1 measurement. A π-pulse is applied to bring the qubit to the excited state. After a varying time τ, a pulse on the resonator measures the qubit's final state. The qubit population is obtained by repeating this sequence 500 times and averaging the results.

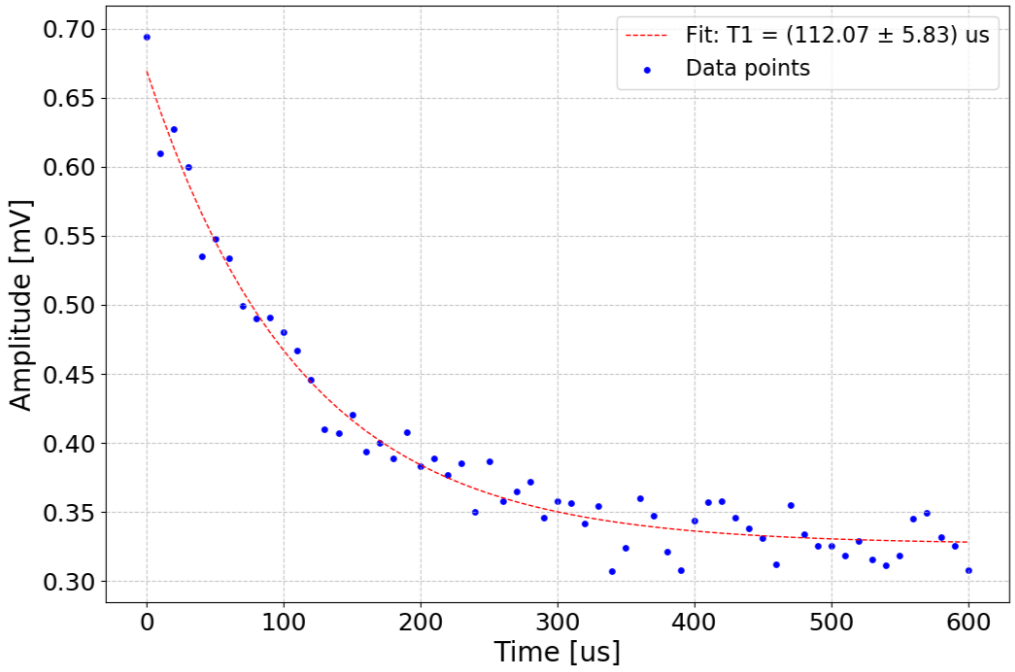


Figure A.4: Typical result of a T_1 measurement. The blue dots represent the qubit population after applying the gate sequence illustrated in Figure A.3, which is reflected in the amplitude of the transmitted readout signal [52]. These data points are fitted to an exponential decay curve $y = A \cdot e^{x/T_1}$ to extract the qubit relaxation time. The uncertainty value provided is the mean-square error of the fit.

B

Appendix B

B.1 Supplementary figures on natural aging

In this Appendix, supplementary plots related to the aging measurements are provided for completeness. These plots depict data for all tested current levels. A description of the experiment and a discussion of the results can be found in Section 4.1.2.

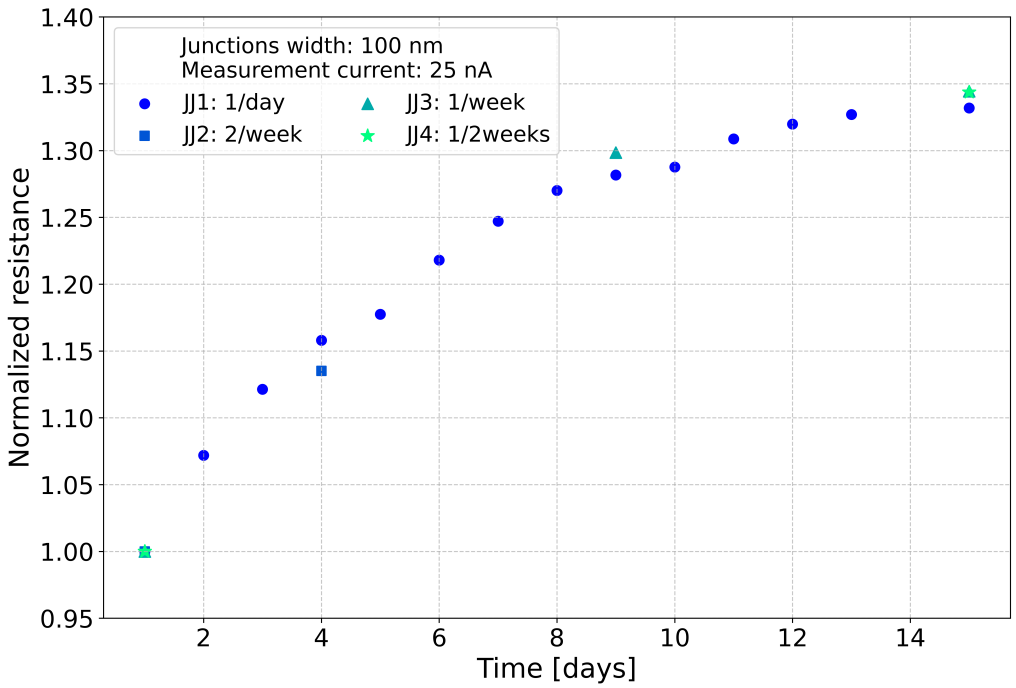
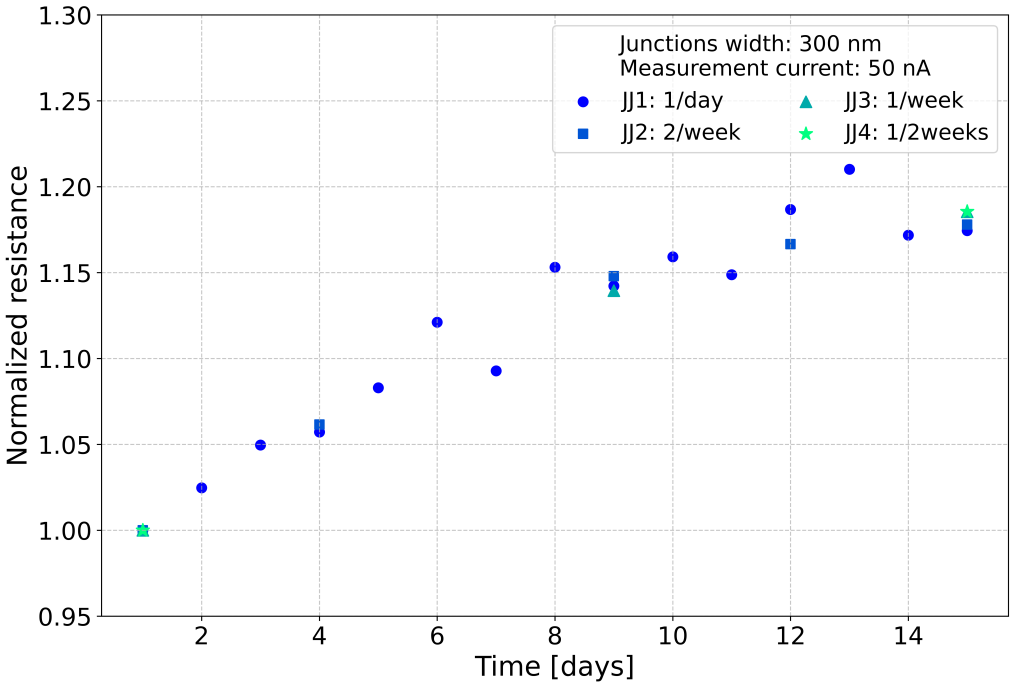
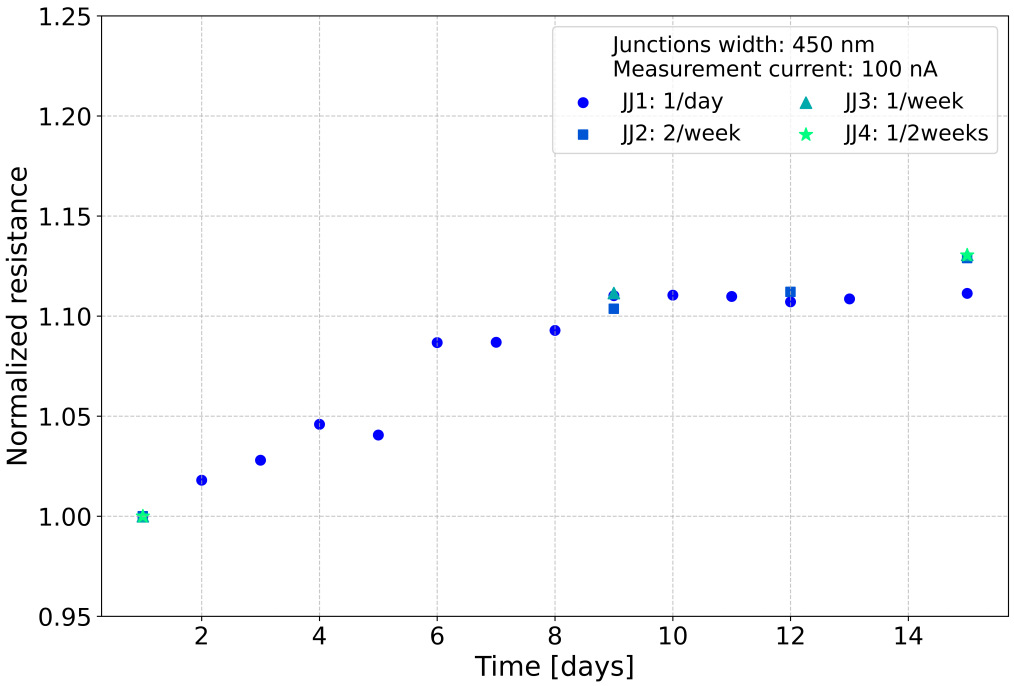


Figure B.1: Aging measurements on thin-oxide junctions. Nominally identical, newly fabricated devices are measured over two weeks at different time intervals. In the plot, data points from different devices are distinguished by color and shape. Four 100 nm width junctions are measured with a maximum current of 25 nA.

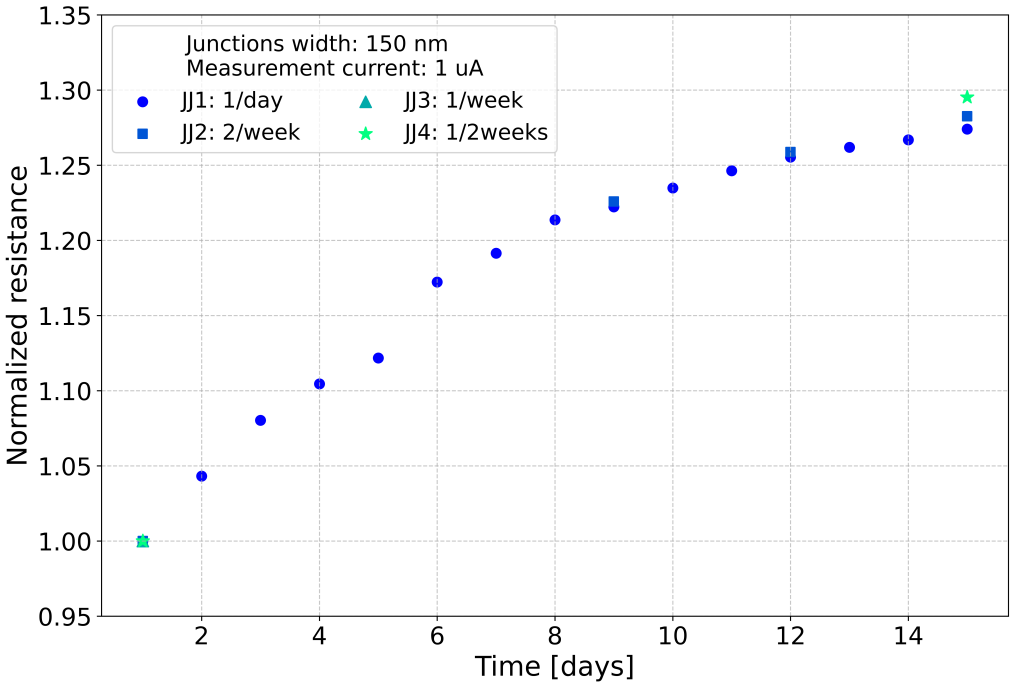


(a)

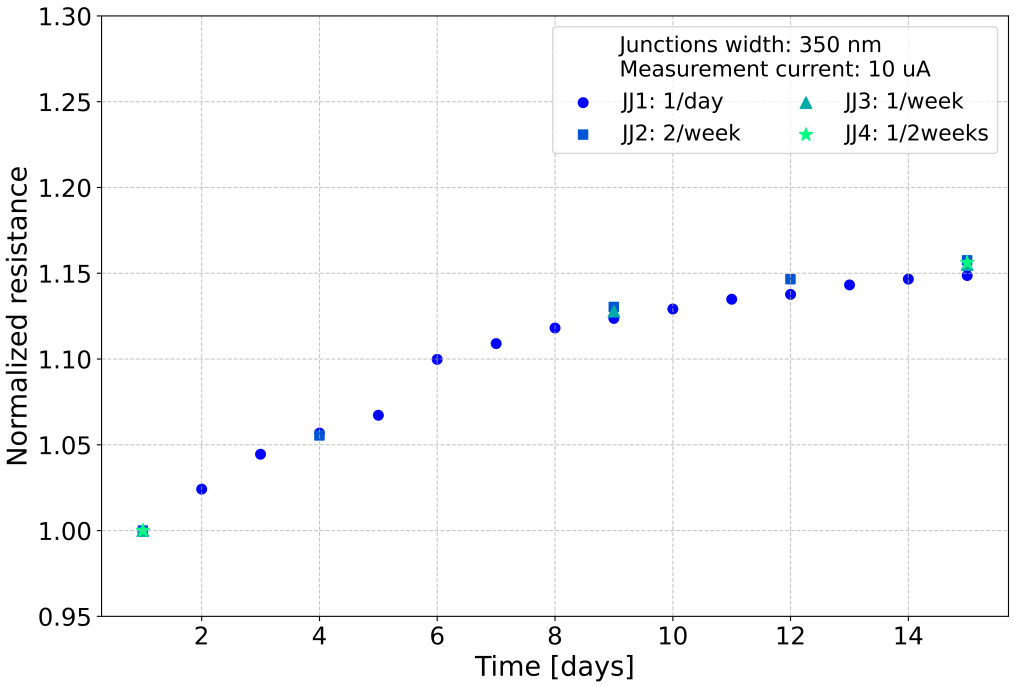


(b)

Figure B.2: Aging measurements on thin-oxide junctions. Nominally identical, newly fabricated devices are measured over two weeks at different time intervals. In the plot, data points from different devices are distinguished by color and shape. **(a)** Four 300 nm width junctions are measured with a maximum current of 50 nA. **(b)** Four 450 nm width junctions are measured with a maximum current of 100 nA.

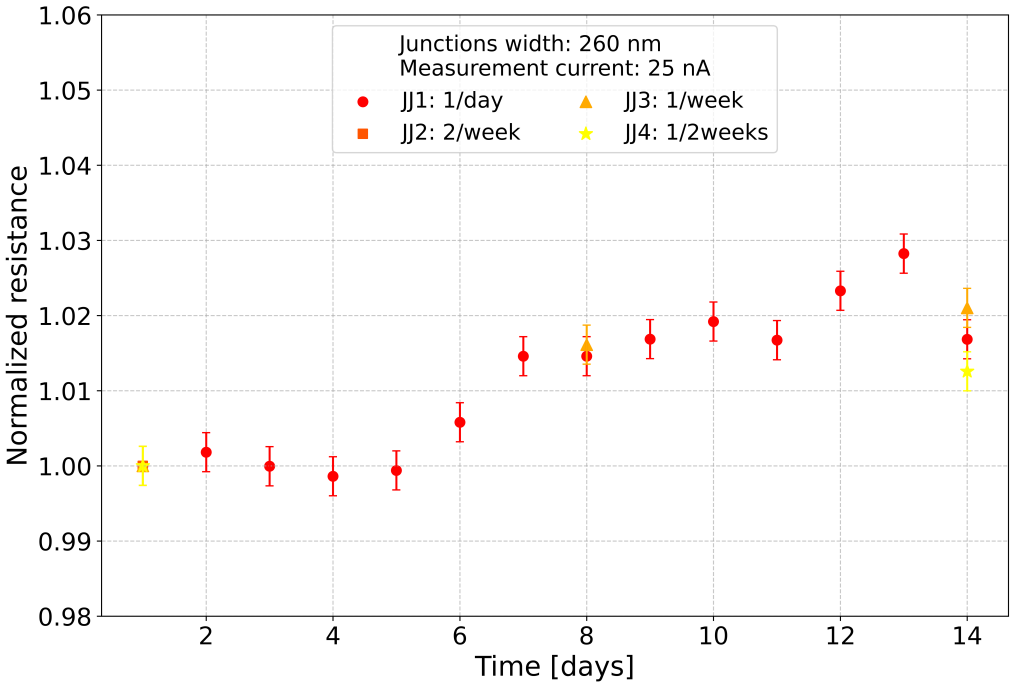


(a)

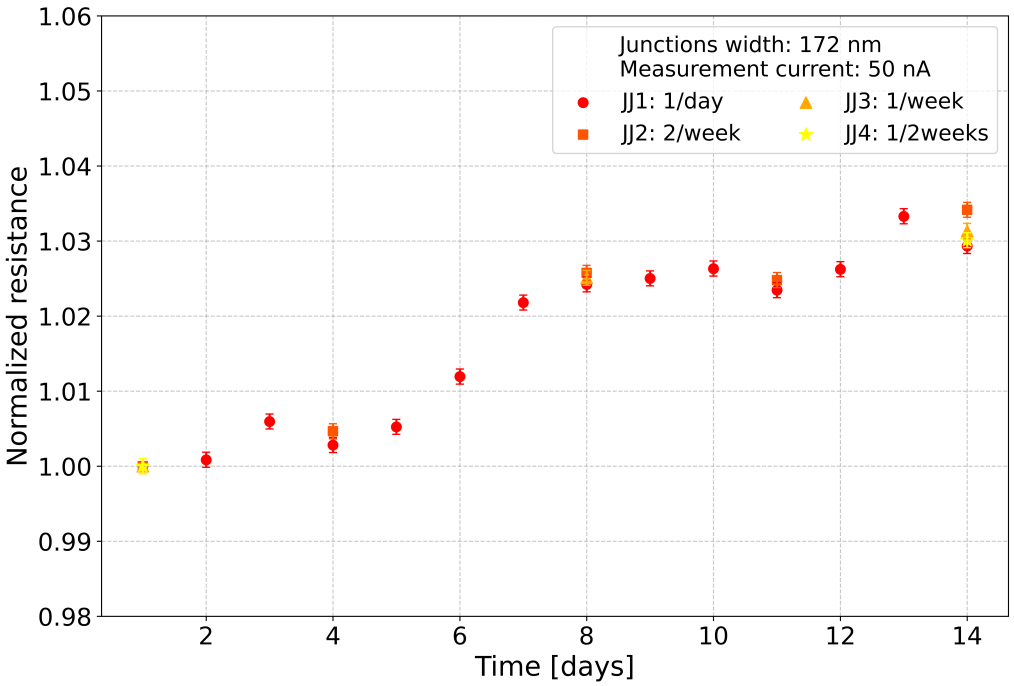


(b)

Figure B.3: Aging measurements on thin-oxide junctions. Nominally identical, newly fabricated devices are measured over two weeks at different time intervals. In the plot, data points from different devices are distinguished by color and shape. **(a)** Four 150 nm width junctions are measured with a maximum current of 1 µA. **(b)** Four 350 nm width junctions are measured with a maximum current of 10 µA.

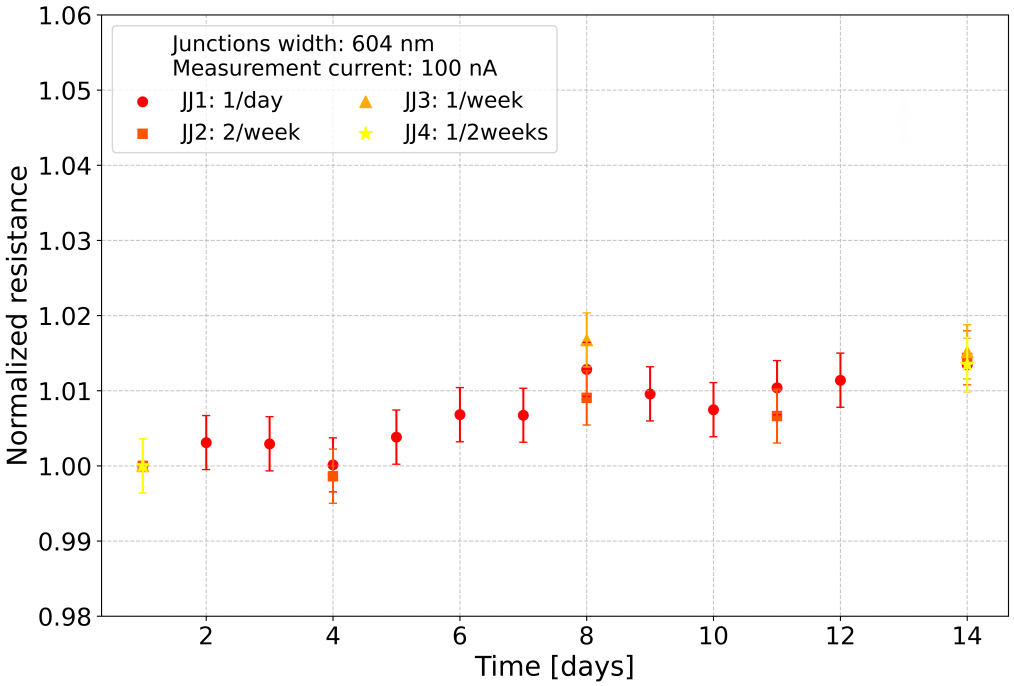


(a)

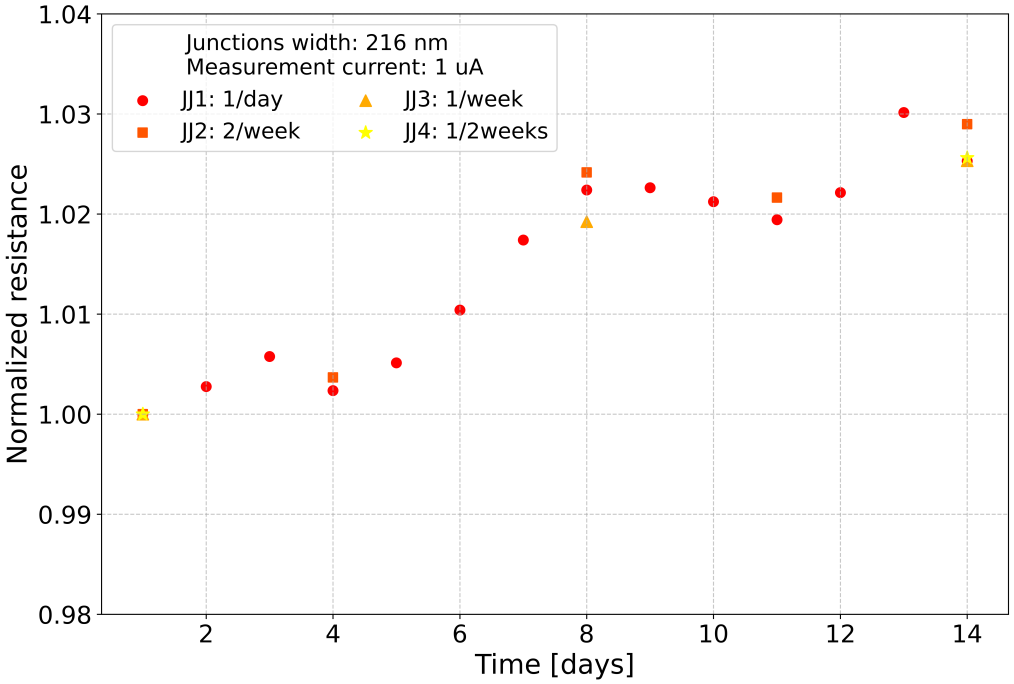


(b)

Figure B.4: Aging measurements on thick-oxide junctions. Nominally identical, newly fabricated devices are measured over two weeks at different time intervals. In the plot, data points from different devices are distinguished by color and shape. The error bars indicate the uncertainty relative to the specific measurement conditions. **(a)** Four 260 nm width junctions are measured with a maximum current of 25 nA. **(b)** Four 172 nm width junctions are measured with a maximum current of 50 nA.



(a)



(b)

Figure B.5: Aging measurements on thick-oxide junctions. Nominally identical, newly fabricated devices are measured over two weeks at different time intervals. In the plot, data points from different devices are distinguished by color and shape. **(a)** Four 604 nm width junctions are measured with a maximum current of 100 nA. The error bars indicate the uncertainty relative to the specific measurement conditions, which is appreciable only in this case and thus plotted. **(b)** Four 216 nm width junctions are measured with a maximum current of 1 µA.

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