CHALMERS
UNIVERSITY OF TECHNOLOGY

Comparison of High-Power DC-DC Converters for Solar Applications with Respect to Efficiency and Chip-area

Master's Thesis in Electric Power Engineering

BABAK ALIKHANZADEHALAMDARI

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

Comparison of High-Power DC-DC Converters for Solar Applications with Respect to Efficiency and Chip-area

Babak AlikhanzadehAlamdari

CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2018

Comparison of High-Power DC-DC Converters for Solar Applications with Respect to Efficiency and Chip-area
Babak AlikhanzadehAlamdari

Supervisor: Amin Bahmani, Department of Electrical Engineering
Examiner: Torbjörn Thiringer, Department of Electrical Engineering

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Typeset in LaTeX
Gothenburg, Sweden 2018

Comparison of High-Power DC-DC Converters for Solar Applications with Respect to Efficiency and Chip-area

Babak AlikhanzadehAlamdari
Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology

Abstract

This thesis is intended to analyze and compare the efficiency of the conventional 2L-DAB with the so-called Multi-Level DAB (ML-DAB) and three-Level DAB (3L-DAB) for the solar applications. The latter features from the three-level legs both on the LV and the MV sides; while, the former is a combination of the 2L-legs on the LV side bridge and the NPC legs on the MV side bridge.

The converters are rated for $1MW$ power with the LVDC-link and the MVDC-link voltages of $1.3kV$ and $16kV$ respectively. The SiC MOSFETs are utilized as the power switches to ensure low switching losses in high switching frequencies. The semiconductor chip-area based comparison algorithm is applied to have a fair comparison between the topologies. The definition of average efficiency for the European solar mix is employed to make the comparison specific to the solar applications. The switching frequency of the converters is swept from $10kHz$ to $80kHz$ to investigate its effect on the performance of the converters. The chip-area of the MOSFETs are also varied to explore the efficiency variations with the chip-area change and therefore, the semiconductor costs.

It has been shown that for the specified modulation parameters and the same operating junction temperature , the 2L-DAB has higher full-load efficiency while, it requires lower chip-area than the ML-DAB for all switching frequency ranges. It has also been demonstrated that for the same amount of investment on the semiconductors, the 2L-DAB can achieve a higher efficiency and a lower operating temperature for the MOSFETs compared to the ML-DAB. It was also shown that by less than 70% increase in the required chip-area, the full-load efficiency and the average efficiency for European solar mix of all converters can increase more than 2% and 0.7% respectively for all switching frequency ranges.

Keywords: SST, DC-DC converter, DAB, NPC, Efficiency, Chip area, PV.

Acknowledgements

I would like to express my profound gratitude to my supervisor, Dr. Amin Bahmani and my examiner, Prof. Torbjörn Thiringer for their valuable guidance that steered me on the right track during the thesis work.

Babak AlikhanzadehAlamdari, Göteborg, 2018

Contents

1
Introduction

1.1 Problem Background

The Solid-State-Transformer (SST), also referred as the intelligent universal transformer or the power electronic transformer, is a high-power high-frequency isolated AC-AC converter which provides peripheral functionalists rather than merely voltage level transformation. It provides the possibility to mitigate various power quality issues through advanced control strategies. Availability of the DC link along with the AC terminals facilitates the connection of various distributed energy resources which is crucial for the future grid [1].

Figure 1.1 shows the essence of the SST. The front-end converter transforms the power-frequency MVAC input to a MVDC output. In the second stage, a DC-DC converter which incorporates a high-frequency medium-voltage transformer and the power electronic switches performs the isolation and voltage transformation task in the frequency range of tens of kilohertz. Due to the high-frequency range of the intermediate stage, the weight and the volume of the passive components (mainly the medium-voltage transformer) could be reduced considerably; which makes the SST a promising substitute for the conventional transformers especially in the weight-sensitive applications [1], [2]. Finally, in the third stage, the voltage is shaped back to 50Hz to feed the loads.

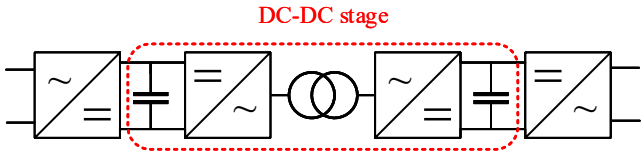


Figure 1.1: General configuration of the solid-state-transformer

The annual energy content of the solar radiation on earth is estimated to be 1800 times the global energy consumption. The solar energy is one of the primary renewable energy resources and its direct harvesting has undergone enormous growth and investment in the last decades. From the year 2000 and on-wards the global installed solar photovoltaic (PV) capacity has experienced an exponential growth [3]. The largest installed PV power plant in 2016, was Yanchi solar PV station located in China with a total capacity of 1GW [4]. However one of the significant challenges of the PV deployment is its low load factor and enormous capital costs [3], encouraging

engineers to design systems with a maximum output from the installed capacity.

The backbone of the PV parks is the collector grid structure. Figure 1.2 depicts the two possible collector grid configurations, namely the DC configuration and the AC configuration. The DC collector grid configuration outperforms the AC configuration by increasing the overall annual energy yield of the PV farms [5], [6].

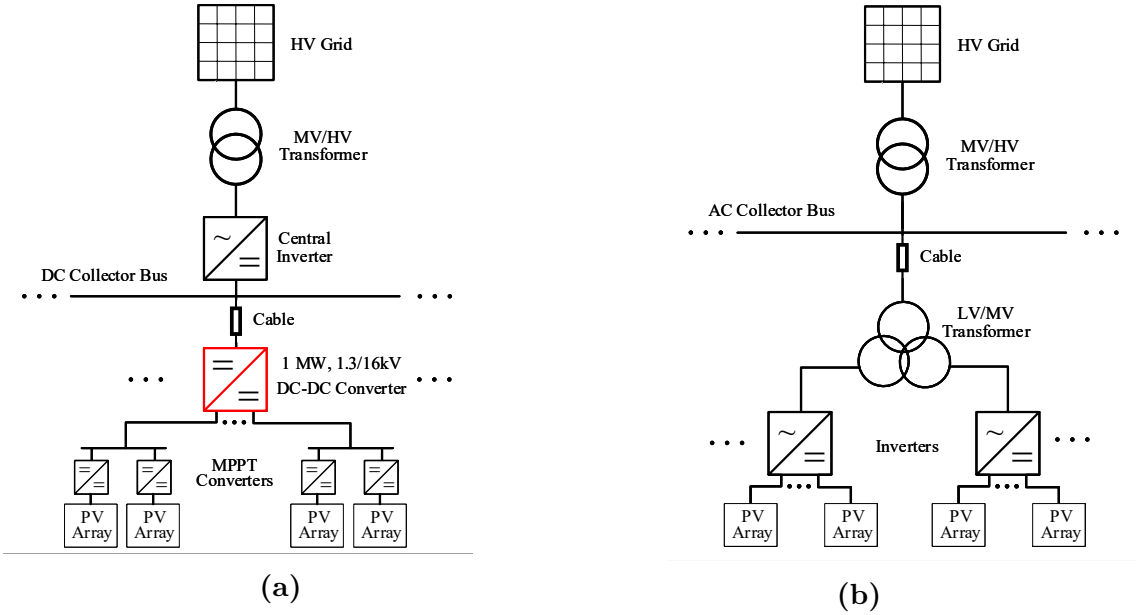


Figure 1.2: Collector grid configurations for the large PV parks (a) DC collector grid, (b) AC collector grid

As can be seen, the DC collector configuration consists of local maximum power point tracking converters, a DC-DC converter, and a central MV inverter. In contrast to the conventional AC configuration, the LV/MV transformer is incorporated as a part of the DC-DC converter indicating a direct correlation between the SST concept and the DC collector configuration for the PV parks. The main functionality of the DC-DC stage is the voltage transformation and the galvanic isolation. Its efficiency will directly affect the total efficiency of the system; Therefore, it is of crucial importance to have a highly efficient DC-DC converter.

1.2 Literature Review

There are various layouts that could be used to implement the DC-DC converter of the DC collector grid configuration. One of the promising candidates is the conventional dual-active-bridge with the two-level bridge legs [7]. It has been used in the DC-DC stage of the solid-state-transformers for the smart grid and the substation applications [2].

Considering the high power, the medium voltage and the high-frequency operation of the DC-DC converter, one of the major challenges is the ratings of the switches [8]. To cope with the medium voltage level, one of the possible solutions would be the series connection of the low-voltage switches [2]. However, this introduces additional levels of complexity to the system [8].

The NPC-based DAB for the solar applications has been proposed in [9]. This topology can potentially eliminate the requirement for the series connection of the power devices due to its inherent lower blocking voltage requirements on the MV side switches. However, it requires a higher number of switches on each leg compared to the conventional DAB. It becomes evident that a fair and comprehensive criterion is required to be able to compare the performance of different converter topologies. Therefore, a literature review on the topology comparison of various converters was performed to figure out a suitable comparison basis.

In [10], the authors have compared two converter topologies for the medium-voltage grid-connected applications. The semiconductor losses have been split into the switching and the conduction losses. The overall losses are also presented, and the efficiency of the converters are compared. An economic evaluation has been performed for the components, and the prices of the semiconductors based on the installed-switch-power are presented for each topology and included in the comparison.

In [11] and [12], the total installed switch power is used as a comparison basis for the switches where it is determined iteratively to limit the junction temperature of the mostly stressed switch in the worst case operating point to a maximum value. The rated semiconductor currents were adjusted in each step along with the switching and the conduction losses to reach the maximum junction temperature. The topologies have been compared based on the semiconductors and the passive components costs and the efficiency at various switching frequencies.

The main shortcoming of methods mentioned above is that the semiconductor chip-area requirement of topologies is not considered in the comparison. The total semiconductor chip-area is introduced in [13]–[15], as a figure-of-merit (FOM) to contrast different topologies with one another. The so-called semiconductor chip-area-based converter comparison (SABC), provides the possibility to select the optimal semiconductors with respect to the topology and the operating point. Thus, paving the way for a fair comparison of different topologies.

1.3 Purpose of Thesis

As mentioned before, the capital costs of the PV farms are enormous, and inexpensive converter layouts with high efficiency are favorable. This document is intended to provide a fair comparison between the conventional DAB, and the NPC-based DABs with respect to the efficiency, the total chip-area requirement of the switches,

and the total semiconductors costs.

2

Chip-Area Based Comparison and Semiconductors

2.1 Power Semiconductors Modeling

To be able to analyze the losses of the power semiconductor switches and thereby the converter efficiency, a comprehensive modeling of the switches is required. Therefore, the utilized semiconductors will be modeled both from an electrical and a thermal point of view in this chapter. A vital source of information for the following chapter has been [16].

2.1.1 Power Semiconductor Losses

The semiconductor losses can be divided into two parts, namely: the switching losses P_{sw}, and the conduction losses P_{cond} which sums up to

$$P_{tot} = P_{cond} + P_{sw} \tag{2.1}$$

The switching loss is normally given as switching transitions energy in the manufacturer datasheets. It can be either presented in the form of total switching energy loss, denoted here by E_{tot}, or subdivided into the turn-on energy loss E_{on}, and the turn-off energy loss E_{off}. The switching energy loss is a function of the junction temperature T_J, the switched current i_{on}, and the blocking voltage v_{block} which can be expressed as

$$E_{tot}(i_{on}, v_{block}, T_J) = E_{on}(i_{on}, v_{block}, T_J) + E_{off}(i_{on}, v_{block}, T_J) \tag{2.2}$$

Then the switching power loss can be obtained by multiplying the switching frequency f_{sw}, with the total switching energy loss as

$$P_{sw} = f_{sw} E_{tot}(i_{on}, v_{block}, T_J) \tag{2.3}$$

On the other hand, the conduction power losses can be calculated using the forward characteristics voltage u_F, which can be extracted from the forward characteristic figure in the datasheet of respective devices. The forward characteristics voltage is a function of the junction temperature T_J, the forward voltage drop U_F, and the

differential forward resistance r_F as

$$u_F(i, T_J) = U_F(T_J) + r_F(i, T_J)i \tag{2.4a}$$
$$P_{cond} = u_F(i, T_J)i \tag{2.4b}$$

2.2 Semiconductor Chip-Area Based Comparison

Different converter topologies can be compared based on the utilized semiconductors in three general methods. In the first method, a common semiconductor device which fulfills the ratings of both converters is selected. In this method, the switch will be over-dimensioned for one of the topologies; which is not favorable from the cost point of view and will not provide a fair comparison bases. In the second method, the ratings of the converters are adapted based on the operation point to limit the maximum junction temperature to the nominal maximum value [13]. In the third method [11], the installed switch power in each topology is adapted to limit the temperature of the most stressed switch in each topology to the maximum junction temperature. The shortcomings of the methods mentioned above are that either the semiconductor chip-area requirement of the topologies are not considered in the comparison, or the chip-area of the switches are considered to be equal; which means that the switches are not optimized based on their position in the electrical circuit.

The SABC method introduced in [13], [15], [16] ensures that the chip-area requirement of the individual semiconductor device is minimized for the converter topology and the operating point in a way that the maximum junction temperature of each device remains below a predefined value.

2.2.1 The SABC Algorithm

The SABC algorithm consists of three steps which have been illustrated in Figure 2.1. In the first step, the topology of the converter, the operating point, a comprehensive chip-dependent loss model, a thermal model and an electrical model of the semiconductors are provided as the inputs of the algorithm. Then, the minimum possible chip-area is provided as the first iteration chip size for all of the switches to initialize the simulation.
The calculation step is the key part of the algorithm where, iteratively, the semiconductor losses and the junction temperature of each switch are calculated. After each iteration, the junction temperature of each switch is compared with a predefined maximum value. If the junction temperature is below its maximum value, the loop will stop for that switch. Otherwise, the chip-area will be increased and based on the semiconductor data provided to the algorithm in the first step, a new switch model will be generated, and the loop will start again from the beginning.
In the last step after convergence of the algorithm, the total chip-area of the converter, the switching and the conduction losses and the efficiency of the converter are calculated based on the final switch model.

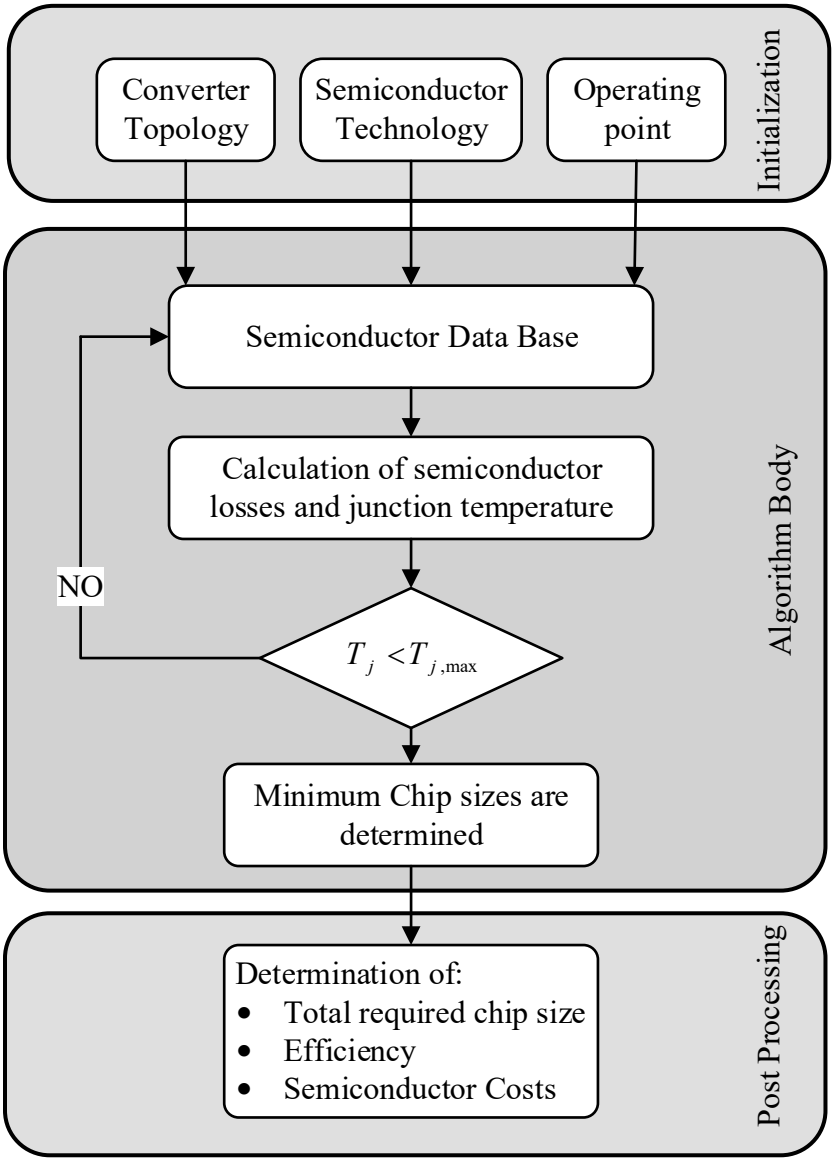


Figure 2.1: The flowchart of the SABC algorithm

2.2.2 Binary Search Algorithm

Although the main concept of the SABC algorithm was introduced in Section 2.2.1, it suffers from a slow simulation speed. For instance, consider a case where the chip requirement of a switch is $20mm^2$, the minimum allowable chip size is $10mm^2$ and the chip size increment is $0.01mm^2$. It will take 1000 iterations for the algorithm to converge. To overcome this issue, one can somehow estimate the minimum required chip size of each switch close to the expected value and initialize the algorithm with the calculated values [16]. Another alternative would be the so-called binary search algorithm. This algorithm compares the middle point of the interval with the target value. If these values do not match, the half of the interval which the target value cannot lie in is eliminated from the search domain, and the algorithm keeps iterating on the other half until it converges. This algorithm reduces the number of required

iterations form n to $log_2(n)$ and also eradicates the need for the chip size estimation.

2.2.3 The European efficiency

Even though the SABC provides an appropriate basis for the converters topology comparison, another criterion is required to push the envelope of the comparison and form it specifically for the PV applications. Due to the intermittency of the solar radiation, PV farms operate below their rated power most of the time. Therefore, the so-called average efficiency for the European solar mix is considered to compare the overall efficiency of the converters [17]. The average efficiency for the European solar mix η_{EU}, is defined as

$$\eta_{EU} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.1\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \tag{2.5}$$

where the subscripts denote the percentage of the nominal power.

2.3 Semiconductors Models

The main requirements of the SABC algorithm is a comprehensive electrical model and a thermal semiconductor model which can be expressed as a function of the chip-area to perform the chip variation in the second step of the algorithm. Therefore, switches with various chip sizes should be modeled based on the data either obtained from experimental tests or manufacturer datasheets. Since performing the experimental tests are out of the scope of this thesis, attempts have been made to find switches with the same semiconductor technology and different current ratings where the chip size is included in the datasheet so that the chip dependent model could be created. Four SiC-MOSFETs, namely C2M0160120D, C2M0080120D, C2M0040120D, and C2M0025120D [18]–[21],from CREE/Wolfspeed with the blocking voltage of 1200 volts were selected. These devices feature the same semiconductor technology and the same package of TO-247-3. The bare die products CPM2-1200-0160B, CPM2-1200-0080B, CPM2-1200-0040B, and CPM2-1200-0025B are the same switches without the packaging which also include the chip-area information in their respective datasheets [22]–[25].

2.3.1 1200V SiC MOSFET Model

Availability of the switches with four chip-areas and the same switch technology eases the modeling of the switch. The data points are extracted from the datasheet graphs with a high precision employing image processing methods. Afterwards, the curve fitting tool of MATLAB was used to derive the current and the temperature dependency of various switch parameters. Since, the equations modeling the characteristics are complicated, presenting the detailed equations here is irrelevant and only general functions are denoted in the upcoming sections.

2.3.1.1 Conduction States

Since the SiC-MOSFET is a unipolar device with an intrinsic anti-parallel diode, three different conduction states are expected.

1. MOSFET Forward Conduction

In this conduction state, $V_{DS} > 0$ and the MOSFET is forward biased. If V_{GS} become positive, the current will flow only through the MOSFET channel from the drain to the source. The forward characteristic of the MOSFET $u_{S,F}$, can be modeled as

$$u_{S,F}(T_J, A_{chip}, i_{S,F}) = r_{S,F}(T_J, A_{chip}, i_{S,F}) i_{S,F} \tag{2.6}$$

where $i_{S,F}$ denotes the MOSFET forward current. T_J is the junction temperature, and A_{chip} and $r_{S,F}$ are the switch chip-area and the forward on-resistance of the MOSFET respectively.

2. Diode Forward Conduction

In this state, the intrinsic body diode is conducting, and V_{GS} is negative. The current flows from the source to the drain and the MOSFET channel is off. The diode forward characteristic $u_{D,F}$, can be modeled as a function of the junction temperature, the diode forward current $i_{D,F}$, and the switch chip-area as

$$u_{D,F}(T_J, A_{chip}, i_{D,F}) = U_{D,F}(T_J) + r_{D,F}(T_J, A_{chip}, i_{D,F}) i_{D,F} \tag{2.7}$$

where $U_{D,F}$ and $r_{D,F}$ are the forward voltage drop and the forward on-resistance of the body diode respectively.

3. MOSFET Reverse and Diode Forward Conduction

In the third quadrant, V_{GS} is positive, and the MOSFET channel is turned on. The current direction is from the source to the drain so that it can flow from both the MOSFET channel and the anti-parallel body diode. The third quadrant characteristic $u_{3rd-quad}$, can be modeled as

$$u_{3rd-quad}(T_J, A_{chip}, i_{S,R}) = r_{3rd-quad}(T_J, A_{chip}, i_{S,R}) i_{S,R} \tag{2.8}$$

where $i_{S,R}$ is the source-to-drain current, and $r_{3rd-quad}$ denotes the third quadrant resistance of the MOSFET.

2.3.1.2 Switching Losses

The turn-off and the turn-on loss of the MOSFET can be expressed in the form of functions depending on the semiconductor chip-area, the MOSFET switched forward current, the junction temperature, and the switched voltage as

$$E_{S,on} = E(T_J, A_{chip}, i_{S,F}, u_{S,F}) \tag{2.9a}$$
$$E_{S,off} = E(T_J, A_{chip}, i_{S,F}, u_{S,F}) \tag{2.9b}$$

2.3.1.3 Thermal Model

The losses occurring in the switch increase the junction temperature which in turn will affect the switch's behavior. The thermal model of the MOSFET can be represented by the equivalent thermal impedance. So, it is required to model the junction-to-ambient thermal impedance $Z_{th,ja}$, as a function of the chip-area, to be able to emulate the thermal behavior of the MOSFET. The $Z_{th,JA}$ can be subdivided into three thermal impedances namely the junction-to-case thermal impedance $Z_{th,JC}$, the case-to-sink thermal impedance $Z_{th,CS}$, and the sink-to-ambient thermal impedance $Z_{th,SA}$.

The $Z_{th,JC}$ can be extracted from the manufacturer datasheets and will be discussed in details in the following. However, implementation of the $Z_{th,CS}$ and the $Z_{th,SA}$ demands modeling of a cooling system which can dissipate the losses reasonably. The problem can be turned around if it is considered that the cooling system has been designed in a way to maintain the heat sink temperature at a constant value $T_h = 80°C$ [10]–[12]. In this way the $Z_{th,SA}$ can be eliminated from the model. Also the $Z_{th,CS}$ can be removed from the impedance network with the assumption that the respective values are small and tolerating the consequent errors. One of the possible errors could be a relatively low junction temperature of the heavily loaded switch due to neglecting the effect of the local temperature rise.

The transient thermal impedance between the junction and the case of the C2M0xxx-120D($xxx \in \{025, 040, 080, 160\}$) is provided in the respective datasheets as a function of a square wave pulse duration. The method presented in [26] is used to generate the thermal model. In this method, the $Z_{th,JC}$ is modeled with a fourth-order Foster network. The Foster network's step response can be represented as

$$Z_{th,JC} = \sum_{j=1}^{4} R_{th,JC,j}(1 - e^{\frac{-t}{\tau_{th,JC,j}}}) \tag{2.10a}$$

$$C_{th,JC,j} = \frac{\tau_{th,JC,j}}{R_{th,JC,j}} \tag{2.10b}$$

where $R_{th,JC,j}$ and $C_{th,JC,j}$ are the jth order Foster network thermal resistance and thermal capacitance respectively. The curve-fitting technique is used to calculate the $R_{th,JC,j}$ and the $C_{th,JC,j}$ values in a way that the resultant curve from (2.10) fits with the single-pulse transient thermal impedance characteristic provided in the datasheet. Figure 2.2 represents the thermal network of N switches modeled with the fourth-order Foster network connected to a same heatsink. The semiconductor losses P_{tot}^{Sw}, are represented by the current sources and the heatsink temperature is modeled with the voltage source T_h.

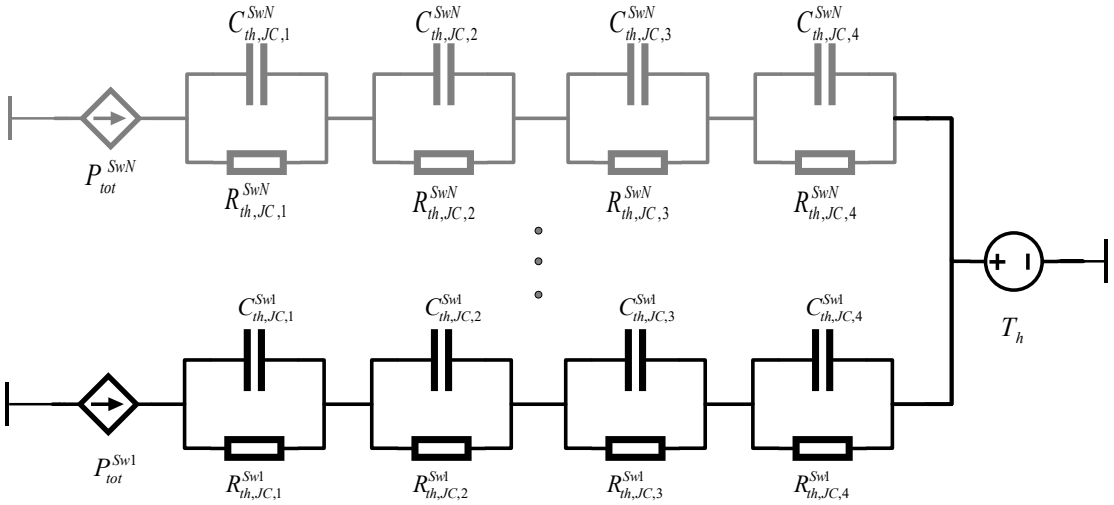


Figure 2.2: The thermal impedance network of N switches connected to a same heatsink

2.3.2 Chip Scaling Methods

Two methods are used to model the chip dependency of the switches. In the first method, the dependency of the characteristics on the chip-area was derived by fitting a surface to match respective curves from the four datasheets. The points between the maximum and the minimum chip-area were interpolated to fit the shape of the available curves. Even though the accuracy of this method is high, the modeling procedure takes lots of effort and the extrapolation is not possible.

The second technique is to use the linear and the inverse scaling laws [27]. In this technique, a base switch has to be selected firstly. Then new switch models are created by scaling the characteristic of the original switch. The scalings applied to the different characteristics can be represented as

$$R_{DS,on}(A_{chip}) = R^*_{DS,on}\frac{A^*_{chip}}{A_{chip}} \tag{2.11a}$$

$$Z_{th,JC}(A_{chip}) = Z^*_{th,JC}\frac{A^*_{chip}}{A_{chip}} \tag{2.11b}$$

$$E_{S,on/off}(A_{chip}, i_{S,F}, u_{S,F}, T_J) = \frac{A_{chip}}{A^*_{chip}} E^*_{S,on/off}(i_{S,F}\frac{A^*_{chip}}{A_{chip}}, u_{S,F}, T_J) \tag{2.11c}$$

where the parameters of the original switch are denoted with the $*$ sign.

2.3.3 Semiconductors Cost Model

Based on a database of several power switches, a linear model for semiconductors cost has been proposed in [28] as

$$\Sigma_{SC} = \Sigma_{pack} + (\sum_n \sigma_{chip(n)} A_{chip,n}) \tag{2.12}$$

where Σ_{SC} denotes the total semiconductor cost. Σ_{pack} is the package cost that depends only on the package type and $\sigma_{chip(n)}$ is the specific price per chip-area. According to the manufacturer datasheets, C2M0xxx120D($xxx \in \{025, 040, 080, 160\}$) devices are packed in TO-247-3 packages with the specific cost per unit of 0.55€ [28]; and for the C2M technology the specific price per chip-area is 72.01€.cm^{-2} [27]. Therefore, the total semiconductor cost Σ_{MOSFET}, for each topology can be estimated in Euros as

$$\Sigma_{MOSFET} = 0.55N + 72.01A_{chip,total} \tag{2.13}$$

where N is the total number of utilized MOSFETs and $A_{chip,total}$ is the total required chip-area.

3

Topologies and Modulation Schemes

The following chapter is intended to introduce the topologies under comparison along with the respective modulation schemes. The dual-active-bridge (DAB) configuration with different bridge layouts is to be considered. The full-active-bridge with the two-level bridge legs and the full-active-bridge with the three-level Neutral-Point-Clamped (NPC) legs are considered as the primary building blocks.

3.1 The 2L-DAB Topology

The first topology to be considered is the well-known 2L-DAB. It comprises of the full-active-bridges with the two-level bridge legs on both the LV and the MV sides interconnected with a medium frequency transformer (MFT).

3.1.1 Configuration and Modulation

Figure 3.1 depicts the configuration of the 2L-DAB. The switches $S_{1,2,...,8}$ could be a cluster of series-connected MOSFETs to cope with the DC link voltages. In this configuration, the total DC-link voltage will appear across the switches in the off-state. The MFT is represented by a simple equivalent circuit consisting of an ideal transformer and a leakage inductance.

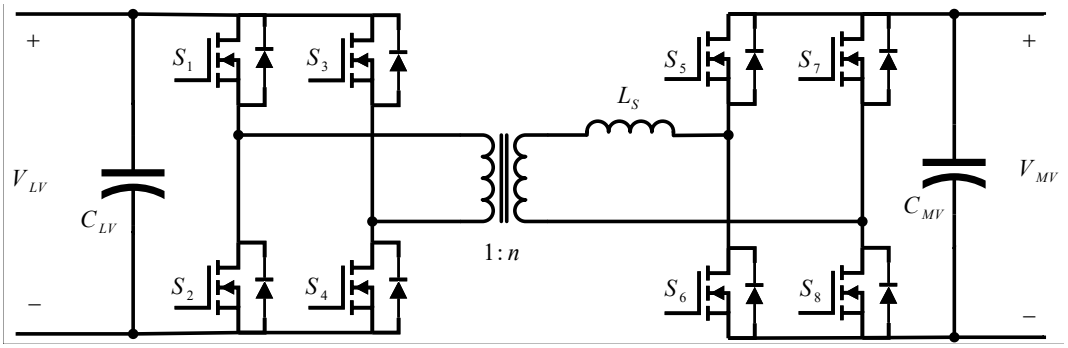


Figure 3.1: The 2L-DAB topology with the two-level bridge legs on the LV and the MV sides

The MOSFETs are switched in a way that phase-shifted square waves are generated on the terminals of the transformer. Figure 3.2b and Figure 3.2a depict the oper-

ating waveforms on the AC-link and the gate signals of the 2L-DAB respectively. The MOSFETs $S_{1,4}$ and $S_{2,3}$ are switched together generating the positive and the negative portions of the LVAC-link square waveform respectively. The switches $S_{5,8}$ and $S_{6,7}$ are gated on in the same manner by ϕ radians phase shift with respect to the LV side switches to generate the MVAC-link square waveform.

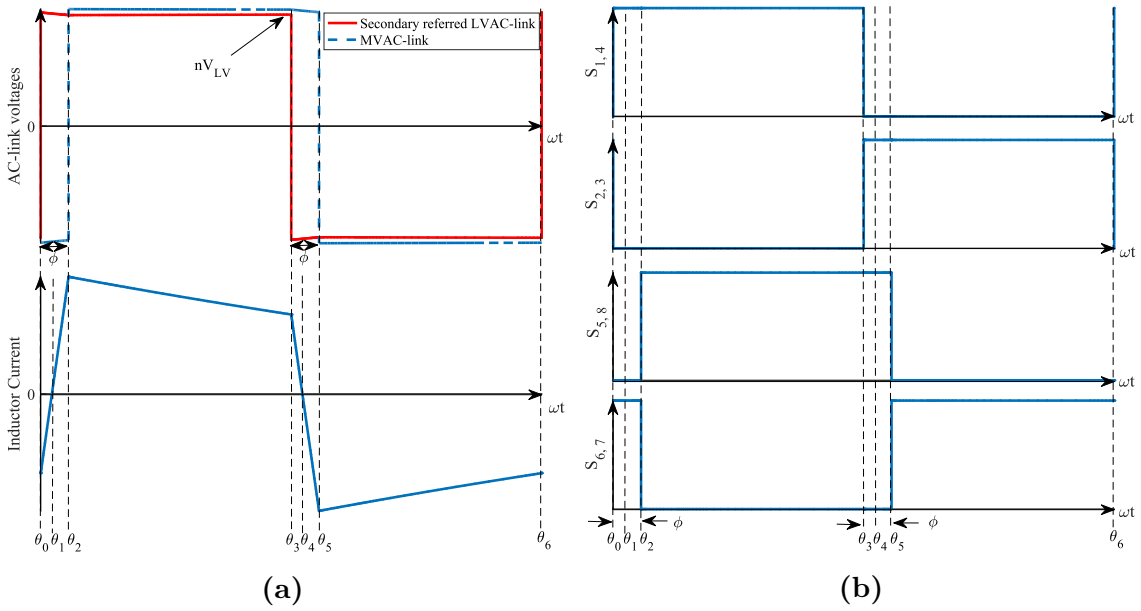


Figure 3.2: The 2L-DAB (a) AC-link voltage and current waveforms (b) MOSFETs gate signals

The anti-parallel diode of the switch must be conducting the current before it gates on to ensure the ZVS during the turn-on period. Based on the conduction stats of the MOSFETs, one switching period can be divided into six different segments as shown in Figure 3.2a. With an assumption that $V_{MV} > nV_{LV}$, the following analysis could be performed to derive a relation between the transferred power and the modulation parameter [29], [30].

1. The interval θ_0 to θ_2

The MOSFETs $S_{6,7}$ were on and the MOSFETs $S_{1,4}$ receive the gate signals. The applied voltage across the inductor of the MFT is $nV_{LV} + V_{MV}$; therefore, its current starts to increase linearly. The current through the inductance of the MFT in this time interval, can be expressed as

$$i(\theta_2) = i(\theta_0) + \frac{\phi}{\omega L_s}(nV_{LV} + V_{MV}) \tag{3.1}$$

where n and L_s are the transformers turns ratio and the leakage inductance respectively. ϕ denotes the phase shift between the two bridges and ω represents the angular switching frequency.

If the current rises from a negative value as shown in 3.2a then the antiparallel diodes of $S_{1,4}$ conduct the current during $[\theta_0, \theta_1]$. At θ_1, the current reverses its

direction and commutates to respective MOSFETs channel ensuring the ZVS. It is noteworthy that, the MOSFETs $S_{1,4}$ are operating in the third-quadrant region due to the negative value of the current when they are gated on.

2. The interval θ_2 to θ_3

The MOSFETs $S_{1,4}$ are still on, and $S_{6,7}$ are gated off, and $S_{5,8}$ receive the gate signals. Since the current is positive, the antiparallel diodes of $S_{5,8}$ freewheel the current. The inductor current starts to decrease because $nV_{LV} - V_{MV} < 0$. The inductor current can be calculated as

$$i(\theta_3) = i(\theta_2) + \frac{\pi - \phi}{\omega L_s}(nV_{LV} - V_{MV}) \tag{3.2}$$

3. The interval θ_3 to θ_5

The switches $S_{1,4}$ are gated off, and $S_{2,3}$ receive the gate signals, while in the secondary side $S_{5,8}$ continue to conduct the current. During the interval $[\theta_3, \theta_4]$ the current is positive, and the antiparallel diodes of all MOSFETs are conducting. Since the applied voltage across the inductor is negative($-nV_{LV} - V_{MV}$), the current starts to decrease. At $\omega t = \theta_4$ the current reverses direction and commutates from the antiparallel diodes to the respective MOSFET channel. The inductor current can be derived as

$$i(\theta_5) = i(\theta_3) - \frac{\phi}{\omega L_s}(nV_{LV} + V_{MV}) \tag{3.3}$$

4. The interval θ_5 to θ_6

In this segment $S_{5,8}$ are turned off and the current starts to freewheel in the intrinsic body diodes and the MOSFET channels of $S_{6,7}$. The inductor current can be derived as

$$i(\theta_6) = i(\theta_5) - \frac{\pi - \phi}{\omega L_s}(nV_{LV} - V_{MV}) \tag{3.4}$$

Due to the symmetry of the current waveform, $i(\theta_3) = -i(\theta_0)$. Therefore the initial inductor current can be calculated as

$$i(\theta_0) = \frac{1}{2\omega L_s}[(\pi - 2\phi)V_{MV} - \pi n V_{LV}] \tag{3.5}$$

Figure 3.3a and 3.3b represent the current and the voltage waveforms of the LV bridge and the MV bridge MOSFETs respectively. It can be seen that the MOSFETs are gated on when the current direction is negative. Therefore, for all of the switches the antiparallel diode conducts the current during the turn-on period, and due to the presence of the gate signals, the MOSFETs are operating in the third-quadrant region. Therefore, the ZVS is achieved in all of the switches.

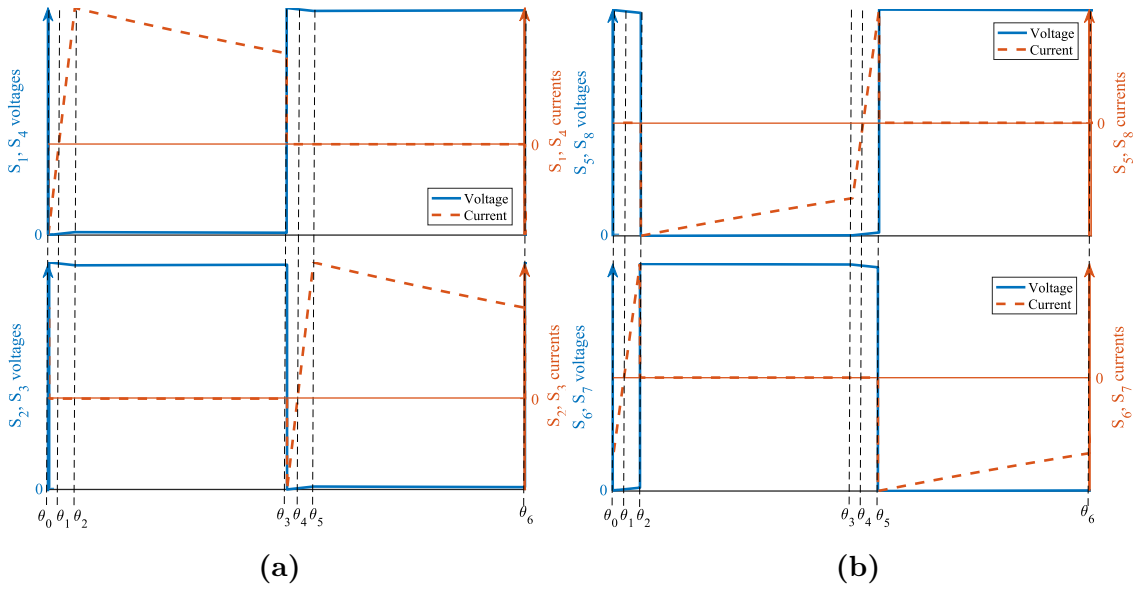


Figure 3.3: The current and the voltage waveforms of the 2L-DAB MOSFETs (a) the LV side switches (b) the MV side switches

The analysis mentioned above and Figure 3.3 is derived based on the assumption of a negative initial current for the inductor ($i(\theta_0) < 0$). With this assumption, it can be ensured that the antiparallel diodes conduct the current initially and therefore guarantees the ZVS during turn-on. Thus the criteria for the ZVS conditions can be derived from (3.5) as

$$\phi_{min} > \frac{\pi}{2}(1 - \frac{nV_{LV}}{V_{MV}}) \tag{3.6}$$

where ϕ_{min} is the minimum value of the phase shift that the 2L-DAB can retain the ZVS on all of the switches. The transferred power through the transformer can be derived by calculating the average current of the leakage inductance and multiplying it by the primary voltage as

$$P_{2L-DAB} = \frac{nV_{LV}V_{MV}}{\omega L_s}\phi[1 - \frac{\phi}{\pi}] \tag{3.7}$$

The transmitted power is a function of ϕ and can be controlled by adjusting the phase shift between the two bridges without varying the switching frequency. It is also notable from (3.6) that keeping the ratio of $\frac{nV_{LV}}{V_{MV}}$ close to the unity decrease the minimum allowable value of ϕ. Therefore, the converter can operate in a broad range of the output power while retaining the ZVS property.

3.2 ML-DAB Topology

The second topology considered for the efficiency analysis is the Multi-level Dual-Active-Bridge (ML-DAB) [9], [31].

3.2.1 Configuration and Modulation

Figure 3.4 shows the configuration of the ML-DAB converter. The LV bridge is comprised of the two-level bridge legs similar to the 2L-DAB configuration. Therefore, the voltage ratings and the number of series connected switches for the LV bridge is the same as the 2L-DAB converter. However, on the MV side, the three-level active-clamped legs are used instead of the two-level bridge legs. The advantage of the ML-DAB over the 2L-DAB is that the switches with half voltage ratings can be used on the MV side. In other words, either the series connection of the switches on the MV side can be eliminated, or the number of series connected switches can be reduced.

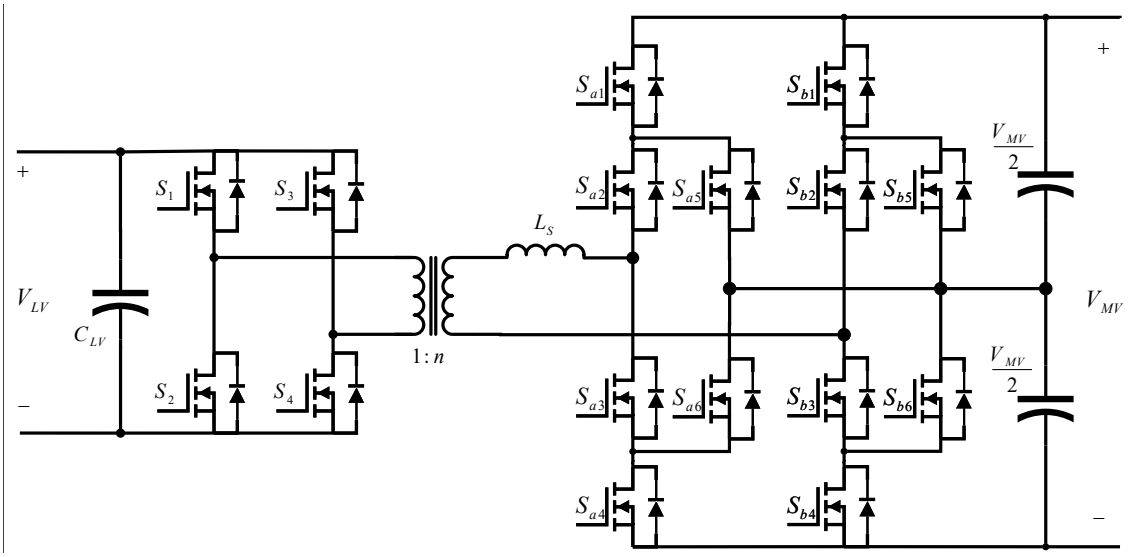


Figure 3.4: The ML-DAB topology with the two-level and the three-level bridge legs on the LV and the MV sides respectively

Similar to the 2L-DAB, the MFT's leakage inductance is used as an energy transfer element. Figure 3.5a depicts the secondary referred voltage waveforms and the MFT's inductor current on the MV side. The MVAC voltage has a five-level waveform, and the converter is operating in the boost mode. Two parameters α and β are used to shape the MV side waveform, and the phase shift between the fundamental components of the AC-link voltages (ϕ) is used to control the power flow. Designation of the ML-DAB refers to the fact that various waveforms can be created on the MVAC-link depending on the values of α and β. The gate signals of the MOSFETs for both the LV and the MV bridges are depicted in Figure 3.5b. The switches S_5 and S_6 on each leg are gated on whenever the respective switches S_2 and S_3 receive the gate signals.

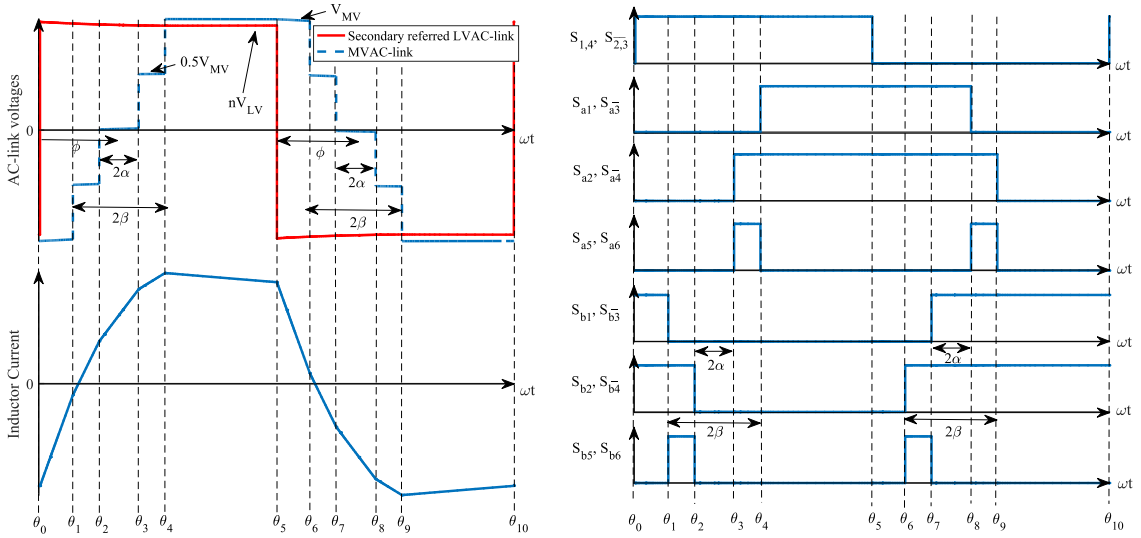


Figure 3.5: The ML-DAB (a) AC-link voltage and current waveforms (b) MOSFET gate signals

Depending on the relation of α, β and ϕ different cases could be considered to derive the power flow relations [32]. However, only the procedure for the case where $\beta < \phi \leq \frac{\pi}{2}$ will be presented, and only the final relations for the rest will be provided. For different time periods relation of the inductor current can be expressed as
for $0 < \omega t \leq (\phi - \beta)$:

$$i_L(\omega t) = \frac{nV_{LV} + V_{MV}}{\omega L_s}\omega t + i_L(0); \tag{3.8}$$

for $(\phi - \beta) < \omega t \leq (\phi - \alpha)$:

$$i_L(\omega t) = \frac{nV_{LV} + \frac{V_{MV}}{2}}{\omega L_s}(\omega t - \phi + \beta) + i_L(\phi - \beta); \tag{3.9}$$

for $(\phi - \alpha) < \omega t \leq (\phi + \alpha)$:

$$i_L(\omega t) = \frac{nV_{LV}}{\omega L_s}(\omega t - \phi + \alpha) + i_L(\phi - \alpha); \tag{3.10}$$

for $(\phi + \alpha) < \omega t \leq (\phi + \beta)$:

$$i_L(\omega t) = \frac{nV_{LV} - \frac{V_{MV}}{2}}{\omega L_s}(\omega t - \phi - \alpha) + i_L(\phi + \alpha); \tag{3.11}$$

for $(\phi + \beta) < \omega t \leq \pi$:

$$i_L(\omega t) = \frac{nV_{LV} - V_{MV}}{\omega L_s}(\omega t - \phi - \beta) + i_L(\phi + \beta) \tag{3.12}$$

With assumption that the DC component of the transformer current is zero ($i_L(\pi) = -i_L(0)$) the initial current of the transformer can be derived from (3.8) to (3.12) as

$$i_L(0) = \frac{1}{2\omega L_s}[(\pi - 2\phi)V_{MV} - \pi n V_{LV}] \tag{3.13}$$

In a similar manner as the 2L-DAB, the transferred active power can be calculated as

$$P_{ML-DAB} = \frac{nV_{LV}V_{MV}}{\omega L_s}[\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}] \tag{3.14}$$

Similar procedure can be taken to calculate the power for cases where $\alpha < \phi \leq \beta$ and $0 < \phi \leq \alpha$. The transferred power for different values of the phase shift between the two bridges can be summarized as

$$\text{For} \quad 0 < \phi \leq \alpha \quad : \quad P_{ML-DAB} = \frac{nV_{LV}V_{MV}}{\omega L_s}\phi[1 - \frac{\alpha}{\pi} - \frac{\beta}{\pi}] \tag{3.15a}$$

$$\text{For} \quad \alpha < \phi \leq \beta \quad : \quad P_{ML-DAB} = \frac{nV_{LV}V_{MV}}{\omega L_s}[\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\phi\beta}{\pi}] \tag{3.15b}$$

$$\text{For} \quad \beta < \phi \leq \frac{\pi}{2} \quad : \quad P_{ML-DAB} = \frac{nV_{LV}V_{MV}}{\omega L_s}[\phi - \frac{\phi^2}{\pi} - \frac{\alpha^2}{2\pi} - \frac{\beta^2}{2\pi}] \tag{3.15c}$$

It is noteworthy that for all of the three cases the initial inductor current is calculated as

$$i_L(0) = \frac{1}{2\omega L_s}[(\pi - 2\phi)V_{MV} - \pi n V_{LV}] \tag{3.16}$$

3.3 3L-DAB Topology

The three-level Dual-Active-Bridge (3L-DAB) topology, introduced recently in [33] and [34], is the third topology under comparison which will be discussed in details in the following.

3.3.1 Configuration and Modulation

The configuration of the 3L-DAB is depicted in Figure 3.6. Both the LV and the MV bridges feature three-level active clamped legs, and the switches are required to block half of the respective DC-link voltage. As for the previous converters the transformer's leakage inductance is used to transfer the energy. The analysis will be performed on the MV-side of the transformer to retain the consistency.

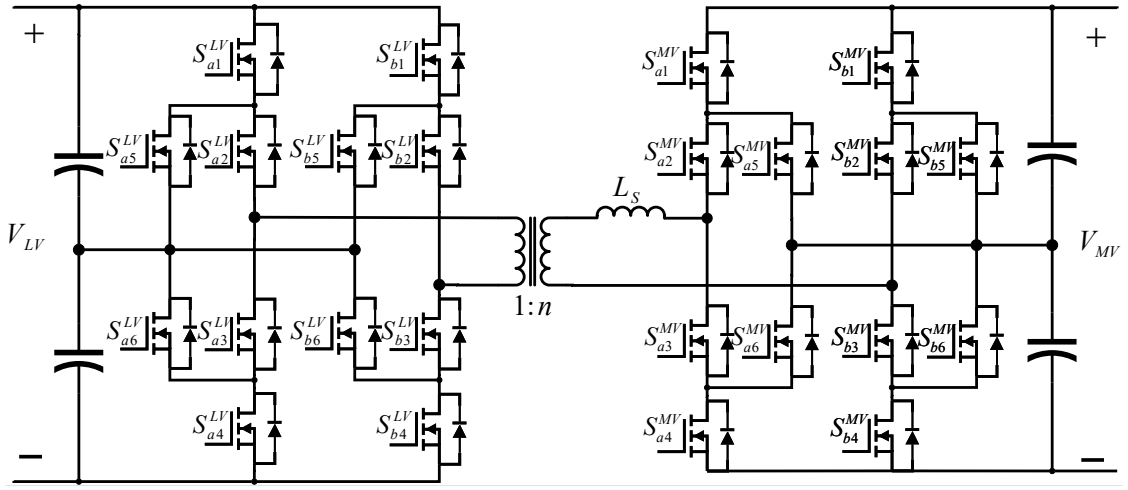


Figure 3.6: The 3L-DAB topology with the three-level bridge legs on both the LV and the MV sides

Figure 3.7 illustrates the MVAC-link voltage and the secondary referred LVAC-link voltage of the 3L-DAB along with the inductor current for a general case.

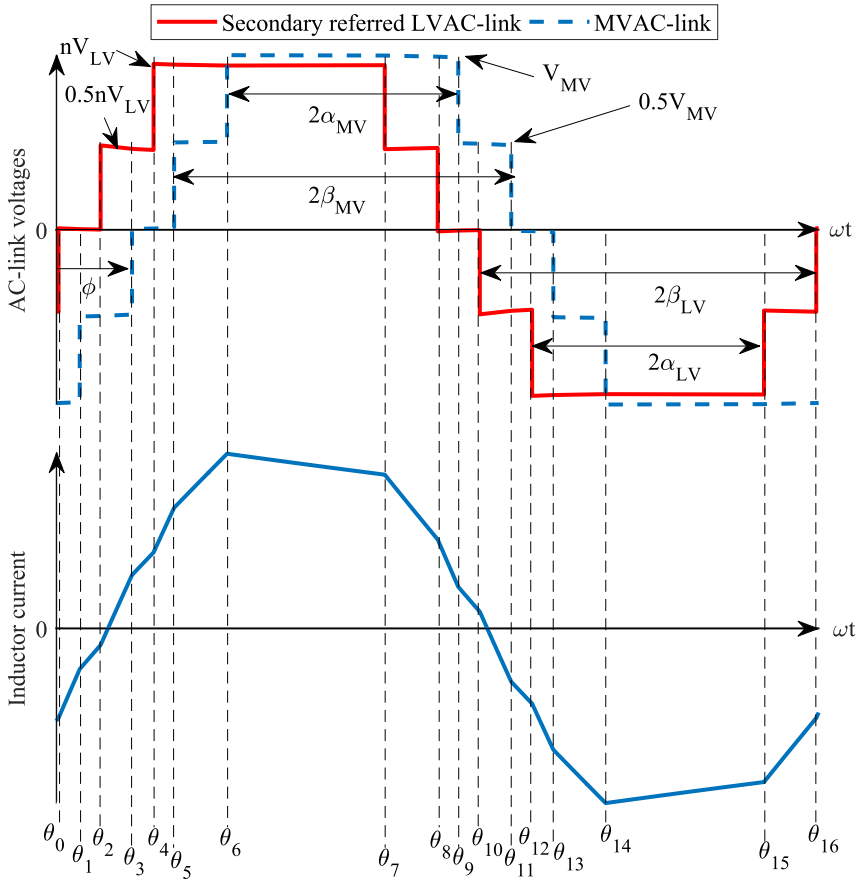


Figure 3.7: The 3L-DAB MVAC-link and MV-side referred LVAC-link voltages and the inductor current

The corresponding LV-bridge and MV-bridge MOSFET's gate signals are depicted

in Figures 3.8 and 3.9 respectively.

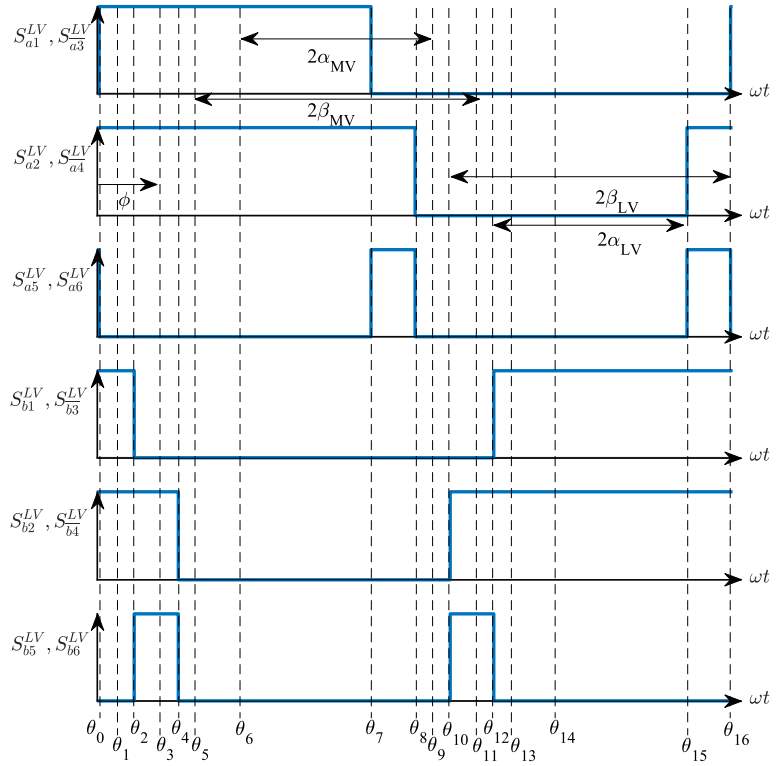


Figure 3.8: The 3L-DAB LV-side MOSFETs gate signals

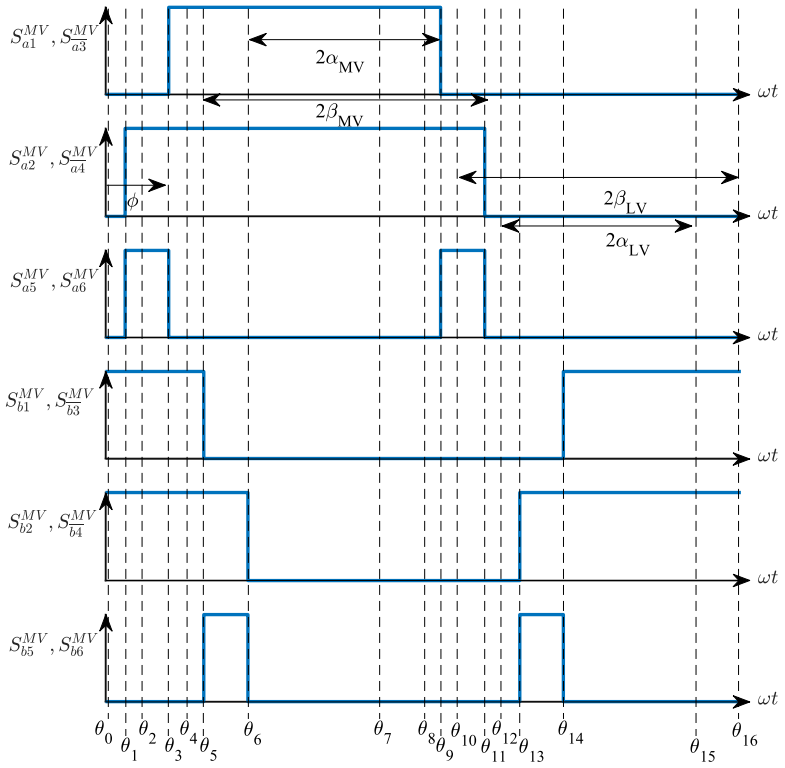


Figure 3.9: The 3L-DAB MV-side MOSFETs gate signals

The operation is shown in the boost mode as the MV-side voltage is higher than the secondary referred LV-side one. The parameters $\alpha_{MV/LV}$ and $\beta_{MV/LV}$ are used to shape the waveforms on the transformer's inputs; while the phase shift between the two bridges ϕ, regulates the transferred power. For $\phi > 0$ the power is transferred from the LV-side to the MV-side. Whereas, for a negative ϕ the direction of the power flow is reversed.
The $\alpha_{MV/LV}$ and $\beta_{MV/LV}$ must be selected such that

$$0 \leq \alpha_{MV} \leq \beta_{MV} \leq \frac{\pi}{2} \tag{3.17a}$$

$$0 \leq \alpha_{LV} \leq \beta_{LV} \leq \frac{\pi}{2} \tag{3.17b}$$

Even order harmonics will be eliminated as the voltages have a half-wave symmetry. Therefore, the AC-link voltages $v_{MV/LV}$, and the inductor current i_{LV}, can be represented in the form of Fourier series as [34]

$$v_{MV/LV} = \sum_{h=1,3,5,\ldots} [\left\| V_{MV/LV,h} \right\| \sin(h\omega t \ + \ \angle V_{MV/LV,h})] \tag{3.18a}$$

$$i_{LV} = \ ni_{MV} \ = \sum_{h=1,3,5,\ldots} [\| I_{LV,h} \| \sin(h\omega t \ + \ \angle I_{LV,h})] \tag{3.18b}$$

where ω is the angular switching frequency, h denotes the harmonic order, and n is the turns ratio of the MFT. $\left\| V_{MV/LV,h} \right\| \angle V_{MV/LV,h}$ and $\| I_{LV,h} \| \angle I_{LV,h}$ are the phasors of the h-order harmonic of the voltage and the current respectively which can be represented as a function of the modulation parameters and the DC-link voltages as

$$V_{LV,h} = [\frac{2V_{LV}}{\pi h}(\cos(h(\frac{\pi}{2} - \alpha_{LV})) \ + \ \cos(h(\frac{\pi}{2} - \beta_{LV})))] \angle 0 \tag{3.19a}$$

$$V_{MV,h} = [\frac{2V_{MV}}{\pi h}(\cos(h(\frac{\pi}{2} - \alpha_{MV})) \ + \ \cos(h(\frac{\pi}{2} - \beta_{MV})))] \angle (-h\phi) \tag{3.19b}$$

$$I_{LV,h} = \frac{n^2 V_{LV,h} - n V_{MV,h}}{j.h\omega L_s} \tag{3.19c}$$

where V_{LV} and V_{MV} are the LVDC link, and MVDC link voltages and L_s denotes the MV-side referred leakage inductance of the MFT. With the assumption of a lossless transformer, the transferred power P, can be calculated as

$$P_{3L-DAB} = \frac{1}{2} \sum_{h=1,3,5,\ldots} \| V_{LV,h} \| \, . \, \| I_{LV,h} \| \cos(\angle I_{LV,h}) \tag{3.20}$$

4

Simulation Procedure

The investigation of the converter efficiency requires calculation of switching and conduction losses. PLECS is a powerful simulation platforms for power electronic systems which provides a possibility of semiconductor loss calculation. PLECS Blockset allows simulations to be performed in the Simulink environment. The inputs can be provided to the system from an M-file, and the outputs can be easily processed in MATLAB. PLECS Blockset was used to simulate the electrical and the thermal aspects of the converters. MATLAB was utilized to initialize the circuit parameters, run the SABC algorithm, perform the parametric sweeps, and do the postprocessing and the Simulink was used as an interface between PLECS Blockset and MATLAB to exchange the required data.

4.1 MOSFET Modeling

As mentioned previously in Section 2.2.1, one of the primary requirements in performing the chip-area sweep is the chip dependent model of the MOSFET. A detailed model of the MOSFET was created based on the manufacturer datasheets as discussed in Section 2.3.1. This model was implemented in M-files that was based on the chip requirements of the switches which generated the desired data to initialize the MOSFET model in PLECS.

The author has faced limitations with the built-in MOSFET model of PLECS which eventually led to setting up a MOSFET model. The first limitation was that the electrical characteristic of the MOSFET was modeled with a single on-resistance for all three conduction states of the MOSFET. Secondly, implementation of both conduction losses for the forward conduction of the body diode and the third-quadrant conduction states was impossible in the built-in model. Finally, as only a single resistance was utilized to model the on-resistance, the dynamic dependency of the MOSFET electrical characteristics on the junction temperature and the drain to source current was neglected. Two MOSFET models with a different degree of complexity were developed, to tackle the mentioned shortcomings.

4.1.1 MOSFET's Static Model

The static model refers to the fact that only the first two problems are addressed in this model, whereas the dynamic changes in the on-resistance are not considered. Figure 4.1 depicts the static model of the MOSFET.

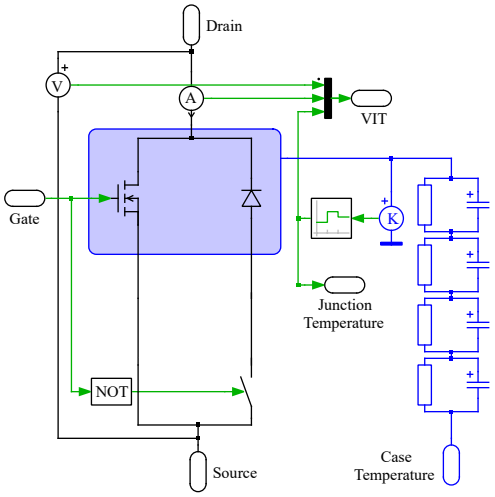


Figure 4.1: The static PLCES model of the MOSFET

The characteristics of the third-quadrant conduction state and the MOSFET forward conduction state for the loss calculations are implemented in an ideal MOSFET. The ideal-MOSFET was chosen instead of an ideal-MOSFET with an ideal-anti-parallel-diode, to avoid the particular switching requirements of the latter. The former conducts the current in both directions between the drain and the source if the gate is activated [35]. Therefore, if the gate signal was applied and the current direction was from the drain to the source, the forward characteristics of the MOSFET will be used to calculate the losses. While for the reverse current direction the third-quadrant characteristics will be utilized.

The body diode characteristic is applied to an ideal diode which incorporates the respective forward voltage and the on-resistance. It should be noted that the third quadrant characteristic includes both the diode and the MOSFET channel conduction. Therefore, to avoid conduction of the current from the diode when the MOSFET is gated on and operating under the third quadrant mode, inverse of the gate signal is used to connect or disconnect the diode from the circuit.

Since the combination of the diode and the MOSFET is used to model the actual MOSFET, the thermal description of these components only contain the loss calculation lookup tables; and the thermal impedance network is implemented separately. The heatsink models the junction of the MOSFET and gathers the heat generated in the MOSFET and the diode. The junction-to-case thermal impedance is modeled with the fourth order Foster network as depicted in Figure 4.1.

4.1.2 MOSFET's Dynamic Model

The static model was modified to incorporate the dynamic change of the electrical characteristics of the MOSFET in PLECS and analyze the effect of this dynamic change in the final results. Figure 4.2a depicts the dynamic model of the MOSFET.

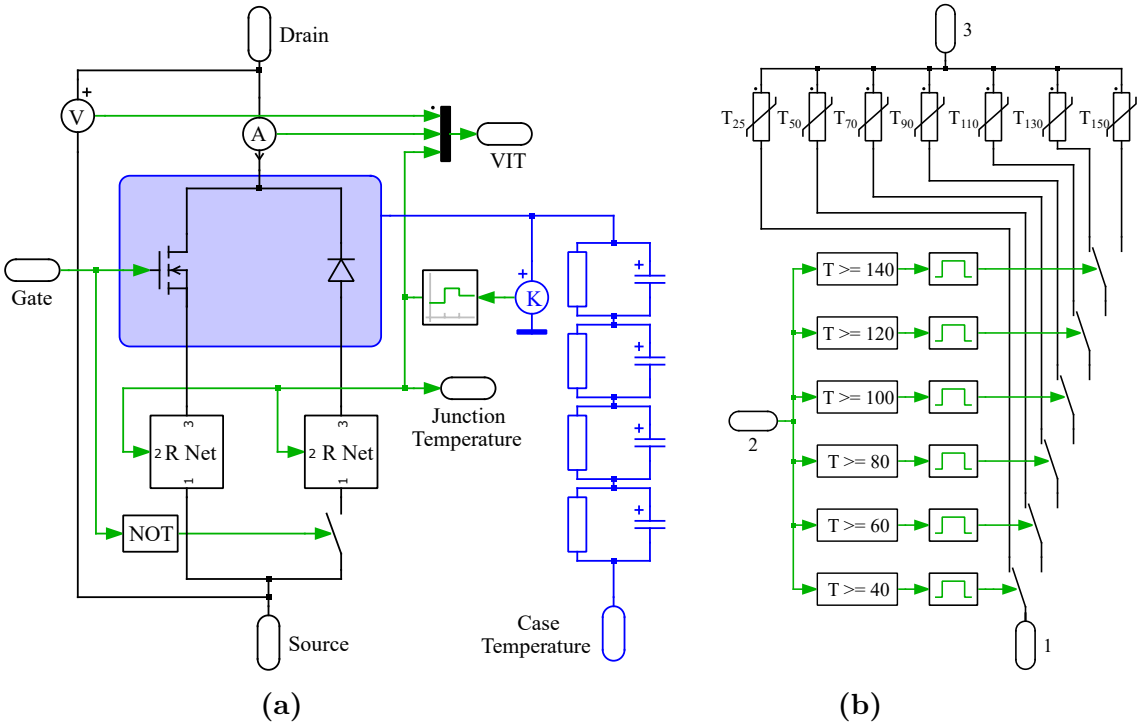


Figure 4.2: (a) The dynamic model of the MOSFET (b) The resistance matrix of the dynamic model

Two resistance matrixes were inserted in the current path which gets a feedback from the junction temperature. These resistance networks approximate the electrical characteristics of the device with a piecewise linear characteristic. The thermal dependency is approximated by fixed seven number of linear pieces. Whenever temperature exceeds the value specified in the comparing block, the trigger signal is sent to the respective double switch to change the characteristic. The current dependency of the characteristics is implemented in the piecewise linear resistors which can be adjusted from the initialization M-files.

It should be noted, since there will be several of these MOSFETs connected in series and parallel, introducing such complicated network of resistors and switches will slow down the simulation. Therefore, utilization of either the static model or the dynamic model must be justified with the converters under simulation.

4.1.3 Series and Parallel Connection

The thermal network of each MOSFET consists of four thermal capacitances. Hence, an array of $S+1$ series-connected MOSFETs and $P+1$ parallel-connected MOSFETs will add $4(S+1)(P+1)$ states to the model which in turn will slow down the simulation. On the other hand, the number of switches will increase dramatically especially if the dynamic model is utilized. Therefore, rather than merely connecting the modules in series and parallel, simplifications have to be done to reduce the number of states and increase the simulation speed.

With the assumption that all the MOSFETs in the array are identical, they will block an equal amount of voltage and the conduction currents will be the same. Thus, the losses occurring in the MOSFETs will be identical. Consequently, a single MOSFET can represent the array behavior if the equivalent electrical circuit of the rest of the array is connected to its terminals. This concept was utilized to simplify the series and the parallel connection of the MOSFETs.

Figure 4.3a illustrates the implemented series connection of $S+1$ MOSFETs. Each of the MOSFET blocks in the model is either a dynamic model or a static model as discussed previously.

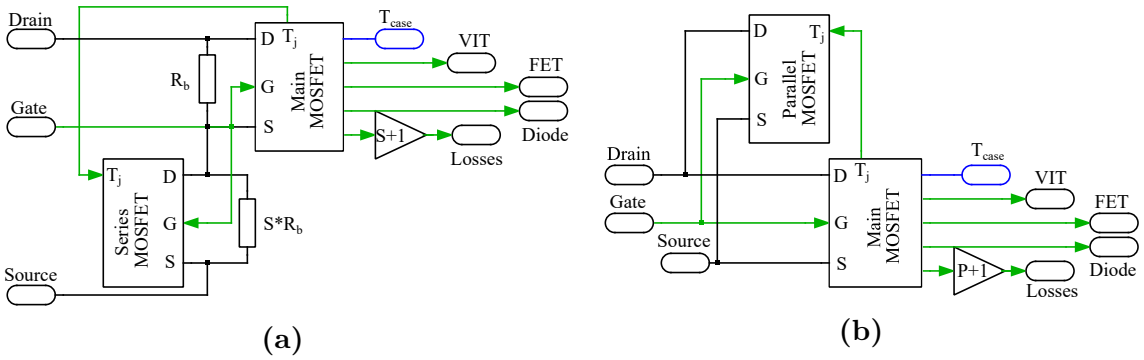


Figure 4.3: PLECS model of (a) the series connected MOSFETs (b) the parallel connected MOSFETs

The calculation of losses and the junction temperature occurs in the Main MOSFET. The thermal network of the Series MOSFET is eliminated which will increase the simulation speed. On the other hand, to simulate the conduction state of the array, the electrical characteristic is modified in a way that for the same current in both MOSFETs, the voltage drop is S times higher for the Series MOSFET. In the blocking state the resistances R_b and $S \times R_b$ guarantee the required voltage sharing between the MOSFETs. Similarly, the parallel connection of the MOSFETs was modeled as depicted in Figure 4.3b. The only difference is that the Parallel MOSFET should conduct P times higher current than the Main MOSFET for the same forward voltage drop.

Combination of the series and the parallel models will result in a model of $(S+1) \times (P+1)$ array of the MOSFETs as depicted in Figure 4.4. By using the proposed model, the number of required thermal capacitances are decreased from $4(S+1)(P+1)$ to 4. Also, the total number of required switches can be reduced $(S+1)(P+1)/3$ times. Consequently, the simulation time will decrease tremendously.

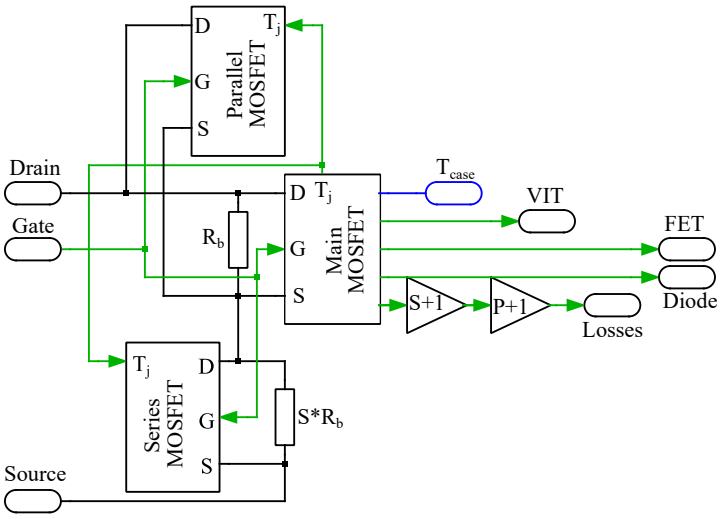


Figure 4.4: PLECS model of the series and the parallel connected MOSFETs

4.2 Converters Modeling

The models of the 2L-DAB and the ML-DAB, introduced in Section 3, are created in PLECS based on the switches developed in Section 4.1. In the following sections, the characteristics of each topology including a number of the MOSFETs connected in series and parallel, the MFT parameters and the modulation parameters will be described.

4.2.1 MOSFETs Series and Parallel Connection

For circuits with a medium stray inductance, the safety margin of 60% is to be used to calculate the repetitive peak voltage rating of the switches [36]. Therefore, the device rating should be higher than $1.6 \times V_{DC}$. The selected SiC MOSFETs blocking voltage is 1200 volts, and the DC-links nominal voltages are 1.3kV and 16kV. With assumption that the full DC-link voltage will be applied across the switches during the turn-off period, it is required to connect two MOSFETs in series on the LV side and 24 MOSFETs on the MV bridge to cope with the DC link voltages.

For the two-level bridge legs in the blocking state, switches must tolerate the full DC-link voltage. Whereas, for the three-level bridge legs the maximum voltage across the switches in the off-state is half of the DC-link voltage. Therefore, the LV bridge of both the 2L-DAB and the ML-DAB comprises two series connected MOSFETs. Where on the MV side, 24 and 12 series connected MOSFETs is required for the 2L-DAB and the ML-DAB respectively.

Also, the parallel connection of the devices is mandatory to deal with the high currents, especially on the LV side. However, as the chip-area sweep will be performed, determination of the parallel connected switches count is not straightforward. The maximum number of the parallel connected switches is limited by the minimum possible chip-area. On the other hand, to tackle the maximum chip-area limit, the

number of parallel connected switches must increase. Since the chip-area sweep is performed linearly, it can be translated into the parallel connection of the switches. Therefore, it has been decided to perform the chip-area sweep with the arbitrary number of parallel connected switches and present the final results in the form of both the chip-area and the respective number of the parallel connected base switches.

4.2.2 2L-DAB Modeling

The MFT specifications and the phase shift between the two bridges must also be determined to operate the 2L-DAB. According to (3.6) to extend the ZVS range of the converter, it is favorable to have $nV_{LV} = V_{MV}$. Therefore, n is selected to be 12 to get nV_{LV} as close as possible to V_{MV}. With this selection according to (3.6) the minimum limit of ϕ to retain the ZVS is 2.25 degrees. For the case of $I_0 < 0$, the reactive power in the AC link can be calculated as

$$Q = \frac{nV_{LV}}{nV_{LV} + V_{MV}} \times \frac{[(\pi - 2\phi)V_{MV} - \pi nV_{LV}]^2}{8\pi\omega L} \tag{4.1}$$

Since the reactive power increases the losses of the system and does not contribute to the output power [37], it is favorable to minimize it. Comparing (4.1) and (3.6), one can conclude that the selection of ϕ close to ϕ_{min} minimizes the reactive power circulation in the system. Selection of the ϕ equal to 20 degrees in the full load, ensures that the switches operate under the ZVS even in 20% of the full load, while a small amount of the reactive power is circulating in the system. With the values of n and ϕ determined, the leakage inductance of the MFT can be calculated from (3.7) as

$$L = \frac{nV_{LV}V_{MV}}{\omega P_{2L-DAB,FL}}\phi_{FL}[1 - \frac{\phi_{FL}}{\pi}] \tag{4.2}$$

where the index FL, denotes the full load operation parameters. For all switching frequencies, the values of n and ϕ_{FL} are kept constant. The value of the leakage inductance is calculated from (4.2) for each switching frequency. It is noteworthy that, to investigate the average efficiency for the European solar mix and to transmit the required amount of power, the phase shift between the two bridges should be varied. The required phase shift ϕ_{req}, to transmit a certain amount of power $P_{2L-DAB,req}$, can be recalculated by substituting (4.2) into (3.7) as

$$\phi_{req}^2 - \pi\phi_{req} + \frac{P_{2L-DAB,req}}{P_{2L-DAB,FL}}[\phi_{FL}(\pi - \phi_{FL})] = 0 \tag{4.3}$$

where the only root laying in $0 \leq \phi_{req} < \pi/2$ is an acceptable phase shift.

4.2.3 ML-DAB Modeling

Similar to the 2L-DAB, the modulation parameters and the MFT specifications must be determined for the ML-DAB too. The transformer turns ratio is selected to be 12 to create enough room for ϕ variations without losing the ZVS in the LV bridge. As can be seen in Figure 3.5b, the zero level in the MVAC link is created by the

phase shift α. α is set to be zero in the simulation to provide a fair comparison with the 2L-DAB where this zero level was not present. On the other hand, to extend the ZVS range to partial loads and minimize the reactive power circulation, β and ϕ were selected to be 10° and 40° respectively by trial and error.

For all switching frequencies, the values of ϕ, α, and β were kept constant, and the value of the leakage inductance of the MFT was calculated based on the full load power. Since $\beta < \phi \leq \pi/2$, the leakage inductance can be calculated from (3.15c) as

$$L = \frac{nV_{LV}V_{MV}}{\omega P_{ML-DAB,FL}}[\phi_{FL} - \frac{\phi_{FL}^2}{\pi} - \frac{\beta^2}{2\pi}] \tag{4.4}$$

where the subscript FL denotes the full load parameters. After the determination of the leakage inductance, it was kept constant and the phase shift between the two bridges ϕ_{req}, was varied to transmit required amount of power $P_{ML-DAB,req}$. It is important to notice that depending on the relation between ϕ, α, and β, one of the (3.15a) to (3.15c) should be used to determine value of ϕ_{req}. After some calculations, the relations to derive the value of ϕ_{req} can be summarized as

$$\text{For} \quad 0 < \phi \leq \alpha \quad : \quad \phi_{req} - [\frac{\pi\omega L P_{ML-DAB,req}}{nV_{LV}V_{MV}(\pi - \alpha - \beta)}] = 0 \tag{4.5a}$$

$$\text{For} \quad \alpha < \phi \leq \beta \quad : \quad 2\phi_{req}^2 + 2(\beta - \pi)\phi_{req} + [\alpha^2 + \frac{2\pi\omega L P_{ML-DAB,req}}{nV_{LV}V_{MV}}] = 0 \tag{4.5b}$$

$$\text{For} \quad \beta < \phi \leq \frac{\pi}{2} \quad : \quad 2\phi_{req}^2 - 2\pi\phi_{req} + [\alpha^2 + \beta^2 + \frac{2\pi\omega L P_{ML-DAB,req}}{nV_{LV}V_{MV}}] = 0 \tag{4.5c}$$

At first, ϕ_{req} is calculated from (4.5a). If the result lays within the bounds, ϕ_{req} is determined. Otherwise, the same procedure will be taken for the second and the third equation. The process is depicted as a flowchart in Figure 4.5.

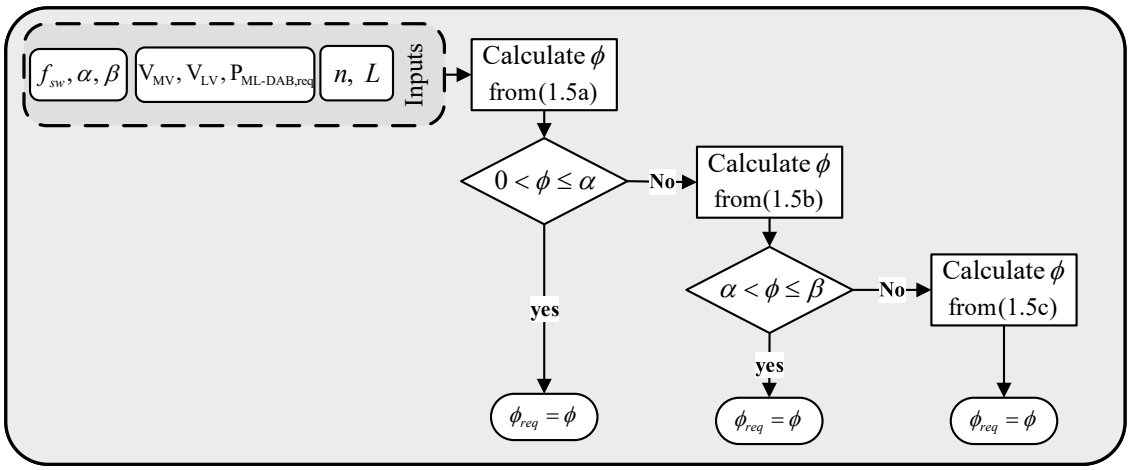


Figure 4.5: The determination process of ϕ_{req}

4.2.4 3L-DAB Modeling

As the dynamic behavior of the converter to the load changes is of no interest in this thesis, such a dynamic controller is not designed for the converter. Due to the absence of the controller, unbalances may occur between the DC-link capacitors voltages. To avoid this situation, constant DC voltage sources with half of the respective DC-link voltage is used instead of the capacitors.

For simplicity, it is assumed that the LV-side and the MV-side have similar waveforms. i.e., the modulation parameters are

$$\alpha = \alpha_{MV} = \alpha_{LV} \tag{4.6a}$$
$$\beta = \beta_{MV} = \beta_{LV} \tag{4.6b}$$

To achieve a high power density and have a fair comparison between converters the zero level is not introduced in the waveforms of the AC-link voltages (or in other words $\beta = 90°$). To minimize the reactive power circulation and extend the ZVS to partial loads, α and ϕ_{FL} are chosen to be 80° and 30° respectively in the full-load for all switching frequencies using trial and error strategy.

A simplified model of the MFT with only a leakage inductance and an ideal transformer is used as depicted in Figure 3.6. The turns ratio is selected to be 12, similar to the previous converters; The value of the leakage inductance is determined for all switching frequencies by solving

$$V_{LV,h} = [\frac{2V_{LV}}{\pi h}(1 + \cos(h\frac{\pi}{18}))]\angle 0 \tag{4.7a}$$
$$V_{MV,h,FL} = [\frac{2V_{MV}}{\pi h}(1 + \cos(h\frac{\pi}{18}))]\angle(-h\phi_{FL}) \tag{4.7b}$$
$$I_{LV,h,FL} = \frac{n^2 V_{LV,h} - nV_{MV,h,FL}}{j.h\omega L_s} \tag{4.7c}$$
$$P_{3L-DAB,FL} = \frac{1}{2}\sum_{h=1,3,5,...} \|V_{LV,h}\| \,.\, \|I_{LV,h,FL}\| \cos(\angle I_{LV,h,FL}) \tag{4.7d}$$

Simultaneously; where the subscript FL denotes the full-load parameters. With L_s determined in the previous step, the value of the phase-shift ϕ_{req}, to transfer the required amount of power $P_{3L-DAB,req}$, in the partial loads can be calculated by substituting ϕ_{req} in (4.7b) as

$$V_{MV,h,req} = [\frac{2V_{MV}}{\pi h}(1 + \cos(h\frac{\pi}{18}))]\angle(-h\phi_{req}) \tag{4.8a}$$
$$I_{LV,h,req} = \frac{n^2 V_{LV,h} - nV_{MV,h,req}}{j.h\omega L_s} \tag{4.8b}$$
$$P_{3L-DAB,req} = \frac{1}{2}\sum_{h=1,3,5,...} \|V_{LV,h}\| \,.\, \|I_{LV,h,req}\| \cos(\angle I_{LV,h,req}) \tag{4.8c}$$

4.3 SABC Algorithm and Parametric Sweeps

Four different levels of the parametric sweeps were performed in this thesis in the form of the nested For loops as shown in Figure 4.6.

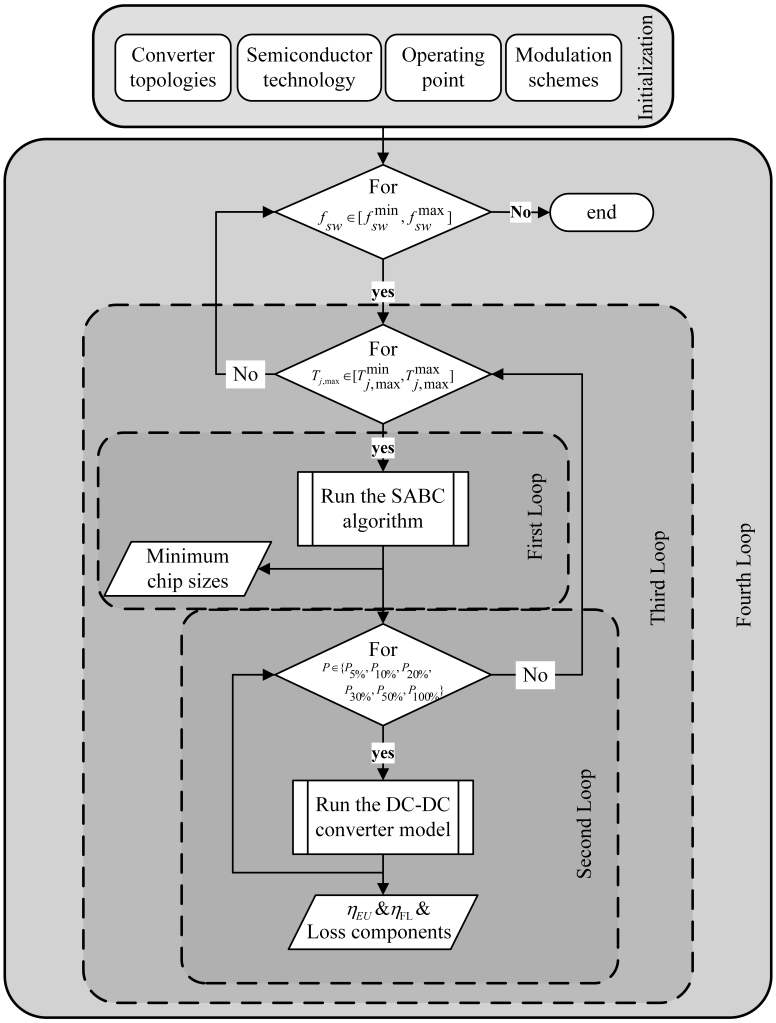


Figure 4.6: The parametric sweep algorithm

The innermost loop is the SABC algorithm which determines the optimum chip-area for individual semiconductors based on the specified switching frequency, the maximum junction temperature, and the modulation parameters. After the determination of the minimum chip sizes, the output power of the converter was swept in the second loop to determine the average efficiency for the European solar mix and also the loss components of the semiconductors. In the third level, the maximum allowable junction temperature of the switches are swept from a maximum value to a minimum value to increase the required chip size of the converter while distributing the available chip size in an optimum form among the switches. To investigate the effect of the switching frequency on the performance of the converters the fourth loop was introduced to the algorithm. This level loops over all of the previous steps for a predetermined range of the switching frequency.

5

Comparative Evaluation and Analysis

The converters discussed in the previous chapters will be compared based on their efficiencies and their chip-area in the following sections.

5.1 The 2L-DAB Results

Figure 5.1 depicts the full-load efficiency of the 2L-DAB as a function of the total amount of the chip-area requirement $A_{Chip,total}$, obtained from the SABC algorithm for various switching frequencies and different maximum junction temperatures. $A_{Chip,total}$ is distributed optimally among the switches so that the junction temperature of all of the switches are kept below $T_{j,max}$.

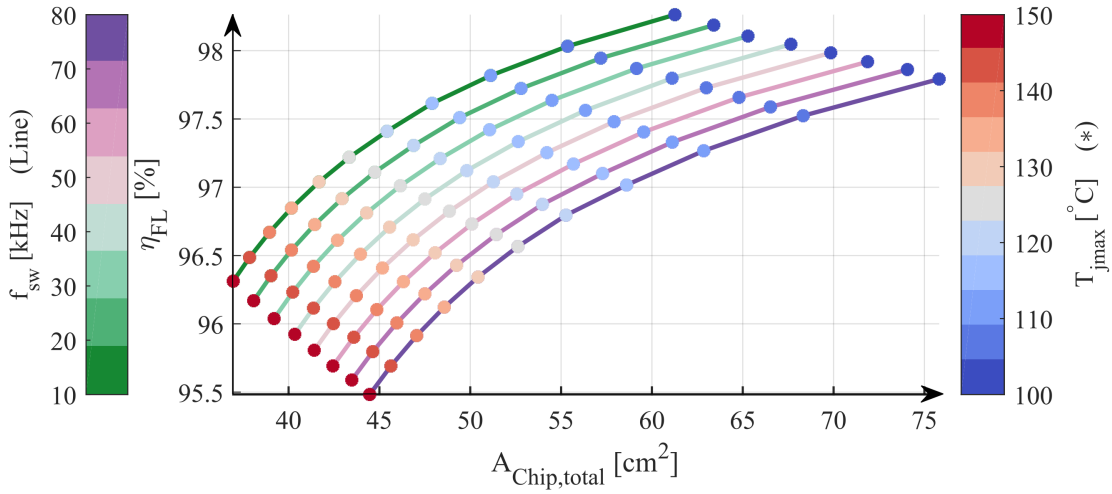


Figure 5.1: The 2L-DAB full-load efficiency versus the total amount of chip-area requirement obtained from the SABC algorithm for various switching frequencies and different maximum junction temperatures

Each solid line represents the efficiency of the 2L-DAB for a constant switching frequency. The asterisks with the same color denote the trajectory of the full-load efficiency for a constant MOSFET junction temperature. The dark green and the dark purple solid lines correspond to the 10 kHz and the 80 kHz switching frequencies respectively. The dark red asterisks mean that the MOSFET's junction temperature in the full-load operation condition is equal to the maximum allowable junction

temperature or $150°C$. As the junction temperature decreases, the asterisk's color shifts toward the dark blue.
The dark red asterisks represent the minimum possible chip-area for the switches. By increasing f_{sw}, $A_{Chip,total}$ increases. Meanwhile η_{FL} decreases. For 70 kHz increase in f_{sw}, η_{FL} decreases from 96.31% to 95.48% and $A_{Chip,total}$ enlarges by $7.5cm^2$.

If one wants to operate the MOSFETs at a lower junction temperature, for the same amount of the transferred power the chip-area of the switches must be increased. Figure 5.1 shows that for $f_{sw} = 10kHz$, reducing the operation temperature of the switches from $150°C$ to $100°C$ requires an increase of $24.31cm^2$ in $A_{Chip,total}$ that consequently results in 1.95% enhancement of the efficiency. Which is a substantial improvement for the high power applications.

However, as discussed earlier, the PV farms do not operate in the full-load hundred percent of the time. Therefore, it is crucial to investigate the aforementioned effects on the European-efficiency η_{EU}. Figure 5.2 illustrates the dependency of η_{EU} on $A_{Chip,total}$, f_{sw} and $T_{j,max}$.

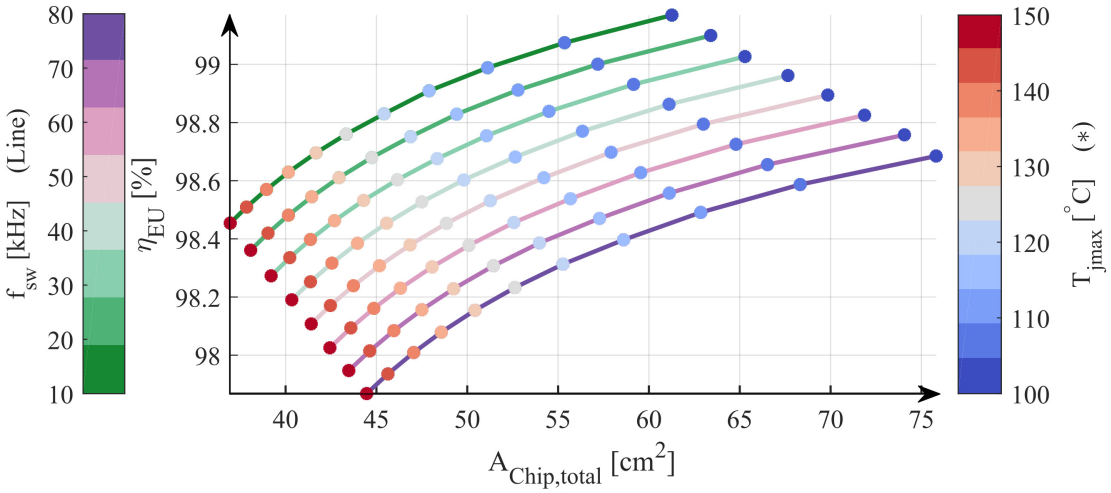


Figure 5.2: The 2L-DAB European-efficiency versus the total amount of chip-area requirement obtained from the SABC algorithm for various switching frequencies and different maximum junction temperatures

It can be seen that η_{EU} for a specific f_{sw} and $T_{j,max}$ is much higher than η_{FL}. Also, the rate of decrease in the efficiency as f_{sw} increases is lowered which means that higher switching frequencies can be used without affecting the overall efficiency that much. However, the rising trend of η_{EU} with reduction of the maximum junction temperature for a constant switching frequency is declined. (e.g., designing of the converter for $T_{j,max} = 100°C$ rather than $150°C$ will result only in 0.72% enhancement of the overall efficiency).

It can be seen from Figure 5.2 that regardless of the switching frequency, reduction of the junction temperature from $105°C$ to $100°C$ requires more chip-area increment than the same amount of reduction from $150°C$. This is due to the fact that the

heatsink temperature is assumed to be constant at $80°C$ and as the junction temperature approaches this value, the amount of the chip-area to reduce the thermal impedance increases dramatically.

The SABC algorithm was applied to the 2L-DAB for three different heatsink temperatures to investigate the effect of the heatsink temperature on the efficiency and the chip-area as illustrated in Figure 5.3.

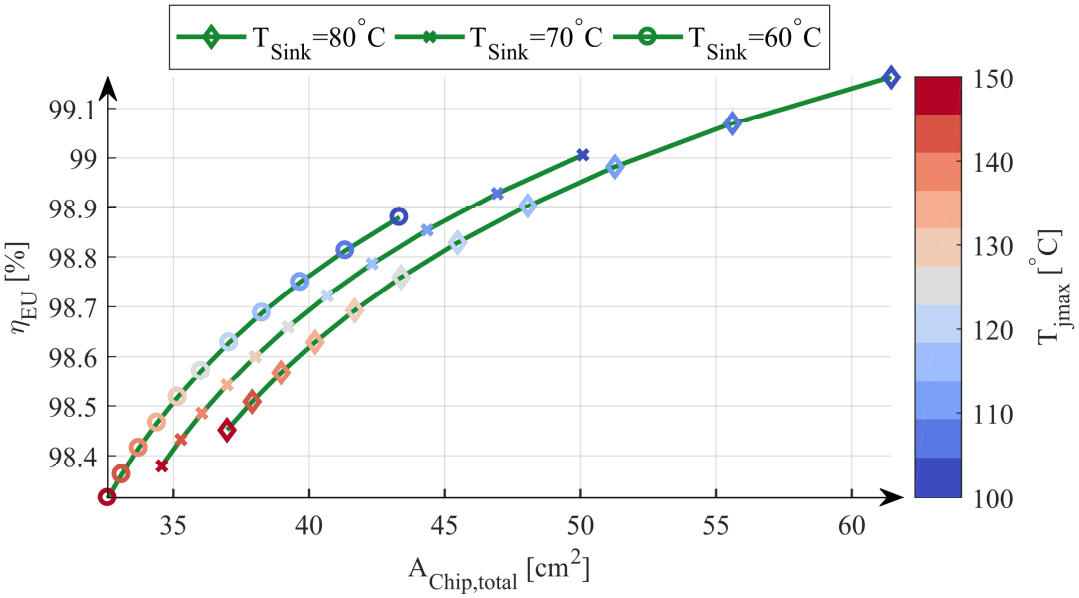


Figure 5.3: The average efficiency for the European solar mix of the 2L-DAB versus the total amount of required chip-area for $f_{sw} = 10kHz$ and three different heatsink temperatures

As can be seen, the amount of increment for the chip-area to decrease the junction temperature for a certain value has been diminished as the heatsink temperature is lowered. The reduction in the chip-area requirement is more evident in the low junction temperatures because the closer the junction temperature is to the heatsink temperature, the higher the chip-area required to reduce the junction-to-case thermal impedance and the losses.

On the other hand, comparing these three lines for the same amount of the chip-area reveals that higher efficiency and lower junction temperature can be achieved by reducing the temperature of the heatsink.

The total semiconductor cost of the converter can be investigated by applying the semiconductor cost model introduced in Section 2.3.3 to the outputs of the SABC algorithm. Figure 5.4 depicts η_{EU} of the 2L-DAB as a function of the total semiconductor cost Σ_{MOSFET}, in Euros. It can be seen that to increase the switching frequency from $f_{sw} = 10kHz$ to $f_{sw} = 80kHz$ by keeping the junction temperature of the MOSFETs at constant value of $150°C$ requires only 540€ more investment in the semiconductors.

A more important point to notice is that for a constant switching frequency(e.g. $f_{sw} = 10kHz$) with 1830€ more investment on the semiconductors, not only the junction temperature of the MOSFETs will reduce from 150°C to 100°C but also the average efficiency for the European solar mix will increase by 0.72%. The increment in the efficiency will pay back higher initial costs of the semiconductors in a short time.

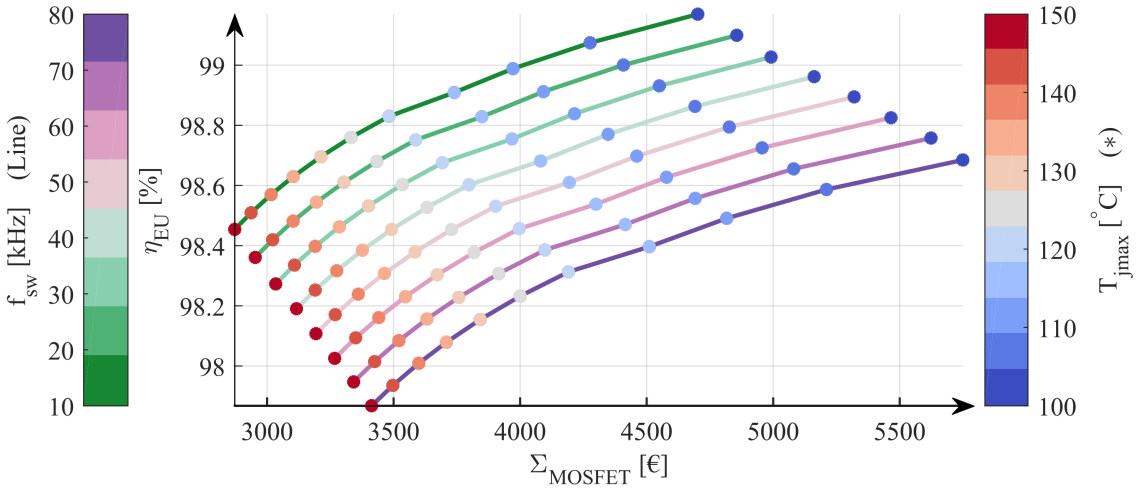
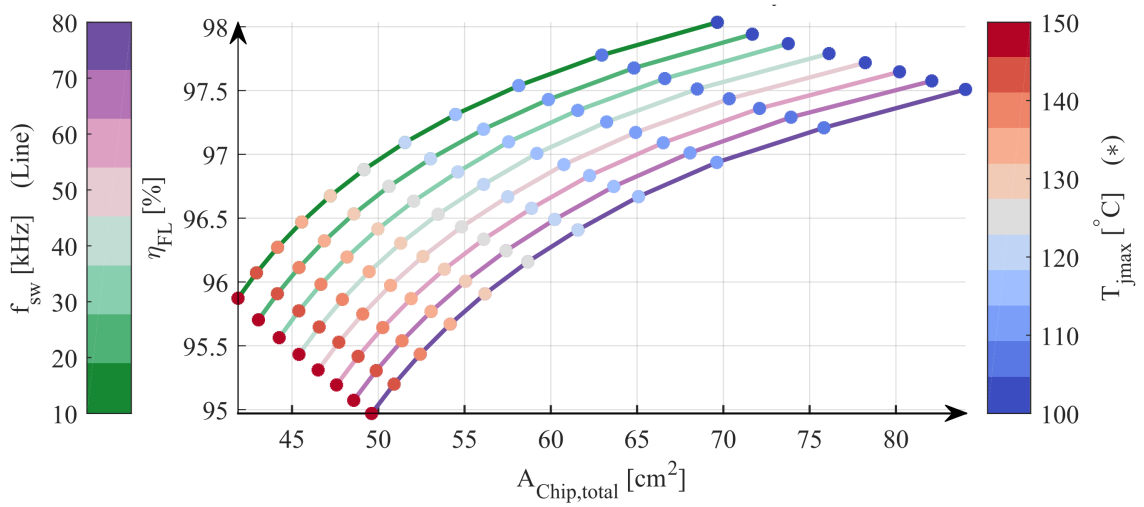


Figure 5.4: The 2L-DAB European-efficiency versus the total switch costs for various switching frequencies and different maximum junction temperatures

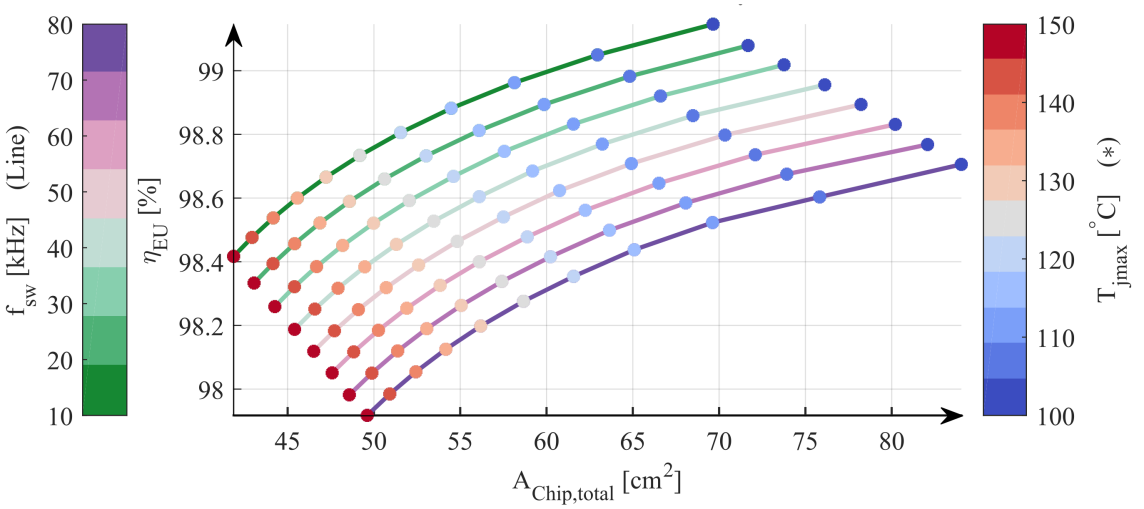
Another noticeable thing in the figure is a small break on the lines around $T_{j,max} = 115°C$ points where the rate of cost rise, increases between $T_{j,max} = 120°C$ and $T_{j,max} = 115°C$ points. It happens because, at $T_{j,max} = 120°C$ the chip-area of the switches approaches its maximum value. Therefore, it is required to increase the number of parallel connected MOSFETs to reduce the junction temperature even more and consequently the package cost will rise which will affect Σ_{MOSFET}.

5.2 The ML-DAB Results

Figure 5.5a and 5.5b shows η_{FL} and η_{EU} of the ML-DAB respectively as a function of $A_{Chip,total}$, obtained from the SABC algorithm for various f_{sw} and different $T_{j,max}$. $A_{Chip,total}$ is distributed optimally among the switches so that the junction temperature of all the switches are kept below $T_{j,max}$.



(a)



(b)

Figure 5.5: (a) The full-load efficiency, (b) the European efficiency; of the ML-DAB versus the total amount of chip-area requirement obtained from the SABC algorithm for various switching frequencies and different maximum junction temperatures

By increasing f_{sw}, $A_{Chip,total}$ grows whereas η_{FL} and η_{EU} decrease. For $70kHz$ raise in f_{sw} from $10kHz$, η_{FL} experience a rapid decline from 95.87% to 94.97% and $A_{Chip,total}$ enlarges by $7.74cm^2$. However, the reduction rate of η_{EU} is not as steep as η_{FL} where it drops only by 0.5% for a increase of f_{sw} from $10kHz$ to $80kHz$. This indicates that similar to the 2L-DAB, the switching frequency can be increased without a substantial effect on the overall efficiency.

Following the same trend as the 2L-DAB, η_{FL} and η_{EU} start to rise as the operating junction temperature is diminished. The enhancement in η_{FL} is more evident than for η_{EU}; which means that for the solar applications increasing the chip-area would not affect the overall efficiency of the ML-DAB that much.

To explore the primary causes of the efficiency improvement by the chip-area increment, the LV bridge and the MV bridge conduction and switching losses are plotted against the total chip-area. Figures 5.6 and 5.7 depict the conduction and the switching losses, respectively, for both bridges and the two switching frequencies. It can be seen that the MV bridge follows the same trend as the LV bridge in both the conduction and the switching losses.

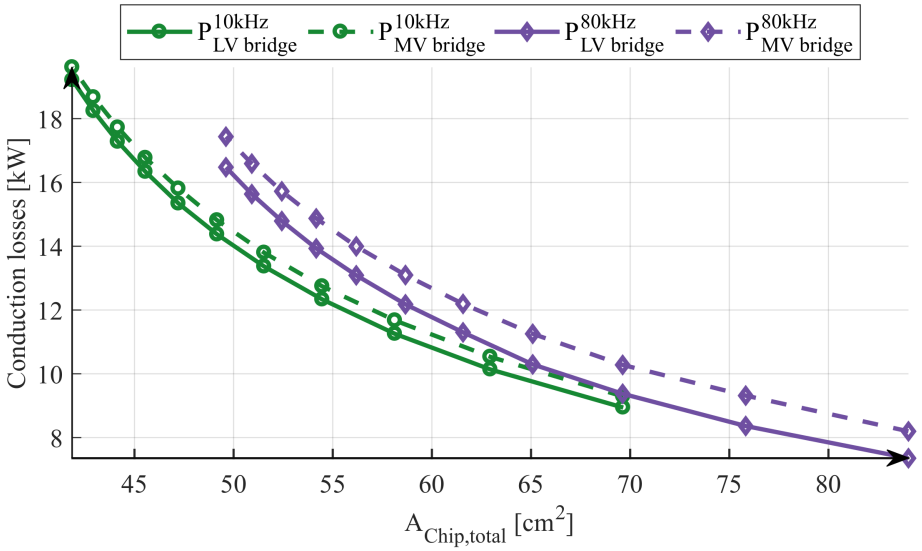


Figure 5.6: The MV bridge and the LV bridge conduction losses of the ML-DAB for two switching frequencies $f_{sw} = 10kHz$ and $f_{sw} = 80kHz$

As expected, the conduction losses are the main factor contributing to the efficiency improvement by the chip-area increment for both switching frequencies. For instance, with the switching frequency of $10kHz$, a 66% increase in the chip size from the minimum value results in 53% reduction in the conduction losses. This is due to high on-resistance of the MOSFETs that varies inversely proportional to the chip-area.

It is noteworthy that the effect of the switching loss reduction on the efficiency improvement becomes more pronounced as the switching frequency increase, while its effect is negligible compared to the effect of the conduction losses for the low switching frequencies.

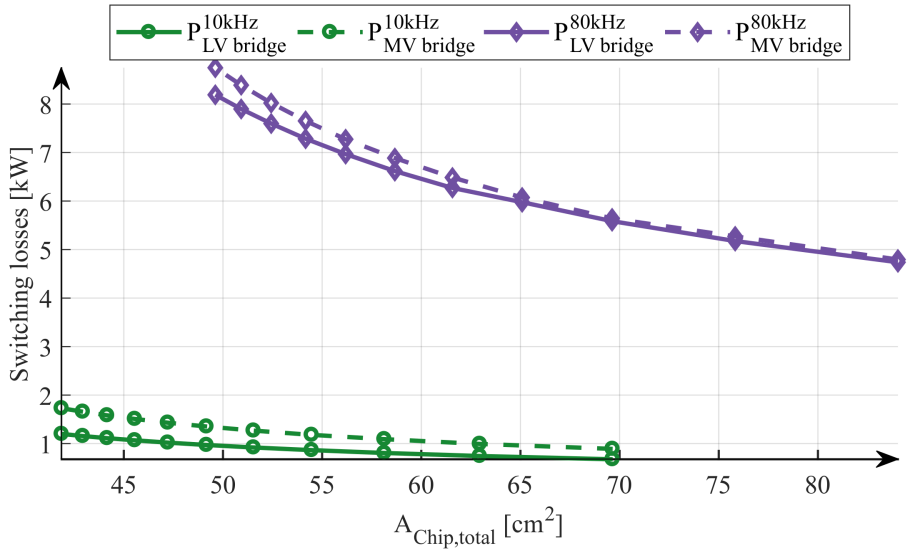


Figure 5.7: The MV bridge and the LV bridge switching losses of the ML-DAB for two switching frequencies $f_{sw} = 10kHz$ and $f_{sw} = 80kHz$

The efficiency versus the semiconductors cost of the ML-DAB is depicted in Figure 5.8. Since the relation between the cost and the chip-area is linear, the graphs have the same trend as Figure 5.5b. Due to higher chip requirement of the ML-DAB than 2L-DAB, the total semiconductor cost is slightly higher for ML-DAB.

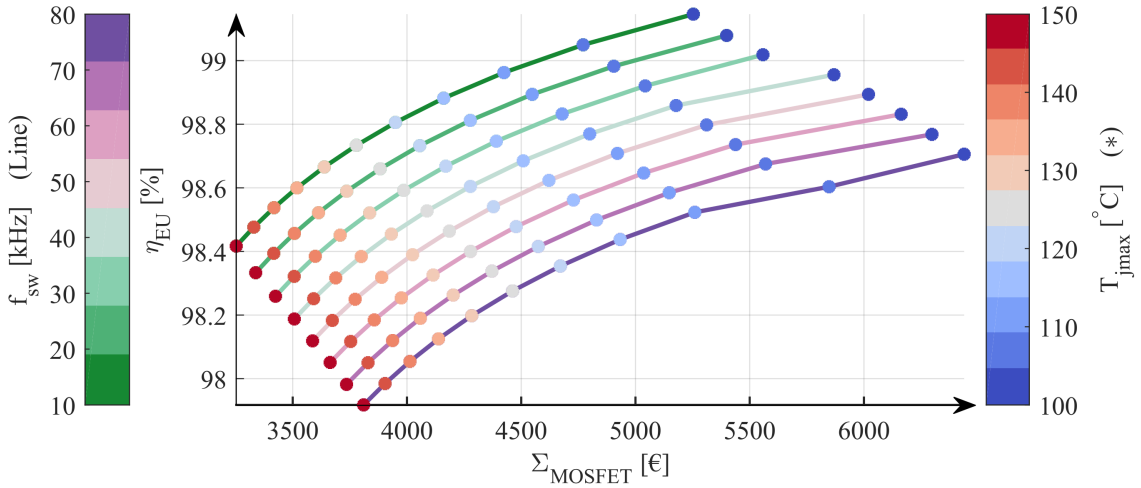
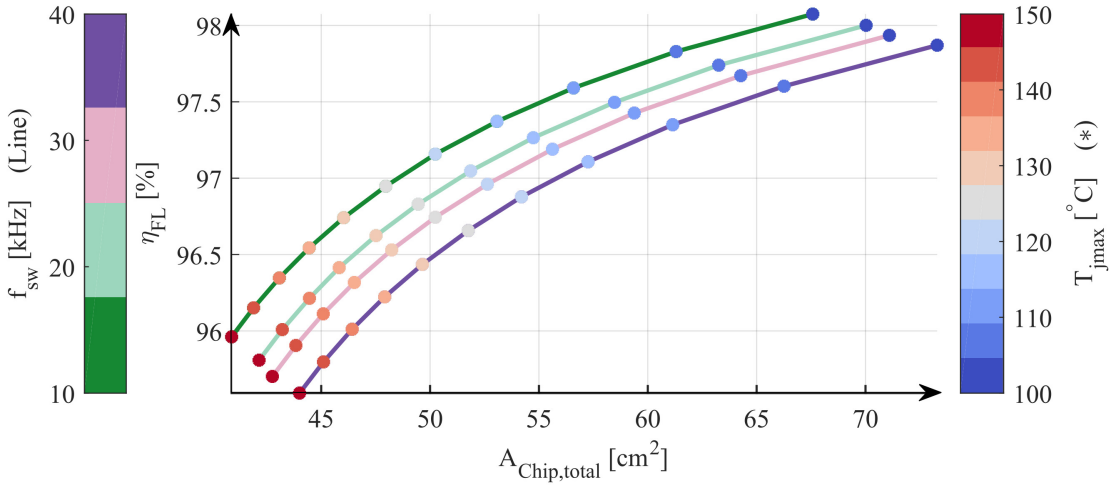


Figure 5.8: The ML-DAB European-efficiency versus the total switch costs for various switching frequencies and different maximum junction temperatures

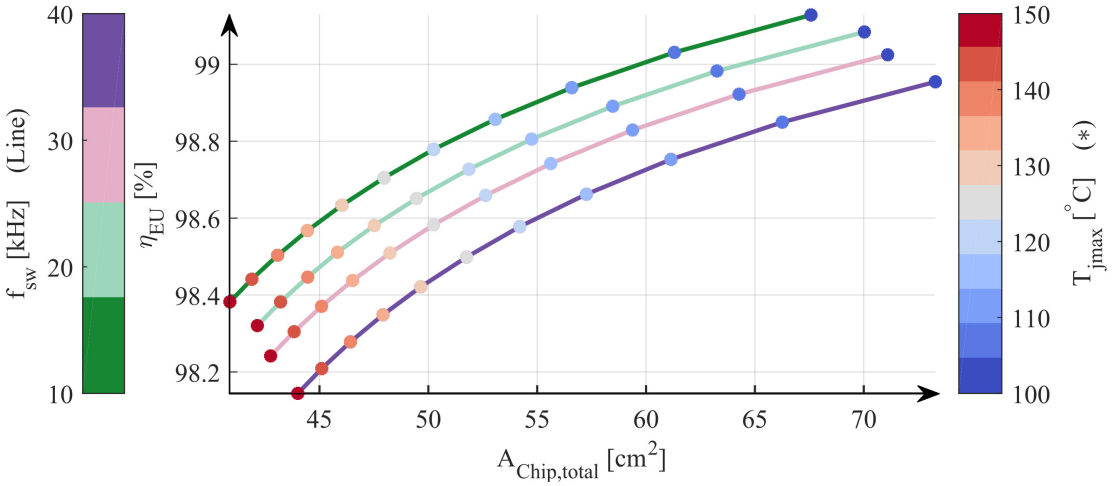
5.3 The 3L-DAB Results

Figure 5.9a and 5.9b shows η_{FL} and η_{EU} of the 3L-DAB respectively as a function of $A_{Chip,total}$, obtained from the SABC algorithm for various f_{sw} and different $T_{j,max}$. Because of convergence issues in the SABC algorithm for this topology, the results are obtained for $T_{j,max} \pm 3°C$ instead of $T_{j,max}$. Due to, the maximum variation of

3°C in the maximum junction temperature, comparing the results of this converter with other topologies is not possible, and it won't be presented here. However, as can be seen from the figures, by less than 70% increase in the chip-area, the full-load efficiency and the average efficiency for European solar mix of 3L-DAB can be improved by more than 2% and 0.7% respectively for all switching frequency ranges.



(a)



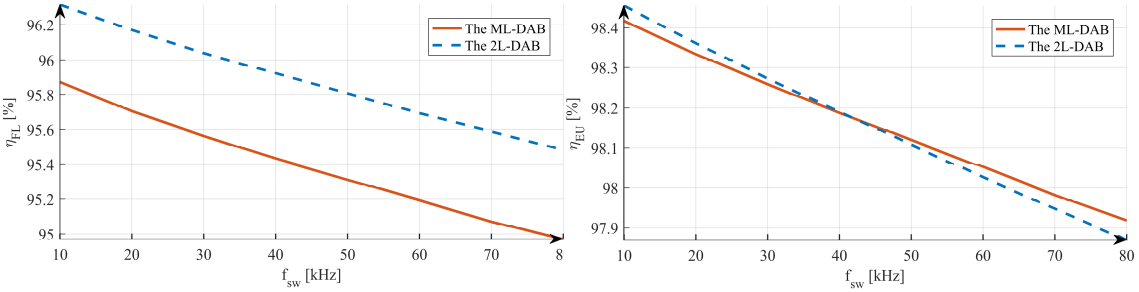
(b)

Figure 5.9: (a) The full-load efficiency, (b) the European efficiency; of the 3L-DAB versus the total amount of chip-area requirement obtained from the SABC algorithm for various switching frequencies and different maximum junction temperatures

5.4 Converter Topologies Comparison

Figure 5.10a shows the full-load efficiency of the 2L-DAB and the ML-DAB as a function of the switching frequency for the MOSFETs junction temperature of 150°C. The dashed blue and the solid red lines represent the 2L-DAB and the

ML-DAB efficiencies respectively. The 2L-DAB outperforms the ML-DAB in the full-load operation. There is a difference of 0.44% between the full-load efficiencies at $f_{sw} = 10kHz$ which increases to 0.51% at $f_{sw} = 80kHz$.

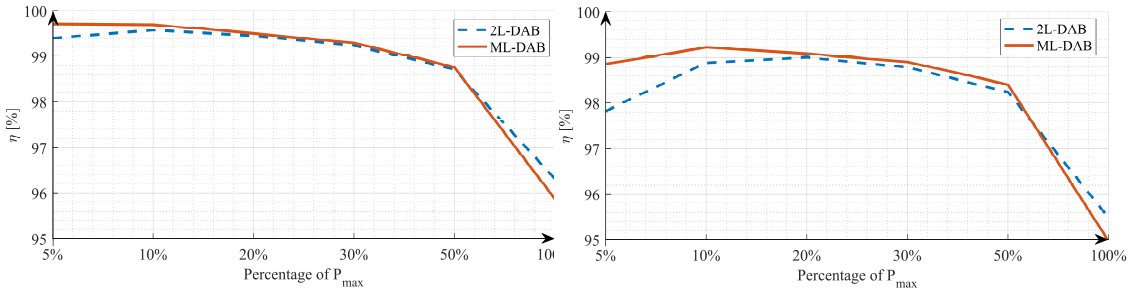


(a) **(b)**

Figure 5.10: (a) The full-load efficiency, (b) The European efficiency; of the 2L-DAB and the ML-DAB as a function of the switching frequency for the junction temperature of $150°C$

The average efficiency for the European solar mix of the converters is shown in Figure 5.10b. The investigation of the average efficiency for the European solar mix shows that not only the disparity between the converter's efficiencies is reduced, but also they intersect each other at $f_{sw} = 40kHz$. In switching frequencies below $40kHz$, the 2L-DAB is superior. Whereas above $40kHz$, the ML-DAB performs better.

As the full-load performance of the ML-DAB is inferior to the 2L-DAB, the reason for intersection in η_{EU} should be in the partial load operating conditions. Figure 5.11 depicts the decomposition of the converters efficiencies in the partial loads for two frequencies; one above and one below the intersection point.



(a) **(b)**

Figure 5.11: The converter's efficiency decomposition for the partial loads (a) $f_{sw} = 10kHz$, (b) $f_{sw} = 80kHz$

In the partial loads below 50% of the rated power, the ML-DAB has higher efficiency than the 2L-DAB for both frequencies whereas, in the full load, the 2L-DAB outperforms the ML-DAB. It is noteworthy that 80% of contribution to the average efficiency for the European solar mix comes from 5% to 50% of the rated power range

where the ML-DAB is superior. In high frequencies, the gap between the efficiencies of the two topologies increases in this power range which results in a crossing point in the European efficiency.

Figures 5.12 and 5.13 show the decomposition of the loss components for different loading conditions of the converters at $f_{sw} = 10kHz$ and $f_{sw} = 80kHz$ respectively. The losses are represented as a percentage of the transmitted power; which itself is denoted by the superscript of $P_{M/2L-DAB}$ on the x-axis.

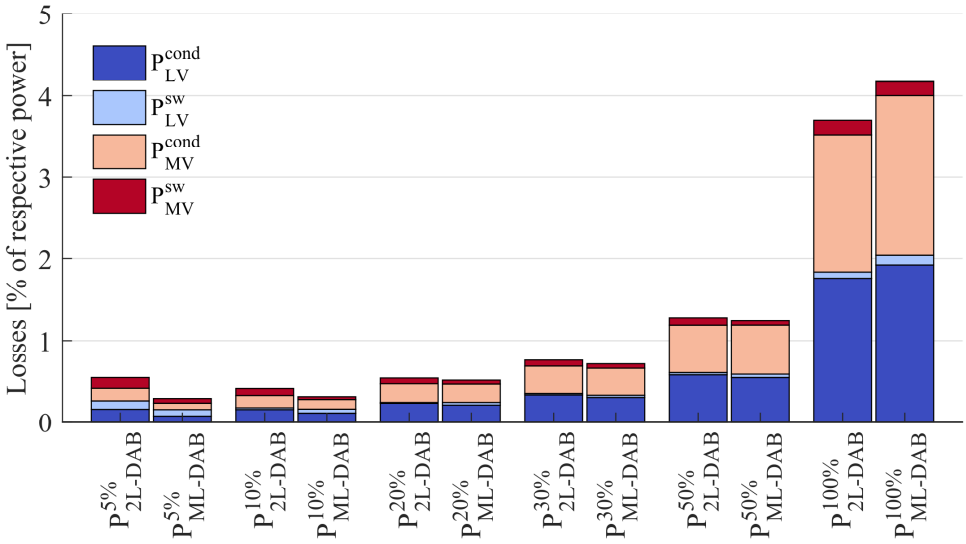


Figure 5.12: The decomposition of the loss components for the partial-loads and the full-load operation of the converters at $f_{sw} = 10kHz$

Excluding the conduction losses which are the primary factor in reducing the total efficiency (particularly at low frequencies), the main differentiating loss component in the partial loads and the high frequencies is the MV-side switching losses. It can be seen that the MV-bridge switching losses of the ML-DAB are lower than the 2L-DAB in both of the frequencies. However, this difference becomes more evident as the switching frequency increases. Since this difference also exists in the full load, it can not be due to the loss of the ZVS during the turn-on period.

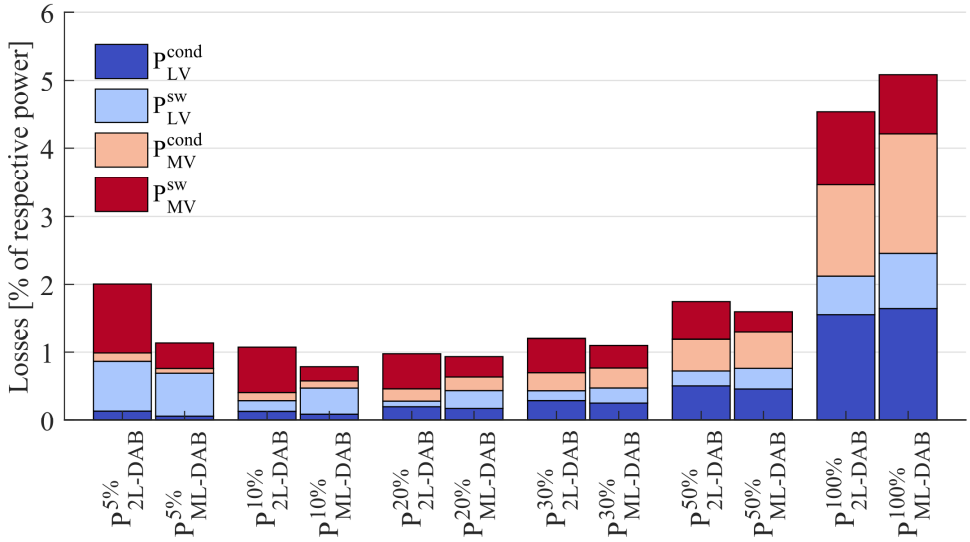


Figure 5.13: The decomposition of the loss components for the partial-loads and the full-load operation of the converters at $f_{sw} = 80kHz$

Figure 5.14 illustrate the current and the voltage waveforms of the MOSFETs of the 2L-DAB in the full-load, $T_{j,max} = 150°C$, and $f_{sw} = 80kHz$. The left axis depicts the voltage across the switch, and the current is shown on the right axis. All of the MOSFETs turn on under the ZVS condition.

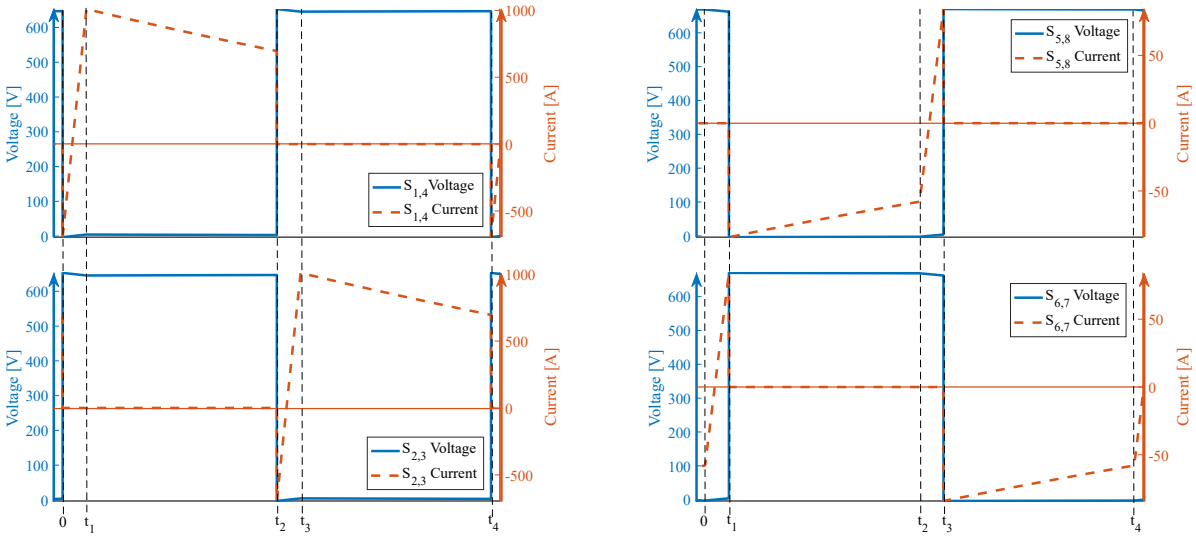


Figure 5.14: The 2L-DAB MOSFET's current and voltage waveforms in the full-load and $f_{sw} = 80kHz$

Figures 5.15 and 5.16 shows the current and the voltage waveforms across the MOSFETs of the ML-DAB in the LV bridge and the MV bridge respectively in the full-load, $T_{j,max} = 150°C$, and $f_{sw} = 80kHz$. Inspection of the waveforms shows that all of the switches retain the ZVS during turn-on. However compared to the 2L-DAB counterparts, the MV bridge's MOSFETs of the ML-DAB are snapping lower currents during the turn-off; which results in lower switching losses at the MV-side of the ML-DAB.

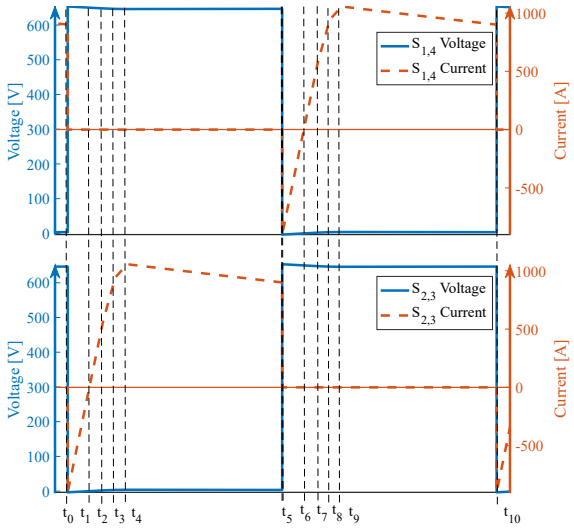


Figure 5.15: The ML-DAB LV bridge MOSFET's current and voltage waveforms in the full-load and $f_{sw} = 80kHz$

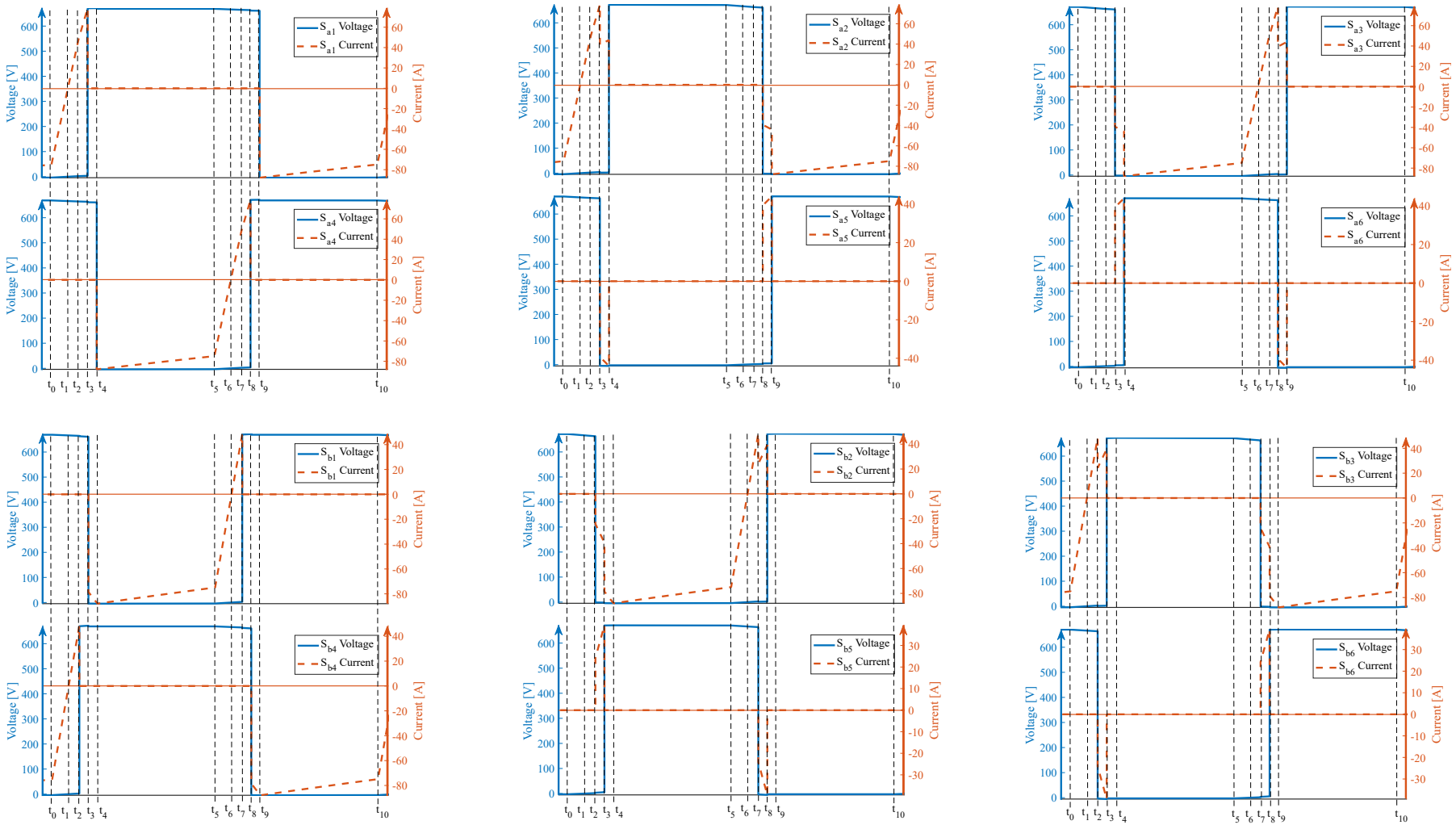


Figure 5.16: The ML-DAB MV bridge MOSFET's current and voltage waveforms in the full-load and $f_{sw} = 80kHz$

To see how the losses are distributed among the switches, the decomposition of the loss components and the required chip-area for each MOSFET of the 2L-DAB is depicted in Figure 5.17. The switching frequency is $10kHz$, and the junction temperature is confined to $150°C$. The MOSFETs marked with the same outline and color have similar losses and chip-area.

The diagonal MOSFETs in each bridge conducts the same currents; as the bridges are operating with 50% duty cycle. On the other hand, the outputs of both bridges on the AC link are symmetrical waveforms which means that on the positive and the negative cycles of the AC-link voltage, the respective MOSFETs will conduct identical currents as was shown in Figure 5.14. Therefore, all MOSFETs in each bridge have similar losses and require the same chip-area.

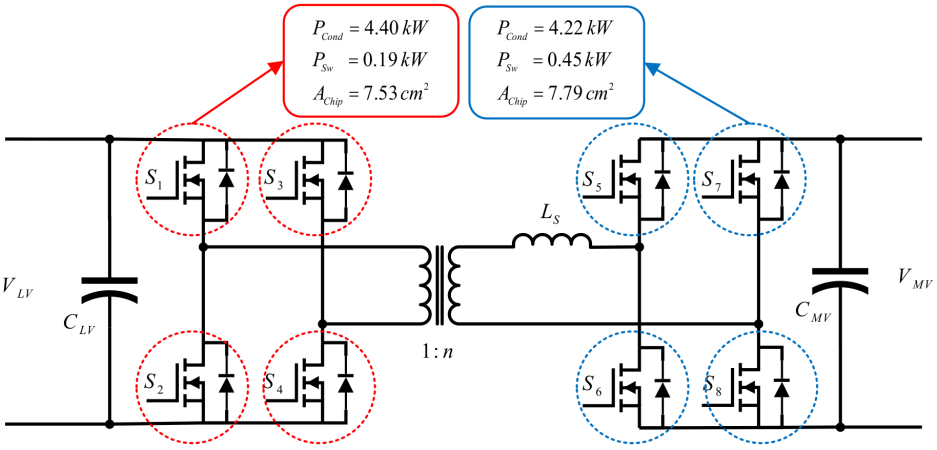


Figure 5.17: The required chip-area and the switching and the conduction losses of each switch in the 2L-DAB for $T_{j,max} = 150°C$, and $f_{sw} = 10kHz$ (the shapes with the same outline and color have similar parameter).

Figure 5.18 shows the switching and the conduction losses for the MOSFETs of the ML-DAB for the switching frequency of $10kHz$ and the junction temperature of $150°C$. Because of the same reasons as mentioned for the 2L-DAB, the LV bridge MOSFETs have the same parameters. However, the situation is different on the MV side. To form the intermediate level of the voltage waveforms, leg A and leg B MOSFETs do not switch at the same time(As depicted in Figure 5.16) which results in different losses and needed chip-area for the two legs.

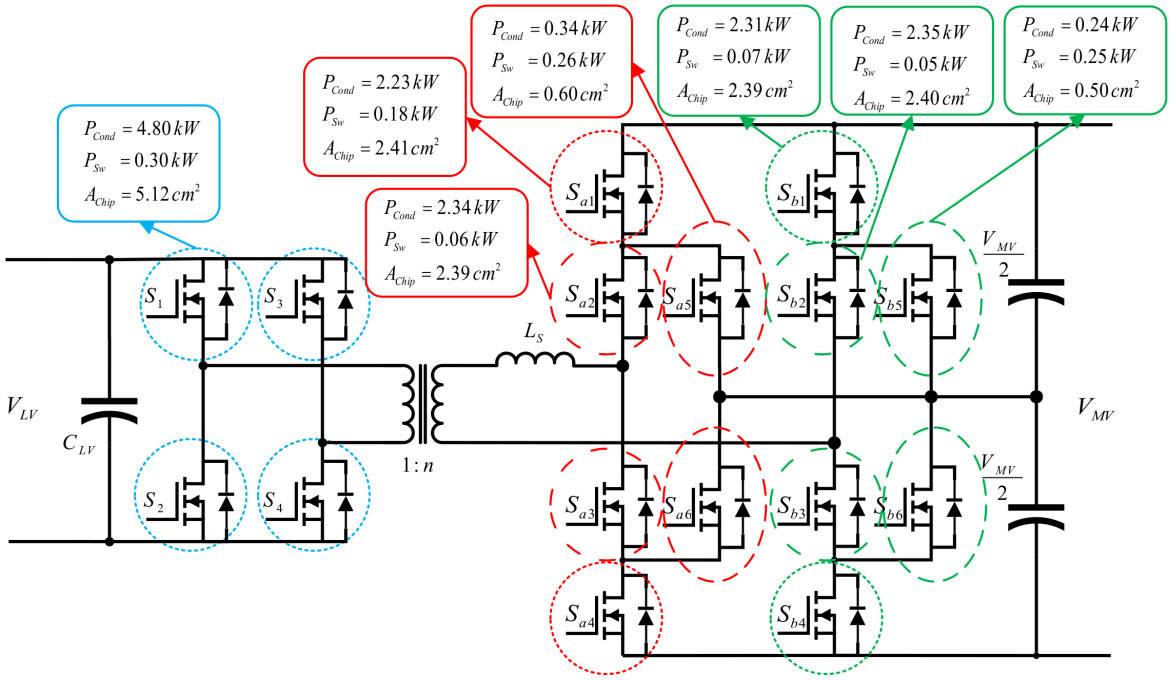
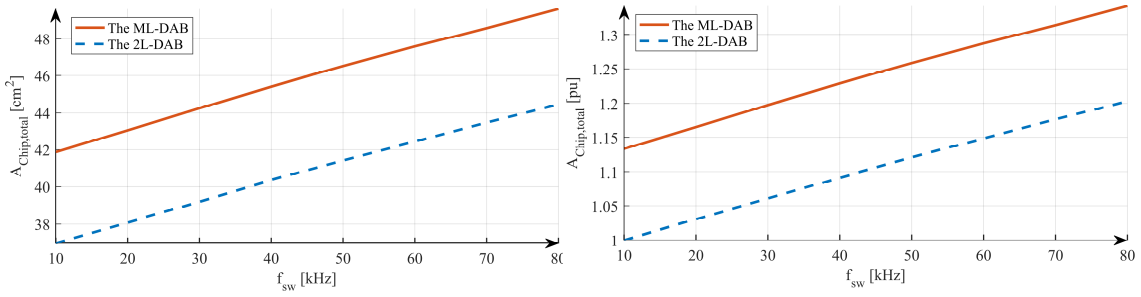


Figure 5.18: The required chip-area and the switching and the conduction losses of each switch in the ML-DAB for $T_{j,max} = 150°C$, and $f_{sw} = 10kHz$ (the shapes with the same outline and color have similar parameter).

Even though the ML-DAB is superior efficiency-wise in the switching frequencies higher than $40kHz$, it requires higher chip-area than the 2L-DAB as depicted in Figure 5.19. If the total chip-area of the 2L-DAB in $f_{sw} = 10kHz$ is considered as a base value, designing a 2L-DAB for $f_{sw} = 80kHz$ will require 20.3% higher chip-area. While for the ML-DAB, these values are 13.3% and 14% higher.



(a) **(b)**

Figure 5.19: The total chip-area requirement of the 2L-DAB and the ML-DAB for different switching frequencies and the junction temperature of $150°C$

Figure 5.20 shows the average efficiencies for the European solar mix of the 2L-DAB and the ML-DAB versus the switching frequency for two values of the total required chip-area. The markers colors denote the maximum junction temperature. For the same amount of total chip-area, the 2L-DAB outperforms the ML-DAB both from the efficiency and the junction temperature points of view. In other words, the 2L-

DAB can achieve higher efficiency and lower junction temperature in all switching frequencies for the same amount of total chip size.

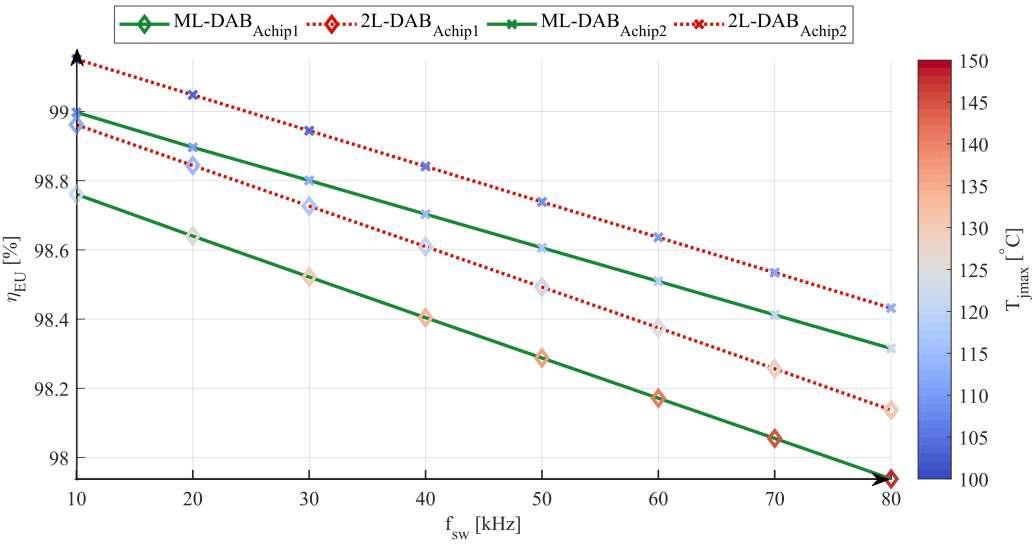


Figure 5.20: The average efficiency for the European solar mix of the 2L-DAB and the ML-DAB as a function of the switching frequency for $A_{chip1} = 50cm^2$ and $A_{chip2} = 60cm^2$

Figure 5.21 depicts the average efficiency for the European solar mix of the converters versus the switching frequency for two semiconductor costs of 3900€ and $Cost2 =$ 4700€. The trends are quite similar to the case of constant chip size(Figure 5.20), and identical conclusions can be made.

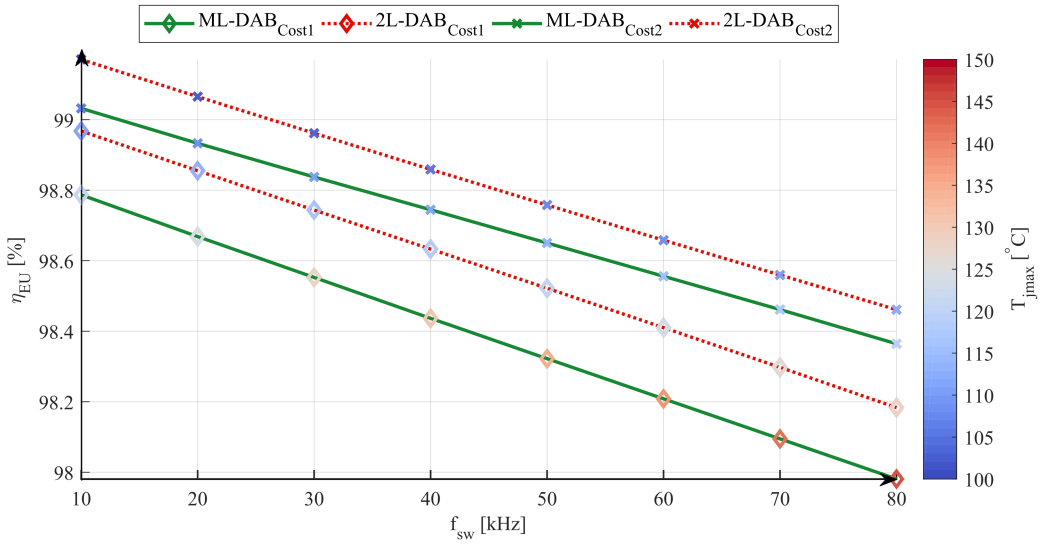


Figure 5.21: The average efficiency for the European solar mix of the 2L-DAB and the ML-DAB as a function of the switching frequency for $Cost1 = 3900€$ and $Cost2 = 4700€$

6
Conclusions and Future Work

The 2L-DAB and the ML-DAB 1MW DC-DC converters are compared based on their efficiencies and the total required chip-area for the PV applications. The chip-area of the MOSFETs is optimized such that the junction temperature is confined to 150°C. The switching frequency is swept from 10 kHz to 80 kHz. The chip-area of the MOSFETs is also varied to achieve lower operating junction temperatures.

6.1 Results From Present Work

It has been shown that for the considered ratings, the operating conditions, and the same operating junction temperature for all MOSFETs the 2L-DAB outperforms the ML-DAB efficiency-wise in the full load while it requires less chip size. However, it was observed that due to a better performance of the ML-DAB in the partial loads and high switching frequencies, higher average efficiency for the European solar mix could be achieved for the ML-DAB in the switching frequencies greater than 40 kHz.

It was also demonstrated that for the same amount of total chip size (or the same amount of initial investment on the semiconductors), the 2L-DAB can achieve higher full-load efficiency and average efficiency for European solar mix, while the operating junction temperature of the MOSFETs are lower than the ML-DAB ones.

Another observation was that, for the LV bridges of both the 2L-DAB and the ML-DAB, only one type of MOSFET is required in order to reach the same junction temperature on all of the switches. The same is true for the MV bridge of the 2L-DAB; whereas to operate the MV-side MOSFETs of the ML-DAB in the same junction temperatures, six types of MOSFETs with different chip-areas are needed.

It was also shown that by less than 70% increase in the required chip-area, the full-load efficiency and the average efficiency for European solar mix of all three converters can increase more than 2% and 0.7% respectively for all switching frequency ranges.

6.2 Future Work

- Other topologies than the compared ones and their three-phase counterparts can also be considered for the comparison in the future.

- A simple model without the losses was considered for the MFT while for an accurate analysis it is also required to model the MFT.
- The modulation parameters were selected based on a trial and error method. As the SABC algorithm is highly dependent on these parameters, it is advised to perform an optimization on them, before making the comparison.
- It was assumed that the cooling system was keeping the heatsink temperature at a constant value, whereas, it is suggested to be modeled in the future.
- The MOSFETs were the only utilized switches in this thesis. It would be interesting to contrast different topologies or even a single topology with different switches (e.g., IGBTs or a combination of both).

Bibliography

[1] Alex Q. Huang. "Medium-Voltage Solid-State Transformer: Technology for a Smarter and Resilient Grid". In: *IEEE Industrial Electronics Magazine* 10.3 (2016), pp. 29–42. ISSN: 1932-4529. DOI: 10.1109/mie.2016.2589061.

[2] She Xu, Alex Q. Huang, and Rolando Burgos. "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 1.3 (2013), pp. 186–198. ISSN: 2168-6777 2168-6785. DOI: 10.1109/jestpe.2013.2277917.

[3] Bram Buijs. "China and the Future of New energy Technologies". In: *Clingendael International Energy Programme, viewed* 14 (2012).

[4] Denis Lenardic. *Large-scale PV power plants*. [online] Available http://www.pv-resources.com.

[5] Hafiz Abu Bakar Siddique, Syed Mansoor Ali, and Rik W. De Doncker. "DC collector grid configurations for large photovoltaic parks". In: (2013), pp. 1–10. DOI: 10.1109/epe.2013.6631799.

[6] Hafiz Abu Bakar Siddique and Rik W. De Doncker. "Evaluation of DC Collector-Grid Configurations for Large Photovoltaic Parks". In: *IEEE Transactions on Power Delivery* (2017), pp. 1–1. ISSN: 0885-8977 1937-4208. DOI: 10.1109/tpwrd.2017.2702018.

[7] B. Zhao, Q. Song, W. Liu, et al. "Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System". In: *IEEE Transactions on Power Electronics* 29.8 (2014), pp. 4091–4106. ISSN: 0885-8993. DOI: 10.1109/TPEL.2013.2289913.

[8] MA Bahmani, K Vechalapu, M Mobarrez, et al. "Flexible HF distribution transformers for inter-connection between MVAC and LVDC connected to DC microgrids: Main challenges". In: *DC Microgrids (ICDCM), 2017 IEEE Second International Conference on*. IEEE, pp. 53–60. ISBN: 1509044795.

[9] M. A. Moonem and H. Krishnaswami. "Control and configuration of three-level dual-active bridge DC-DC converter as a front-end interface for photovoltaic system". In: *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, pp. 3017–3020. ISBN: 1048-2334. DOI: 10.1109/APEC.2014.6803734.

[10] H. A. B. Siddique, A. R. Lakshminarasimhan, C. I. Odeh, et al. "Comparison of modular multilevel and neutral-point-clamped converters for medium-voltage grid-connected applications". In: *2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA)*, pp. 297–304. DOI: 10.1109/ICRERA.2016.7884555.

[11] D. Krug, S. Bernet, S. S. Fazel, et al. “Comparison of 2.3-kV Medium-Voltage Multilevel Converters for Industrial Medium-Voltage Drives”. In: *IEEE Transactions on Industrial Electronics* 54.6 (2007), pp. 2979–2992. ISSN: 0278-0046. DOI: 10.1109/TIE.2007.906997.

[12] D. Krug, S. Bernet, and S. Dieckerhoff. “Comparison of state-of-the-art voltage source converter topologies for medium voltage applications”. In: *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003.* Vol. 1, 168–175 vol.1. DOI: 10.1109/IAS.2003.1257499.

[13] T. Friedli and J. W. Kolar. “A Semiconductor Area Based Assessment of AC Motor Drive Converter Topologies”. In: *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 336–342. ISBN: 1048-2334. DOI: 10.1109/APEC.2009.4802678.

[14] M. Schweizer, I. Lizama, T. Friedli, et al. “Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies”. In: *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, pp. 391–396. ISBN: 1553-572X. DOI: 10.1109/IECON.2010.5674994.

[15] T. Friedli, J. W. Kolar, J. Rodriguez, et al. “Comparative Evaluation of Three-Phase AC-AC Matrix Converter and Voltage DC-Link Back-to-Back Converter Systems”. In: *IEEE Transactions on Industrial Electronics* 59.12 (2012), pp. 4487–4510. ISSN: 0278-0046. DOI: 10.1109/TIE.2011.2179278.

[16] Thomas Friedli. “Comparative evaluation of three-phase Si and SiC ac-ac converter systems”. Thesis. 2010.

[17] Benoit Bletterie, Roland Bründlinger, Heinrich Häberlin, et al. “Redefinition of the European efficiency–finding the compromise between simplicity and accuracy”. In: *Proc. EU PVSEC* (2008), pp. 2735–2742.

[18] *C2M0160120D: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode.* [online] Available http://www.wolfspeed-.com/. Cree.

[19] *C2M0080120D: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode.* [online] Available http://www.wolfspeed-.com/. Cree.

[20] *C2M0040120D: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode.* [online] Available http://www.wolfspeed-.com/. Cree.

[21] *C2M0025120D: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode.* [online] Available http://www.wolfspeed-.com/. Cree.

[22] *CPM2-1200-0160B: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode.* [online] Available http://www.wolfspeed-.com/. Cree.

[23] *CPM2-1200-0080B: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode.* [online] Available http://www.wolfspeed-.com/. Cree.

[24] *CPM2-1200-0040B: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode.* [online] Available http://www.wolfspeed-.com/. Cree.

[25] *CPM2-1200-0025B: Silicon Carbide Power MOSFET, C2M MOSFET technology N-channel enhancement mode*. [online] Available http://www.wolfspeed-.com/. Cree.

[26] K. L. Pandya and W. McDaniel. "A simplified method of generating thermal models for power MOSFETs". In: *Eighteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium. Proceedings 2002 (Cat.No.02CH37311)*, pp. 83–87. ISBN: 1065-2221. DOI: 10.1109/STHERM.2002.991350.

[27] R. M. Burkart and J. W. Kolar. "Comparative $\eta-\rho-\sigma$ Pareto Optimization of Si and SiC Multilevel Dual-Active-Bridge Topologies With Wide Input Voltage Range". In: *IEEE Transactions on Power Electronics* 32.7 (2017), pp. 5258–5270. ISSN: 0885-8993. DOI: 10.1109/TPEL.2016.2614139.

[28] Ralph Burkart and Johann W Kolar. "Component cost models for multi-objective optimizations of switched-mode power converters". In: *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*. IEEE, pp. 2139–2146. ISBN: 1479903361.

[29] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala. "A three-phase soft-switched high-power-density DC/DC converter for high-power applications". In: *IEEE Transactions on Industry Applications* 27.1 (1991), pp. 63–73. ISSN: 0093-9994. DOI: 10.1109/28.67533.

[30] C. Mi, H. Bai, C. Wang, et al. "Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter". In: *IET Power Electronics* 1.4 (2008), pp. 507–517. ISSN: 1755-4535. DOI: 10.1049/iet-pel:20080004.

[31] M. A. Moonem and H. Krishnaswami. "Analysis and control of multi-level dual active bridge DC-DC converter". In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1556–1561. ISBN: 2329-3721. DOI: 10.1109/ECCE.2012.6342628.

[32] MA Moonem, CL Pechacek, R Hernandez, et al. "Analysis of a multilevel dual active bridge (ML-DAB) DC-DC converter using symmetric modulation". In: *Electronics* 4.2 (2015), pp. 239–260.

[33] A Filba-Martinez, Sergio Busquets-Monge, and J Bordonau. "Modulation and capacitor voltage balancing control of a three-level NPC dual-active-bridge DC-DC converter". In: *Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE*. IEEE, pp. 6251–6256. ISBN: 1479902241.

[34] Alber Filba-Martinez, Sergio Busquets-Monge, Joan Nicolas-Apruzzese, et al. "Operating Principle and Performance Optimization of a Three-Level NPC Dual-Active-Bridge DC–DC Converter". In: *IEEE Transactions on Industrial Electronics* 63.2 (2016), pp. 678–690. ISSN: 0278-0046.

[35] Plexim GmbH. *PLECS-user manual*. 2017.

[36] B. Backlund, M. Rahimo, S. Klaka, et al. "Topologies, voltage ratings and state of the art high power semiconductor devices for medium voltage wind energy conversion". In: *2009 IEEE Power Electronics and Machines in Wind Applications*, pp. 1–6. DOI: 10.1109/PEMWA.2009.5208365.

[37] H. Bai and C. Mi. "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge DC-DC Converters Using Novel

Dual-Phase-Shift Control". In: *IEEE Transactions on Power Electronics* 23.6 (2008), pp. 2905–2914. ISSN: 0885-8993. DOI: 10.1109/TPEL.2008.2005103.