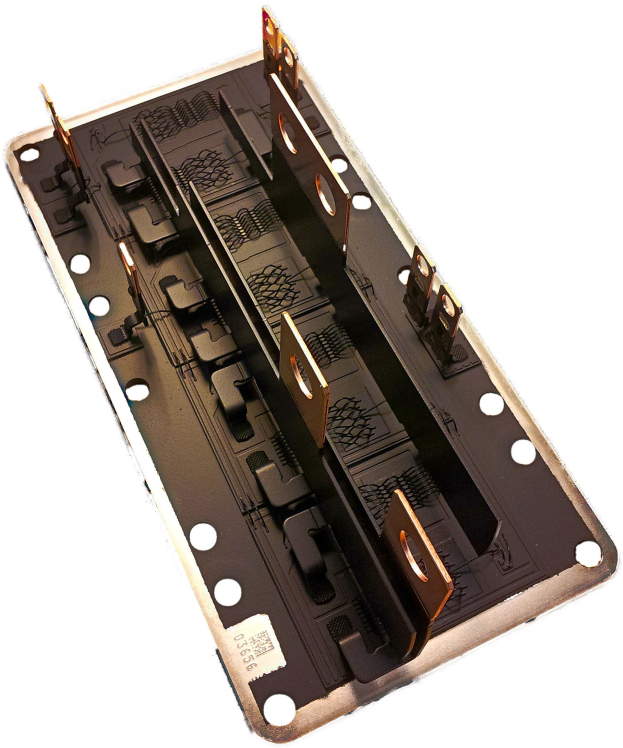
CHALMERS
UNIVERSITY OF TECHNOLOGY



Power Losses and Thermal Impedance Characterization of Power Modules

Master's thesis in Electric Power Engineering

KONSTANTINOS GIANNOULOUDIS

Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2015

Master's thesis 2015:06

Power Losses and Thermal Impedance Characterization of Power Modules

KONSTANTINOS GIANNOULOUDIS



CHALMERS
UNIVERSITY OF TECHNOLOGY

Department of Energy and Environment
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2015

Power Losses and Thermal Impedance Characterization of Power Modules
KONSTANTINOS GIANNOULOUDIS

© KONSTANTINOS GIANNOULOUDIS, 2015.

Supervisor: Dr Jonas Ottosson, Advanced Technology and Research Department, Volvo Group Trucks Technology
Examiner: Prof Yujing Liu, Energy and Environment Department, Chalmers University of Technology

Master's Thesis 2015:06
Department of Energy and Environment
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Telephone +46 31 772 1000

Cover: The Infineon™ FF600R12IE4 IGBT Power Module.

Typeset in LaTeX
Printed by [Chalmers Reproservice]
Gothenburg, Sweden 2015

Power Losses and Thermal Impedance Characterization of Power Modules
KONSTANTINOS GIANNOULOUDIS
Department of Energy and Environment
Chalmers University of Technology

Abstract

The trend of electrification in automotive industry over the last years, has lead to the production of numerous vehicles that have either fully electric or hybrid drive-trains. The main component of the power electronics in the drive-train of such vehicles, are the power modules. During driving cycles, the heat produced from power losses at power electronics, forces the power modules to thermal cycling, consequently to thermal-mechanical stress. Thus, sufficient knowledge of the power losses and the thermal behavior of the power modules is necessary for the sake of proper dimensioning and reliability. This thesis deals with the measurement of power losses for an IGBT power module, the extraction of the power losses according to its manufacturer and the comparison between them. In addition, a Finite Element model of a power module is built and verified with experimental measurements, to extract the self and mutual thermal impedances of its silicon chips. As a result, look-up tables with power losses of the power module in several operating points are obtained, as well as mathematical models that describe the thermal behavior of the module are derived after simulations.

Keywords: IGBT, Module, Power, Losses, Thermal, Impedance, Coupling, FEM, Convection, Material.

Acknowledgements

Primarily I would like to thank my supervisor Dr Jonas Ottosson for his continuous support and restless guidance throughout the whole duration of this thesis. It is a privilege to work with such a talented person.

I would also like to thank my examiner from Chalmers, Professor Yujing Liu for his clear advice and effective cooperation.

Many thanks go also to the staff of ATR Department of Volvo Trucks for their willingness to help and answer questions.

Lastly and most remarkably, I would like to thank my family for supporting me all these years. My father Georgios for his calm and balanced suggestions whenever I feel in doubt. My mother Naouma for patiently listening to my thoughts and encouraging me. My brothers Stelios and Alexandros for being there, eager to help and visiting me when I needed it. Niki, you have been the cornerstone for what I am now.

Konstantinos Giannouloudis, Gothenburg, June 2015

Contents

List of Figures **x**

List of Tables **xiii**

1 Introduction **1**
1.1 Electric drive systems . . . 1
1.2 Power electronics . . . 2
1.3 The Insulated Gate Bipolar Transistor . . . 3
1.4 Theory of thermal models . . . 6
1.5 Problem presentation . . . 7
1.6 Objectives . . . 10

2 Power Losses **13**
2.1 Power loss modeling . . . 13
2.2 Calculations according to manufacturer data . . . 16
2.3 Experimental determination . . . 22
2.3.1 Task description . . . 22
2.3.2 Method description . . . 22
2.3.3 Test setup . . . 23
2.3.4 Measurements and results . . . 25
2.4 Comparison of manufacturer and measured data . . . 31
2.4.1 Conduction losses . . . 31
2.4.2 Switching losses . . . 34
2.5 Correlation of measurements with higher temperatures . . . 35
2.6 Discussion . . . 36

3 Thermal Measurements **39**
3.1 Convection coefficient . . . 39
3.1.1 Analytical calculations . . . 39
3.1.2 Experimental determination . . . 42
3.1.3 Discussion . . . 45
3.2 Calibration of chip temperature measurements . . . 46
3.2.1 Climate chamber test - $U_{ce}(T)$ determination . . . 46
3.2.2 Transient chip temperature measurements . . . 49
3.2.3 Discussion . . . 55

4 Finite Element Calculations and Foster Networks **57**
4.1 Finite Element Model 57
4.1.1 Initial FEM model 57
4.1.2 Improvements on FEM model 60
4.1.3 Discussion on Finite Element Model 63
4.2 Foster Networks 64
4.2.1 Derivation of the Foster equivalent 64
4.2.2 Discussion on Foster networks 66

5 Conclusions and Future Work **69**
5.1 Conclusions 69
5.2 Future work 70

Bibliography **70**

A Appendix 1 **I**
A.1 Power losses measurement equipment and look-up tables example . . I
A.2 Climate chamber test results III
A.3 Module Geometry and Finite Element Analysis specifications IV

List of Figures

1.1 Electric motor control loop. 1
1.2 IGBT power module package and its equivalent circuit. 2
1.3 The layout of a n-channel IGBT. 3
1.4 Symbol and equivalent circuit of an IGBT. 4
1.5 The IGBT output characteristics for different parameters. 5
1.6 The physical layout of a power module. 5
1.7 The Cauer equivalent network. 7
1.8 The Foster equivalent circuit. 7
1.9 Two different driving cycles for a hybrid vehicle with the corresponding rotational speed and torque for the electrical motor versus time. . 8
1.10 Complete simulation model of drive system. 8
1.11 The power module topology. 10
1.12 The power module layout with the name of each chip and the module layers. 10

2.1 The turn ON, turn OFF curves and the energy losses of an IGBT. . . 14
2.2 Stray inductance equivalent circuit. 15
2.3 The IGBT and diode output characteristics. 16
2.4 The IGBT switching losses for various operating points. 17
2.5 The diode switching losses for various operating points. 18
2.6 Comparison between conduction power losses calculated from manufacturer data and calculated after curve fitting according to (2.15), for the IGBT and diode respectively. 19
2.7 Switching losses of the IGBT for 125 and 150 ℃ and $R_g = 1.8\ \Omega$. . . 21
2.8 Switching losses of the diode for 125 and 150 ℃ and $R_g = 1.8\ \Omega$. . . 21
2.9 The VPEC with its internal components and load inductor. 24
2.10 The double pulse test topology. 24
2.11 The IGBT measured output characteristics $U_{ce} - I_c$. 25
2.12 The IGBT measured conduction losses. 26
2.13 The diode measured output characteristics $U_d - I_d$. 26
2.14 The diode measured conduction losses. 27
2.15 Double pulse test current and voltage waveforms of IGBT at 23 ℃ and 511 A test current. 27
2.16 The switching time instances current and voltage waveforms. 28
2.17 The IGBT switching energy as highlighted area. 29
2.18 The IGBT total switching energy loss versus current for 600 V. . . . 29

2.19 Double pulse test current and voltage waveforms of diode at 23 ℃ and 511 A test current. 30
2.20 The switching OFF time instance current and voltage waveforms and the energy loss during turn OFF of the diode. 30
2.21 The diode switching energy loss versus current for 600 V. 31
2.22 Comparison of the IGBT output characteristics between measurement and manufacturer data. 32
2.23 Comparison of the IGBT conduction losses between measurement and manufacturer data. 32
2.24 Comparison of the diode output characteristics between measurement and manufacturer data. 33
2.25 Comparison of the diode conduction losses between measurement and manufacturer data. 33
2.26 Comparison of the IGBT switching energy loss between measurement and manufacturer data. 34
2.27 Percentage difference between measured and manufacturer provided switching energy loss for the IGBT. 34
2.28 Comparison of the diode reverse recovery energy loss between measurement and manufacturer data. 35
2.29 Percentage difference between measured and manufacturer provided reverse recovery loss for the diode. 35

3.1 The area A through which convective heat transfer occurs at each duct. 41
3.2 Analytical Calculation of average h*A product for different water flow rates. 42
3.3 The electrical part of the convection coefficient measurement set-up. . 43
3.4 The interior of the heat-sink, its dimensions and the water supply circuit. 44
3.5 Measured h*A product for different water flow rates. 45
3.6 A comparison between calculation and measurement of the convection coefficient. 46
3.7 The setup of the climate chamber test. 47
3.8 Measured U_{ce} for each chip type with respect to its temperature. . . . 48
3.9 The test set-up for heating and measuring the thermal response of an IGBT switch. 51
3.10 The whole cooling down path of I13 and a closer look at the raw measured data. 52
3.11 The temperature increase of selected chips when I13 is heated. 52
3.12 The temperature increase of selected chips when D23 is heated. . . . 53
3.13 The steady state temperature of the area of each chip from the IR camera at 127 W of input power. 53
3.14 The steady state temperature profile of the diagonal of each chip at 127 W of input power. 54
3.15 The temperatures recorded with the IR camera and the $U_{ce}(T)$ method. 55

4.1 The 3D geometrical model used in Finite Element Analysis. 57

4.2 Comparison between measurements and FEM initial simulation for I13 heating. 59
4.3 Comparison between measurements and FEM initial simulation for D23 heating. 60
4.4 The modified $3D$ geometry 61
4.5 Comparison of measured and FEM calculated thermal impedances for the case of I13 heating. 62
4.6 Comparison of measured and FEM calculated thermal impedances for the case of D23 heating. 62
4.7 The simulated and fitted curve of $Z_{th,I13}$. 64
4.8 The simulated and fitted curve of $Z_{th,I13}$. 65
4.9 The equivalent Foster network for $I13$ and $D13$ chips. 65
4.10 Fitting $Z_{th,I13-D24}$ accepting and not accepting negative RC values. . 66

A.1 The power module cross section with its progressive layers IV

List of Tables

3.1 The heated and measured chips combinations 49

4.1 Foster equivalent RC values for $I13$ self thermal impedance 64
4.2 Foster equivalent RC values for $I13 - D13$ coupling thermal impedance 65

A.1 IGBT Conduction losses (W) II
A.2 Diode Conduction losses (W) II
A.3 IGBT Switching losses (mJ) for $R_g = 5.1\ \Omega$ II
A.4 Diode Switching losses (mJ) for $R_g = 5.1\ \Omega$ II
A.5 Measured U_{ce} for the upper row of switches III
A.6 Measured U_{ce} for the lower row of switches III
A.7 First Order polynomial coefficients for the $U_{ce}(T)$ equation for each chip of the module III
A.8 Dimension and material of each layer. IV
A.9 The time steps and increments used in FEM simulation. V

1
Introduction

1.1 Electric drive systems

One of the most popular applications in the broad field of electro-mobility, is the electric vehicle. This kind of vehicle utilizes an electric motor and usually chemical batteries or super-capacitors to store the energy required for propulsion. In contrast with conventional internal combustion engine (ICE) vehicles, an electric vehicle consumes no fuel in the form of gasoline or diesel. In case of a hybrid vehicle (that combines ICE with electric motors), it achieves lower fuel consumption and lower CO_2 and NO_x emission which makes both hybrid and electric vehicles environmental friendly [1].

Hybrid electric vehicles (HEV) or fully electric vehicles (EV) utilize electric motors for propulsion. In such an electric drive system, the main parts are the electric motor, the power electronics converter and the motor control unit (MCU). The electric motor as part of the power-train converts electric energy provided by on-board energy source into mechanical energy to move the vehicle. The opposite is also possible, since the electric motor can operate as a generator to convert mechanical energy into electric energy and charge the energy source during braking (regenerative braking) [1].

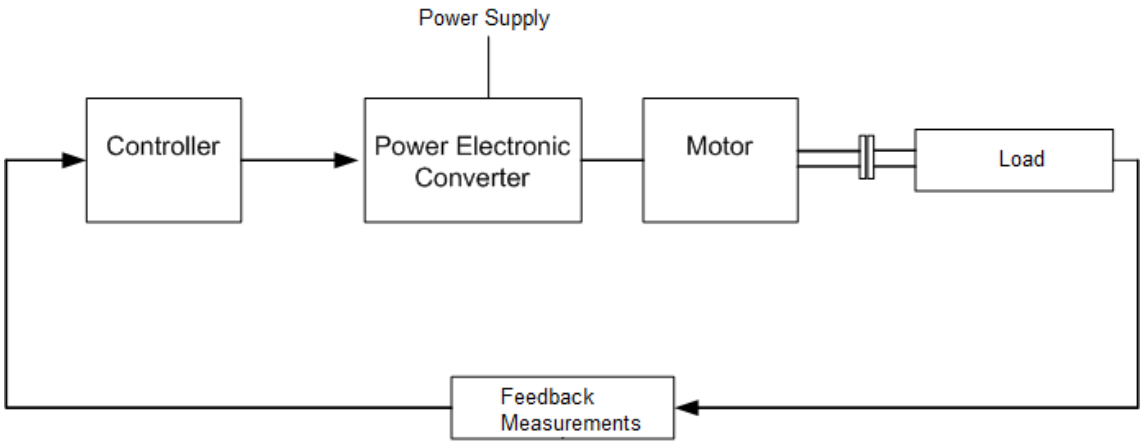


Figure 1.1: Electric motor control loop.

Depending on the application, different kind of control is required for the electric motor operation in such vehicles. Usually speed or torque control is desirable and this can be achieved by controlling the power supply to the motor. The general and mostly used concept is a closed loop control as illustrated in Figure 1.1 where,

depending on the application, speed or torque is monitored. This quantity is fed back to a controller which has a reference value of the same quantity to follow. The controller then, drives a power electronic inverter which in turn provides the motor with the appropriate voltage to eliminate any difference between the reference and measured quantities [5].

1.2 Power electronics

The energy storage of an HEV or an EV is usually batteries or super capacitors. Since the output of these sources is a DC voltage and control of the electric motor is required, a DC/AC inverter is necessary to supply the electric motor with controllable AC voltages. Depending on the driving cycle of the vehicle, different operating points (electro-mechanical torque and rotational speed) of the electric motor are required, so the inverter is designed to deliver a controllable voltage output both in frequency and in magnitude to drive the electric motor at the desired operating point [1].

In principle, a power electronic system consists mainly of several semi-conductor switches and a micro-controller. Its purpose is to control the flow of electric power from the power supply to the electric motor. This is normally done by providing a suitable voltage or current to the motor. This output can be controlled by switching the valves in an appropriate pattern. The micro-controller is responsible for comparing the actual output with a reference value and operate the switches so as to minimize any error between them.

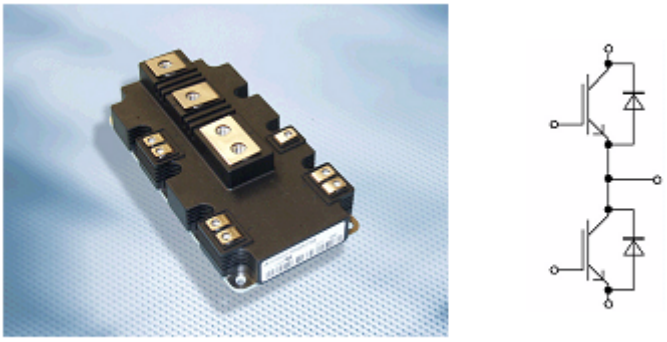


Figure 1.2: IGBT power module package and its equivalent circuit.

The building block of a power electronic system is usually a power electronic converter (PEC). The PEC is a topology of semi-conductor switches along with energy storage devices (inductors and capacitors) that converts power flow between its two sides. In case average power flows from DC to AC side, the system is called inverter, otherwise when average power flows from AC to DC side, it is called rectifier [5]. Even though the term power electronic converter is commonly used to ambiguously describe such systems, in this thesis the term inverter is adopted, since for the automotive application this thesis deals with, average power flows from DC to AC

side. The basic components of such an inverter are power switching devices, realized from semi-conductor chips such as IGBT's, MOSFET's, GTO's etc, combined with anti-parallel power diodes and usually packed in power modules such as the one illustrated in Figure 1.2 [2, 3].

1.3 The Insulated Gate Bipolar Transistor

The Insulated Gate Bipolar Transistor (IGBT) is a minority carrier semiconductor device, controlled by voltage. It shares common properties with MOSFET:s and BJT:s since it is a result of their combination in a monolithic form on the same chip [5],[6].

Its advantages include significantly lower on-state losses than a MOSFET which can be close to those of a BJT, faster switching than the BJT but not as fast as a MOSFET as well as higher current density than both MOSFET and BJT due to its structure, leading to smaller and more cost-effective chips. In addition it can be controlled easier than current driven devices, such as the BJT or the Thyristor, due to its voltage driven MOSFET gate input. Moreover it has a wide safe operating area (SOA) with higher current conduction capability compared to the BJT and also high forward and reverse blocking capability without any increase of the on-resistance which is observed at the MOSFET. On the other hand it is slower than the MOSFET especially at turn-off but still faster than a BJT. Finally the presence of a parasitic Thyristor into the IGBT structure indicates posibility of latchup [6].

In the context of this thesis an n-channel field-stop IGBT is investigated and its structure is illustrated in Figure 1.3. The main difference compared to a MOSFET structure, is found in the implanted p injecting layer that forms the Emitter of the IGBT. The Gate and Collector terminals are also shown, while the doping densities are similar to that of a MOSFET (n^+ around $10^{19}cm^{-3}$, n^- around $10^{14}cm^{-3}$, p and p^+ around $10^{16}cm^{-3}$) except of the body region. Alternative and more complicated structures are used to avoid activation of the parasitic $n^+pn^-p^+$ thyristor shown with dashed line [5],[6].

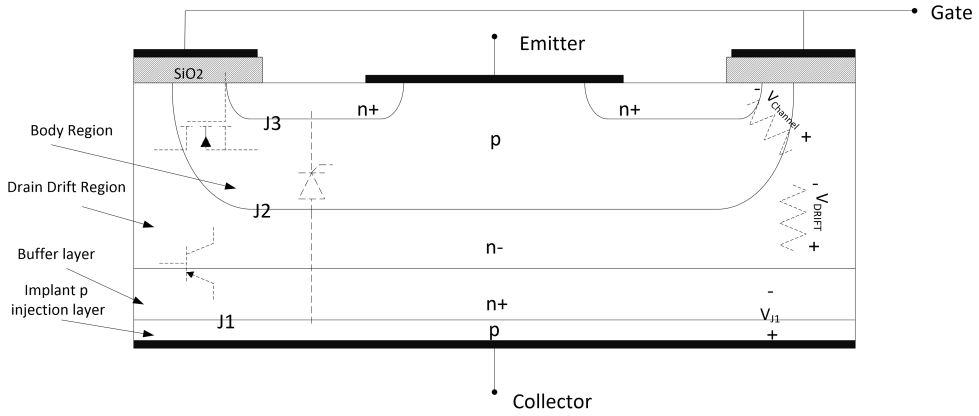


Figure 1.3: The layout of a n-channel IGBT.

The most commonly used symbol of the IGBT is illustrated in Figure 1.4a and a

simplified-normal operation circuit in Figure 1.4b, showing how a MOSFET and a BJT are partially combined in Darlington circuit to form an IGBT. These two are also sketched with dashed line in Figure 1.3 and placed at the locations of the IGBT structure, that their behavior appears. During on-state, most of the forward current flows through the MOSFET, marked in Figure 1.4b with dashed line and forming a forward voltage drop as

$$V_{CE,ON} = V_{J1} + V_{DRIFT} + I_D R_{Channel} \tag{1.1}$$

where each term represents the corresponding voltage drop of each region. The voltage drop V_{J1} across junction $J1$ is a normal forward biased pn-junction voltage drop, its value varies exponentially with the current and to first order, it approximately equals to $0.7 - 1\ V$. The drift region voltage drop is approximately constant and similar to that of a drift region in a high power pn-junction, but comparing an IGBT to a power MOSFET, the drift region voltage drop of the IGBT is significantly lower, leading in lower on-state losses for the later. Finally, the voltage drop over the MOSFET, is due to the ohmic resistance of the partial MOSFET channel and it's value is comparable to that of a MOSFET. This model explains how the forward voltage drop of an IGBT is connected with its forward current [5].



(a) The symbol of a n-channel IGBT.

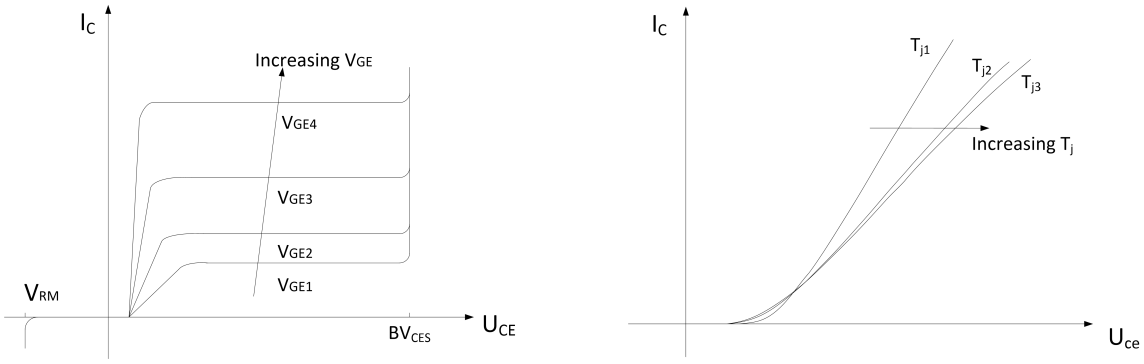
(b) The simplified equivalent circuit of an IGBT.

Figure 1.4: Symbol and equivalent circuit of an IGBT.

Both switching and conduction losses of the IGBT depend on its junction temperature. Collector emitter voltage increases with temperature as a result of increased $R_{Channel}$ of (1.1) and reduced minority carriers availability in field stop designs for higher temperatures [7]. Thus, its conduction losses increase with temperature.

During turn OFF of the IGBT, tailing is observed at the falling current waveform. This is a result of charge (minority carriers) stored in the n^- drift region exactly after the MOSFET part of the chip has turned OFF. This charge cannot be swept out, so it starts getting eliminated by recombination, a procedure that requires specific time and depends on temperature [5]. Thus for increased temperatures, recombination time is higher and tailing current lasts longer resulting in higher turn OFF energy loss. On the other hand, turn ON energy loss of the IGBT itself is unaffected by temperature [8], but the current it overtakes from the reverse recovery of the anti-parallel diode increases with temperature, leading to higher turn ON energy loss for the IGBT [9].

Its output characteristics in Figure 1.5a, illustrate the collector-emitter current I_C versus the forward collector-emitter voltage drop U_{CE}, with the gate voltage V_{GE} as parameter. Typical output characteristic is illustrated in Figure 1.5b with junction temperature T_j as parameter.



(a) U_{CE} - I_C with V_{GE} as parameter. **(b)** U_{CE} - I_C with T_j as parameter.

Figure 1.5: The IGBT output characteristics for different parameters.

The IGBT chip, mentioned also as silicon chip, can be packed in either a discrete IGBT package or ina power module formation, able to hold more than one chips. Both solutions can be found in low power applications but for medium to higher power ratings, power modules are almost exclusively preferred.

There is a wide variety of power module design, construction and material combinations. The most popular among manufacturers lately, is the solution of a plastic lid, containing the baseplate, the DBC and the semiconductors covered by silicon gel. This is also the solution, this thesis deals with and is illustrated in Figure 1.6.

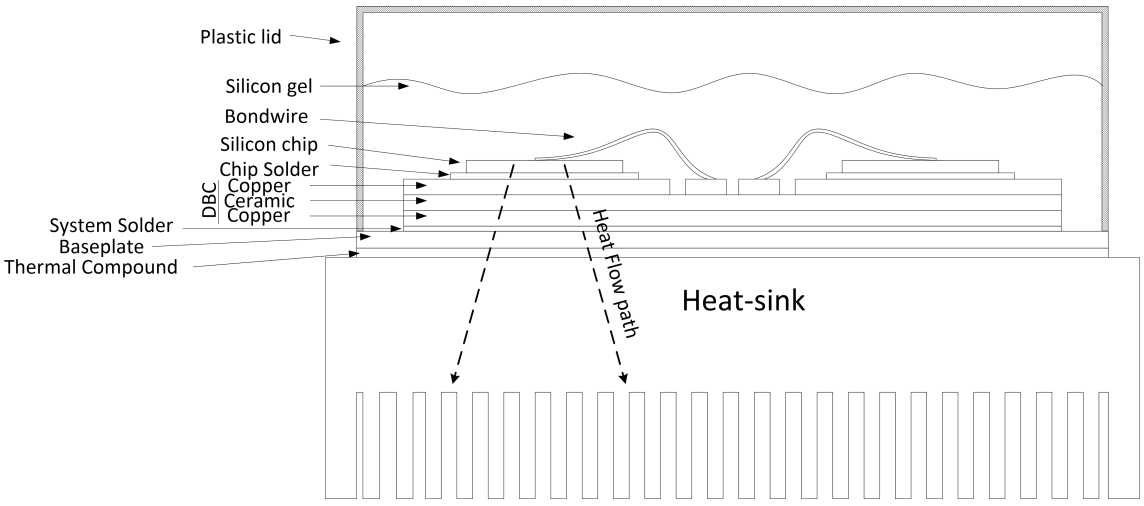


Figure 1.6: The physical layout of a power module.

The plastic lid is used to contribute to the mechanical stability of the module, protect it from pollution, insulating it from its neighboring components and ensuring sufficient creepage distance especially for higher blocking voltage applications. The

DBC (Direct Bonded Copper) substrate is mostly used as substrate nowadays. it consists of a ceramic dielectric insulator, bonded on both sides with copper layers. The most widely used materials for the ceramic are aluminum oxide (Al_2O_3), aluminum nitride (AlN) and to a lower extend silicon nitride (Si_3N_4). The purpose of the substrate is to provide electrical insulation between the chip and the layers beneath the ceramic. It also provides path to the current between the chips, through its upper copper layer trails and ensures good thermal connection for the heat to flow from the silicon chip to the cooling medium, sketched in the figure with dashed arrows. On top of the DBC, the silicon chips are mounted and electrical as well as thermal contact is achieved with a solder layer in between. A metalization layer made of aluminum or copper above the silicon chip carries the current and leads it to bond wires again made of aluminum or copper. A substrate can hold one or more silicon chips, while each module can consist of several substrates. All of the substrates are mounted on top of a baseplate that provides mechanical stability as well as good heat conduction. The baseplate is finally placed on top of the heat-sink with thermal compound in between to ensure sufficient thermal contact. The thermal compound can be thermal grease or aluminum foil, while the heat-sink is usually made of pure aluminum or its alloys.

1.4 Theory of thermal models

In order to quantify the transient thermal behavior of chips in the form of power module packages, equivalent circuits built of resistances and capacitances (R and C respectively) are utilized. The modeling procedure starts with measuring the response of the module at a heat flow step applied to it, usually created by load current through its chips. The temperature increase of every chip is logged versus time and its transient thermal impedance is calculated as

$$Z_{th,ja}(t) = \frac{T_j(t) - T_a}{P} \tag{1.2}$$

where $T_j(t)$ is the junction temperature of the chip, T_a is a reference temperature (usually heatsink, coolant or ambient temperature) and P is the injected heat flow [10].

An equivalent circuit topology close to the physical structure of the module can then be built. The Cauer network seen in Figure 1.7 forms an RC ladder, with every component being related to the structural layers of the power module. The RC pairs of a Cauer model, would match exactly with the layers of a power module package, as long as specific conditions are fulfilled (mainly one dimensional heat flow and increasing time constant for progressive layer along the heat propagation path). When deviations from these conditions occur, then the Cauer RC pairs, fit approximately one or several progressive layers of the power module. Moreover, additional Cauer ladders can be inserted in series to describe more complex layered structures. Finally, mathematical representation of the Cauer network is quite complicated having no simple formula to describe it. Therefore it is difficult to extract its RC parameters directly from Z_{th} measurements by fitting [11] [12].

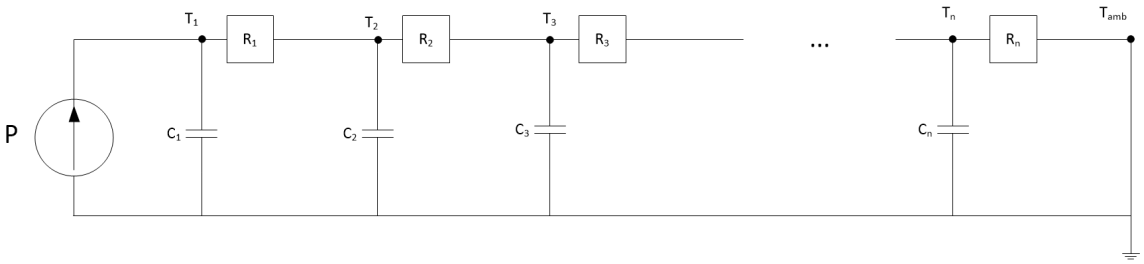


Figure 1.7: The Cauer equivalent network.

The equivalent Foster RC network, illustrated in Figure 1.8, can be directly used to approximately describe that thermal transient response. The Foster equivalent response is given as

$$Z_{th}(t) = \sum_{i=1}^{n} R_i(1 - e^{\frac{-t}{\tau_i}}),\ \tau_i = R_i C_i \tag{1.3}$$

where R_iC_i are the Foster equivalent RC pairs and τ_i is each one's time constant. A few RC pairs (usually 4-6) are enough to closely reproduce the measured thermal impedance and the RC values can be determined by curve fitting with nonlinear least square functions. Nonetheless, the Foster network is just a behavioral model and has no physical meaning, but it is preferred over Cauer network, due to its easier handling and parameters extraction.

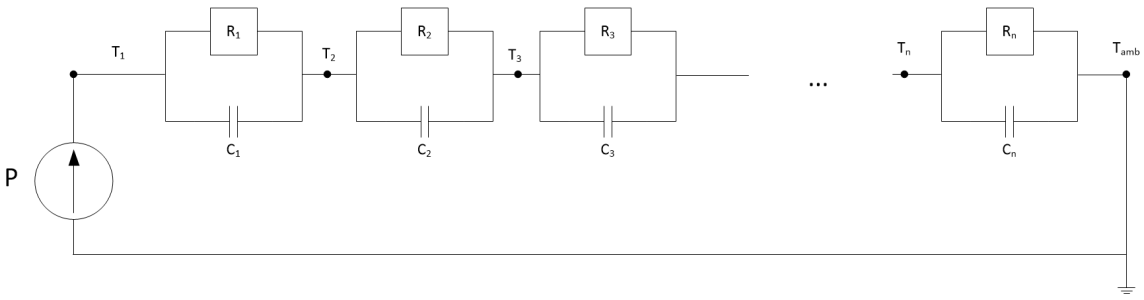
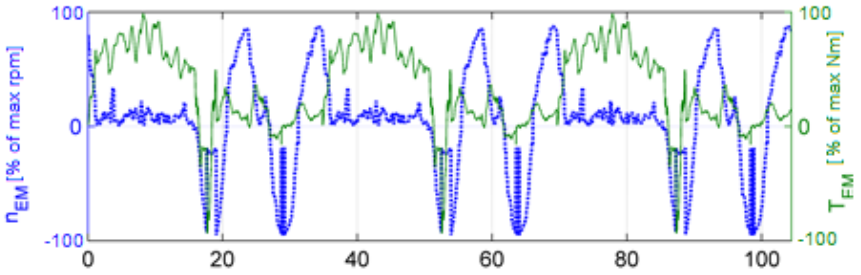


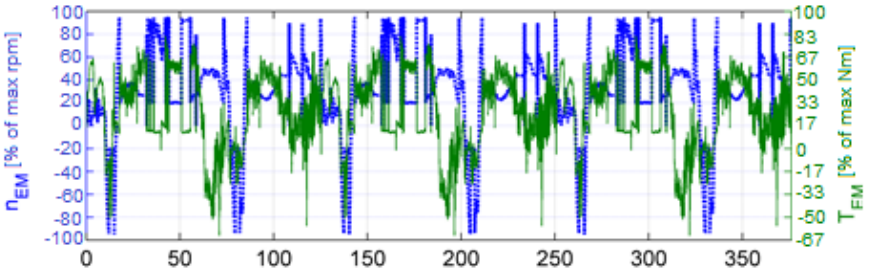
Figure 1.8: The Foster equivalent circuit.

1.5 Problem presentation

This thesis deals with a power module that could be used in a Volvo hybrid vehicle. Predefined driving cycles such as the ones illustrated in Figure 1.9, are already selected as reference and under these cycles the junction temperature of the IGBT chip must be accurately estimated.



(a) Driving cycle 1.



(b) Driving cycle 2.

Figure 1.9: Two different driving cycles for a hybrid vehicle with the corresponding rotational speed and torque for the electrical motor versus time.

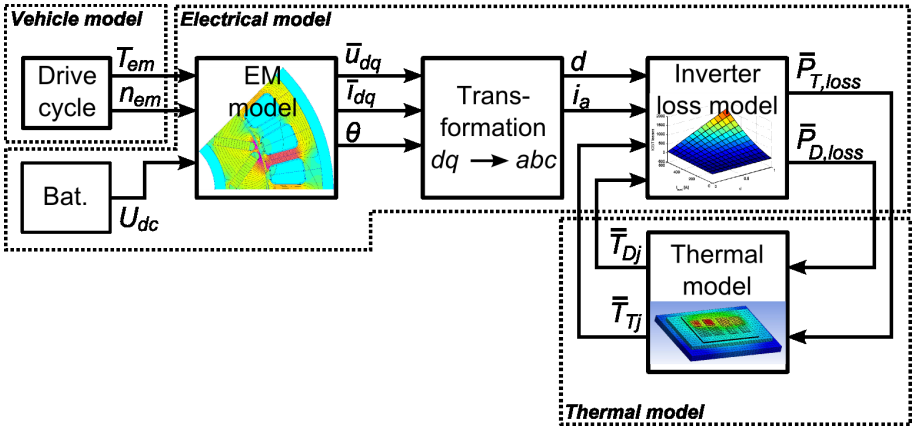


Figure 1.10: Complete simulation model of drive system.

In Figure 1.10 the complete simulation model of a drive system used in hybrid vehicles is illustrated. The drive cycle defines the operating point in electromechanical torque T_{em} and rotational speed n_{em} that an electric motor should deliver. In order for a machine to work on this operating point, considering the available source (battery) voltage U_{dc} and using a simplified machine model, voltage $\overline{U}_{dq}$, current $\overline{I}_{dq}$ and position θ of the motor are calculated. The voltage and current dq values are transformed to 3-phase values (abc) and are produced by a voltage source inverter, with power electronic modules as the main parts. The desired $\overline{U}_{dq}$ dictated

by the controller corresponds to duty ratios d_a, d_b, d_c for the inverter switches and the desired $\overline{I}_{dq}$ to phase currents $\bar{i}_a, \bar{i}_b, \bar{i}_c$ produced by the inverter. In a 3-phase inverter the phase current flows through the valves of each leg and depending on the direction of the current, it may flow through a switch or through its anti parallel diode. Thus, both conduction and switching losses are present for switches and diodes, represented in the figure with $\overline{P}_{T,loss}$ and $\overline{P}_{D,loss}$ respectively. These losses increase the temperature of the chip ($\overline{T}_{Tj}$ and $\overline{T}_{Dj}$), but they also depend on that temperature, so there is a closed loop connection between losses and temperature as seen in the figure.

As the use power electronic devices is constantly increasing in automotive industry, so are the demands in higher power ratings, switching frequency and power density. This results in higher cooling demands, otherwise it would lead to high operating temperatures which may influence reliability in a negative way [4]. During a driving cycle, power losses force the module to thermal cycling, consequently to thermal-mechanical stress. Due to different Coefficient of Thermal Expansion (CTE) of the layers of the module, an accurate estimation of the junction temperature of each chip is critical for the lifetime and reliability of the module. This is a result of the fact that failure caused by bond wire lift-off and/or solder cracking is directly connected to thermal stress cycling [13]. For this to be done, manufacturers provide thermal impedance information for each chip, along with an integrated temperature sensor (NTC) located on the module. In addition, conduction and switching losses characteristics are also provided by the manufacturer in associated data-sheets for the module. Thus, calculation of junction temperature for a specific operating state is at the moment performed by calculating the losses under this state and combining it with the thermal impedance of the chip, according to the data provided by the manufacturer.

This method though, has been proven insufficient, since unacceptable errors have been observed in the chip temperature prediction in case of multi-chip modules or operating conditions different than the ones that the manufacturer has used during characterization of the module [4]. Moreover, when custom packages are manufactured by the designer or new cooling methods are applied, there is not standardized data available at all. When more than one chip is used in the same module or even mounted on the same heat sink and one of them is heated during operation, it influences its neighbors by contributing to their temperature increase. Thus a method to verify and consider this interconnection is necessary. In addition, the operating conditions of a module may differ from the ones at which it is tested by its manufacturer to determine its losses characteristics. Stray inductance and capacitance existing in the final setup of the module at its operating environment, may affect its losses, making them deviate from the ones measured by the manufacturer.

Having mentioned all the above, it is concluded that the information provided by the manufacturer about power losses and thermal impedance characteristics, are not enough and may differ from the ones applicable in the real operating conditions. Consequently, a method to determine these quantities is necessary.

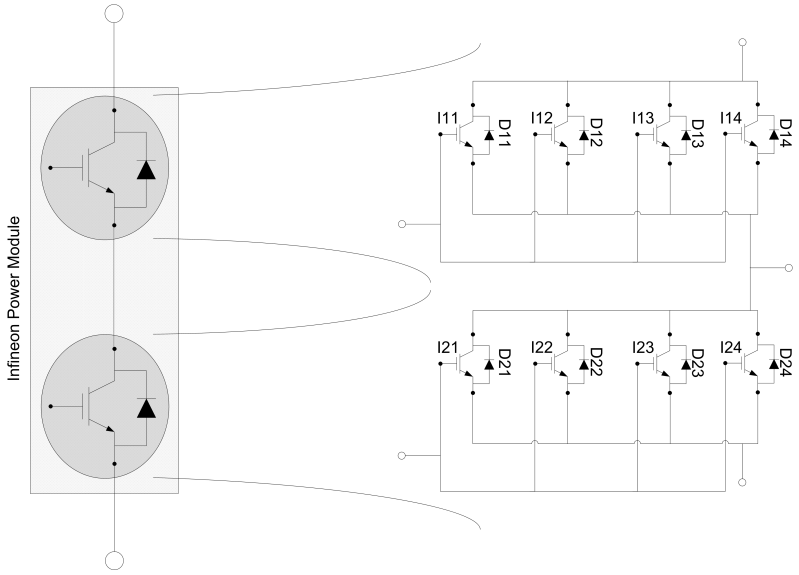


Figure 1.11: The power module topology.

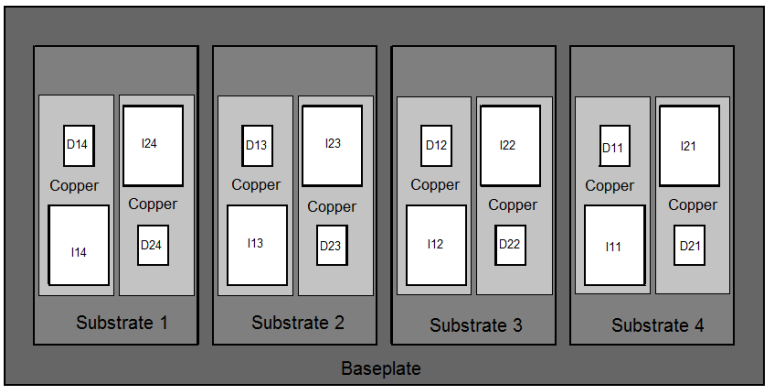


Figure 1.12: The power module layout with the name of each chip and the module layers.

The device under study is an Infineon™ FF600R12IE4 IGBT Power Module in half-bridge formation, with four switches for each valve, as shown in Figure 1.11. It can handle 1200 V across its collector-emitter terminals, while its nominal collector current is 600 A [3]. In Figure 1.12 a schematic layout of the module is shown, where the name of each IGBT is noted as Ixy and of each anti-parallel diode as Dxy for the sake of convenience, where x and y denote a row and column index respectively.

1.6 Objectives

As stated in Section 1.5, a power module consists of several IGBT and diode chips, placed in the same package. During operation of the module, the heat produced from power losses at each chip needs to be removed and dissipated, in order to maintain the module at a safe operating temperature. Especially for increasing power rating

and power density requirements from a power module, its cooling effectiveness is a critical aspect for its performance and usability. Hence, both power losses and thermal behavior of the module need to be investigated.

Failure of a power module can be caused by bond-wires lift off or deterioration of its heat flow path, as a result of thermal cycling leading to mechanical stress. The difference coefficient of thermal expansion for different layers of the module, usually leads to cracks in solder and grease layer. Thus,bad thermal contact between progressive layers, results in obstructed heat flow from the silicon layer to the heat-sink. As a result, temperature increases and hot spots are formed, causing even higher power losses and multiplication of the deterioration phenomena.

The value of an accurate model able to simulate the thermal behavior of the module, lies to the information it would provide about several thermal aspects and its contribution to the selection of a suitable power module. Such aspects are prevention of over-dimensioning the components of the module leading to lower cost, estimation of its lifetime and increase of its reliability, as well as determination of its cooling requirements. Combining its thermal behavior with its expected power losses as the origin of heat generation, results in a complete combination of cause and result.

Having mentioned all the above, the objective of this thesis is dual:

- determine the power losses of an IGBT power module through measurements at various operating points and under operating conditions similar to realistic applications of electric vehicles and
- develop with a combination of Finite Element Analysis simulations and experimental verification of it, a simulation model able to calculate the self and coupling thermal impedances of the chips of a power module in order to extract their mathematical representation.

The outcome is a mathematically described thermal model and a power losses look-up table able to be embedded in Matlab/Simulink™environment models, such as an aggregate model of a complete electric drive system.

2
Power Losses

2.1 Power loss modeling

In a semiconductor device such as an IGBT or a diode, there are three categories of power losses. The first category named conduction losses P_{cond}, consists of the energy that is dissipated as heat when the device is conducting. The second category is switching losses P_{sw} and includes the energy lost when the device is switching ON or OFF. The third category is named blocking (leakage) losses P_b and regards the losses when the device is fully OFF, but is normally neglected compared to the other two categories [14].

Conduction losses can be calculated as the product between the forward voltage drop and the current through the device. For an IGBT the forward voltage drop is the collector-emitter voltage U_{ce}, so the instantaneous conduction losses are calculated as

$$P_{cond}(t) = U_{ce}(t)I_c(t) \tag{2.1}$$

where $I_c(t)$ is the current through the IGBT. For a diode similarly, the forward voltage drop is the voltage between its anode and its cathode noted as V_f and can be used instead of U_{ce} in (2.1). That forward voltage drop depends both on IGBT or diode current (I_c and I_d respectively) and on the junction temperature of the chip. For a constant junction temperature and almost the whole nominal current range of the device, the forward voltage drop can be modelled as

$$U_{ce}(I_c) = U_{ce0} + r_c I_c \tag{2.2}$$

for the IGBT and

$$U_D(I_D) = U_{D0} + r_D I_D \tag{2.3}$$

for the diode. As a consequence, the instantaneous power losses after combining (2.2) and (2.3) respectively with (2.1) are given as

$$P_{cond,T}(t) = U_{ce0}I_c(t) + r_c I_c(t)^2 \tag{2.4}$$

and

$$P_{cond,D}(t) = U_D I_D(t) + r_D I_D(t)^2 \tag{2.5}$$

where the subscripts T and D refer to the IGBT and the diode respectively [14]. The temperature dependence can be included if the coefficients U_{ce0}, r_c, U_{D0} and r_D become a function of the junction temperature [15].

Switching losses occur every time the device changes its state between conduction and blocking. In Figure 2.1, the collector-emitter voltage and current waveforms are illustrated for turn ON and turn OFF of an IGBT.

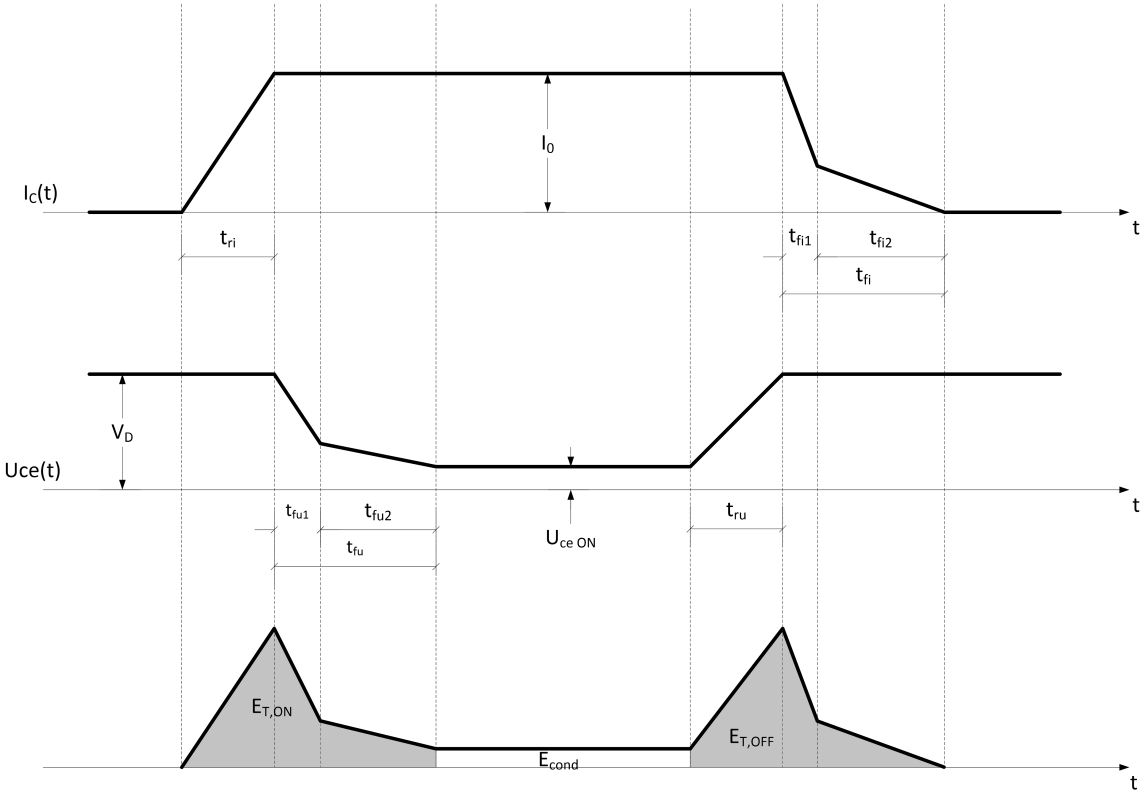


Figure 2.1: The turn ON, turn OFF curves and the energy losses of an IGBT.

The instantaneous power loss is given again as the product between $U_{ce}(t)$ and $I_c(t)$. For switching losses it is more convenient to work with the energy which is given by the integral of instantaneous power during the switching duration. In more detail, the energy dissipated during switch ON is given by

$$E_{T,ON} = \int_0^{t_{ri}+t_{fu}} U_{ce}(t)I_c(t)dt \tag{2.6}$$

where t_{ri} is the current rising time and t_{fu} is the voltage falling time as noted in Figure 2.1. Accordingly, the energy dissipated during turn OFF is calculated as

$$E_{T,OFF} = \int_0^{t_{ru}+t_{fi}} U_{ce}(t)I_c(t)dt \tag{2.7}$$

where t_{ru} is the voltage rising time and t_{fi} is the current falling time as seen in Figure 2.1. The highlightened areas of the same figure represent the energy losses during switching ON or OFF.

When it comes to the diode, the turn ON losses are calculated similarly to the IGBT as

$$E_{D,ON} = \int_0^{t_{ri}+t_{fu}} U_D(t)I_D(t)dt \tag{2.8}$$

but are usually neglected compared to the turn OFF losses. The turn OFF losses consist mainly of the reverse recovery energy which is calculated as

$$E_{D,OFF} = \int_{0}^{t_{ru}+t_{fi}} U_D(t) I_D(t) dt \approx \frac{1}{4} Q_{rr} U_{rr} \tag{2.9}$$

where Q_{rr} is the reverse recovery charge and U_{rr} is the voltage across the diode during reverse recovery. The total switching losses eventually are calculated as

$$P_{sw,IGBT} = (E_{T,ON} + E_{T,OFF}) f_{sw} \tag{2.10}$$

and

$$P_{sw,DIODE} = (E_{T,ON} + E_{T,OFF}) f_{sw} \approx E_{T,OFF} f_{sw} \tag{2.11}$$

where f_{sw} is the switching frequency.

In a half bridge formation such as the one in Figure 1.11, when I2 is turned ON, the current will commutate from D1 to I2, which means that the reverse recovery current of D1 will flow through I2 and introduce additional turn ON losses for I2. As a result, $E_{T,ON}$ for I2 consists of the self turn ON losses and the losses caused by the reverse recovery current of D1 while the same happens between I1 and D2. Finally, the switching losses also depend on junction temperature [15].

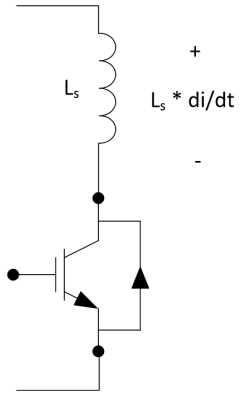


Figure 2.2: Stray inductance equivalent circuit.

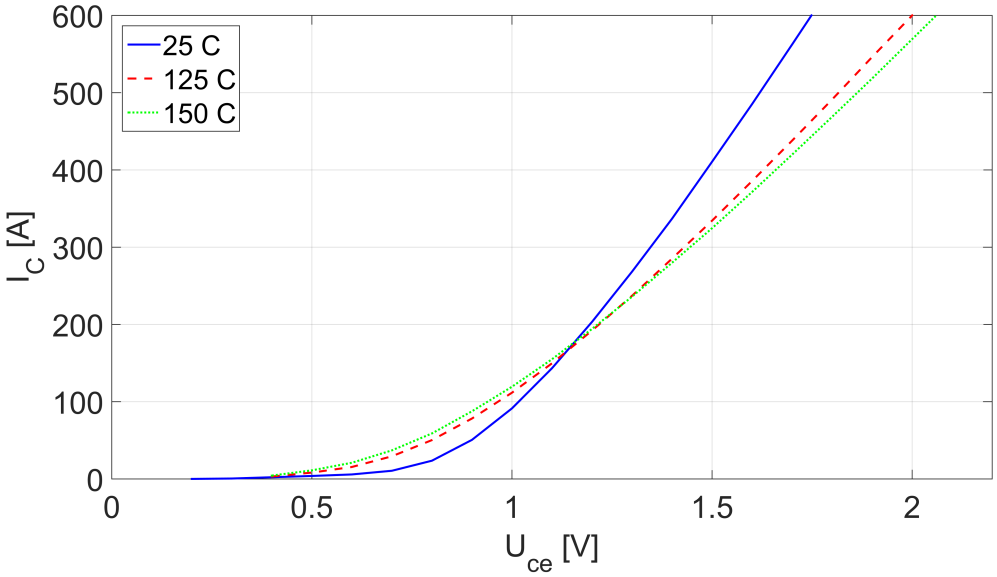
Stray inductance existence affects the switching losses mainly by increasing the turn OFF energy loss. As seen in Figure 2.2, the stray inductance is usually modeled as an inductor in series with the IGBT [5]. Thus, during turn OFF and as the IGBT current decreases, stray inductance causes a voltage overshoot that is added to the collector emitter voltage. This overshoot is given by

$$U = -L_s \frac{di}{dt} \tag{2.12}$$

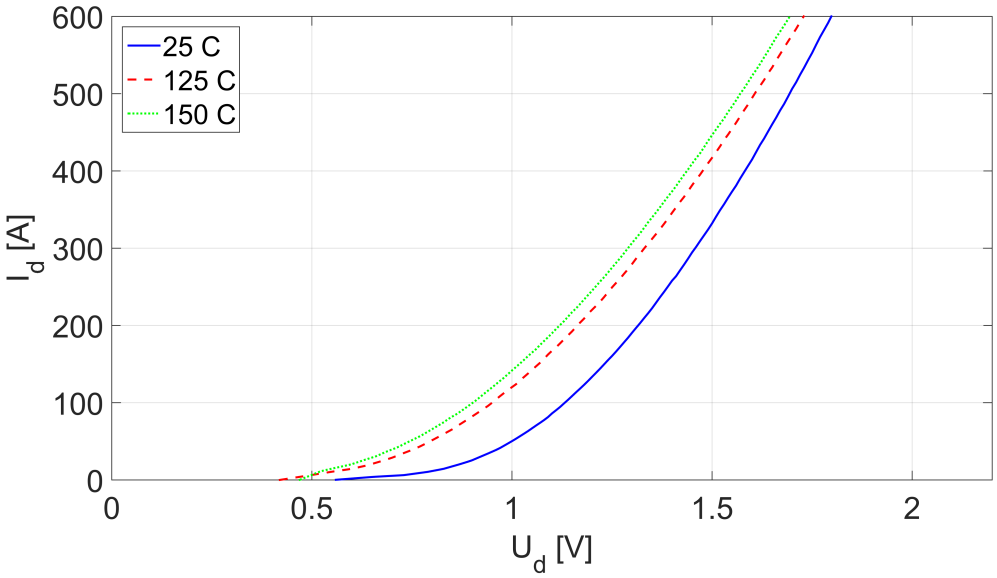
where L_s is the stray inductance value in the range of tenths of nH and $\frac{di}{dt}$ is slope of the falling current. Such an overshoot can be observed in the voltage waveform of Figure 2.16a and as a result, increased turn OFF energy loss can be expected.

2.2 Calculations according to manufacturer data

The data-sheet provided with the power module includes information about its conduction characteristics and switching losses under various current, temperature and gate resistance operating points. In more detail, regarding conduction losses of both IGBT and anti parallel diode, the curve relating their forward voltage drop with their current (output characteristic I_c-U_{ce} or I_d-U_d) is provided for three junction temperatures. In Figure 2.3, the output characteristics of the IGBT and the diode are presented.



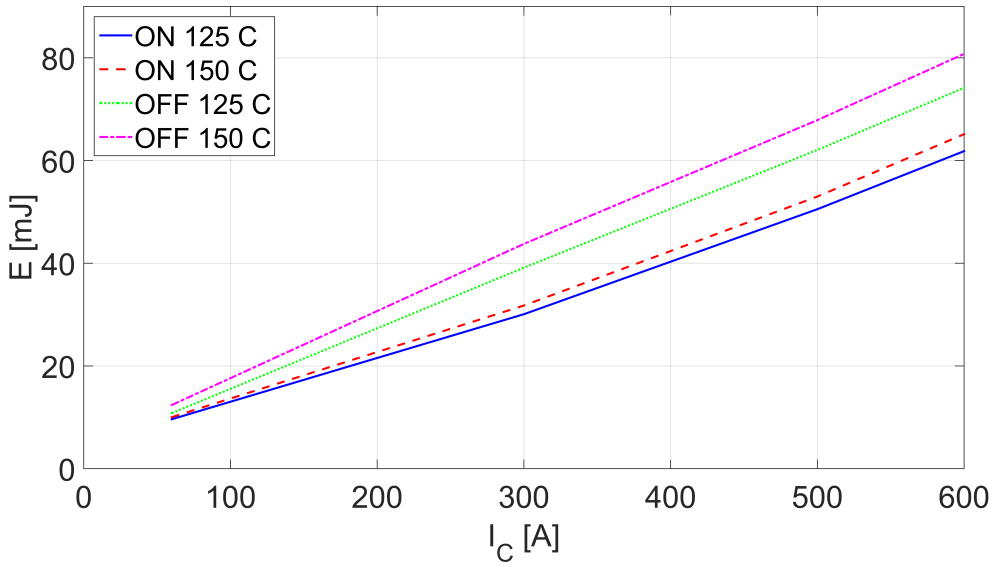
(a) The IGBT output characteristic.



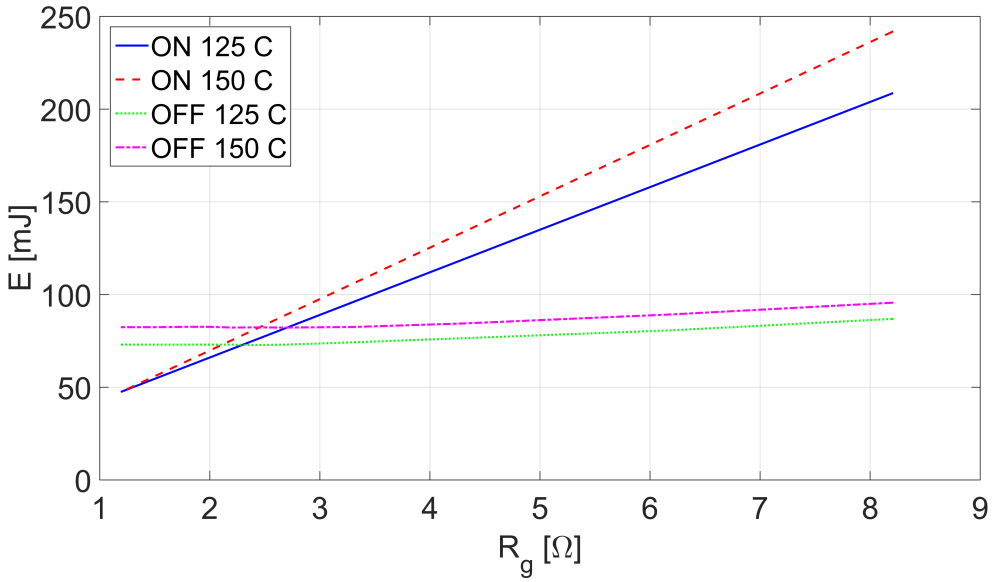
(b) The diode output characteristic.

Figure 2.3: The IGBT and diode output characteristics.

The IGBT energy losses are given by the manufacturer with respect to current separately as ON and OFF losses ($E_{on}(I_c, T)$ and $E_{off}(I_c, T)$) for two different temperatures and for gate resistance $R_{g,on} = 1.8\ \Omega$ and $R_{g,off} = 2.2\ \Omega$ as seen in Figure 2.4a. E_{on} includes the reverse recovery losses caused by the turn OFF of the diode [14]. The switching energy losses of the IGBT are also given with respect to R_g ($E_{on}(R_g, T)$ and $E_{off}(R_g, T)$) for constant current of 600 A and identical temperatures as shown in Figure 2.4b.



(a) The IGBT switching losses versus current.

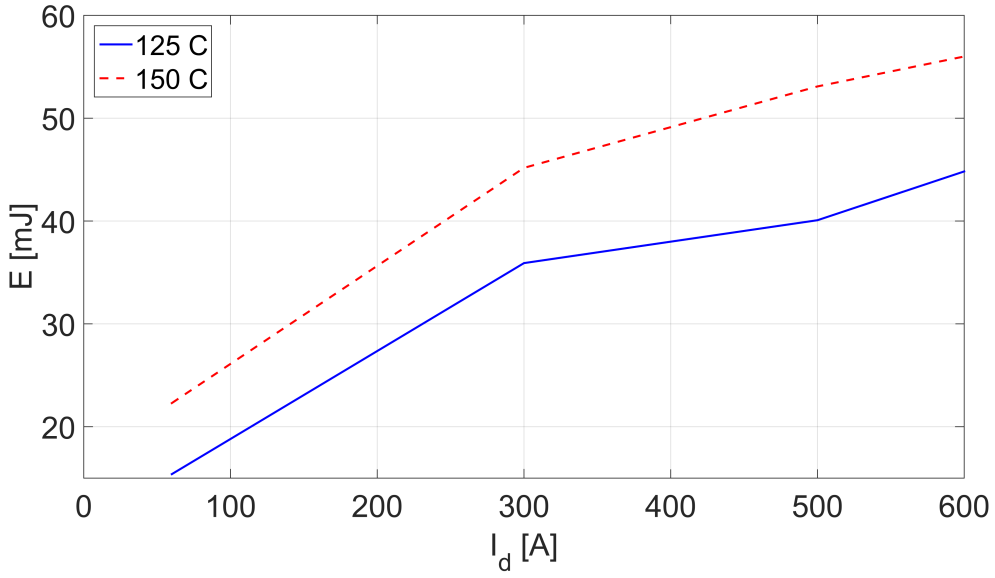


(b) The IGBT switching losses versus gate resistance.

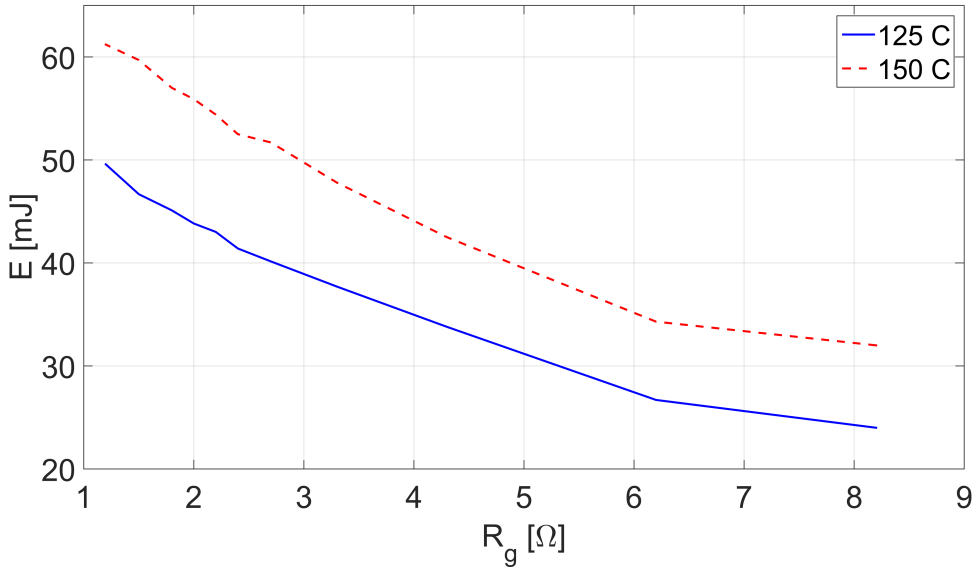
Figure 2.4: The IGBT switching losses for various operating points.

Regarding diode switching losses, these are given as reverse recovery losses mainly when diode turns OFF (turn ON losses for the diode are neglected) with respect to

current ($E_{rec}(I_c, T)$), for two temperatures and for $R_g = 1.8\ \Omega$ in Figure 2.5a. Finally the same losses are given with respect to R_g ($E_{rec}(R_g, T)$) for constant current of 600 A and two different temperatures in Figure 2.5b.



(a) The diode switching losses versus current.



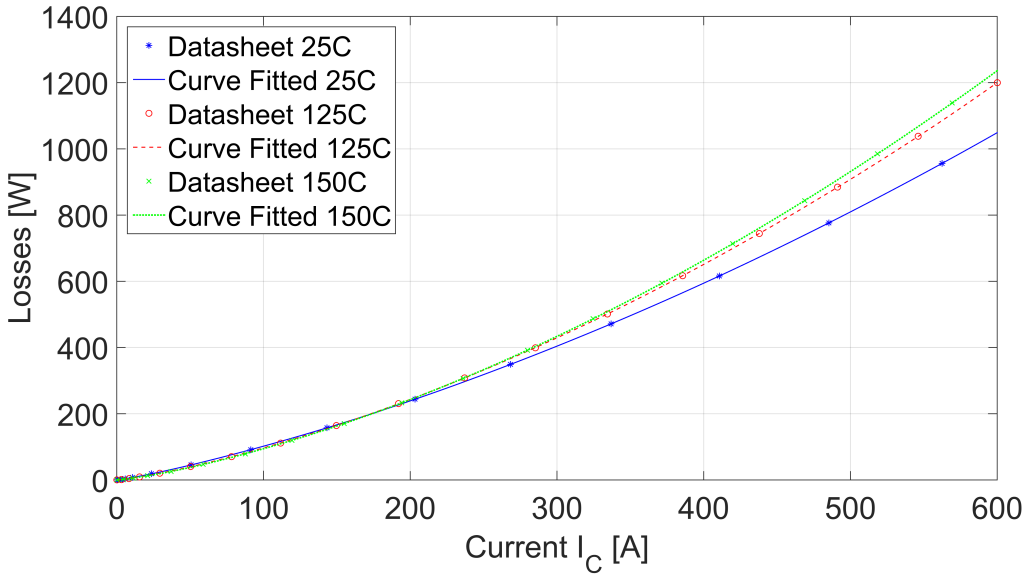
(b) The diode switching losses versus gate resistance.

Figure 2.5: The diode switching losses for various operating points.

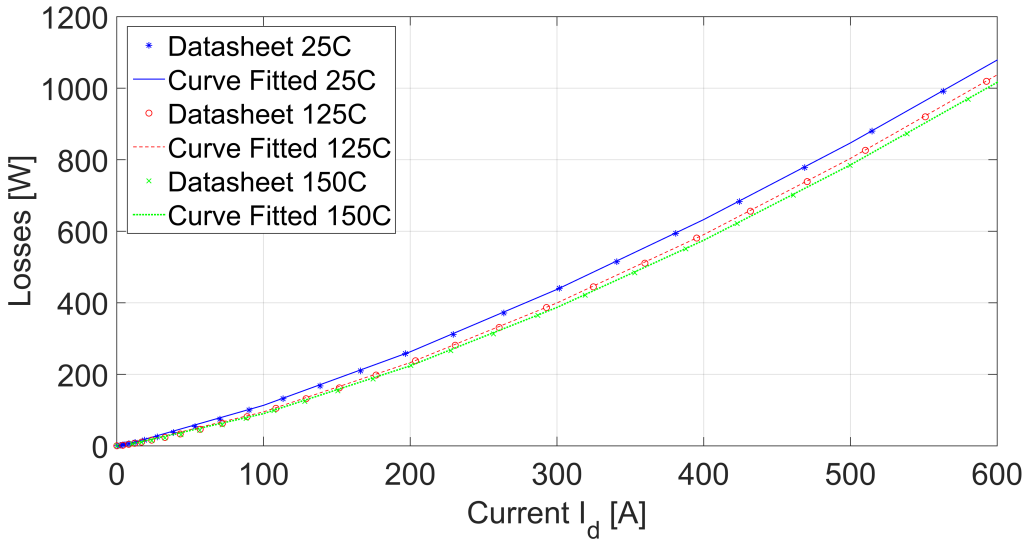
In order to establish a convenient way to calculate conduction and switching losses, the data given by the manufacturer is used to extract matching equations by curve fitting. Starting with IGBT conduction losses a new data set is derived from the output using (2.1) modified as

$$P_{IGBT,cond,Tx}(I_c) = U_{ce} I_c \tag{2.13}$$

where $P_{IGBT,cond,Tx}$ are conduction losses of the IGBT with respect to its current for temperature Tx.



(a) IGBT



(b) Diode

Figure 2.6: Comparison between conduction power losses calculated from manufacturer data and calculated after curve fitting according to (2.15), for the IGBT and diode respectively.

Having enough data points, it is possible to use a $9th$ order polynomial to fit the $P_{IGBT,cond,Tx}(I_c)$ curve as

$$P_{IGBT,cond,Tx}(I_c) = aI_c^9 + bI_c^8 + cI_c^7 + dI_c^6 + eI_c^5 + fI_c^4 + gI_c^3 + hI_c^2 + iI_c + j \quad (2.14)$$

where $a...j$ are coefficients extracted using curve fitting tool in Matlab. Regarding the different temperatures, there are three data sets available, so according to [15] it

is possible make $a...j$ temperature depended after fitting them with a second order polynomial relationship as

$$\begin{aligned} P_{IGBT,cond}(I_c,T) = &(a_1T^2+a_2T+a_3)I_c^9+(b_1T^2+b_2T+b_3)I_c^8 \\ &+(c_1T^2+c_2T+c_3)I_c^7+(d_1T^2+d_2T+d_3)I_c^6 \\ &+(e_1T^2+e_2T+e_3)I_c^5+(f_1T^2+f_2T+f_3)I_c^4 \\ &+(g_1T^2+g_2T+g_3)I_c^3+(h_1T^2+h_2T+h_3)I_c^2 \\ &+(i_1T^2+i_2T+i_3)I_c+(j_1T^2+j_2T+j_3) \end{aligned} \tag{2.15}$$

and the comparison between the manufacturer's data and the fitted curves is presented in Figure 2.6a. Identical steps are used to calculate conduction losses for the diode, which are presented in Figure 2.6b.

Calculations become more complicated when it comes to switching losses since there are three parameters (I_c, T, R_g) that influence their value and the desired result is a unique function that will calculate the switching losses when temperature, current and gate resistance are known. Taking as an example the switching ON losses, there are two curves provided for 600 A with respect to R_g, one for 125 ℃ and another for 150 ℃ . It is also observed from the data that there is a common operating point between $E_{on}(I_c,T)$ and $E_{on}(R_g,T)$ and this is for 600 A and 1.8 Ω so it is considered that for this operating point, the switching losses have a scaled value equal to 1. Assuming that, $E_{on}(I_c,T)$ can be calculated for any combination of current and temperature under $R_g = 1.8$ and then inserted to the scaling curve to find the corresponding losses for different R_g values. Therefore, $E_{on}(R_g,T)$ curve is divided with $E_{on}(1.8,T)$ and this outcome named $Scale_{on}(R_g,T)$ will be used as scaling factor for the turn ON switching losses. The curve $Scale_{on}(R_g,T)$ is line fitted with a second order polynomial with temperature depended coefficients similarly to the derivation method used for the conduction losses. Eventually $Scale_{on}(R_g,T)$ ends up as

$$Scale_{on}(R_g,T) = (a_1T+a_2)R_g^2+(b_1T+b_2)R_g+(c_1T+c_2) \tag{2.16}$$

with the only difference that temperature dependent coefficients are of first order since there where two temperature levels available to fit. The $E_{on}(I_c,T)$ curve is also fitted with a second order polynomial with temperature depended coefficients as

$$E_{on}(I_c,T) = (a_1T+a_2)I_c^2+(b_1T+b_2)I_c+(c_1T+c_2) \tag{2.17}$$

and the scaled switching ON losses are calculated as

$$E_{on}(I_c,R_g,T) = E_{on}(I_c,T) * Scale_{on}(R_g,T) \tag{2.18}$$

The same procedure is followed for turning OFF losses of the IGBT. The directly comparable results between manufacturer data and fitted curves are presented in Figure 2.7 where total switching losses as sum of ON and OFF losses are presented for 125 and 150 ℃ with the corresponding manufacturer curves. In Figure 2.8, the diode switching losses are presented accordingly.

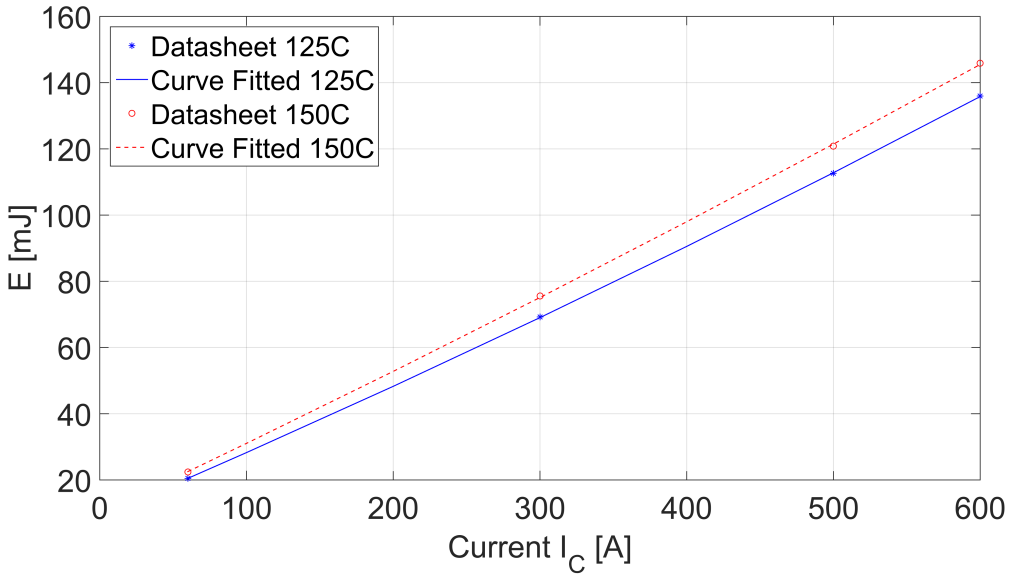


Figure 2.7: Switching losses of the IGBT for 125 and 150 ℃ and $R_g = 1.8\ \Omega$.

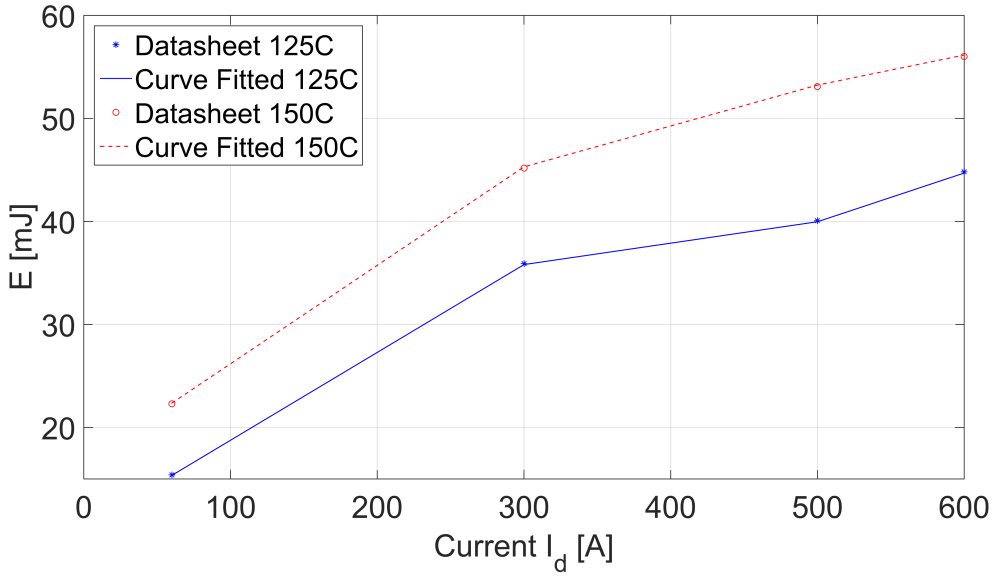


Figure 2.8: Switching losses of the diode for 125 and 150 ℃ and $R_g = 1.8\ \Omega$.

The diode switching losses curve fitting differs only in the order of the polynomials chosen. Thus, a $5th$ order polynomial with temperature depended coefficients is selected to fit the scale curve as

$$\begin{aligned} Scale_{diode}(R_g, T) = (a_1T + a_2)R_g^5 + (b_1T + b_2)R_g^4 + (c_1T + c_2)R_g^3 \\ +(d_1T + d_2)R_g^2 + (e_1T + e_2)R_g + (f_1T + f_2) \end{aligned} \tag{2.19}$$

and a $3rd$ order polynomial describes the diode losses with respect to current and temperature as

$$E_{rec}(I_c, T) = (a_1T + a_2)I_c^3 + (b_1T + b_2)I_c^2 + (c_1T + c_2)I_c + (d_1T + d_2) \tag{2.20}$$

obtaining the total losses as

$$E_{rec}(I_c, R_g, T) = E_{rec}(I_c, T) * Scale_{diode}(R_g, T) \tag{2.21}$$

and the result is presented in Figure 2.8.

As seen so far, the manufacturer provides data for the switching losses in the form of curves, only for 125 and 150 ℃ . There is one additional operating point losses and that is for 600 A, 1.8 Ω and 25 ℃ both for the IGBT and for the diode. Having that operating point, validation of the temperature dependency curve fitting can be done and correction in case it is necessary. For the IGBT, the temperature dependency as estimated from the two known temperatures, agrees well if extended to 25 ℃ giving energy losses of 97 mJ, when the manufacturer claims 102 mJ. Things are different for the diode, since the losses estimated for 25 ℃ are negative, which indicates that temperature dependency is not sufficiently extracted by only two temperatures.

For this common operating point, there are three loss values available for the diode $E_{op,rec,25}, E_{op,rec,125}, E_{op,rec,150}$ at 25 ℃ 125 ℃ and 150 ℃ respectively. With a power expression as

$$E_{op,rec}(T) = aT^b + c \tag{2.22}$$

each point between these three can be extracted. In addition, $E_{op,rec}(T)$ is normalized to $E_{op,rec,125}$. Thus for temperatures lower than 125 ℃ a corrected loss extraction is established as

$$E_{rec}(I_c, R_g, T) = E_{rec}(I_c, R_g, 125)\frac{E_{op,rec}(T)}{E_{op,rec,125}} \tag{2.23}$$

2.3 Experimental determination

2.3.1 Task description

The power module under investigation is part of a fully functional three-phase converter and as a consequence, its operating conditions probably differ than the ones under which its manufacturer has standardized it. Thus, the power losses measured by the manufacturer might differ in the real application, mainly due to different gate resistance values, as well as the presence of stray inductances coming from the layout of the converter components and affecting the switching losses. At this section the experimental measurement of switching and conduction losses under real application conditions is presented.

2.3.2 Method description

For switching losses measurement, double pulse tests are utilized. The purpose is to measure the switching losses for different voltage and current values. According to that procedure, in the circuit illustrated in Figure 2.10, $IGBT_{TOP}$ is chosen as switch under test and is turned ON. A current starts to build up from the DC link to the inductor through $IGBT_{TOP}$. After a time interval governed by the inductance

value, the current reaches the desired test level and $IGBT_{TOP}$ is switched OFF. At this instance, the $IGBT_{TOP}$ collector current I_c and the collector-emitter voltage U_{ce} are logged, leading to turn OFF losses measurement using (2.7).

Since the inductor is a current stiff device, it will force its current to flow through $diode_{BOT}$. After a relatively small time interval (such that the inductor current should not drop dramatically from its prior value) $IGBT_{TOP}$ is turned ON and current commutates back through it. At this point, I_c and U_{ce} are recorded and can later be used to calculate the turn ON losses using (2.6). It's worth mentioning that I_c includes reverse recovery current of $diode_{BOT}$ caused by its turn OFF.

Regarding diode losses, typically its turn ON losses are neglected [14] and only its turn OFF losses are measured. The procedure is the same as with the IGBT but the measurement is done for the current of the diode and its terminal voltage, when IGBT is turned ON using the integration as in (2.9).

When it comes to conduction losses, measurements are more straight forward, since it is enough to measure U_{ce} and I_c or U_D and I_D for different current values and insert them in (2.1). The measurements can be performed during the double pulse test and measure the $diode_{BOT}$ conduction losses after the turn OFF of the $IGBT_{TOP}$, as well as the $IGBT_{TOP}$ conduction losses after its second turn ON.

One important factor for all the above measurements is the junction temperature for both chips. The switching losses differ for varying temperatures mainly because reverse recovery current of the diode changes. This happens since with increasing temperature, density of the carriers increases as a result of their longer lifetime. Consequently during reverse recovery the current peak becomes higher and the reverse recovery duration longer for increased junction temperature, affecting both turn OFF losses of the diode as well as turn ON losses of the IGBT. Finally conduction losses are also affected by temperature, since forward voltage drop for both diode and IGBT differs for different temperatures [16].

2.3.3 Test setup

The Volvo ™ VPEC consists of three identical Infineon FF600R12IE4 power modules in full bridge 3-phase converter. The modules are mounted on a common heat sink in the same housing with their input inductor, DC link capacitors and controller board. On top of everything a metallic lid is placed, which internally is shaped with copper bars to connect the DC link components with the IGBT modules and the output. The whole setup except the copper bars lid is illustrated in Figure 2.9 where every component is visible and marked.

The double pulse test setup topology illustrated in Figure 2.10, consists of the IGBT module under test, an inductor as load and the measuring equipment. The inductor is a custom built solenoid with wooden core and inductance of 66 μH made by copper wire having resistance around 5 $m\Omega$. The double pulse test sequence is loaded in the control software of the VPEC and the ON and OFF time intervals can be selected using with maximum resolution of 1 μs. For the double pulse test only one leg of the 3-phase converter is used. The converter is fed by a voltage source and its DC link voltage is set at 600 V which is the voltage level of the batteries in its real application. Finally the total gate resistance value R_g, including the internal

gate resistance of the module, is 5.1 Ω .

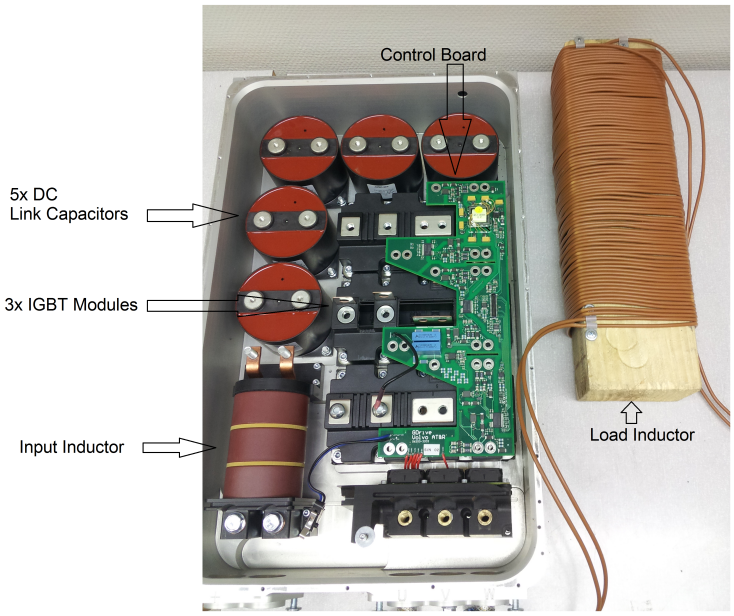


Figure 2.9: The VPEC with its internal components and load inductor.

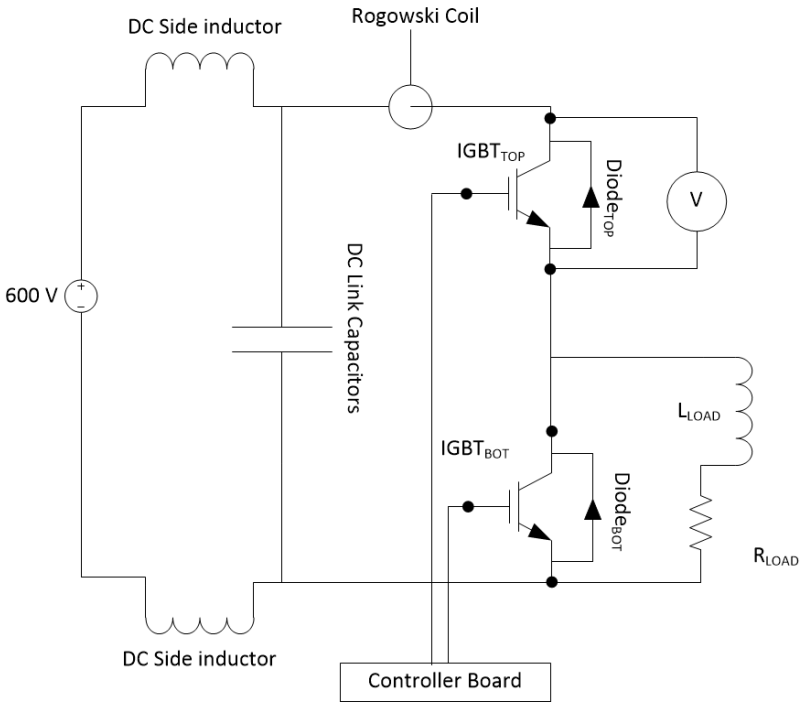


Figure 2.10: The double pulse test topology.

In order to be able to measure the chip temperature, the IR camera is placed above the middle IGBT module which is under measurement. A hole is opened on the cap

of the middle module to provide clear field of view on one IGBT and one diode chip for the IR camera. A Rogowski coil is used to measure the current and a high bandwidth - high voltage probe to measure the voltage. A high bandwidth oscilloscope logs all the measured data. All equipment that is used for this measurement is listed in Appendix A.1 .

2.3.4 Measurements and results

For a constant DC voltage of 600 V, six current levels are chosen. The different current levels can be achieved by adjusting the first turn ON time interval for the IGBT under test, since current through an inductor is given by

$$U = L\frac{di}{dt} \Rightarrow \Delta i = \frac{V\Delta t}{L} \tag{2.24}$$

where L is the load inductance, U is the DC link voltage and Δt the first turn ON time interval. Thus six Δt_{on} values from 10 μs to 60 μs with an increment of 10 μs are chosen.

Conduction losses

Conduction losses for the IGBT can be extracted experimentally by measuring the U_{ce} voltage under known - measured I_c. A power supply in current control mode, forces current through the IGBT and its collector emitter voltage is measured. The current is forced through the chip under test as a 500 ms rectangular pulse. Due to limitations in the experimental setup, measurements are conducted for room temperature of 23 ℃ the highest current that could be injected is 480 A and the output characteristics of the IGBT are illustrated in Figure 2.11. It's measured conduction losses can then be calculated using (2.1) and are illustrated in Figure 2.12.

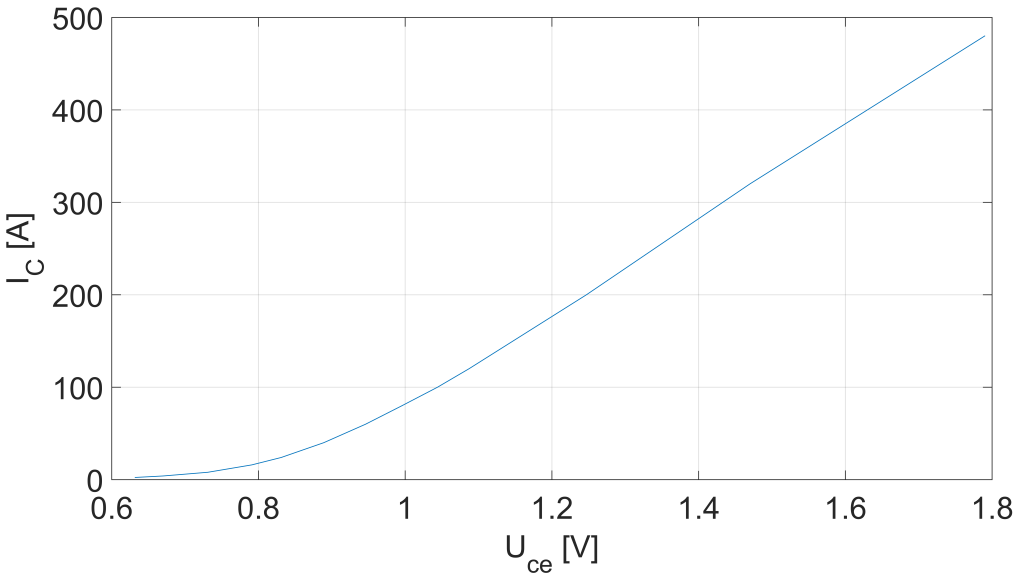


Figure 2.11: The IGBT measured output characteristics $U_{ce} - I_c$.

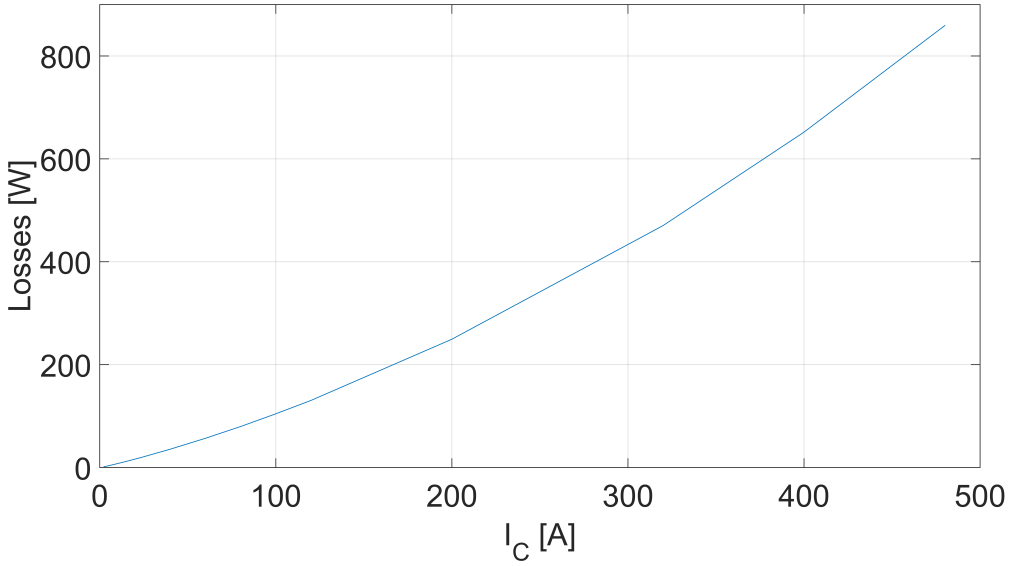


Figure 2.12: The IGBT measured conduction losses.

Regarding conduction losses of the diode,the same experimental procedure is followed as for the IGBT conduction. In Figure 2.13, the forward voltage drop of the diode versus its current are presented, while Figure 2.14 presents its conduction losses.

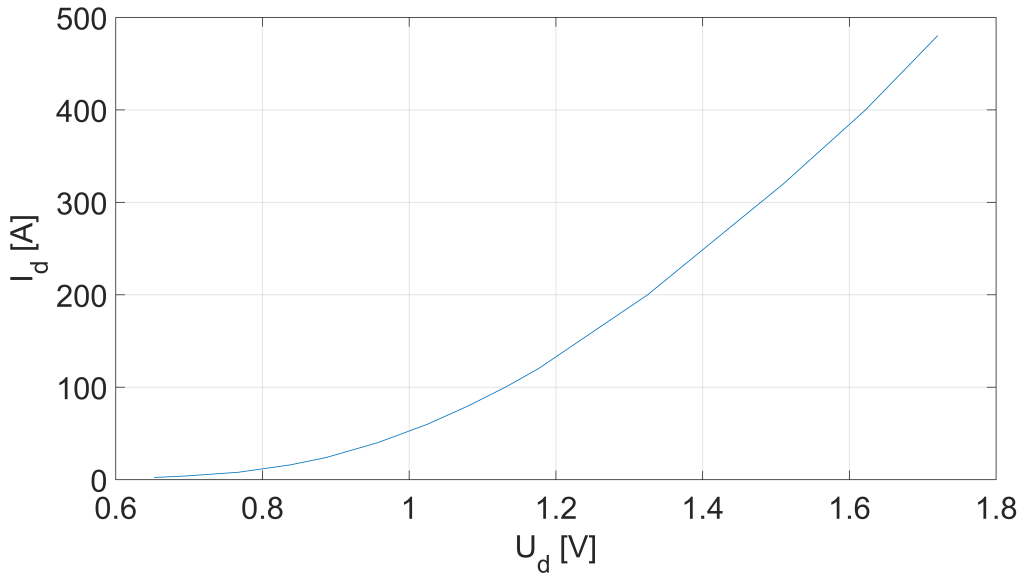


Figure 2.13: The diode measured output characteristics $U_d - I_d$.

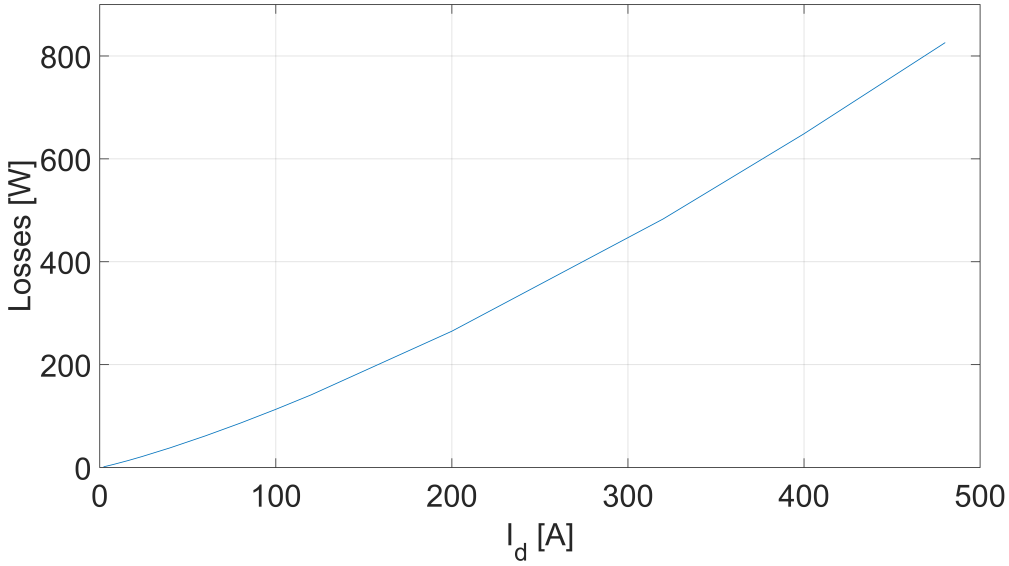


Figure 2.14: The diode measured conduction losses.

Switching losses

The voltage and current waveforms of the double pulse test for an IGBT are illustrated for room temperature in Figure 2.15. The first turn ON interval in the presented case is 50 μs resulting in a current level of 511 A.

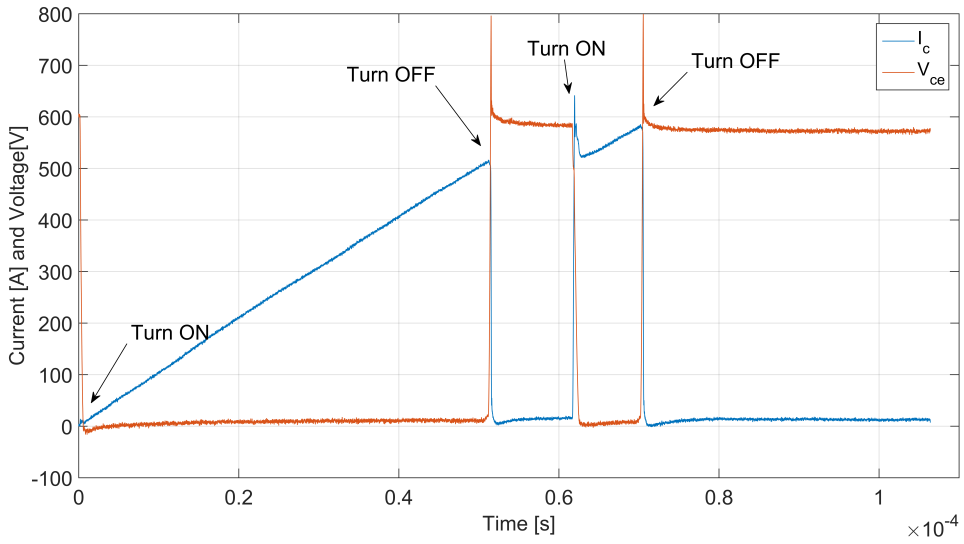
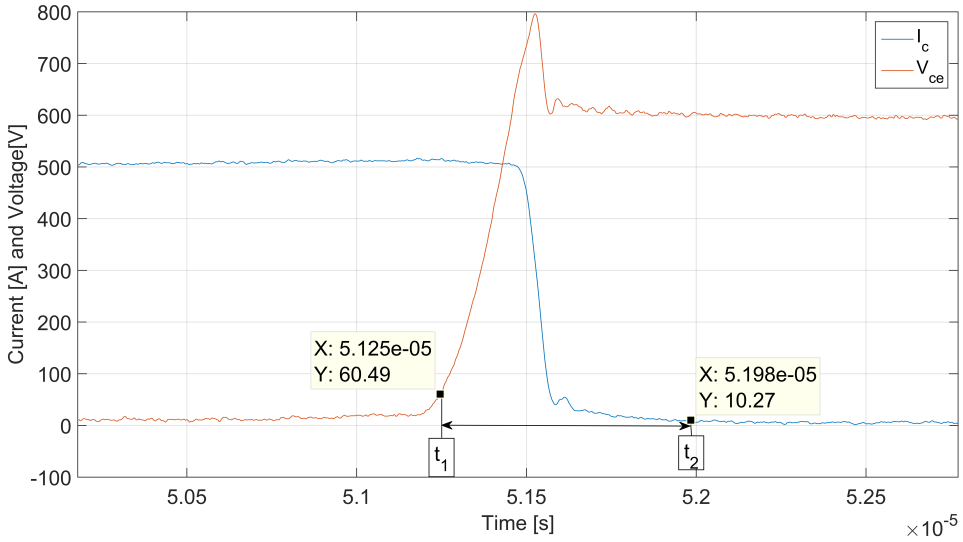


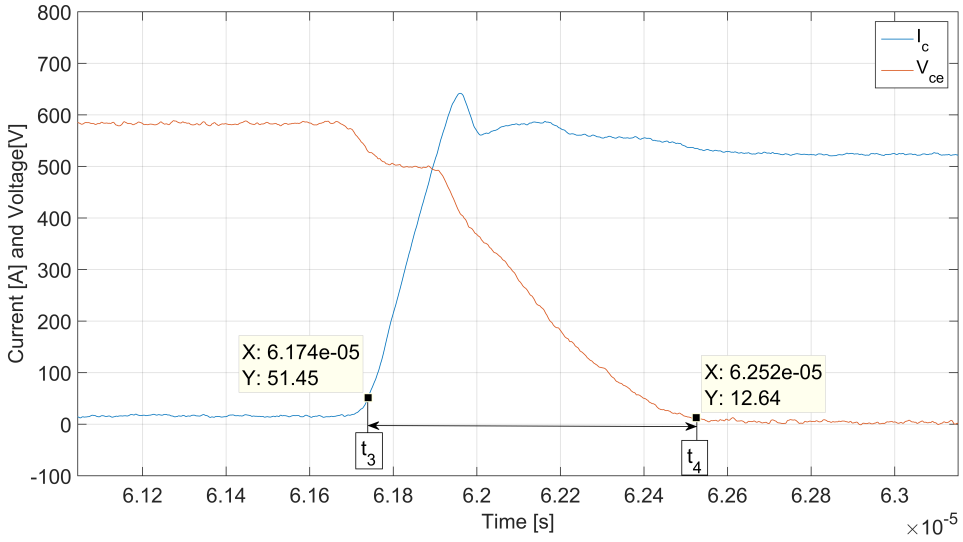
Figure 2.15: Double pulse test current and voltage waveforms of IGBT at 23 ℃ and 511 A test current.

A closer look at the first turn OFF and second turn ON of the IGBT is illustrated in Figures 2.16a and 2.16b respectively. From these time instances the turn OFF and turn ON energy is calculated. The manufacturer specified the so called 10% to 2% levels, meaning that the integration limits of (2.7) (2.6) are chosen from these

levels. In more detail, for the turn OFF energy in Figure 2.16a, t_1 is the time when the increasing U_{ce} is at 10% of its steady state value and t_2 is the time when the decreasing I_c is at 2% of its steady state value. The turn ON integral time limits are selected accordingly as seen in Figure 2.16b.



(a) Turn OFF



(b) Turn ON

Figure 2.16: The switching time instances current and voltage waveforms.

By applying (2.7) (2.6) for the waveforms of Figure 2.16, the area highlighted in Figure 2.17, represents the switching energy. The sum of turn ON and turn OFF energy loss for currents in the range of 0 up to 600 A and voltage of 600 V are gathered in Figure 2.18, as total switching loss versus current.

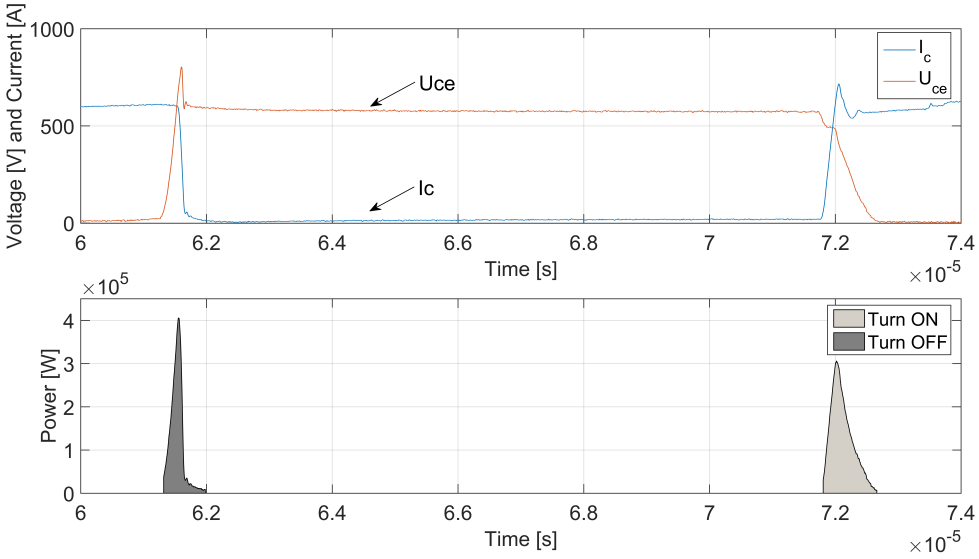


Figure 2.17: The IGBT switching energy as highlighted area.

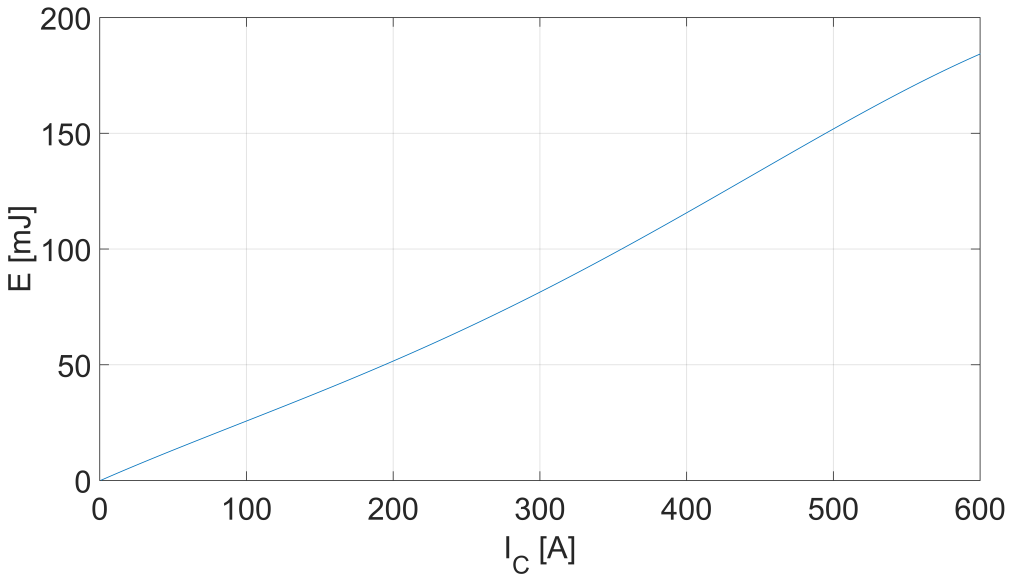


Figure 2.18: The IGBT total switching energy loss versus current for 600 V.

To what concerns switching losses of the diode, the entire double pulse test sequence waveforms are presented in Figure 2.19. Only its turn OFF losses are considered, since they are caused by the reverse recovery current and are significantly higher than turn ON losses, which can be neglected. Regarding the limits in (2.9), the integration starts when $I_{rr,d}$ crosses zero (reverse recovery current) marked as t_1 in Figure 2.20a and ends at t_2 when $I_{rr,d}$ reaches 2% of its maximum reverse recovery value. As a result, the highlighted area of Figure 2.20b is obtained. The switching energy loss of the diode, versus its current is illustrated in Figure 2.21.

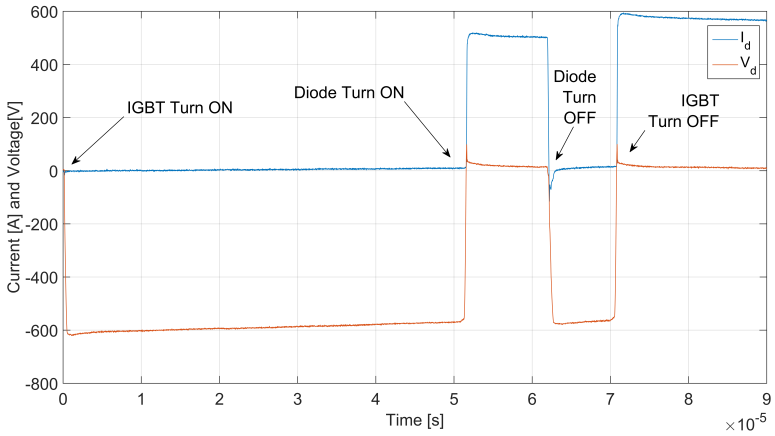
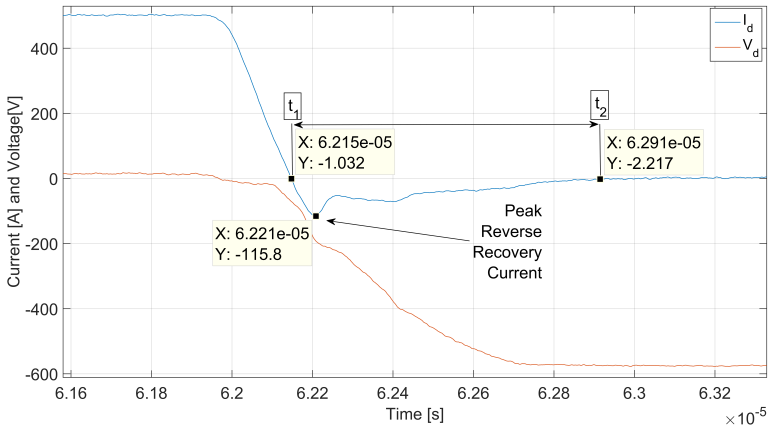
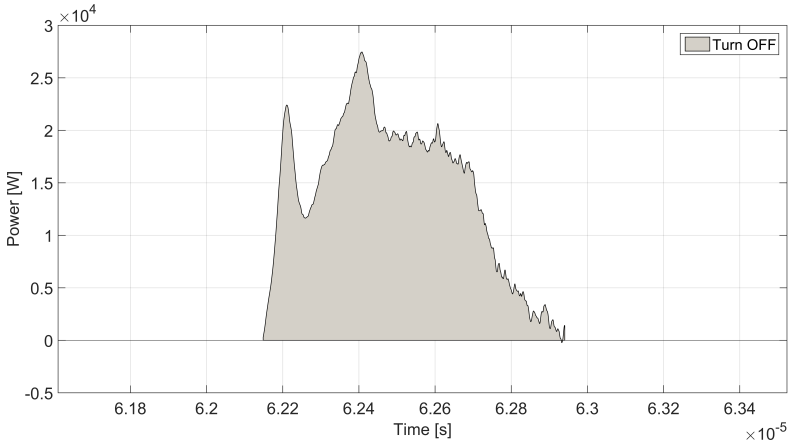


Figure 2.19: Double pulse test current and voltage waveforms of diode at 23 ℃ and 511 A test current.



(a) Turn OFF waveforms of the diode.



(b) Turn OFF energy.

Figure 2.20: The switching OFF time instance current and voltage waveforms and the energy loss during turn OFF of the diode.

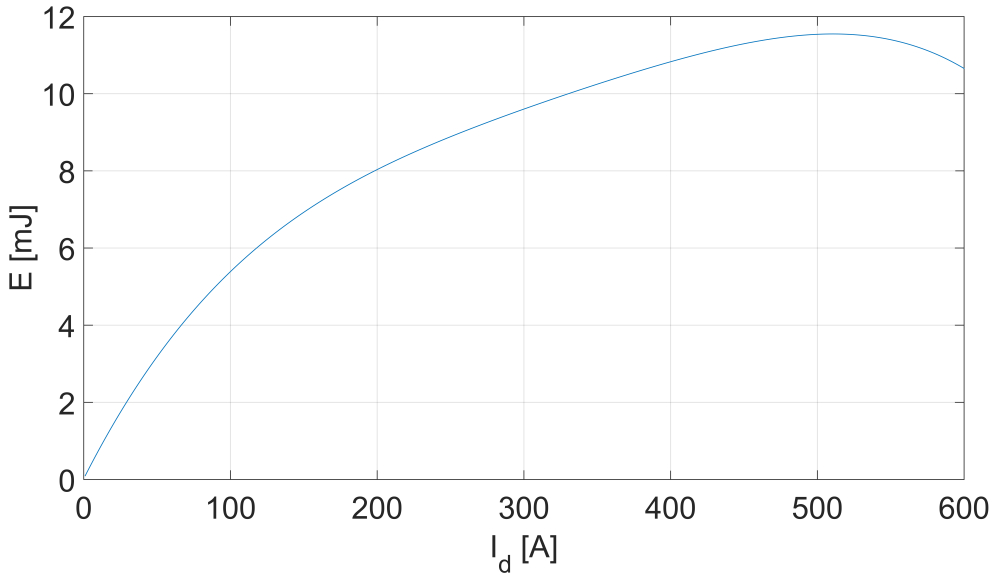


Figure 2.21: The diode switching energy loss versus current for 600 V.

2.4 Comparison of manufacturer and measured data

After obtaining a set of measurements for room temperature, it can be compared to the corresponding data provided by the manufacturer, to determine the deviations between them. The percentage difference is calculated as

$$Deviation\ [\%] = 100 * \frac{Measured\ Value - Manufacturer\ Value}{Manufacturer\ Value} \tag{2.25}$$

2.4.1 Conduction losses

The IGBT output characteristics comparison is presented in Figure 2.22, where it is observed that for the same current, measured U_{ce} is higher than what is claimed by the manufacturer. This difference is reflected in conduction power losses of Figure 2.23a and the same difference is quantified in percent in Figure 2.23b.

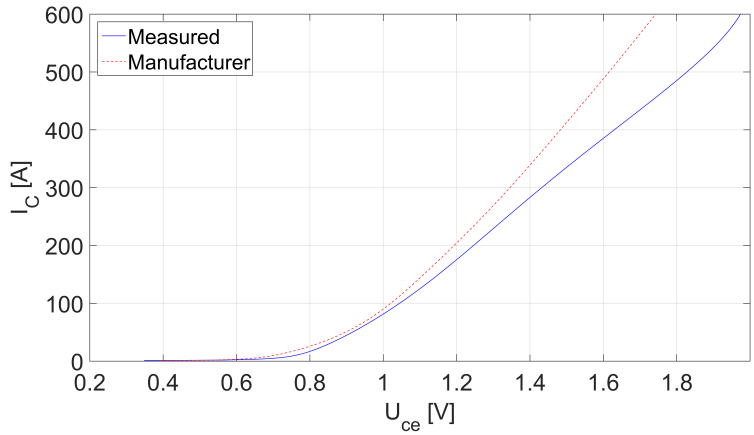
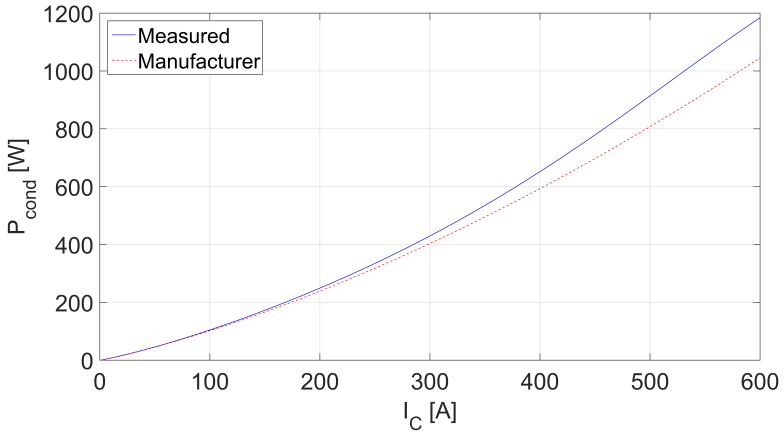
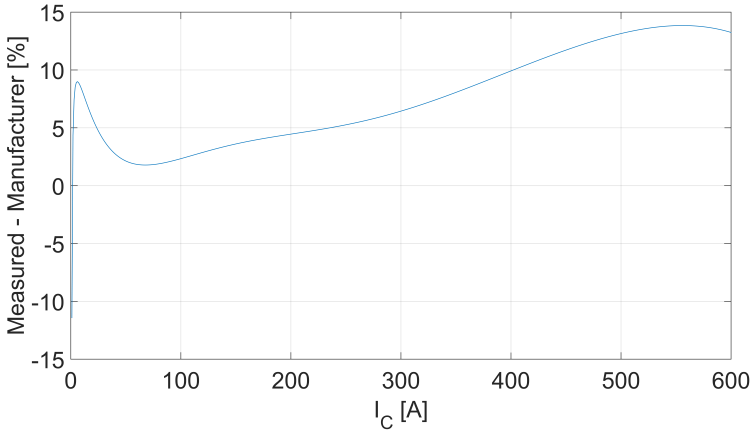


Figure 2.22: Comparison of the IGBT output characteristics between measurement and manufacturer data.



(a) IGBT Conduction Losses.



(b) Percentage difference.

Figure 2.23: Comparison of the IGBT conduction losses between measurement and manufacturer data.

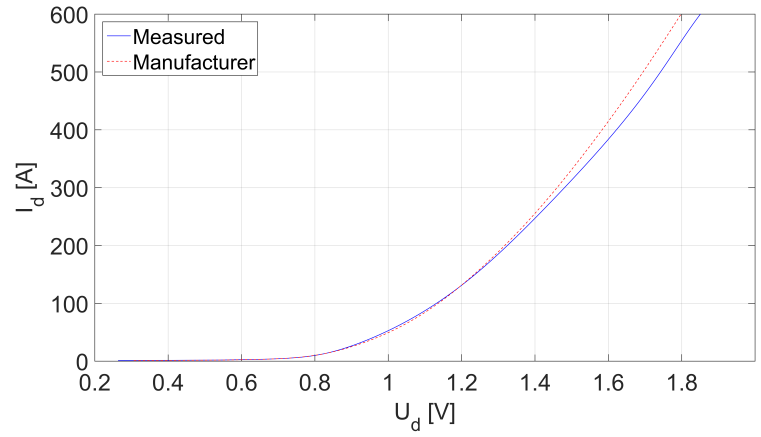
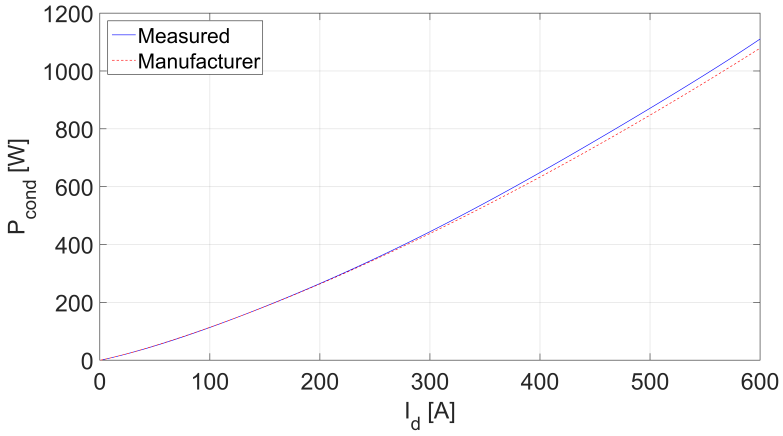
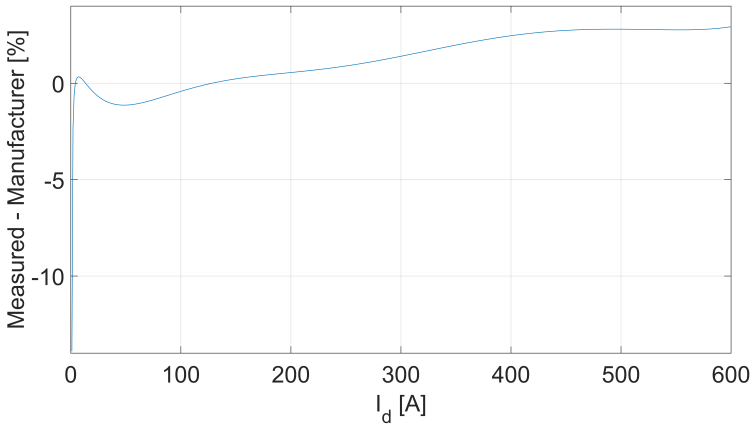


Figure 2.24: Comparison of the diode output characteristics between measurement and manufacturer data.



(a) Diode Conduction Losses.



(b) Percentage difference.

Figure 2.25: Comparison of the diode conduction losses between measurement and manufacturer data.

The same comparison pattern is followed for the diode, giving a comparison for its output characteristics in Figure 2.24. Regarding its conduction power losses, an absolute value comparison is illustrated in Figure 2.25a, while a percentage difference in Figure 2.25b. The measured losses are again higher that what manufacturer provides, but the difference for the diode is lower than for the IGBT.

2.4.2 Switching losses

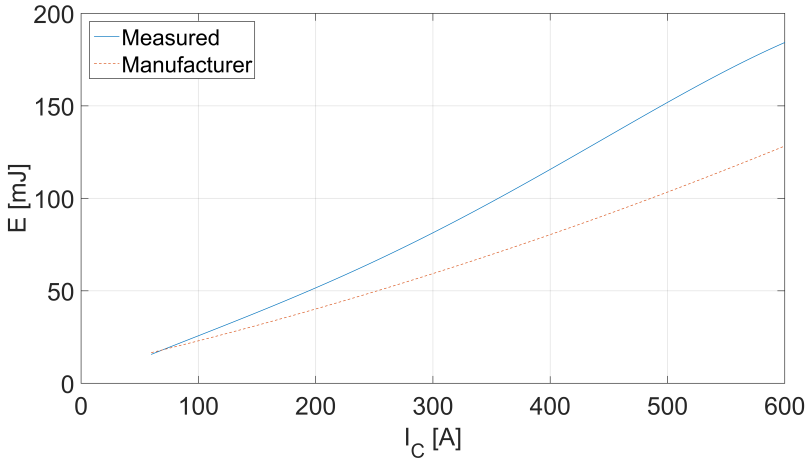


Figure 2.26: Comparison of the IGBT switching energy loss between measurement and manufacturer data.

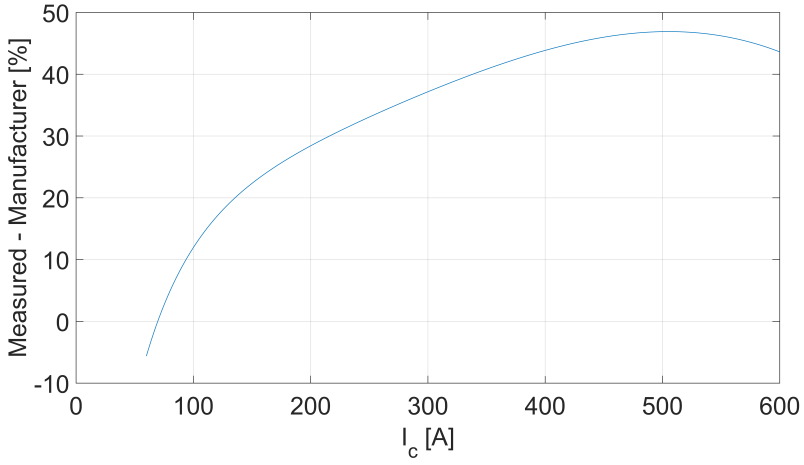


Figure 2.27: Percentage difference between measured and manufacturer provided switching energy loss for the IGBT.

For the IGBT switching energy loss comparison, the total energy is considered, as sum of turn ON and turn OFF values. Figure 2.26, illustrates the measured energy loss compared to that extracted from the data-sheet, while the difference in percent between them is presented in Figure 2.27.

The measured reverse recovery energy loss of the diode during its turn off is compared to the corresponding manufacturer value in Figure 2.28. Their percentage difference is illustrated in Figure 2.29 .

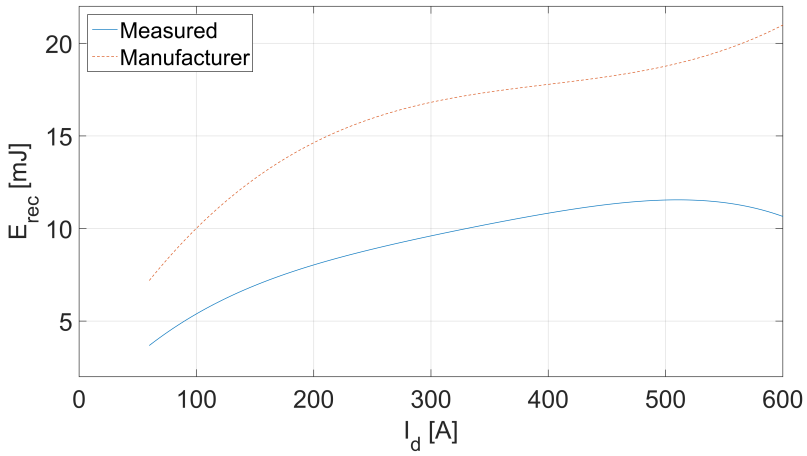


Figure 2.28: Comparison of the diode reverse recovery energy loss between measurement and manufacturer data.

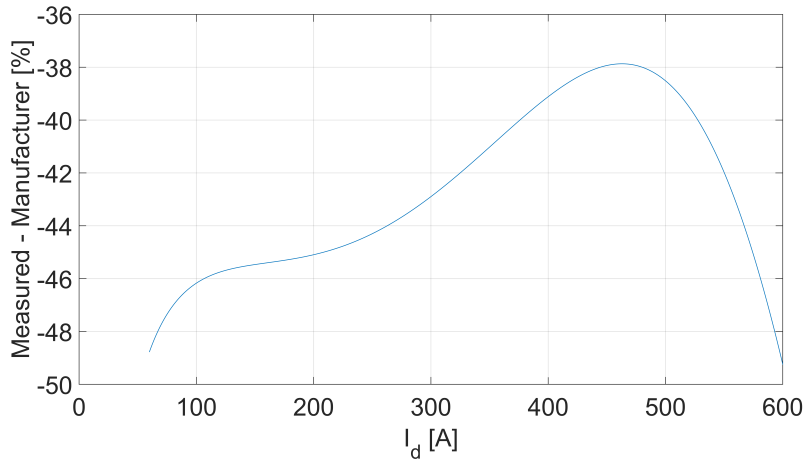


Figure 2.29: Percentage difference between measured and manufacturer provided reverse recovery loss for the diode.

2.5 Correlation of measurements with higher temperatures

As a result of both equipment and time limitations, experimental measurements of power losses for regulated higher junction temperatures have not been conducted. Temperature control of the junction would require the module to be mounted on a hot plate or heated by high current flowing through it. For the time being, no such

technique could be applied, so to compensate for that, a method to correlate the measured losses at room temperature with higher temperatures is proposed.

As stated already, the manufacturer provides conduction and switching losses information for different temperature levels. The proposed method extends the measured losses in higher temperatures, based on the temperature dependency as it is provided by the manufacturer. Thus, for an arbitrary temperature level T_x the ratio between the manufacturer losses value at T_x and at 23 ℃ is calculated as

$$r_{23 \longmapsto T_x} = \frac{Losses_{manuf,T_x}}{Losses_{manuf,23}} \tag{2.26}$$

where as *Losses* can be used either conduction or switching losses provided by the manufacturer, for any type of chip according to the case of interest. This ratio then, can be multiplied with the same type of measured losses at 23 ℃ to estimate a pseudo-measured losses value for T_x temperature as

$$Losses_{pseudo,T_x} = r_{23 \longmapsto T_x} * Losses_{meas,23} \tag{2.27}$$

Having established a model to obtain power losses for every operating point, look-up tables such as the ones in Appendix A.1 can be built.

2.6 Discussion

Conduction losses as extracted from data-sheet appear quite reliable, since they are not sensitive to changes between their standardization and the real application topology. In addition a wide range of temperatures is covered by the manufacturer, so it is safe to calculate precisely the conduction losses for different operating points. On the other hand, switching losses are provided for only two temperatures and extrapolating calculations for lower temperatures beyond the ones provided may introduce uncertainties. The existence of information about losses for an operating point at temperature of 25 ℃ though, improves that extrapolation. Calculating switching losses for different R_g values and current combinations than the operating point of 600 A provided, may also affect the accuracy of the result, since assumptions are considered as explained in Section 2.2.

Measurement of power losses of an IGBT module can be a demanding task. Regarding conduction losses, the junction temperature increases while current flows through each chip, so a short current pulse is preferred, to avoid excessive heating of the chip. The measurement should be taken as close as possible to the beginning of the current pulse, to correspond to the initial chip temperature. When it comes to switching losses, accuracy and bandwidth of the measuring equipment play important role for the quality of the measurement. The voltage and current probes must be able to measure accurately in a wide range of values, that for this thesis extended from 0 to more than 600 Volts and Amperes respectively.

Comparing the measured and the data provided by the manufacturer, it is observed that all measurements result in higher losses apart from the switching losses of the diode. As stated earlier, conduction losses are not affected by the operating environment, so the difference between experimental measurement and manufacturer

provided data is maximum 13 %, which may be a result of measurement accuracy for the experimental determination. Instead, switching losses appear 48 % higher for the IGBT and 38 % lower for the diode. This is an indication that operating conditions such as stray inductance, may differ between manufacturer and real application environment, causing large deviation between the two data-sets.

Finally, the method to correlate measurements with higher temperatures can give sufficient accuracy. This is confirmed if a comparison is made between a value obtained from this method and an experimentally obtained one. More specifically, during IR camera calibration tests, one IGBT chip is heated to 85 °C under 100 A and 180 W. That could correspond to heating four IGBT chips at the same temperature and 400 A, resulting in 720 W of heat. For the same current and temperature values, the pseudo-measured conduction losses result is 692 W, which is 3.8 % less compared to the actually measured value.

3

Thermal Measurements

3.1 Convection coefficient

3.1.1 Analytical calculations

As described in Section 2.3.3, the power module is mounted on top of an aluminum heat-sink that uses water as coolant. The heat-sink consists of metal fins, forming rectangular ducts through which the water flows. In order to asses the performance of the heat-sink, its heat transfer coefficient should be known. This coefficient is also used in the Finite Element Analysis as described in Section 4. In the following analysis, a numerical calculation of the heat-sink heat transfer coefficient is derived.

The heat exchange occurs through convection between the heat sink fins and the water that flows through the ducts. The heat-sink consists of 18 ducts with dimensions a_1 x b x l = 4.1 x 28 x 174 mm named Duct 1 and 2 ducts with dimensions a_2 x b x l = 6 x 28 x 174 mm named Duct 2.

For rectangular ducts, the hydraulic diameter D_h is defined as

$$D_h = \frac{2ab}{a+b} \tag{3.1}$$

where a and b are the width and the height of each duct respectively [17]. In that case $D_{h1} = 7.15\ mm$ and $D_{h2} = 9.88\ mm$ for the two different ducts.

Assuming a water flow $\dot{V}$ equal to 6 lit/min or 100 10^{-6} $\frac{m^3}{s}$ and an ambient temperature T_∞ of 20 ℃ for the water, its dynamic viscosity μ is 1.002 10^{-3} $\frac{Ns}{m^2}$, its density ρ is 998.3 $\frac{kg}{m^3}$, its thermal conductivity k is 598.40 10^{-3} $\frac{W}{mK}$ and its Prandtl number Pr is 7.01 [18].

The cross section that the water flows through in total is

$$A_{tot} = 9{*}a_1{*}b{+}1{*}a_2{*}b = 9{*}4.1{*}28{+}1{*}6{*}28 = 1201.20\ mm^2 = 0.0012012\ m^2 \tag{3.2}$$

and assuming that the water flow is divided equally to that total cross section, the flow through each Duct 1 would be

$$\dot{V}_1 = \dot{V}\frac{a_1 * b}{A_{tot}} = 9.56\ \frac{m^3}{s} \tag{3.3}$$

and the flow through each Duct 2

$$\dot{V}_2 = \dot{V}\frac{a_2 * b}{A_{tot}} = 13.99\ \frac{m^3}{s} \tag{3.4}$$

The speed at which the water flows through the ducts is then

$$U = \frac{\dot{V}}{A_{tot}} = 0.083 \ \frac{m}{s} \tag{3.5}$$

and the kinimatic viscosity of water is given as

$$\nu = \frac{\mu}{\rho} = \frac{1.002 \ 10^{-3}}{998.3} = 1.0038 \ 10^{-6} \ \frac{m^2}{s} \tag{3.6}$$

The dimensionless Reynolds number is calculated as

$$Re = \frac{U * D_h}{\nu} \tag{3.7}$$

so for the two different ducts it should be

$$Re_1 = \frac{U * D_{h1}}{\nu} = 593.20 \ and \ Re_2 = \frac{U * D_{h2}}{\nu} = 819.59 \tag{3.8}$$

Since both Re_1 and Re_2 are less that 2300, the flow through all ducts is characterized as *laminar* [17].

The thermal entry length is calculated as

$$L_t = 0.05 * Re * Pr * D_h \ so \ L_{t1} = 1487.20 \ mm \ and \ L_{t2} = 2838.90 \ mm \tag{3.9}$$

meaning that the flow through every duct is *thermally developing* (nowhere fully developed), since the entralce length is longer than the actual length of the ducts [17].

As discussed in [17], there are two ideal cases that can be studied and give the boundaries that the convection coefficient lies between. One case assumes uniform temperature across the walls of the duct (fins, top and bottom regions of the heat-sink) and the other assumes uniform heat flux all over them.

Starting by the uniform temperature case and considering the specific geometry and dimensions of each duct that define the coefficients of the following equations, the dimensionless Nusselt number Nu is given according to [17] as

$$Duct \ 1: \ Nu_{1T} = 5.37 + \frac{0.03 * \frac{D_{h1}}{l} * Re_1 * Pr}{1 + 0.016 * [\frac{D_{h1}}{l} * Re_1 * Pr]^{\frac{2}{3}}} \Longrightarrow Nu_{1T} = 8.80 \tag{3.10}$$

and

$$Duct \ 2: \ Nu_{2T} = 4.44 + \frac{0.03 * \frac{D_{h2}}{l} * Re_2 * Pr}{1 + 0.016 * [\frac{D_{h2}}{l} * Re_2 * Pr]^{\frac{2}{3}}} \Longrightarrow Nu_{2T} = 10.01 \tag{3.11}$$

where the index T refers to the uniform temperature case.

Having both Nusselt numbers the convection coefficient is calculated as

$$Duct \ 1: \ h_{1T} = \frac{Nu_{1T} * k}{D_{h1}} = \frac{8.80 * 598.40 \ 10^{-3}}{7.15} \Longrightarrow h_{1T} = 736.66 \ \frac{W}{m^2 K} \tag{3.12}$$

and

$$Duct\ 1:\ h_{2T} = \frac{Nu_{2T} * k}{D_{h1}} = \frac{10.01 * 598.40\ 10^{-3}}{9.88} \Longrightarrow h_{2T} = 605.96\ \frac{W}{m^2K} \quad (3.13)$$

For the case of uniform heat flux the only difference with the previous case is the first term of (3.10), that is modified according to [17] and considering the corresponding duct geometry as

$$Duct\ 1:\ Nu_{1F} = 6.27 + \frac{0.03 * \frac{D_{h1}}{l} * Re_1 * Pr}{1 + 0.016 * [\frac{D_{h1}}{l} * Re_1 * Pr]^{\frac{2}{3}}} \Longrightarrow Nu_{1F} = 9.71 \quad (3.14)$$

and

$$Duct\ 2:\ Nu_{2F} = 5.33 + \frac{0.03 * \frac{D_{h2}}{l} * Re_2 * Pr}{1 + 0.016 * [\frac{D_{h2}}{l} * Re_2 * Pr]^{\frac{2}{3}}} \Longrightarrow Nu_{2F} = 10.90 \quad (3.15)$$

where the index F refers to the uniform heat flux case.

Accordingly, the convection coefficient is calculated as

$$Duct\ 1:\ h_{1F} = \frac{Nu_{1F} * k}{D_{h1}} = \frac{9.71 * 598.40\ 10^{-3}}{7.15} \Longrightarrow h_{1F} = 811.95\ \frac{W}{m^2K} \quad (3.16)$$

and

$$Duct\ 2:\ h_{2F} = \frac{Nu_{2F} * k}{D_{h1}} = \frac{10.90 * 598.40\ 10^{-3}}{9.88} \Longrightarrow h_{2F} = 659.85\ \frac{W}{m^2K} \quad (3.17)$$

The amount of heat Q that is absorbed by convective heat transfer is given by

$$Q = h * A * \Delta T \Longleftrightarrow Q = h * A * (T_w - T_\infty) \quad (3.18)$$

where h is the convection coefficient, A is the surface through which the convection takes place, T_w is that surface temperature and T_∞ is the coolant ambient temperature, defined as an average value along the path of the coolant. In the case described above, the area A would be the surface of the duct along its length axis, as seen in Figure 3.1, where this area is highlighted. For Duct 1 this area equals to $A_1 = 2 * (a_1 + b) * l = 0.0112\ m^2$ and for Duct 2 to $A_2 = 2 * (a_2 + b) * l = 0.0118\ m^2$.

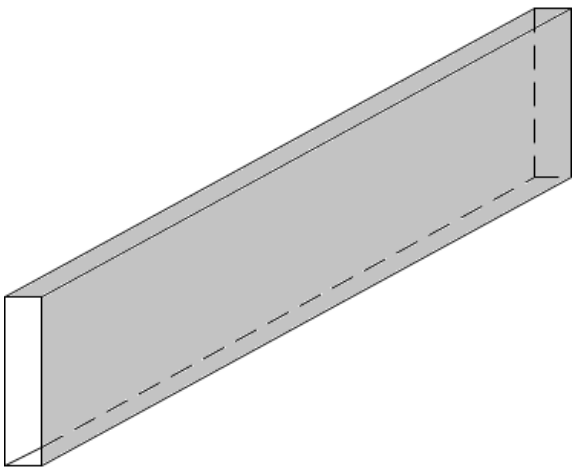


Figure 3.1: The area A through which convective heat transfer occurs at each duct.

Since there is no evidence about which condition (uniform temperature of heat flux) is fulfilled for the body of the heat-sink, an average convection coefficient between these two cases can be calculated. Starting again with the temperature case, the $h * A$ product of (3.18) would be

$$h_T A = 18 * h_{1T} * A_1 + 2 * h_{2T} * A_2 = 162.46 \frac{W}{K} \tag{3.19}$$

and for the flux case

$$h_F A = 18 * h_{1F} * A_1 + 2 * h_{2F} * A_2 = 178.88 \frac{W}{K} \tag{3.20}$$

so an average value would be

$$hA = \frac{h_T A + h_F A}{2} = 170.67 \frac{W}{K} \tag{3.21}$$

In Figure 3.2 the derivations above are repeated for different values of flow rates in the range of 3 up to 10 $\frac{lit}{min}$.

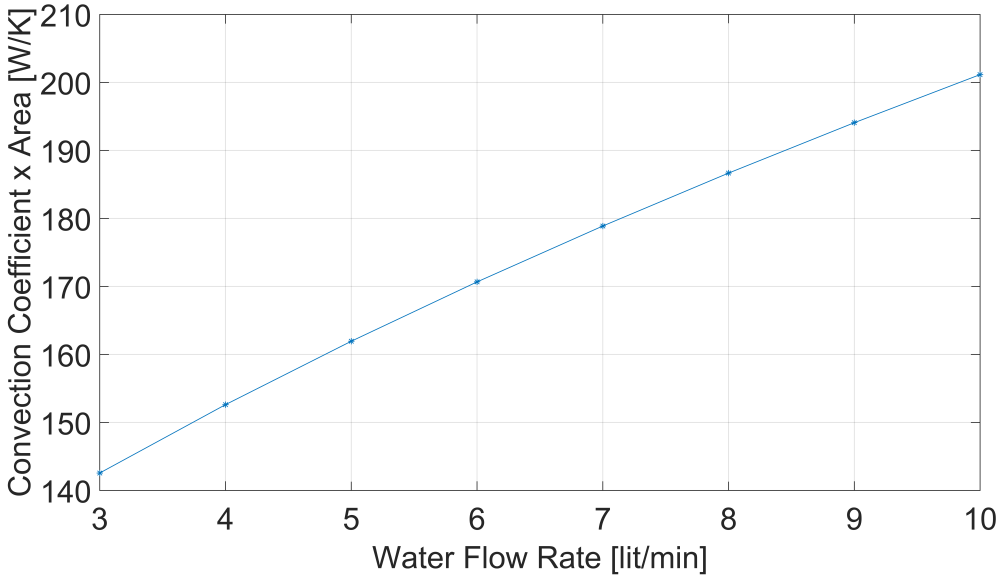


Figure 3.2: Analytical Calculation of average h*A product for different water flow rates.

3.1.2 Experimental determination

Method description

Since the analytical calculation for the convection coefficient of the aluminum heat-sink may introduce uncertainties about the actual value, an experimental determination has been conducted through measurements. The method is based on (3.18), where Q,A,T_w and T_∞ can be determined by measurements, allowing for h to be calculated. The convection coefficient is also determined for various water flow rates.

The heat Q injected in the heat-sink is generated using resistors attached on the heat-sink surface. In that case and in contrast with the analytical calculation, as area A is considered the upper surface of the heat sink where the IGBT module would be attached, with dimensions 280x180 mm. The reason for this selection is connected with the Finite Element Analysis where, as explained in Section 4, the convection surface is considered as the top plane of the heat-sink. As T_w is defined the average temperature of two measurement points in the body of the heat-sink and as T_∞ is considered the arithmetic average of the inlet and outlet water temperature.

Test setup and measurements

The practical set-up for the implementation of this measurement consists of the heat-sink with attached resistors on its top surface, a DC power supply, measuring and logging equipment and finally a water circuit of hoses and pipes. The heat generated by the resistors is absorbed by the heat-sink and the temperatures are monitored.

Specifically, the electric part includes a Delta Elektronika™ SM $15 - 200$D DC power supply, adjusted to output a voltage of 12.91 V. This voltage is applied to six resistors of 1 Ω connected in parallel. The heat-sink is covered with thermal insulation, to avoid heat dissipation out of the heat-sink body, so as a result a total input power of 1 kW is injected as heat in the heat-sink. In Figure 3.3 the electric part of the set-up is illustrated. An ampere- and a voltmeter are used to accurately monitor the power dissipated in the resistors.

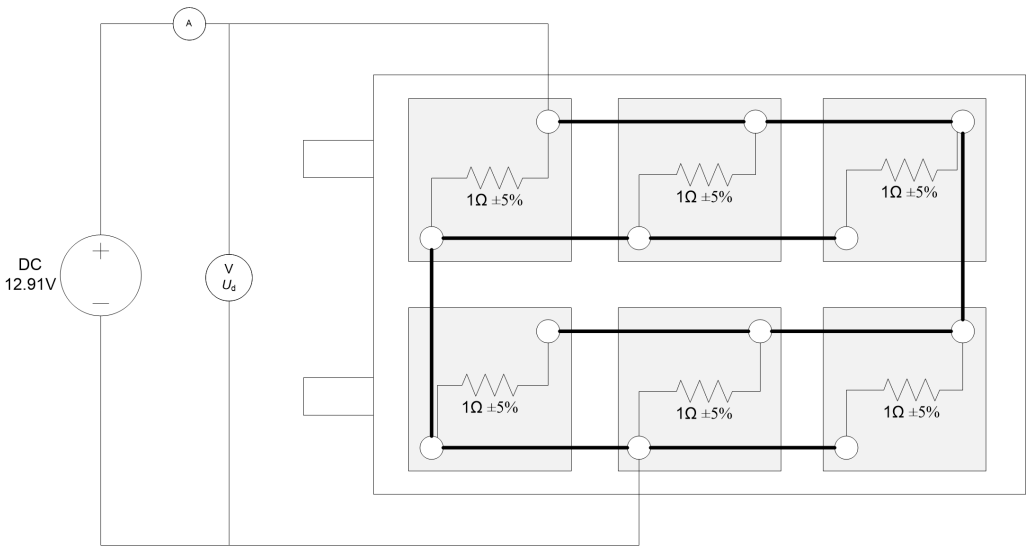


Figure 3.3: The electrical part of the convection coefficient measurement set-up.

The water flowing circuit consists of a pump that circulates water through hoses with a pressure of 2 $bars$. Since the measurement requires different water flow rates through the heat-sink, but the pump can only adjust its pressure, a free-wheeling path with an adjustable valve is built between the inlet and the outlet of the heat-sink for part of the flow to by-pass the heat-sink. The water temperature for both the inlet, $T_{water,inlet}$, and outlet, $T_{water,outlet}$, of the heat-sink is measured using type K

thermocouples. In addition, the flow rate is also measured for both sides. Two type K thermocouples are placed in the body of the heat-sink by drilling two holes in it and measuring $T_{heatsink,1}$ and $T_{heatsink,2}$ at the upper surface of the ducts. The whole set-up with the corresponding dimensions of the heat-sink elements are illustrated in Figure 3.4.

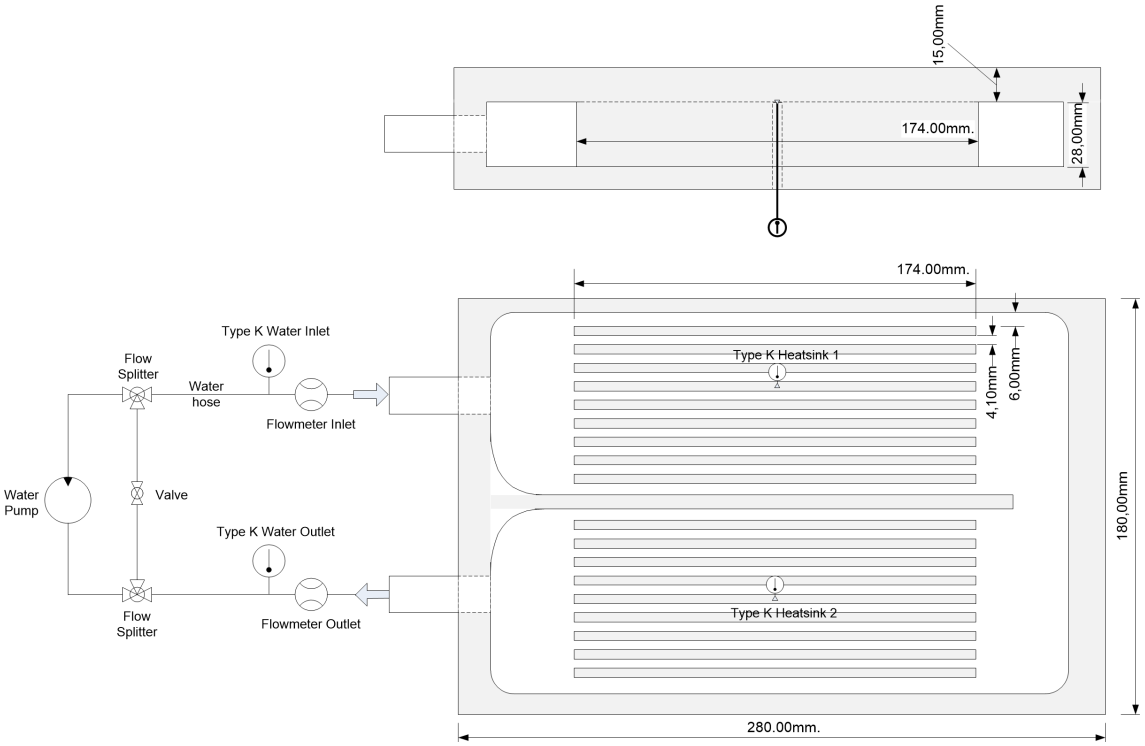


Figure 3.4: The interior of the heat-sink, its dimensions and the water supply circuit.

The practical procedure starts with the adjustment of the water flow to the desired level, by operating the by-pass valve. The DC power supply is then turned on and its output voltage is set to 12.91 V. The heat-sink temperatures are monitored and when steady state is achieved (no further increase in $T_{heatsink,1}$ and $T_{heatsink,2}$) the input power Q, the inlet and outlet water temperatures and the heat-sink temperatures are logged for a time span of 15 min at a rate of 5 Hz. Then each of these measurements is averaged over time to suppress noise, resulting in $\bar{Q}$, $\bar{T}_{water,inlet}$,$\bar{T}_{water,outlet}$,$\bar{T}_{heatsink,1}$ and $\bar{T}_{heatsink,2}$. Logging is done using LabView software from Natural Instruments™ in combination with data acquisition devices from the same company.

Results

The convection coefficients are calculated using (3.18), here reformulated as

$$h = \frac{Q}{A * (T_w - T_\infty)} \tag{3.22}$$

where Q is the electric input power, A is the heat-sink area equal to 0.0504 m^2, T_w is the average of $\bar{T}_{heatsink,1}$ and $\bar{T}_{heatsink,2}$ and T_∞ the average of $\bar{T}_{water,inlet}$ and $\bar{T}_{water,outlet}$. The graph of Figure 3.5 presents the product hA for different water flows, as a result of the method described above.

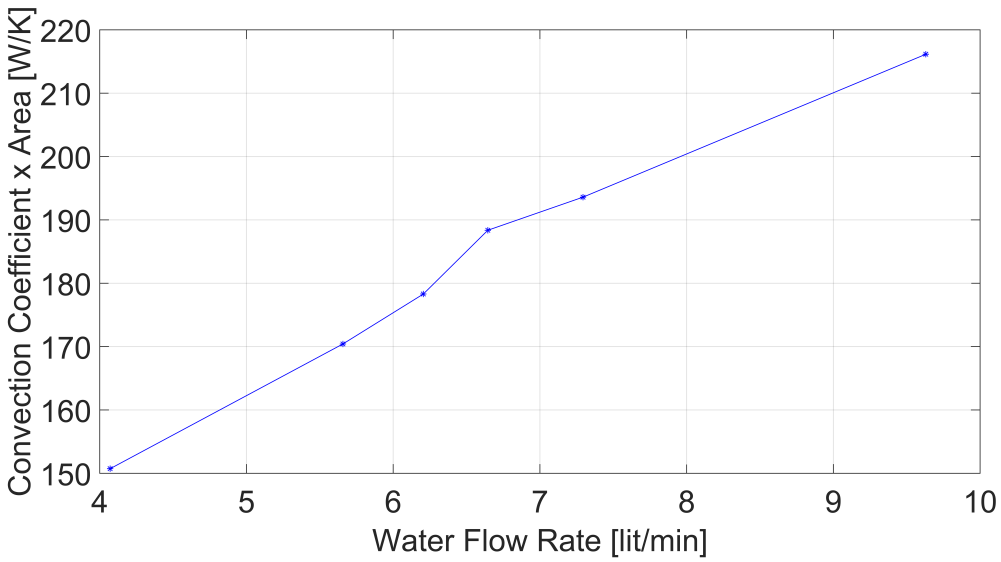


Figure 3.5: Measured h*A product for different water flow rates.

3.1.3 Discussion

This approach of analytically calculating the total convection coefficient for the heat-sink, by considering the convection coefficient of each duct, provides an acceptable estimation as seen from the comparison between the calculations of Section 3.1.1 and the measurements of Section 3.1.2. There are though some deviations coming from assumptions and approximations as discussed below.

According to [17], this analytical method based on dimensionless numbers such as Prandtl, Nusselt and Reynolds is oriented on empirical determination of the coefficients of the equation such as (3.10). Moreover, the fact that the heat-sink thermal condition may lie anywhere between the uniform temperature and uniform heat flux case, introduces one more uncertainty to the calculations. Finally, there has been no accurate determination of the way the water enters the heat-sink and spreads through the ducts, rather than assuming a uniform division of the water flow.

On the other hand, a more accurate approach would be to simulate the heat-sink in a CFD (Computational Fluid Dynamics) software package that would calculate more accurately the water flow through each duct and extract a more accurate model of the convective heat transfer mechanism. However, that would be a more complicated and resource demanding solution that is not considered necessary for this application.

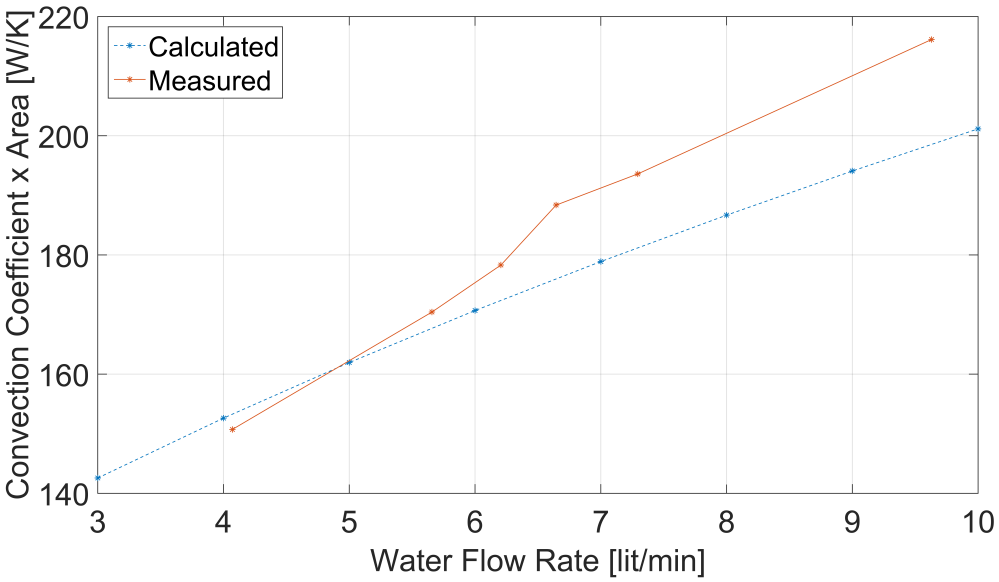


Figure 3.6: A comparison between calculation and measurement of the convection coefficient.

In Figure 3.6 a comparison between the measured and calculated convection coefficient is presented. As seen, for lower flow rates the two cases match closely but for higher flow rates the difference starts to grow, resulting in higher values for the measured coefficients compared to the calculated ones. This could be a result of turbulence presence in the flow when water velocity increases. For the theoretical, calculation laminar flow was assumed along the whole duct for the whole flow rate range. However, for higher flow rates it is possible that the water is not split evenly for all the ducts, resulting in higher velocities and transitional flow towards turbulence for some ducts. This turbulence has the effect of increasing the convective heat transfer, explaining the difference between theoretically and practically determined convection coefficients for higher flows. Nevertheless, the maximum deviation is approximately less than 10% which is acceptable considering the assumptions.

3.2 Calibration of chip temperature measurements

3.2.1 Climate chamber test - $U_{ce}(T)$ determination

Description of method

The key point to evaluate the thermal behavior of the power module, is to know the junction temperature of its chips. There could be various ways to measure that temperature, such as attached thermocouples or infra-red thermal cameras but constraints in accuracy and bandwidth of the measurement call for an improved procedure [19]. In this section the widely used $U_{ce}(T)$ method is described.

This method is based on the linear relationship between the collector emitter voltage U_{ce} and the junction temperature T_j of the chip, originating from the temperature dependence of diffusion voltage in a pn junction. For nominal currents of

several hundred Amperes, there is a positive coefficient between U_{ce} and T_j, but for low currents in the order of a few decades of mA , that coefficient is negative and usually close to $-2\ mV/K$. Thus a calibration process is enough to reveal the $U_{ce}(T)$ connection and obtain an accurate measurement of the temperature of the chip in a simple way by using the chip itself as its own temperature indicator [19].

Test setup and measurements

For this test, the power module is placed in a climate chamber able to accurately regulate its temperature and hold it between ±0.5 ℃ of the desired value. A sensing current of 100 mA is provided by a current source, carefully chosen to maintain a constant current output regardless of its operating conditions. Finally a voltage source is used to provide 15 V to the gate terminal of the IGBT, in order to control its turn-on and turn-off and a high resolution volt-meter is used to measure the voltages of interest. The whole test setup is illustrated in Figure 3.7.

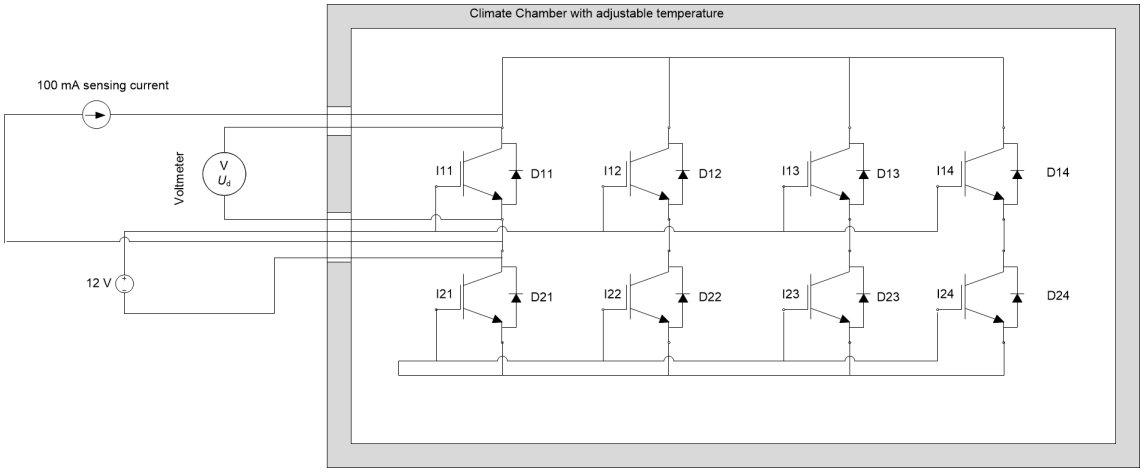
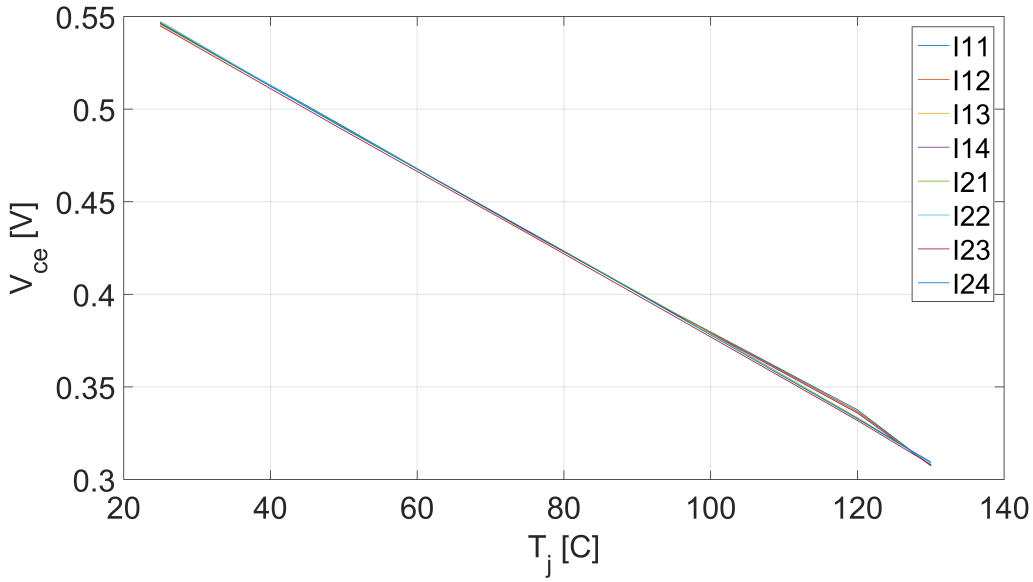
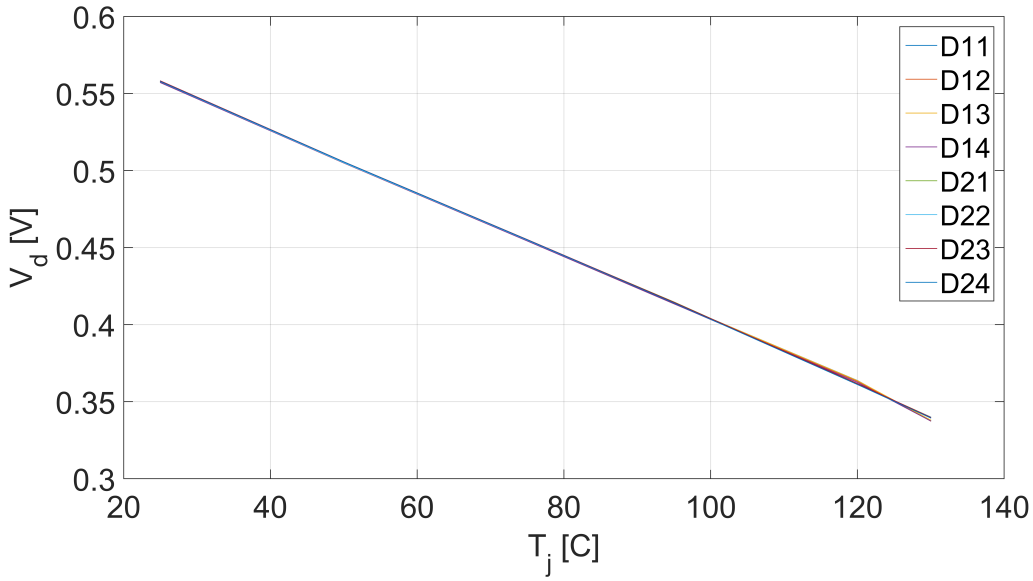


Figure 3.7: The setup of the climate chamber test.

The procedure of the test starts by setting the climate chamber to a desired temperature and letting the module inside the climate chamber long enough (around 20′) to obtain this temperature value all over its mass in a steady state, homogeneous condition. Then the 100 mA sensing current is provided through an IGBT while its gate is held at $+15\ V$ to allow conduction. The voltage between the collector and emitter of the IGBT, U_{ce} is measured. The same task is performed for all eight IGBT:s on the module. Similarly, the same sensing current is provided at the anti-parallel diodes of each IGBT in their forward direction and the voltage between the anode and the cathode is measured. This way the module, consequently the chip itself, are kept at a uniform temperature and the measured voltage is characteristic of that temperature. The same measurements are repeated for several temperatures in the range between 25 ℃ and 130 ℃ in steps as shown in Tables A.5 and A.6 along with the measured voltages in Volts for each IGBT (Ixy) and Diode (Dxy), where x and y denote a row and column index respectively. The raw data from these tables is plotted in Figures 3.8a and 3.8b, revealing the linearity between U_{ce} and T_j.



(a) IGBT:s



(b) Diodes

Figure 3.8: Measured U_{ce} for each chip type with respect to its temperature.

Results

Having the measurements between U_{ce} and T_j, the corresponding equation to describe their relationship is needed. For that reason each column of Tables A.5 and A.6 was fitted to a first order polynomial that would describe the linear relation between U_{ce} and T_j. A first order equation would be of the form

$$U_{ce}(T) = \alpha T_j + \beta \Leftrightarrow T_j = \frac{U_{ce} - \beta}{\alpha} \tag{3.23}$$

where α and β are the coefficients extracted by curve fitting. These coefficients are presented in Table A.7 for each IGBT and diode. Using (3.23) with the coefficients from Table A.7, it is possible to obtain the junction temperature of each chip with high accuracy as well as high speed of sampling. Finally, this method provides a temperature value that is approximately equal to the area weighted temperature of the chip surface.

3.2.2 Transient chip temperature measurements

Description of Method

The purpose of this experimental test is to measure and log the way that the temperature of each chip on the power module is increased, when a heat step is applied to it, as if it would operate under real-world load and cooling conditions. This method takes advantage of the fact that cooling of the chips follows exactly the same temperature-time path as heating [19] and considering that it is more convenient to apply a sudden heat step-down and measure, than the opposite, cooling of the chip is studied. A controlled current is then driven through the chip heating it up and after several minutes in steady state, the current is quickly turned off. Water flows through the heat-sink under known rate for the whole experiment duration. The chip temperature is logged with a fixed frequency as it cools down and this data is used to derive the thermal impedance of the chip. The temperature of the nearby chips is also logged to study the thermal coupling between the chip under load and its neighbors and obtain this thermal impedance as well.

Table 3.1: The heated and measured chips combinations

Chip under heat	Chip under measurement
I13	D12
	D13
	D23
	D24
	I12
	I13
	I23
	I24
D23	D12
	D13
	D22
	D23
	I12
	I13
	I22
	I23

Considering the topology and the symmetry of the chips on the physical power module, seen in Figure 1.11, it is enough to heat one IGBT and one diode for one

substrate layer. This way, both kind of chips (Diode and IGBT) are studied on the way they heat up themselves, as well as the way they affect all their nearby chips on the same and on different substrates. As a result, two cases are formed as seen in Table 3.1. The naming of the chips can be found in Figure 1.12.

It is assumed that there is no thermal coupling between the heated chip and chips more than two chips away. This has been verified by Finite Element simulations for convection coefficients above 3000 $\frac{W}{m^2K}$.

Test setup and measurements

The test set-up could be divided in two sections. The first section is the cooling circuit, where water flows in the heat-sink and the power module is mounted on it, using a phase changing aluminium thermal film (HALA™ ALUFilm TPC-T102-AL-CB) in between to ensure good thermal contact. The second part is the electrical circuit where a Delta Elektronika™ SM $15-200$D DC power supply provides constant power by controlling the current through each chip. The measured channels are monitored and logged using LabView software from Natural Instruments™ again coupled with data acquisition devices from the same company.

In more detail, water flows in the heat-sink at a constant rate of 6.2 $\frac{lit}{min}$, while inlet and outlet water temperatures, as well as its flow rate are logged during steady state and before the current is shut off. The DC power supply is set to 100 A when I23 is heated and 108 A when a D23 is heated, resulting in a constant input power of 180 W for both chips. The required load current differs due to different forward voltage drops of the two chips, since uniform power is desired. The sensing current is also driven through the chip under measurement. The NTC temperature is monitored and when it is stabilized, meaning that the module is in thermal steady state, the load current is turned off using a MOSFET to achieve as fast turn-off as possible and emulate a heat step-down. During the cooling down, the U_{ce} is logged at 5 kHz and converted to junction temperature using the coefficients of Section 3.2.1. It is worth mentioning that the four parallel switches of each row are isolated from each other in order to be studied and controlled separately. Figure 3.9 illustrates the test set-up for heating one chip of the upper row IGBT:s and measuring its cool down. For the rest combinations, the set-up remains the same except of the load and sensing current paths. The highlighted text-boxes represent monitored signals.

As a supplement to the test described above, an IR heat camera is used to verify the steady state measured temperatures, as well as indicate any temperature gradient on the chip surface. For that reason the power module is painted with high emissivity black coating, I14 and D14 are heated in separate tests and the heat camera is placed above them. The reason for choosing these switches is a consequence of the module topology. They are the only ones that offer clear field of view for the heat camera. Three different input power levels are chosen for the chips at 84 W,127 W and 179 W and pictures of the chip area are obtained using the thermal camera.

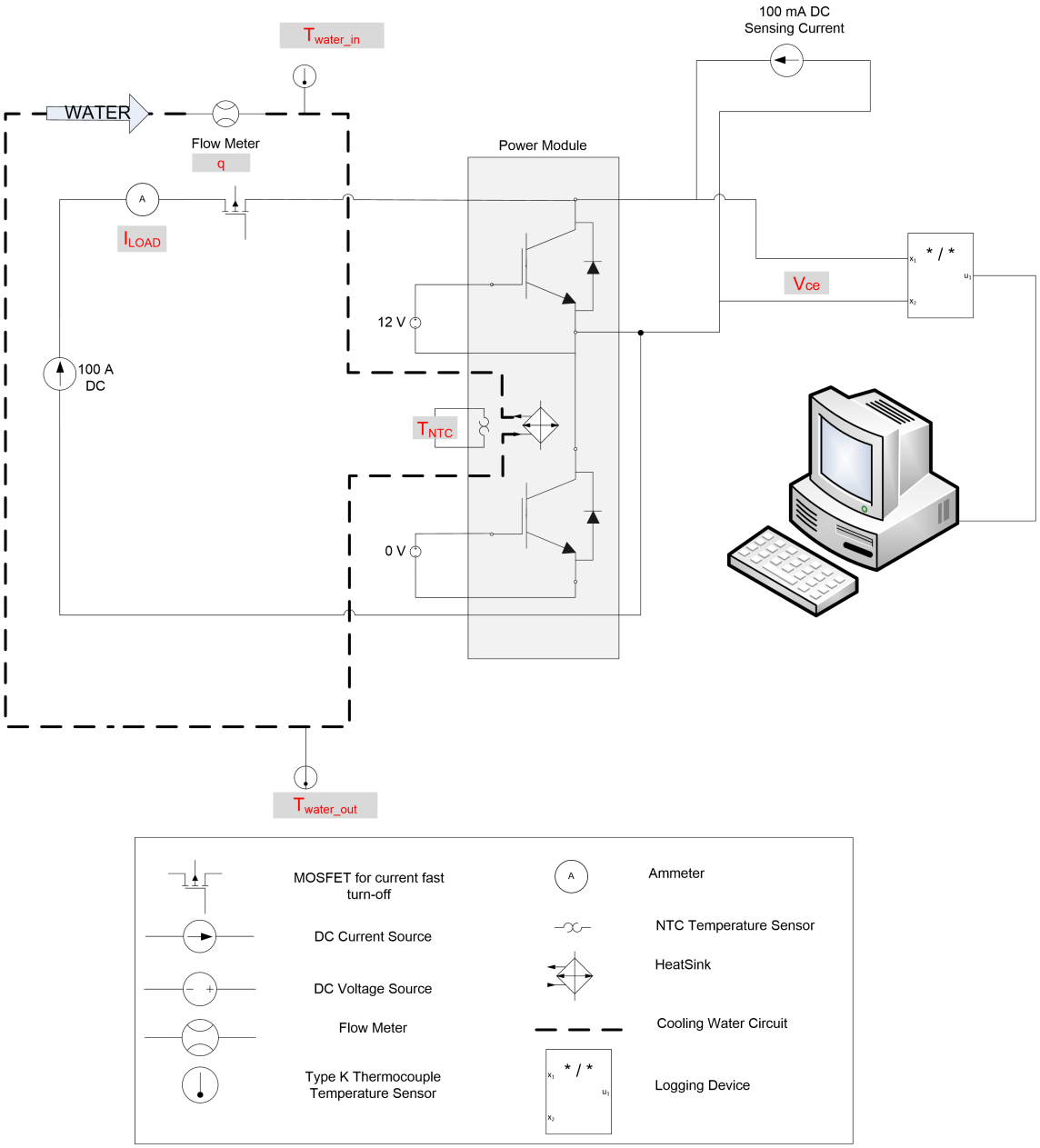
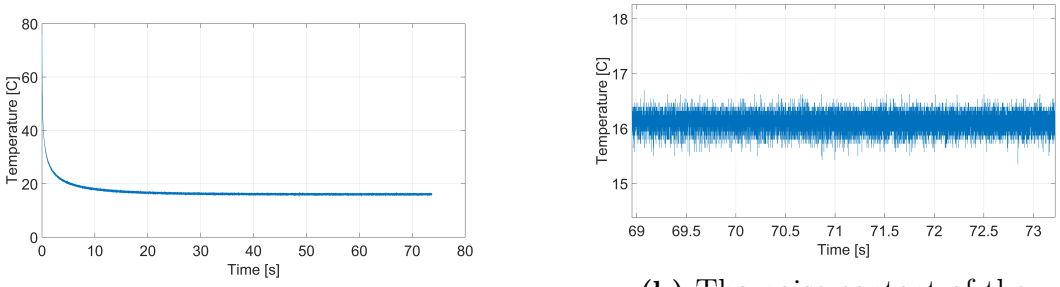


Figure 3.9: The test set-up for heating and measuring the thermal response of an IGBT switch.

Results

The measured U_{ce}, after being transformed to the corresponding junction temperature, forms an exponentially descending graph similar to that of Figure 3.10. In Figure 3.10a the whole cooling down path is illustrated and in Figure 3.10b a closer view of the measurement is depicted. As it is observed the high frequency noise that is captured along with the useful data, forms a peak-to-peak distortion of 1 °C. For that reason each measurement is filtered during post-processing using a moving average filter.



(a) The chip cooling down.

(b) The noise content of the measurement.

Figure 3.10: The whole cooling down path of I13 and a closer look at the raw measured data.

In order to depict the heating-up path of each chip, the filtered measurement is flipped vertically resulting in an ascending temperature waveform. That transformation is realized by creating a new waveform as

$$g(t) = T_{max} + T_{min} - f(t) \tag{3.24}$$

where T_{max} and T_{min} are the maximum and minimum captured temperatures, $f(t)$ is the input sample and $g(t)$ is the flipped sample. The minimum temperature is considered as the average value the samples during the last 3 seconds of each input waveform. Moreover, since the transient phase occurs during the first seconds, a logarithmic time scale is selected to illustrate more accurately the heating response during this period. In Figure 3.11, the temperature response of each measured chip is illustrated when $I13$ is heated, while in Figure 3.12, the same result is presented for the case of $D23$ heating.

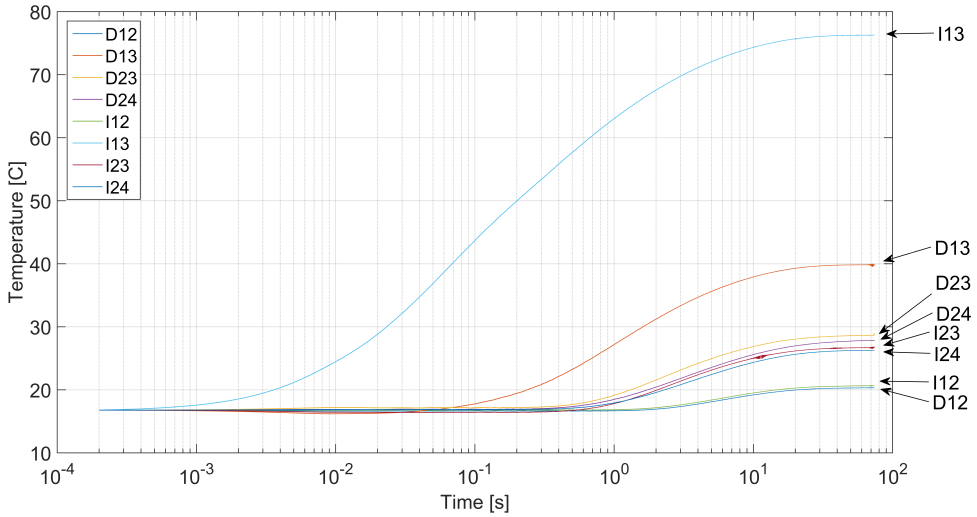


Figure 3.11: The temperature increase of selected chips when I13 is heated.

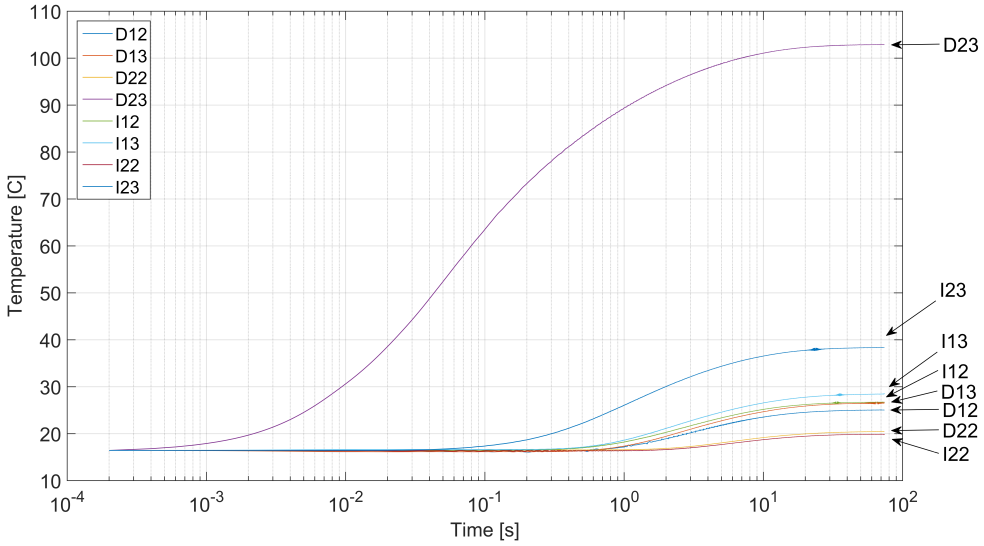
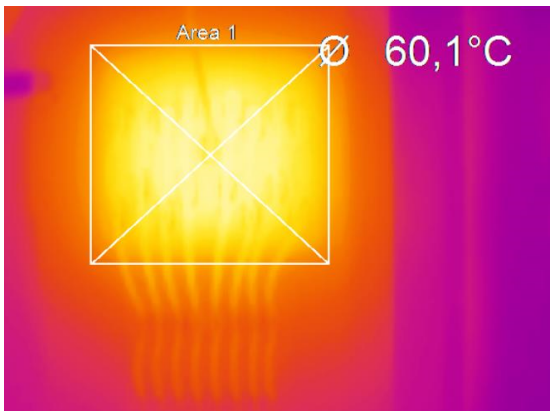
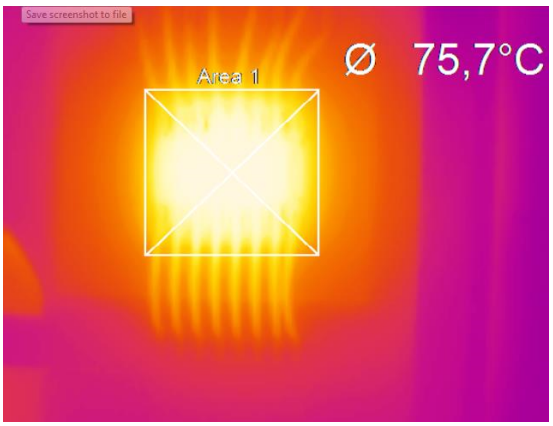


Figure 3.12: The temperature increase of selected chips when D23 is heated.

The raw data obtained, has minor deviations in the initial temperatures in the range of 2 ℃ at $t = 10^{-4}$. This is partially a result of fluctuations in the cooling water temperature, but also of $U_{ce}(T)$ method measurement noise. Since this test aims in obtaining the thermal impedance of the module and this is calculated based in temperature differences (as will be explained later), it is possible to align the temperature increase of each chip to a common initial temperature, without introducing any distortion to its temperature increase curve. Thus, the average of each chip temperature is calculated for $t = 10^{-4}$ and every curve is moved to start from this average.



(a) Steady state temperature of I14.

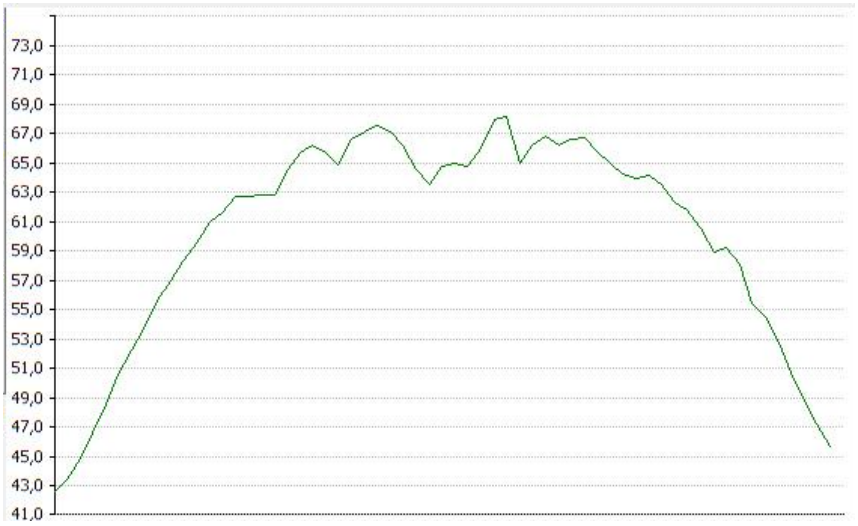


(b) Steady state temperature of D14.

Figure 3.13: The steady state temperature of the area of each chip from the IR camera at 127 W of input power.

Regarding the IR camera recordings, for every chip and input power level the chip area is selected in the camera frame and its average temperature is automatically calculated by the IR camera software for this area as seen in Figure 3.13 for the case

with 127 W of input power. In addition a diagonal line temperature profile is built and the temperature across this line is extracted and presented in Figure 3.14.



(a) Steady state temperature profile of I14.



(b) Steady state temperature profile of D14.

Figure 3.14: The steady state temperature profile of the diagonal of each chip at 127 W of input power.

In the graph presented in Figure 3.15, the heat camera results are gathered for every chip and every power level and compared to the corresponding temperatures obtained with the $U_{ce}(T)$ method. The area average of the chip temperature is the value that can be directly compared to the temperature obtained with $U_{ce}(T)$ method. The value obtained from the IR camera though appears always lower than the average temperature from $U_{ce}(T)$ method and this is a result of the shading caused by the bond wires that are placed on top of the chip surface having slightly lower temperature than the chip surface. This difference increases as the input power (consequently the chip temperature) increases. For the same input power the difference in values between the two methods is higher in the diode chip, because it

is smaller in area, so the bond wire shading phenomenon is more evident.

Another interesting point is how maximum temperature correlates with the average value and as observed from the same graph, the difference between the average and maximum temperature value increases for increased input power. As seen in Figure 3.14 the temperature gradient for the chip area is significant and spans up to 40 K. The spikes observed in the temperature profile of the same figure are the shading effect of the bond wires.

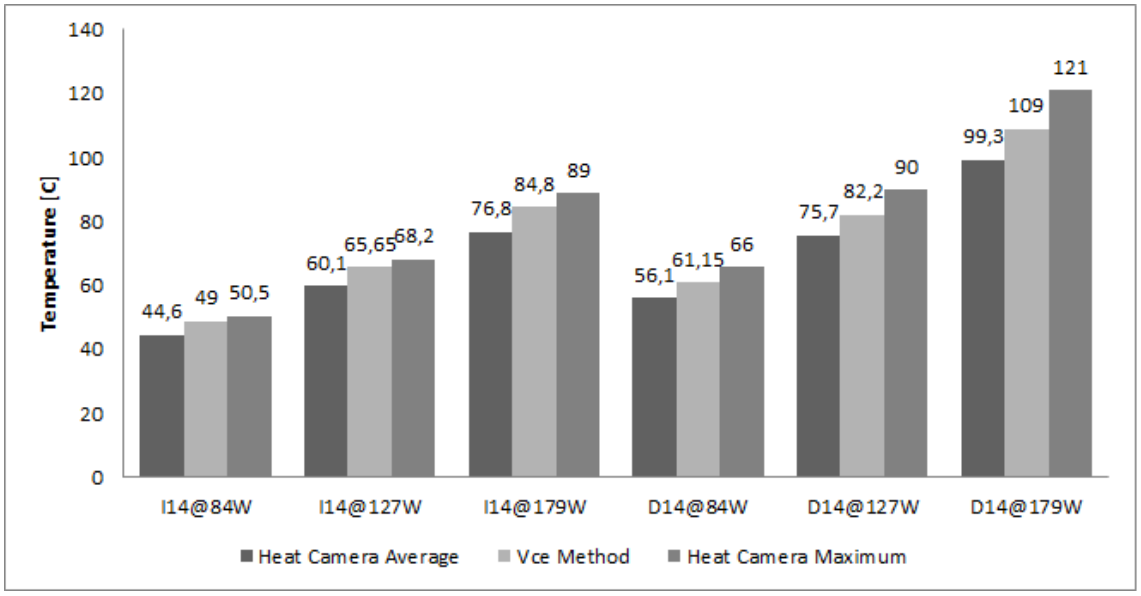


Figure 3.15: The temperatures recorded with the IR camera and the $U_{ce}(T)$ method.

3.2.3 Discussion

$U_{ce} - T$ determination

The $U_{ce} - T$ method is a convenient, fast and relatively accurate way to determine the junction temperature of the chip with error around $2 - 3$ ℃ . There are though some facts that are worth mentioning about that single value of temperature this method provides.

Over the whole area of the chip, there is temperature gradient that can span up to 40 K between the corners of the chip and its central region. This temperature gradient comes from the internal structure of the chip and the way that the load current density is distributed through its entire volume. Similar distribution that depends on temperature gradient can also be expected for the sensing current. During the calibration process the chip is uniformly heated in a climate chamber, so there is no temperature gradient across its surface and the voltage measured under the (uniformly distributed) sensing current corresponds to a common temperature value for the whole chip. Under load conditions where the chip temperature differs across its surface, the sensing current has higher density at the areas with increased temperature. The voltage measured then corresponds to a "current weighted" value, which is close to an area weighted value [19]. In other words the obtained value

is approximately the average temperature over the entire chip area. Deviation up to $+10\ K$ can be expected for the center of the chip with respect to the average temperature and this is something crucial when it comes to reliability assessment of the module [19].

Transient chip temperature measurements

As seen from Figures 3.11 and 3.12, the temperature of the chip that is heated has the faster and higher increase. The neighbor chips are also affected but each in a different way, depending on their location and size. In the case of $I13$ heating, $D13$ is the chip that starts to heat right after $I13$ and reaches the second highest steady state temperature. This is a result of its proximity to the heat source as well as its location on the same copper layer with $I13$, compared to the other neighboring chips that heat up slower and at lower temperatures. $D23$, $D24$ and $I23$ and $I24$ seem grouped together following close heating paths. It is interesting the fact that $D24$ heats faster than $I23$ despite being placed at different substrate. This is a result of its smaller dimensions compared to $I23$, which leads to higher area average temperature for the diode chip even if heat flux towards it is less than towards $I23$. Finally, $D12$ and $I12$ have the slowest and lowest temperature change, since they are located at a different substrate, two chips away from the heated one. In the same logic, respective comments can be made for the case of $D23$ heating.

The causes of deviations observed for the initial temperature of the raw data mentioned in Section 3.2.2 before any heat is applied are discussed briefly in the following. Noise presence in the measured voltage may affect the initial temperature level, considering that the sampling is done at 5 kHz and the frequency content of the measured quantity is in the range of 1 kHz. The peak-to-peak content of this disturbance is in the worst case after filtering 0.5 ℃ which equals to 2.95 % of the initial temperature level of 17 ℃ and can be neglected. Variation in the range of 1 ℃ with period of several minutes has been observed in the pipe water used for cooling, that has possibly affected the steady state temperature of the whole setup before heat is applied. In addition, to what concerns $U_{ce} - T$ method measurements, since temperature is derived from voltage and the voltage range is in the order of hundreds of millivolts, it is sensitive to contact resistance as well as resistance variations of the cable. It has been observed that compared to the $U_{ce} - T$ calibration, even a minor change to the signal cables or the contacts of the setup introduces deviations in the temperature measurement in the range of $1 - 2$ ℃ . Moreover, the same signal cables under different temperature, therefore different resistivity, cause voltage drops that affect the measured U_{ce}, so the junction temperature measured. Having mentioned all the above, it is concluded that application of $U_{ce} - T$ method to measure absolute values of temperatures may introduce small errors in the range of $2 - 3$ ℃ . Nonetheless, in order to extract thermal impedances, differences in temperature are considered, thus the errors discussed earlier apart from noise presence, are inherently eliminated in (1.2) and giving accurate results.

4

Finite Element Calculations and Foster Networks

4.1 Finite Element Model

4.1.1 Initial FEM model

The Finite Element Analysis is utilized to simulate the thermal behavior of the power module, compare the experimental results with the simulated ones and improve the simulation to match reality as close as possible. The layout of the module, presented in Appendix A, is used to build a 3D model, while the thermal conditions such as convection coefficients and heat fluxes are obtained from the experimental measurements. Material properties for the module layers are provided by the manufacturer and are temperature dependent.

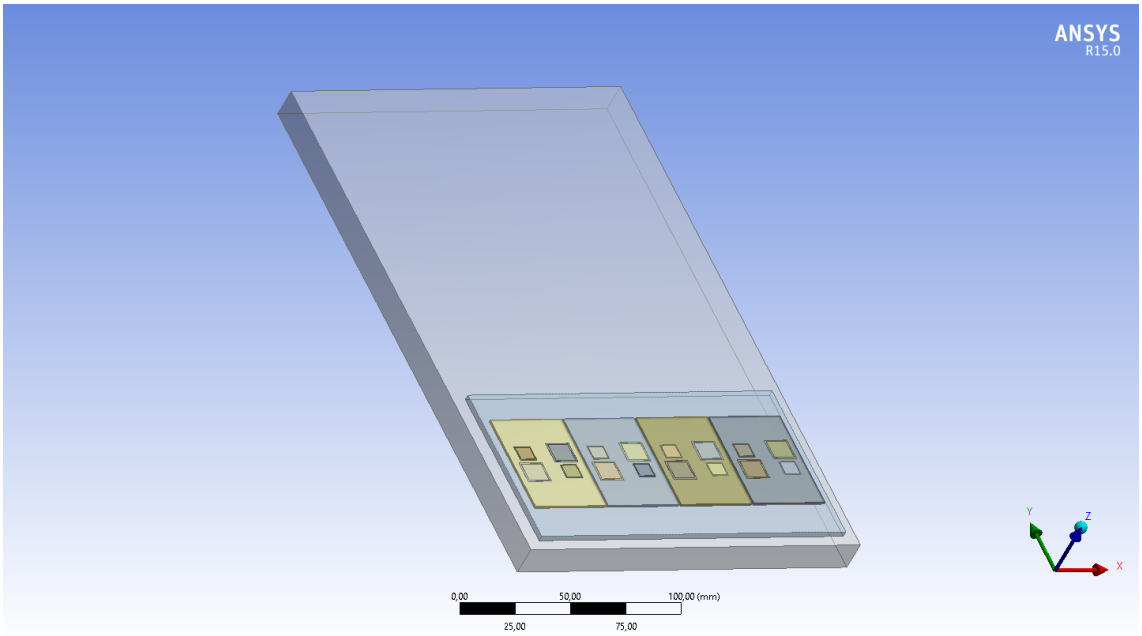


Figure 4.1: The 3D geometrical model used in Finite Element Analysis.

The software package used is ANSYS ™ Mechanical *R*15.0 and the 3D geometry used is illustrated in Figure 4.1. From bottom to top, there is the heat-sink, represented as the largest structure in the background. The heat sink is initially

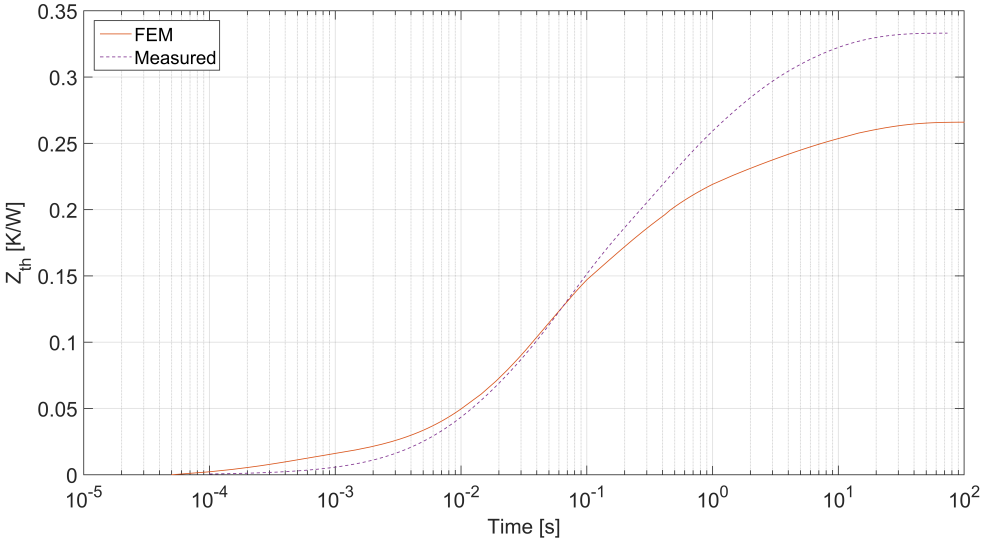
considered as pure aluminum, since no information about its material is available. The module baseplate is mounted on top of the heat sink and on top of the baseplate there is a layer of solder. This solder layer holds a Copper-Ceramic-Copper (Direct Bonded Copper - DBC) substrate layer on top of which the Silicon chip is mounted having again solder in between. The geometry inserted in ANSYS is a simplified representation of the real module, consisting of stacked parallelepipeds based on the corresponding dimensions of the module, in order to reduce the complexity of the simulation.

The mesh used to discretize that geometry is refined in order to divide the thin layers in more than one elements along their depth. Transient Thermal analysis is utilized so that the entire heating up phenomenon can be examined. In the real module, the baseplate is mounted on the heat-sink having between them a thermal conducting aluminum film. This film has phase changing surfaces, which when heat beyond 52 ℃ become liquid, resulting in good contact between the baseplate, the aluminum film and the heat-sink. Due to its small thickness relative to its neighboring masses, that phase changing aluminum film is not included as a layer in the simulation, but inserted as boundary condition of the upper heat-sink surface. This surface in the simulation is characterized by a constant thermal conductance value that corresponds to the thermal conductance of the film.

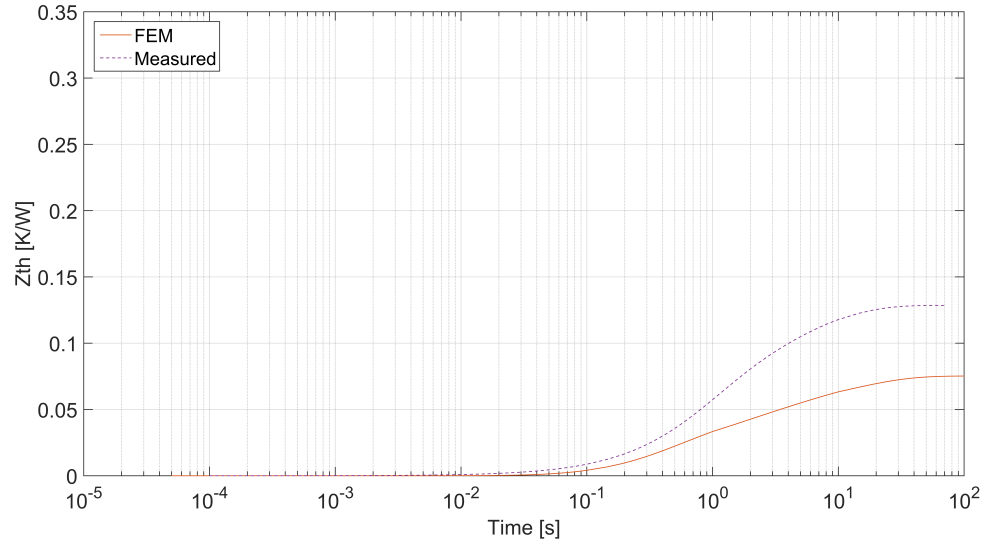
The model simulates heat injection to any of the chips by considering the upper chip area as a surface heat source and obtain the temperature increase in this chip, as well as its neighboring chips. From the experimental tests described in Section 3.2.2, the heat injected in every chip is set to 180 W and that value is used in the simulations. The initial temperature of the analysis is set to 17 ℃ which is the steady state temperature when no heat is injected and pipe water is circulating in the heat-sink. Finally, as convective cooling, the lower surface of the heat-sink is chosen to have a constant convection coefficient of 3538 $\frac{W}{m^2 C}$ and 17 ℃ ambient temperature, which corresponds to 6.2 $\frac{lit}{min}$ of pipe water flow in the heat-sink and an convection effective area of 0.0504 m^2 (the lower heat-sink surface area). The time increments are chosen to be dense at the beginning of the phenomenon to track fast changing temperatures, but become more sparse as time passes. In Section A.3 the time steps chosen are presented in tabular form.

The average temperature on the surface of each chip is used as a result, in order to match closer with the current weighted temperature obtained from the $U_{ce}(T)$ method. For IGBT chips their lower surface was chosen to extract their average temperature, while for diodes the upper surface is selected. The reason for this differentiation, is the location of the actual *pn*-juntion of each kind of chip, that $U_{ce}(T)$ method utilizes to give temperatures [20].

The results from the initial FEM model are presented in Figures 4.2 and 4.3 for heating of $I13$ and $D23$ respectively. As results, the thermal impedances are considered instead of the temperatures for the rest of the report, since this is the quantity of interest, calculated using (1.2). As seen, there is significant deviation between measured and simulated curves both for self heating and for thermal coupling, so finer adjustment of the simulation model is necessary.

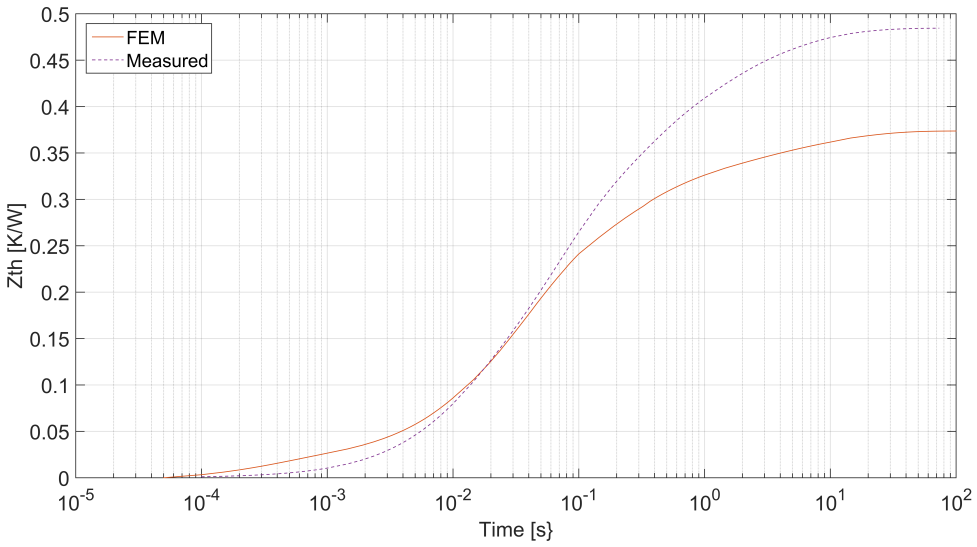


(a) Self heating of I13.

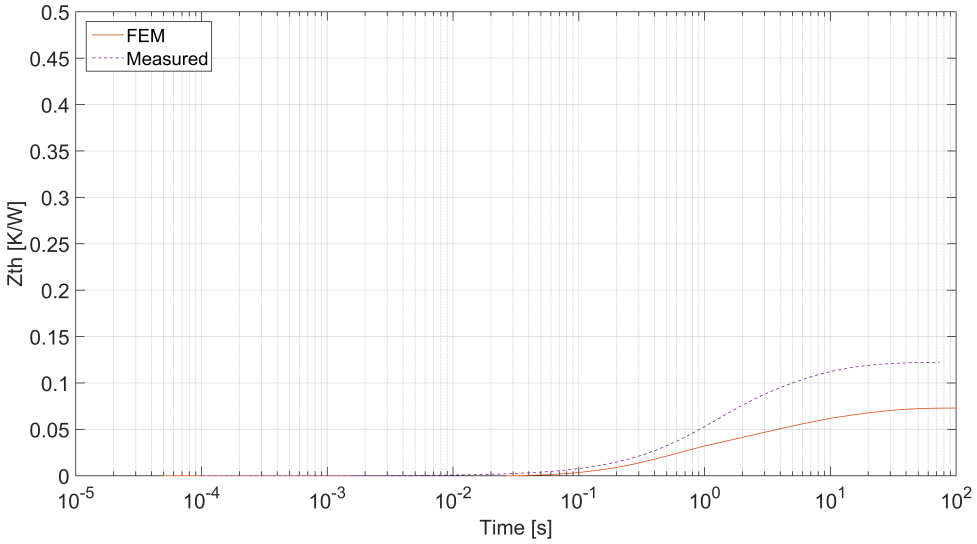


(b) Coupling between I13 and D13.

Figure 4.2: Comparison between measurements and FEM initial simulation for I13 heating.



(a) Self heating of D23.



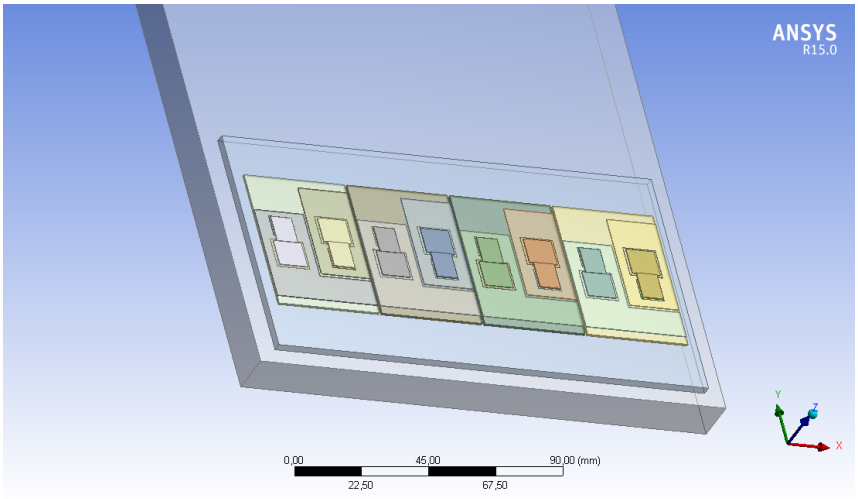
(b) Coupling between D23 and I23.

Figure 4.3: Comparison between measurements and FEM initial simulation for D23 heating.

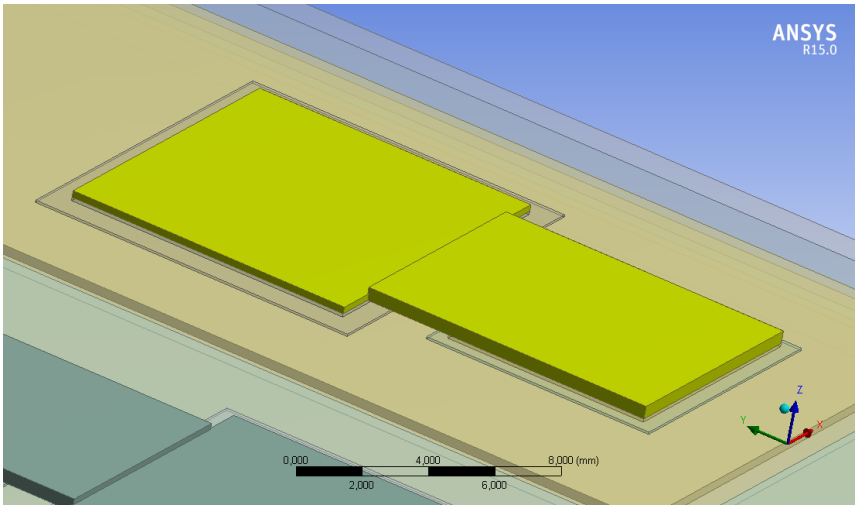
4.1.2 Improvements on FEM model

Since material properties of the module are known from the manufacturer, investigation for improvement is focused on the geometry of the module, the thermal resistance of the contacting layers, as well as the material of the heat-sink. The model adjustment is based on changing only one parameter at a time and see what influence this change has on the transient thermal impedance curve extracted by the model. Observing that small time constants are connected to the thiner layers such as silicon and chip solder, while higher time constants are connected to more bulky layers such as baseplate and heat-sink, it is possible to recognize differences

and modify the model accordingly.



(a) The entire model where the improved upper copper layer is visible.



(b) Detail of the chip region with aluminum mass over the chip surface to emulate metalization and bond-wires existence.

Figure 4.4: The modified $3D$ geometry

A closer look at the time region around 10^{-4} s to 10^{-3} s in Figure 4.2a reveals that the measured curve starts to increase slower than the simulated one. That can be connected to the existence of a thermal capacitance close to the silicon layer (chip) that is not modeled. That missing capacitance is found to be the aluminum metalization of the chip and its bond-wires that were initially neglected from the simulation. Adding an aluminum mass approximately equal to the missing one, on top of the silicon body, improves the curve matching for the lower time constants. Moreover, connecting the aluminum masses over each IGBT and its anti-parallel diode chip, improves the simulated thermal coupling as well. Another modification is also implemented at the upper copper layer of the DBC, where the parallelepiped is replaced by a shape closer to the real module copper layer, in order to increase

accuracy at the middle range time constants that DBC influences. The modified $3D$ geometry is illustrated in Figure 4.4, showing the improved upper copper layer and the silicon chip region with its aluminum top layer.

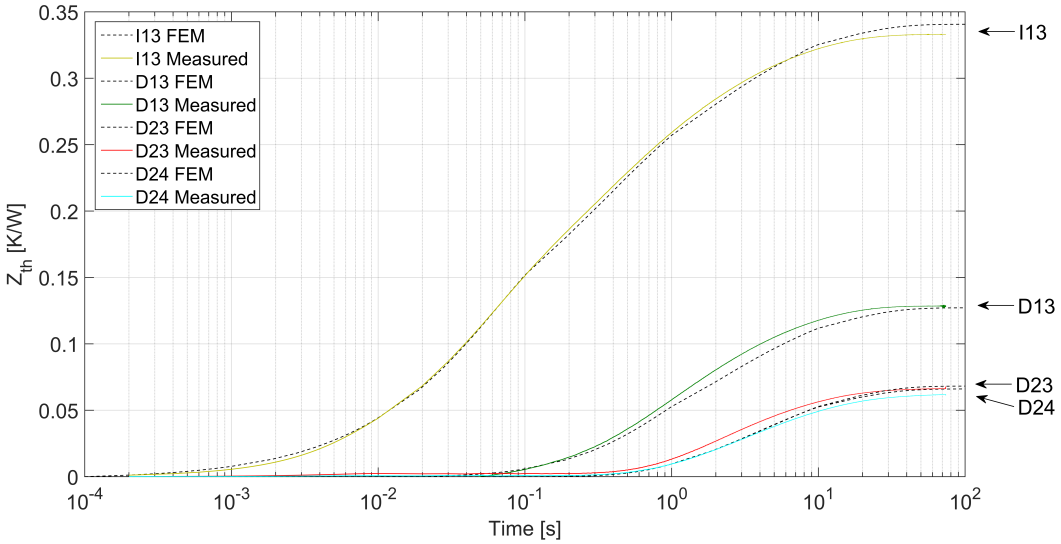


Figure 4.5: Comparison of measured and FEM calculated thermal impedances for the case of I13 heating.

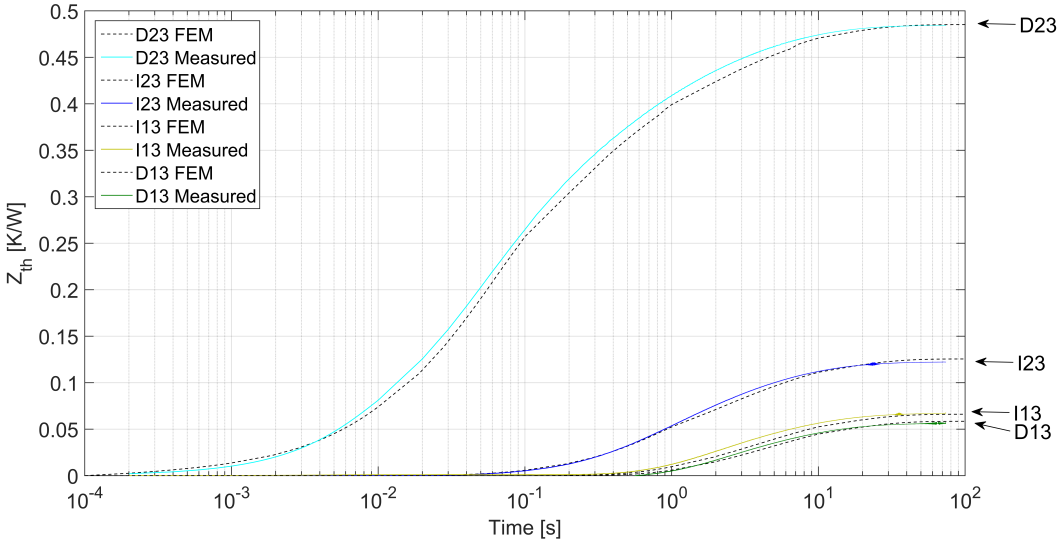


Figure 4.6: Comparison of measured and FEM calculated thermal impedances for the case of D23 heating.

For the larger time constants, the investigation is concentrated at the properties of the aluminum heat-sink as well as its connection to the base plate through the aluminum film, modeled as a contact resistance between heat-sink and baseplate. By changing the heat-sink material from pure Aluminum to "Aluminum 2024, Temper-$T4$" alloy which has lower thermal conductivity and specific heat capacitance, the

simulated curves both of self heating and coupling, match closer the measured ones. One final adjustment for better agreement is the conductance representing the aluminum film, which is set to 9000 $\frac{W}{m^2K}$ and governs the steady state value of the thermal impedances. as seen in Figures 4.5 and 4.6.

As seen from the graphs, the FEM model results are improved compared to the initial model. There are still deviations from absolute accuracy, but the maximum error between the measured and FEM calculated impedance is around 0.01527 $\frac{K}{W}$ and if translated to temperature under 180 W of input power, it remains around 2.7 ℃.

4.1.3 Discussion on Finite Element Model

The FEM approach is used in order to obtain a simulation model that is able to represent the thermal behavior of the real module as close as possible and allow for calculation of every thermal impedance of the module, without the need of experimental measurement. An idealized model would consist of the electro-thermal behavior of the module, combined with Computational Fluid Dynamics analysis for the heat-sink convective cooling and all these under the finest possible geometry and mesh. Such a model would require extremely high computational resources, as well as accurate knowledge of the geometries and material properties.

In this thesis a more simplified model is adopted, by utilizing only the thermal part of the ideal model. The Joule heating losses are modeled as surface heating losses, while in reality losses occur in a thin layer in the IGBT volume [20]. Moreover the chip temperature is measured as an area average rather than as current weighted according to $U_{ce}(T)$ method, but the difference is in the order of 1 ℃ and can be tolerated [19].

Regarding the geometry of the FEM model, an exact representation including bond-wires shapes or copper plate current paths would be difficult to mesh and simulate and would result in a computational burdensome model that require resources and long simulation times. Moreover its accuracy contribution would not counteract its complexity. On the other hand, as presented in Section 4, ignoring components such as metalization and bond-wires masses, leads to ill-behavior of the model for the corresponding time constants. Finally, wrong material properties can also strongly influence the simulation results, since as observed from the tests described in Section 4, the thermal coupling between chips is mainly happening through the larger mass layers (baseplate and heat-sink [20]), thus influenced by their material.

Eventually, a simple model with acceptable error is built, making the FEM approach reliable and convenient to describe the self and coupled heating between chips, through their thermal impedances. These small deviations between simulation model and measurements are compensated by its lack of complexity.

4.2 Foster Networks

4.2.1 Derivation of the Foster equivalent

The aim of using a Foster equivalent model, is to describe mathematically the thermal impedance by deriving a function which fits $Z_{th}(t)$ as close as possible. That function can be a sum of exponentials given by (1.3), so it is enough to find the proper number of RC pairs and the values of R_i and C_i that provide the optimum matching between the exponential sum and $Z_{th}(t)$.

In order to find the optimum RC values, non-linear least square function is used to fit the two cases. The function used in this case is $lsqnonlin()$ from Matlab. The number of desired RC pairs, as well as a starting point of R_i and C_i is given as an initial guess to $lsqnonlin()$ along with a set of options (maximum iterations number, tolerance limits, etc) and the result of the function is a set of optimum RC pairs for the $Z_{th}(t)$ under investigation.

For the power module case, each thermal impedance is calculated by the FEM model and its Foster equivalent is extracted by the least square fitting function. For the self thermal impedance, 6 RC pairs are used, while for coupling thermal impedances 3 pairs are enough.

As an example, $Z_{th}(t)$ of $I13$ self heating and $I13-D13$ thermal coupling impedances are fitted. In Figures 4.7 and 4.8, the simulated and fitted curves are presented. Tables 4.1 and 4.2 contain the corresponding RC pairs for each case.

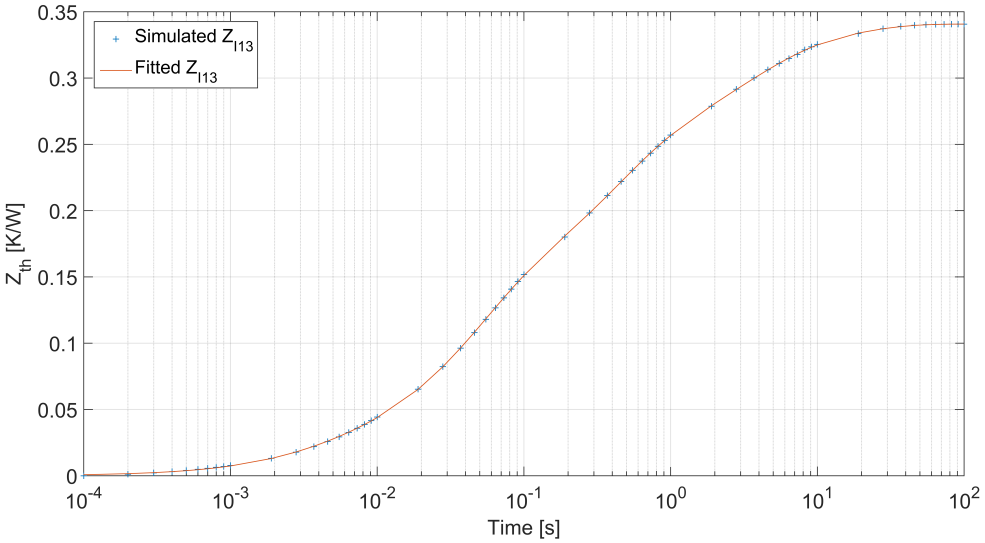


Figure 4.7: The simulated and fitted curve of $Z_{th,I13}$.

Table 4.1: Foster equivalent RC values for $I13$ self thermal impedance

$Z_{th,I13}$	1	2	3	4	5	6
R_i	0.0172	0.1161	0.0294	0.0612	0.0236	0.0932
C_i	0.1996	0.3644	34.3659	58.5060	623.0688	3.5921

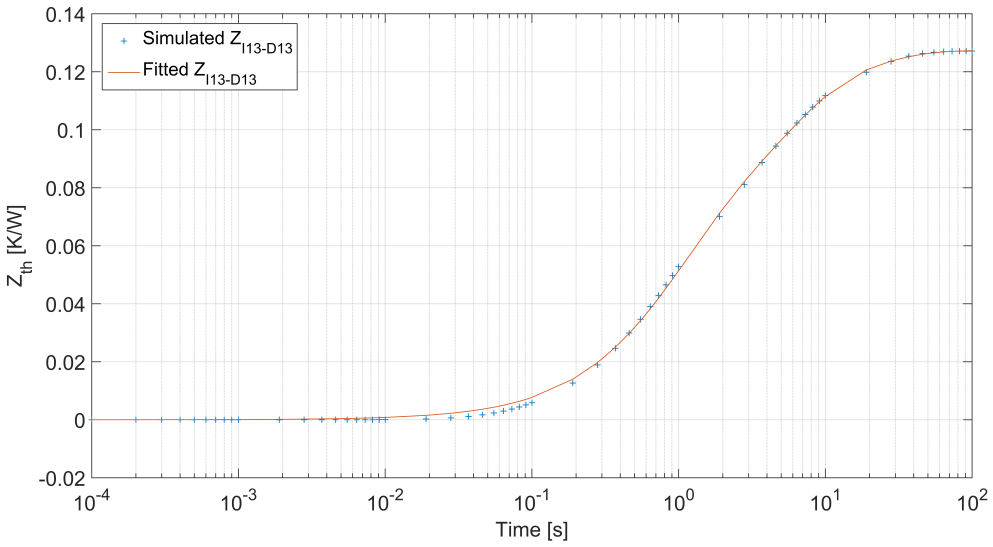


Figure 4.8: The simulated and fitted curve of $Z_{th,I13}$.

Table 4.2: Foster equivalent RC values for $I13 - D13$ coupling thermal impedance

$Z_{th,I13-D13}$	1	2	3
R_i	0.0586	0.0522	0.0165
C_i	14.4625	90.9705	1059.91

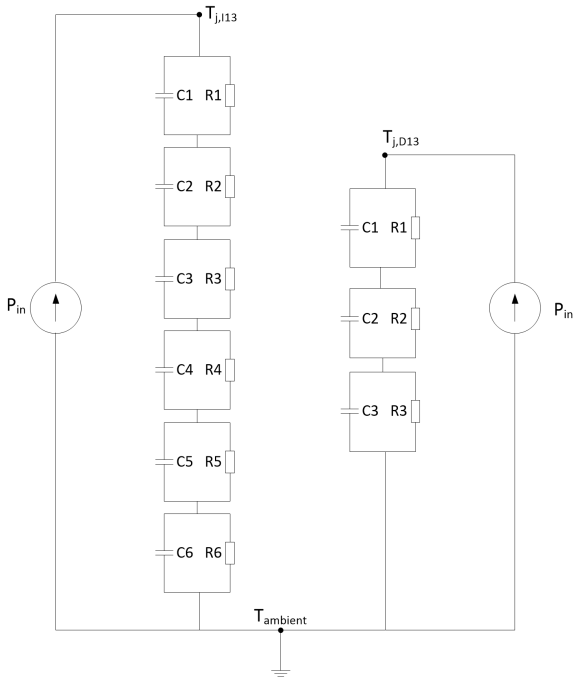


Figure 4.9: The equivalent Foster network for $I13$ and $D13$ chips.

On the same logic, every thermal impedance can be fitted to a sum of exponentials. A schematic representation of a Foster equivalent is illustrated in Figure 4.9. In that case, both self and coupling impedances are represented with their corresponding RC pairs and the junction temperature for each chip is calculated with respect to the ambient temperature, which in that case is the cooling water temperature.

4.2.2 Discussion on Foster networks

The Foster electrical equivalent is a convenient and compact model to describe mathematically the thermal behavior of a power module. It can be solved by circuit simulators and it is easily handled compared to a FEM simulation. On the other hand, it constitutes only a behavioral representation, meaning that it has no physical connection to the real module.

Fitting a thermal impedance to a Foster equivalent is straightforward for self impedances, but can be more demanding when it comes to thermal coupling. This is a result of the time interval between heat application to a chip, and the instance when heat reaches the chip under investigation and starts to increase its temperature. In Figure 4.10, the thermal impedance of $D24$ is illustrated when heat is applied at $I13$. For the first 1.1 ms, there is no effect on $D24$ since heatwave has not reached it until then. Fitting such a thermal impedance with only positive RC values, results in mismatches between the two curves but accepting negative RC values, improves the fitting. The drawback of accepting negative coefficients though, is that a potential transformation to Cauer equivalent to connect the model with the physical structure is not directly possible.

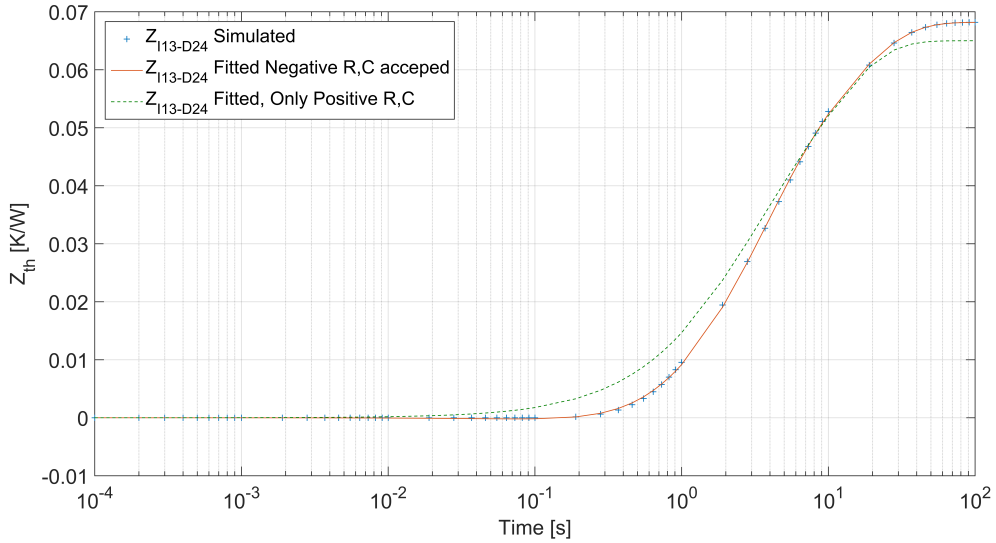


Figure 4.10: Fitting $Z_{th,I13-D24}$ accepting and not accepting negative RC values.

In case negative RC values are acceptable, the Foster model can still be valid in the Laplace frequency domain for further handling in a state space representation. The Laplace transformation of exponential sums takes the form

$$Z_{th}(s) = \sum_{i=1}^{n} \frac{R_i}{sR_iC_i + 1} \tag{4.1}$$

meaning that in case of both negative RC pairs, $R * C > 0$ and the poles remain in negative region of the s-plane. Thus even in case of negative coefficients, the system can be considered stable.

5

Conclusions and Future Work

5.1 Conclusions

Throughout this thesis, a complete method to obtain power losses and thermal impedances of power modules is presented. The results consist of look-up tables of power losses for various operating points, as well as mathematical expressions to describe thermal impedance curves. Power losses are extracted from the manufacturer data-sheet and compared to experimentally measured losses. The look-up tables are eventually derived from power losses provided by the manufacturer and corrected according to measurements based on an actual application environment. A Finite Element model of the power module is built to simulate its thermal behavior, including both self and mutual thermal impedances. The model is refined to generate thermal impedance curves that agree with measured curves of the simulated module. Foster Networks are utilized to resemble the thermal behavior and quantitative representation of thermal impedances is achieved after curve fitting.

This method is not restricted to the specific module on which it is applied. It can be used to obtain the thermal behavior of any IGBT power module, regardless of its number of chip components, as long as the guidelines presented in this thesis are followed and adjusted to the object under test. The procedures used throughout this thesis are not something new as separate tasks, but it is their combination that provides a versatile way towards accurate thermal modeling of power modules.

Obtaining power losses based solely on data provided by the manufacturer may lead to erroneous results that are not accurate for the application under investigation. This thesis then suggests measurement of power losses on the final setup, so derived data shall correspond to the real application conditions. However, lack of measurements for higher temperatures still introduces uncertainties in the accuracy of results, but the results obtained are closer to reality than the ones provided by the manufacturer.

Regarding Finite Element model, this method also provides a quick and cost-effective way to evaluate the behavior of the whole setup, since simulation for the total heat flow path is built and experimentally verified. Other methods are focused on modeling individual components of a power module - cooling system setup or build time transient simulation models without verifying, something that could lead to inaccuracy in the real application, especially when the interest is focused on time transient phenomena.

To sum up, this method is a compensation between simplicity and accuracy. The results are reliable, but margins for improvement exist. On the other hand, its

versatility and holistic aspect (regarding the overall application setup) compared to other methods, make it a valuable tool for designers that seek the proper power module for each application.

5.2 Future work

As an extension of this project, future work can include measurement of power losses for higher junction temperatures to achieve total independence from manufacturer data. Moreover, further improvements of the Finite Element model to eliminate minor deviations from reality are proposed. Self thermal impedances can be analyzed using Network Identification by Deconvolution techniques to connect physical layers of the module with their contribution in self thermal impedance and eventually derive a more accurate FEM model.

Bibliography

[1] M. Ehsani, Y. Gao, S. E. Gay, and A. Emadi, *Modern Electric,Hybrid Electric, and Fuel Cell Vehicles - Fundamentals, Theory, and Design.* CRC PRESS, 2005.

[2] E. R. C. da Silva and M. E. Elbuluk, "Fundamentals of power electronics," in *Power Electronics for Renewable and Distributed Energy Systems*, S. Chakraborty, Ed. Springer, 2013, ch. 2.

[3] *Technical datasheet for FF600R12IE4*, Infineon, August 2009.

[4] L. Wei, R. Kerkman, R. Lukaszewski, B. Brown, N. Gollhardt, and B. Weiss, *Junction Temperature Prediction of a Multiple-chip IGBT Module under DC Condition*, Rockwell Automation - Allen Bradley, 6400 West Enterprise Drive, Mequon, WI, 53092 USA, 2006, IEEE.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics - Converters, Applications and Design*, 3rd ed. John Wiley and Sons Inc, 2003.

[6] A. Sattar, *Insulated Gate Bipolar Transistor (IGBT) Basics*, IXYS Corporation.

[7] J. Dodge, *Application Note APT0408 - IGBT Technical Overview*, APT.

[8] B. W. Williams, *Power Electronics: Devices, Drivers, Applications, and Passive Components.*

[9] P. Haaf and J. Harper, Eds., *Understanding Diode Reverse Recovery and its Effect on Switching Losses.* Fairchild Semiconductor Europe.

[10] A. Poppe, "Thermal measurements and modeling - the transient and multichip issue," in *Proc of 11th Therminic.* MicRed, September 2005.

[11] M. März and P. Nance, *Thermal Modeling of Power-electronic Systems*, Infineon AG.

[12] Y. C. Gerstenmaier, W. Kiffe, and G. Wathutka, "Combination of thermal subsystems modeled by rapid circuit transformation," in *Proc. of Therminic 2007.* EDA Puplishing.

[13] T. Poller, S. D'Arco, M. Hernes, and J. Lutz, "Influence of thermal cross-couplings on power cycling lifetime of igbt power modules." Nuremberg Germany: CIPS - VDE VERLAG GMBH, March 2012.

[14] D. D. Graovac and M. Purschel, *IGBT Power Losses Calculation Using the Data-Sheet Parameters*, 1st ed., Infineon Technologies AG, Germany, January 2009.

[15] U. Drofenik and J. W. Kolar, *A General Scheme for Calculating Switching- and Conduction- Losses of Power Semiconductors in Numerical Circuit Simulations of Power Electronic Systems*, Power Electronic Systems Laboratory - ETH, Zurich.

[16] I. Hemp, L. Göhler, and S. Bönisch, "An automated test set-up for the dynamic characterization of igbt modules under different thermal and electrical conditions," Hochscule Lausitz, Germany, Tech. Rep., March 2012.

[17] Y. A. Çengel, *Heat Transfer: A Practical Approach*, 2nd ed. Mcgraw-Hill, 2002.

[18] The engineering toolbox. [Online]. Available: http://www.engineeringtoolbox.com/thermal-conductivity-d_429.html

[19] R. Schmidt and U. Scheuermann, *Using the chip as a temperature sensor - The influence of steep lateral temperature gradients on the $U_{ce}(T)$ measurement*, SEMIKRON Elektronik GmbH, Sigmundstraße 200 Nuremberg Germany, published in IEEE Xplore.

[20] T. Hunger and O. Schilling, *Numerical investigation on thermal crosstalk of silicon dies in high voltage IGBT modules*, Infineon.

A

Appendix 1

A.1 Power losses measurement equipment and look-up tables example

A list of the equipment used for the double pulse test:

- Rogowski Coil - $CWT\ 3B$
- Collector emitter high voltage probe - $LeCroy\ ADP305$ (Differential) 100 MHz
- Gate voltage probe - $Hioki\ Differential\ Probe$ 9322
- Oscilloscope - $LeCroy\ Wavesurfer$ 454 500 MHz
- Power Supply - $EA\ PSI$ $81000 - 30$ $(1000V\ -\ 30A)$
- Load inductance - Custom Solenoid with wooden core $2x2.5\ mm^2$ 44 turns of double wire giving 65 μH
- $VPEC$ with control boards

Table A.1: IGBT Conduction losses (W)

I_C (A) \ T_j (℃)	25	50	75	100	125
10	6.968	6.314	5.677	5.061	4.466
50	44.715	43.047	40.889	38.281	35.274
100	102.003	100.941	98.889	95.876	91.949
200	239.039	243.911	247.153	248.730	248.628
300	404.808	419.601	433.206	445.554	456.585
400	595.586	626.302	656.454	685.950	714.700
500	811.711	862.982	914.964	967.581	1020.761
600	1052.087	1131.265	1211.880	1293.786	1376.840

Table A.2: Diode Conduction losses (W)

I_d (A) \ T_j (℃)	25	50	75	100	125
10	7.876	6.576	5.517	4.665	3.991
50	49.696	44.712	40.011	35.587	31.440
100	112.932	104.414	95.986	87.680	79.527
200	262.478	249.311	235.388	220.805	205.665
300	436.906	421.774	404.556	385.401	364.479
400	632.185	617.558	598.996	576.690	550.870
500	846.564	833.825	815.393	791.463	762.291
600	1078.624	1070.649	1054.296	1029.761	997.336

Table A.3: IGBT Switching losses (mJ) for $R_g = 5.1\ \Omega$

I_C (A) \ T_j (℃)	25	50	75	100	125
60	17.236	26.273	37.410	50.746	66.382
100	23.799	35.820	50.594	68.267	88.985
200	41.542	60.799	84.306	112.331	145.149
300	61.190	87.385	119.165	156.931	201.095
400	82.743	115.599	155.246	202.227	257.099
500	106.202	145.456	192.609	248.348	313.381
600	131.567	176.969	231.301	295.396	370.118

Table A.4: Diode Switching losses (mJ) for $R_g = 5.1\ \Omega$

I_d (A) \ T_j (℃)	25	50	75	100	125
60	7.212	7.481	8.390	10.580	15.197
100	10.021	10.394	11.657	14.700	21.115
200	14.646	15.192	17.038	21.485	30.862
300	16.831	17.458	19.579	24.691	35.466
400	17.802	18.465	20.709	26.115	37.512
500	18.786	19.485	21.853	27.558	39.585
600	21.009	21.791	24.439	30.819	44.269

A.2 Climate chamber test results

Table A.5: Measured U_{ce} for the upper row of switches

Temperature \Chip	I11	D11	I12	D12	I13	D13	I14	D14
25 ℃	0.54658	0.55727	0.54602	0.55713	0.54567	0.55769	0.5462	0.55703
50 ℃	0.49057	0.50511	0.49	0.50484	0.48998	0.50536	0.48985	0.5049
75 ℃	0.43407	0.45461	0.43391	0.45427	0.43381	0.45475	0.43404	0.45427
95 ℃	0.39021	0.41406	0.39018	0.41347	0.38983	0.41405	0.38982	0.41351
120 ℃	0.33768	0.36375	0.33684	0.3632	0.33628	0.36367	0.33587	0.36252
130 ℃	0.30766	0.33767	0.30775	0.33737	0.30742	0.33804	0.30744	0.33743

Table A.6: Measured U_{ce} for the lower row of switches

Temperature \Chip	I21	D21	I22	D22	I23	D23	I24	D24
25 ℃	0.54674	0.55788	0.54734	0.55764	0.54491	0.55818	0.54634	0.55774
50 ℃	0.49008	0.50533	0.48974	0.50509	0.48851	0.50566	0.48965	0.50557
75 ℃	0.43455	0.45503	0.4345	0.45479	0.43307	0.45521	0.43444	0.45502
95 ℃	0.39022	0.41471	0.38937	0.41421	0.38825	0.41449	0.38943	0.41403
120 ℃	0.33337	0.36137	0.33281	0.36109	0.3319	0.36174	0.3328	0.36112
130 ℃	0.30935	0.34005	0.30889	0.33999	0.30806	0.33978	0.30948	0.33937

Table A.7: First Order polynomial coefficients for the $U_{ce}(T)$ equation for each chip of the module

Coefficients \IGBT	I11	I12	I13	I14	I21	I22	I23	I24
$\alpha[V/℃]$	-0.0022	-0.0022	-0.0022	-0.0022	-0.0023	-0.0023	-0.0022	-0.0023
$\beta[V]$	0.6028	0.6022	0.6021	0.6026	0.6032	0.6037	0.6013	0.6027
Coefficients \Diode	D11	D12	D13	D14	D21	D22	D23	D24
$\alpha[V/℃]$	-0.0021	-0.0021	-0.0021	-0.0021	-0.0021	-0.0021	-0.0021	-0.0021
$\beta[V]$	0.6091	0.6090	0.6095	0.6091	0.6096	0.6093	0.6100	0.6098

A.3 Module Geometry and Finite Element Analysis specifications

The cross-section of the power module on top of its heat-sink is presented in Figure A.1.

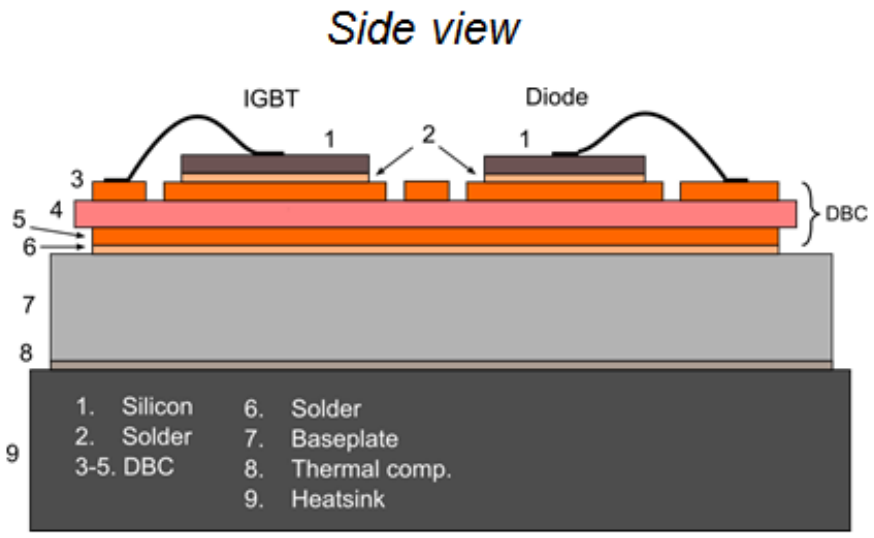


Figure A.1: The power module cross section with its progressive layers

The vertical dimension of each layer as well as each layer's material are presented in Table A.8.

Table A.8: Dimension and material of each layer.

Nr	Layer	Material	Thickness [μm]
1	Silicon die	$Silicon$	Confidential
2	Solder	$60Sn40Pb$	Confidential
3	Copper foil (DBC)	$Copper$	Confidential
4	Ceramic substrate (DBC)	Al_2O_3	Confidential
5	Copper foil (DBC)	$Copper$	Confidential
6	Solder	$60Sn40Pb$	Confidential
7	Baseplate	$Copper$	Confidential
8	Thermal Film	$Aluminum$	102
9	Heatsink	$AluminumAlloy$	15000

The time steps used in the Finite Element Analysis are presented in Table A.9. In a logarithmic time scale 6 decades are selected starting from 1 ms up to 100 s divided in 10 substeps per decade. The first time step is consequently in the range of 200 μs to effectively track the fast changing temperatures at the beginning of the heating.

Table A.9: The time steps and increments used in FEM simulation.

Step	End Time (s)	Number of substeps
1	1,00E-03	10
2	0,01	10
3	0,1	10
4	1	10
5	10	10
6	100	10