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Design and Experimental Verification of a Prototype Guitar Amplifier

Bachelor's Degree Project Report in Electrical Engineering, 15 hp

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Abstract

Keywords: guitar amplifier, analog preamplifier, Class-D amplifier, single-supply op-amp, breadboard prototype, signal conditioning, digital signal processing, ESP32

This project presents the design, construction, and experimental verification of a prototype guitar amplifier system, developed using standard analog audio design principles and validated through staged breadboard prototyping. The system consists of a Class-D power amplifier module and a custom analog preamplifier capable of accepting both guitar and auxiliary line-level audio inputs. Phase 1 verified the power amplifier and speaker stage using a TPA3116D2-based Class-D module. Phase 2 implemented a single-supply guitar preamplifier using a TLC272 operational amplifier with a resistive bias network, achieving a measured small-signal voltage gain of approximately 7.35 at 1 kHz with a 12 V supply—sufficient to bring guitar signal levels into the power amplifier's usable input range. Input clipping was first observed at approximately 0.92 V peak input amplitude. Qualitative frequency sweeps indicated audible output over much of the nominal 20 Hz to 20 kHz range, though the acoustic response was not quantitatively characterised. The project also includes preliminary Phase 3 digital signal processing results: a delay and a Schroeder reverb effect were implemented on an ESP32 microcontroller with a PCM5122 Digital-to-Analog Converter (DAC) and verified using internally generated test signals. Analog-to-Digital Converter (ADC) integration could not be completed; both PCM1808 modules from the same production batch failed to produce output, likely due to a manufacturing defect. Major design choices are motivated using circuit calculations and experimental observations. A 3D-printed enclosure was designed and manufactured. Battery integration and full DSP chain verification remain as future work.

Acknowledgements

I would like to thank my supervisor and examiner Rob Maaskant for guidance throughout this project. I am grateful to Rikard Karlsson at CASE (Chalmers Applied Signal Processing and Electronics) for granting access to the CASE laboratory and its equipment, including oscilloscopes, function generators, and power supplies, which were essential throughout the project.

I would like to thank Karl Johan Oskar Baumann for his help with the 3D-printed enclosure design. After reviewing the CAD model, he advised adding 0.4 mm tolerance to the mounting holes and introduced grooves on the bottom section to reduce the risk of warping during printing, since the part is printed from bottom to top. These modifications are expected to improve printability and reduce the risk of warping.

AI-based language tools were used during this project to understand concepts, obtain explanations of circuit behaviour, and assist in structuring parts of the written report. The author reviewed and is responsible for all content. All technical decisions, measurements, and conclusions are the author's own.

Contents

Chapter 1

Introduction

1.1 Background

Portable guitar amplifiers require careful coordination of analog signal conditioning, power amplification, and acoustic design. Guitar pickups produce weak signals with high source impedance, and amplifying these to levels suitable for driving a loudspeaker involves several engineering challenges: input stage design for high-impedance sources, single-supply biasing for analog circuits, efficient power amplification, and noise management in breadboard prototypes.

This project was motivated by the opportunity to replace a non-functional personal amplifier with a custom-built prototype while investigating the design of compact audio amplification systems. The system was designed and built incrementally, with each stage verified before integration.

1.2 Problem Statement

The project investigates the following design questions:

1. What analog front-end design is suitable for conditioning a passive guitar signal for a Class-D amplifier module?

2. How does single-supply op-amp biasing affect signal headroom and gain in a preamplifier stage?

3. How does breadboard implementation affect noise and signal integrity in an analog audio circuit?

The system was built from discrete analog front-end components combined with a commercial Class-D power amplifier module.

1.3 Purpose and Objectives

The core objectives were to design, build, and verify a prototype guitar amplifier system with:

- A guitar input stage with input impedance of approximately 1 MΩ, sufficient voltage gain to bring guitar signal levels to power amplifier input range, and a maximum clean input amplitude above 0.5 V peak
- A TPA3116D2-based Class-D amplifier module, nominally rated up to 2×50 W under specified datasheet conditions, used at 12 V laboratory supply
- A 4 Ω, 8 W full-range speaker driver tested without a completed enclosure
- Audio output with no visible clipping at low-to-moderate input amplitudes and no significant hum after grounding fixes

Secondary objectives included developing a systematic approach to staged breadboard prototyping and creating a foundation for future digital effects implementation.

1.4 Scope and Limitations

The project was structured into six phases according to a planning report submitted in February 2026: Phase 0 (research), Phase 1 (power amplifier), Phase 2 (preamplifier), Phase 3 (digital effects), Phase 4 (battery and enclosure), and Phase 5 (documentation). This report covers Phase 1 and Phase 2 in full, with Phase 3 and Phase 4 results. Phase 5 documentation is in progress.

The work is limited to breadboard prototyping. Breadboard implementation introduces parasitic capacitance, intermittent contacts, and constrained ground layout that would not be present in a soldered Printed Circuit Board (PCB). Testing was

performed under laboratory conditions using bench equipment. The system relies on a laboratory power supply and should be considered a prototype toward a portable amplifier, not a finished product. The enclosure was designed in Onshape and manufactured via Fused Deposition Modeling (FDM) 3D printing using Polylactic Acid (PLA). Battery integration and full Digital Signal Processing (DSP) chain verification remain as future work.

Chapter 2

Theoretical Framework

2.1 Audio Signals and Signal Conditioning

The nominal human audible range is commonly approximated as 20 Hz to 20 kHz. Guitar pickups produce weak signals with high source impedance, which requires careful input stage design before any power amplification can take place [1].

In single-supply systems, where the negative rail sits at ground potential, AC audio signals must be biased around a mid-supply reference voltage [2]. This allows the signal to swing both above and below the bias point while staying within the supply rails.

2.2 Operational Amplifiers

Operational amplifiers are widely used in audio signal conditioning. A non-inverting configuration was chosen here because it provides high input impedance and straightforward gain control. The closed-loop voltage gain is:

$$G = 1 + \frac{R_f}{R_g} \tag{2.1}$$

where R_f is the feedback resistor and R_g is the gain-setting resistor connected to the AC bias reference node (VREF). The effective guitar input impedance is designed to be approximately 1 MΩ, dominated by the external bias resistor [1].

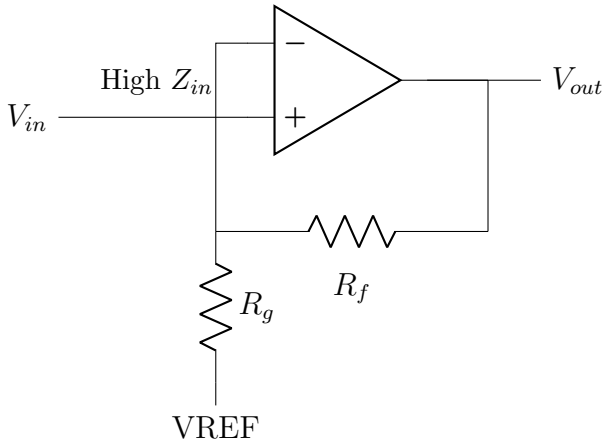

Figure 2.1: Non-inverting op-amp configuration. The signal V_{in} is applied to the non-inverting input (+), which presents high input impedance. Gain is set by R_f and R_g: $G = 1 + R_f/R_g$. The inverting input (−) is connected to the VREF bias reference through R_g.

Single-supply operation requires a bias network to provide a DC reference point [2]. A resistive divider creates a mid-supply voltage (VREF) used as a reference for both the signal bias network and the inverting input of the op-amp, as shown in Figure 2.1.

The TLC272 used in this prototype has a maximum input offset voltage of up to 10 mV and a gain-bandwidth product of 4.5 MHz [3]. At a closed-loop gain of 9 and 1 kHz, the gain-bandwidth product is not a limiting factor. The offset voltage may contribute a small Direct Current (DC) error at the output.

2.3 AC Coupling and Blocking Capacitors

Alternating Current (AC) coupling capacitors block DC components while passing AC audio signals. Combined with a resistor, they form a first-order high-pass filter with a cutoff frequency f_c:

$$f_c = \frac{1}{2\pi RC} \tag{2.2}$$

where R is the resistance and C is the capacitance. Signals above f_c pass with minimal attenuation; signals below f_c are attenuated. For audio applications, f_c must be well below 20 Hz to avoid attenuating audible bass content.

2.4 Passive Summing Networks

Multiple audio sources can be combined using a passive resistive summing network. Series resistors on each input prevent direct shorting of source impedances and provide isolation between signal paths. The network introduces some attenuation, determined by the ratio of series resistors to load impedance.

2.5 Class-D Power Amplification

Class-D amplifiers use high-frequency pulse-width modulation (PWM) [4] to drive the output transistors fully on or off, which reduces power dissipation compared to linear amplifiers. The TPA3116D2 is rated for up to 50 W per channel under specific datasheet conditions (21 V supply, 4 Ω load, 10% Total Harmonic Distortion (THD)) [4]. At the 12 V laboratory supply used here, achievable output power is significantly lower. Practical losses include switching loss, dead-time distortion, and conduction loss in the output filter and speaker.

The bridge-tied load (BTL) output topology drives both output terminals actively. The speaker must connect between R+ and R-, not between either terminal and ground. Oscilloscope ground clips must not be attached to BTL output nodes, as this would short one terminal to earth ground through the probe. Figure 2.2 illustrates the BTL connection.

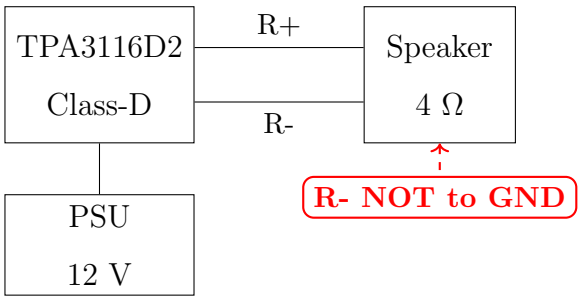

Figure 2.2: BTL output topology. The speaker connects between R+ and R-; neither terminal connects to ground. Connecting R- to ground would short the output.

2.6 Speaker Systems and Impedance

The 4 Ω, 8 W Visaton FRS 7 speaker used has a measured DC resistance (DCR) of approximately 4–4.5 Ω. Speaker impedance is not constant; it varies with frequency due

to voice coil inductance and mechanical resonances. Mechanical resonances arise from the interaction between the moving cone mass and the compliance of the suspension system, causing impedance peaks at and around the speaker's resonant frequency. The rated impedance of 4 Ω is a nominal value defined at a specific frequency range and does not represent the full impedance curve.

Chapter 3

Method and System Design

3.1 Overall Approach

The project followed an incremental development methodology. Each phase was designed, implemented on breadboard, and tested using a defined set of electrical and qualitative audio checks before moving on. This approach made it easier to catch design errors early and fix them before integration.

Objective measurements—oscilloscope amplitude, multimeter DC voltage—were used for quantitative characterisation. Listening tests served as qualitative checks only and are reported as such.

3.2 Phase 1: Power Amplifier and Speaker Verification

The objectives here were to verify Class-D amplifier operation, confirm speaker integrity, establish a qualitative frequency response baseline, verify operation across 5–12 V supply, and identify noise sources.

A function generator was connected to RIN, and a 10 kΩ resistor was connected from RIN to Analog Ground (AGND) to define the input reference. The speaker was connected between R+ and R-. Power was supplied via a Tenma 72-8345A laboratory Power Supply Unit (PSU); the test setup is shown in Figure 5.1.

3.3 Phase 2: Guitar Preamplifier Design

The objectives for Phase 2 were to implement a high-impedance guitar input stage, create a stable single-supply bias network, achieve controlled amplification, implement passive summing, and characterise gain, frequency response, and clipping.

The op-amp gain stage was originally planned to use the OPA1678IDR, a dedicated low-noise audio operational amplifier. The components did not arrive within the project timeline, so the TLC272IDR was used as a substitute instead, mounted on a Small-Outline Integrated Circuit (SOIC-8) to Dual In-line Package (DIP) adapter board for breadboard compatibility. Table 3.1 compares the two devices.

Table 3.1: Comparison of planned OPA1678 [5] and substitute TLC272 op-amps [3]

Parameter	**OPA1678**	**TLC272**
Input offset voltage (max)	±0.5 mV	10 mV
Input noise density (1 kHz)	4.5 nV/$\sqrt{\text{Hz}}$	10.8 nV/$\sqrt{\text{Hz}}$
Gain-bandwidth product	16 MHz	4.5 MHz
Supply voltage range	5–36 V	3–16 V
Package	SOIC-8	SOIC-8

Feedback network values of $R_f = 80$ kΩ and $R_g = 10$ kΩ were used. All reported measurements correspond to the TLC272 implementation. The output was AC-coupled before integration with the passive summing network. Passive summing combined the guitar signal with stereo-to-mono converted auxiliary audio through 4.7 kΩ resistors per channel.

3.4 Testing and Validation Strategy

Each phase was validated using:

- **Oscilloscope measurements (Rohde & Schwarz RTB2004):** Waveform shape, amplitude, and frequency. Probe set to 10× attenuation. AC coupling mode used for gain measurements.
- **Function generator:** Controlled sine wave inputs at defined frequency and amplitude

- **Multimeter (Tenma 72-7732A):** DC voltage measurements (VREF, supply voltages)
- **Qualitative listening tests:** Used only to confirm audible output and rough frequency range; not used as primary evidence of frequency response
- **Oscilloscope waveform inspection:** Primary method for clipping detection (visible peak flattening)

Chapter 4

Implementation and System Architecture

4.1 System Overview

The system integrates two parallel signal paths that combine at a passive summing node:

1. **Guitar path:** Guitar → Preamplifier → Passive summing node → Power amplifier → Speaker

2. **Auxiliary path:** PC stereo → Passive summing node → Power amplifier → Speaker

Both paths are independent until the summing node, with source isolation provided by series summing resistors. The complete signal flow is described in Section 4.4. The full system schematic (Figure A.1 in Appendix A) shows all component connections; the block diagram below gives an overview of the signal paths.

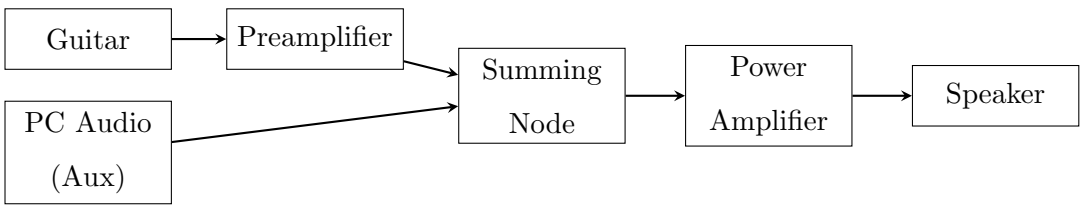

Figure 4.1: System-level block diagram showing the guitar and auxiliary signal paths combining at the passive summing node before the power amplifier.

4.2 Phase 1: Power Amplification Stage

The power amplifier stage uses a TPA3116D2-based Class-D module operating at 12 V. A 10 kΩ resistor from RIN to AGND provides input reference. The speaker connects between R+ and R-, not to ground; connecting either output terminal to ground would short the BTL output through the probe or cable. The 4 Ω speaker nominal impedance is compatible with the amplifier module's supported load range. The Phase 1 test setup is shown in Figure 5.1.

4.3 Phase 2: Analog Preamplifier Stage

4.3.1 Biasing Network (VREF Generation)

A resistive voltage divider generates the DC reference voltage VREF. R3 connects between the supply voltage V_{CC} and the VREF node; R4 connects between the VREF node and ground. With the actual resistor values R3 = 46 kΩ and R4 = 55 kΩ:

$$V_{REF} = V_{CC} \times \frac{R_4}{R_3 + R_4} = 12 \times \frac{55}{101} \approx 6.53 \text{ V} \tag{4.1}$$

The measured value of 5.9 V is approximately 9% below this. The cause of the approximately 10% deviation was not conclusively identified. Possible contributors include resistor-value mismatch, wiring and contact issues on the breadboard, leakage, or measurement setup effects. The VREF node has no active buffer; any current drawn from it by the bias resistor and op-amp inputs loads the divider and pulls the output slightly lower. Since the measured VREF still provided sufficient headroom for the tested input amplitudes, the deviation did not prevent functional verification of the prototype.

A 22 μF bypass capacitor stabilises VREF against supply noise.

4.3.2 Non-Inverting Amplifier Stage

$$G = 1 + \frac{R_f}{R_g} = 1 + \frac{80\text{k}}{10\text{k}} = 9 \text{ (theoretical)} \tag{4.2}$$

Measured gain was 7.35 (see Section 5.2.2). Output loading from the downstream summing resistors is a likely contributor to the reduced measured gain.

4.3.3 Input Impedance

The effective guitar input impedance is dominated by the 1 MΩ bias resistor, giving approximately 1 MΩ. This meets the approximately 1 MΩ requirement for guitar pickups [1].

4.3.4 Output Coupling and Summing

The op-amp output is AC-coupled through C3 (10 μF) before the passive summing node. C3 is visible in the schematic (Figure A.1, Appendix A) between the op-amp output (pin 1) and NODE_A. The schematic is placed in the appendix to keep the main text concise, but it is the primary reference for all component connections described here. PC audio L/R channels are combined through R1 and R2 (4.7 kΩ each). Guitar signal enters through R5 (10 kΩ). The VREF network uses a resistive divider with bypass capacitor only, with no active buffer present.

4.4 Signal Flow Architecture

1. Guitar jack J2 → C1 (10 μF, AC coupling) → GTR_BIASED node
2. GTR_BIASED → 1 MΩ bias resistor to VREF
3. GTR_BIASED → op-amp non-inverting input (+IN)
4. Op-amp output → R6 (80 kΩ) to inverting input (-IN), R7 (10 kΩ) from -IN to VREF
5. Op-amp output → C3 (10 μF) → NODE_A
6. NODE_A → R8 (100 kΩ) to GND; R5 (10 kΩ) to MONO_MIX
7. PC audio L/R → R1, R2 (4.7 kΩ each) → MONO_MIX
8. MONO_MIX → TPA3116 RIN → Speaker (R+, R-)

The relative volume between guitar and auxiliary inputs is not independently controllable in this prototype. If the PC output level differs substantially from the guitar preamp output, the mix balance may be suboptimal. This is noted as a limitation and future improvement.

Chapter 5

Results

5.1 Phase 1: Power Amplifier Verification

5.1.1 Frequency Response

Qualitative frequency sweeps using a function generator confirmed audible output across the tested range. The function generator output amplitude was kept constant at 200 mV peak throughout the sweep; no amplitude correction was applied for frequency-dependent loading. Table 5.1 reports observations only and these are not calibrated measurements.

Table 5.1: Phase 1 qualitative frequency response observations (function generator input, listening test only)

Frequency Range	**Qualitative Observation**
20–100 Hz	Weak output
100 Hz–8 kHz	Strongest output
8 kHz–20 kHz	Audible but reduced

The strongest response was in the mid-frequency range (100 Hz to 8 kHz). Low-frequency output was weak, consistent with the absence of an acoustic enclosure.

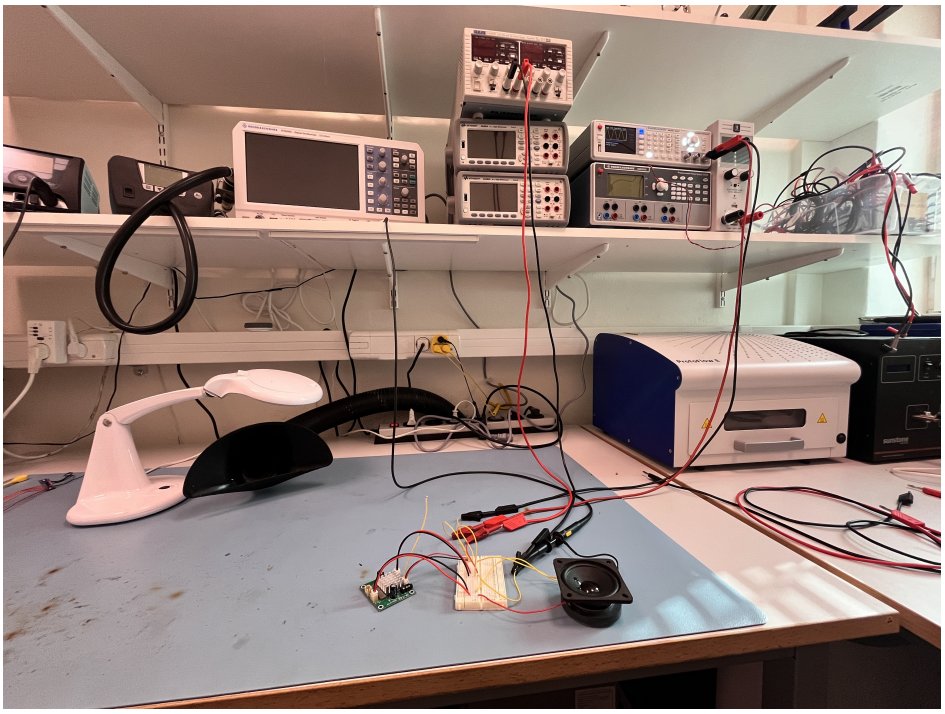

Figure 5.1: Phase 1 breadboard test setup showing TPA3116D2 amplifier module, speaker, PSU, and function generator connections.

5.1.2 Supply Voltage Behaviour

Table 5.2: Phase 1 supply voltage versus qualitative audio output (sine input, 1 kHz, 200 mV peak)

Set Voltage (V)	Measured Voltage (V)	Output Observation
5	5.0	Audible
9	9.0	Louder than at 5 V
12	12.0	Loudest tested

Minimum audible operating voltage was approximately 4.4 V at 1 kHz, 200 mV peak input, consistent with the TPA3116D2 Undervoltage Lockout (UVLO) threshold [4]. Supply ripple at 12 V was measured at approximately 44 mV RMS on the VDD rail, which did not cause visible problems under the tested conditions.

5.1.3 Noise Analysis

Initial testing showed significant 50 Hz hum with no input signal. Oscilloscope measurements at RIN (AC coupling, 10× probe, 100 Hz bandwidth) showed noise approxi-

mately −20 dBV Root Mean Square (RMS) before any fixes were applied. Two causes were identified:

1. **Floating input:** RIN had no DC reference, making it susceptible to electric field coupling at 50 Hz (the mains supply frequency in Sweden)
2. **Ground loop:** Multiple ground return paths through the PSU chassis, oscilloscope probe, and signal cables

Fixes applied:

- 10 kΩ resistor from RIN to AGND
- Star grounding: all grounds to one node, one wire to PSU minus terminal
- Oscilloscope probe ground removed from amplifier output

After these changes, noise at RIN reduced to approximately −40 dBV RMS, limited by the oscilloscope noise floor. The 50 Hz hum was no longer audible. Remaining crackle at higher volumes was likely related to intermittent breadboard contacts, though this was not quantified.

5.2 Phase 2: Preamplifier Verification

5.2.1 Voltage Reference Measurement

Table 5.3: VREF measurements at different supply voltages (R3 = 46 kΩ, R4 = 55 kΩ)

Supply (V)	**Calculated VREF (V)**	**Measured VREF (V)**	**Deviation**
12	6.53	5.9	−9.7%
9	4.90	4.4	−10.2%

The measured VREF is approximately 10% below the calculated value. Contributing factors likely include loading effects in the bias network, breadboard contact resistance, and measurement uncertainty. Despite this, VREF remains near mid-supply and provided adequate signal headroom for the input levels tested.

5.2.2 Gain Verification

Gain was measured with a 1 kHz sine input, 12 V supply. Input amplitude was measured at op-amp non-inverting input (pin 3); output amplitude was measured directly at op-amp output (pin 1), before C3 and the summing network. All amplitudes are peak values read from the oscilloscope.

Figure 5.2 shows the supply voltage and VREF measured simultaneously, confirming stable DC levels before signal measurements.

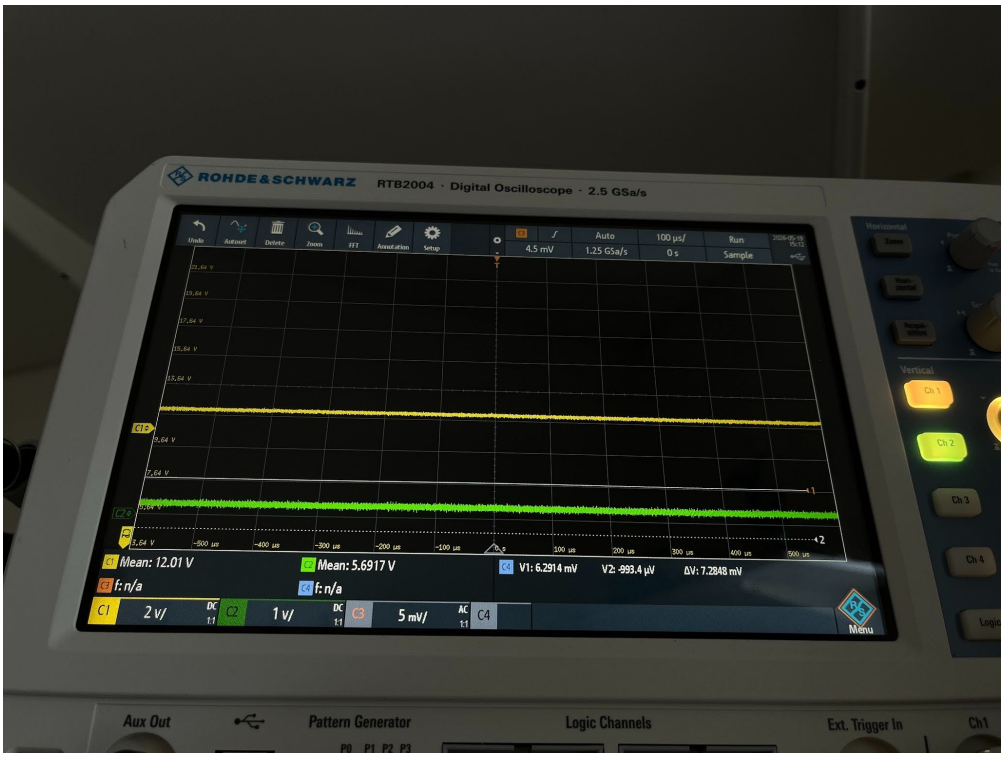

Figure 5.2: Oscilloscope measurement of supply voltage (Ch1, VDD = 12.0 V) and bias reference voltage (Ch2, VREF = 5.9 V). Supply ripple is approximately 44 mV RMS. VREF is stable and separate from GND.

Figure 5.3 shows the guitar input signal at J2 and at op-amp pin 3, confirming correct AC coupling through C1.

Figure 5.3: Guitar input signal at J2 (Ch2) and op-amp non-inverting input pin 3 (Ch4) at 1 kHz. Frequencies match (1.00 kHz), confirming AC coupling through C1 and signal transmission through the input network.

Table 5.4: Measured gain at op-amp output (1 kHz, 12 V supply, peak amplitudes)

Input (V peak)	**Output (V peak)**	**Gain**
0.098	0.720	7.35

Figure 5.4 shows the gain measurement waveforms at 1 kHz.

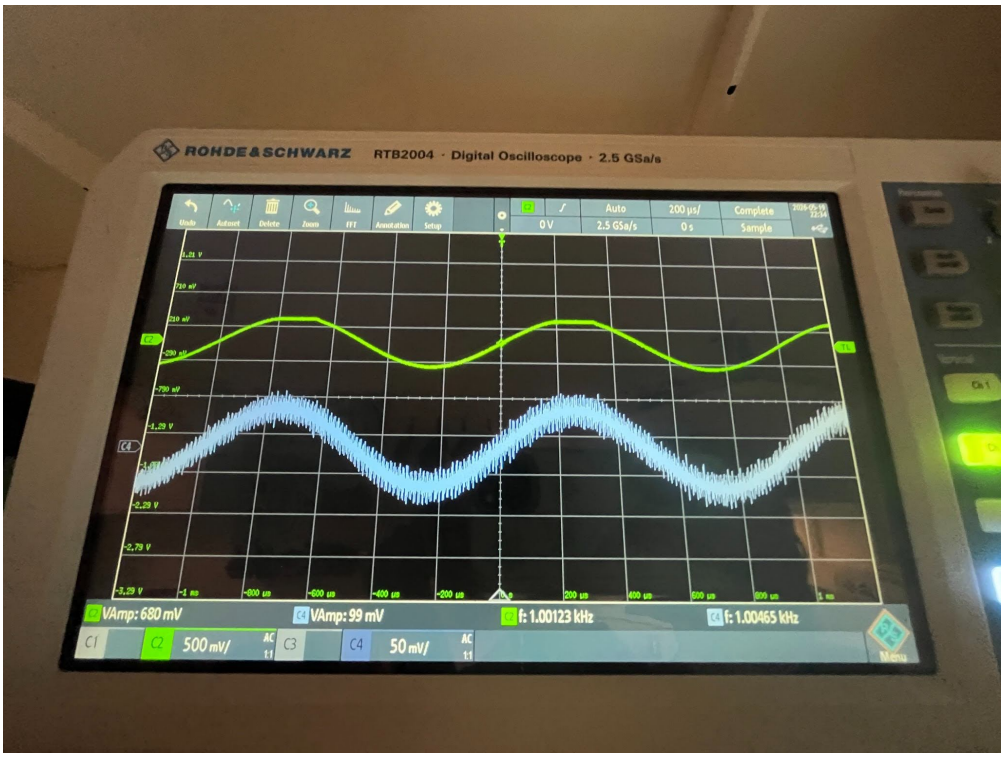

Figure 5.4: Op-amp gain measurement: input at pin 3 (Ch3, 98 mV peak) and output at pin 1 (Ch4, 720 mV peak) at 1 kHz, 12 V supply. Measured gain = 7.35 V/V. Output is centred around VREF (5.9 V), with no visible clipping at this input level.

The measured gain of 7.35 is approximately 18% below the theoretical value of 9. R6 and R7 were verified with a multimeter as 80 kΩ and 10 kΩ respectively, confirming that resistor tolerance is not the primary explanation. Possible contributors to the discrepancy include loading from the downstream coupling and summing network, measurement uncertainty, and non-ideal op-amp behaviour under breadboard test conditions. Signal amplitude at the MONO_MIX node was observed to be approximately 300–400 mV compared to 720 mV at pin 1, indicating significant attenuation through the summing network. A dedicated measurement with the downstream network disconnected would be needed to isolate the op-amp gain stage and determine the exact cause.

5.2.3 Frequency Response

Table 5.5 reports qualitative listening observations for the complete system (preamp + power amp + speaker). These do not characterise the preamplifier frequency response in isolation.

Table 5.5: Phase 2 qualitative system frequency observations (function generator, complete chain, listening only)

Frequency	**Qualitative Observation**
20 Hz	Barely audible
100 Hz	Audible
1 kHz	Strongest output
10 kHz	Audible
20 kHz	Barely audible

5.2.4 Clipping Characterisation

Clipping was detected by oscilloscope observation at op-amp output (pin 1). Input amplitude is peak value at pin 3. Supply voltage 12 V. VREF measured at 5.9 V.

Table 5.6: Clipping behaviour at op-amp output (peak input amplitude, 1 kHz, 12 V supply)

Input Amplitude (V peak)	**Observation at op-amp output**
0.50	Clean sine
0.80	Clean sine
0.92	First visible peak flattening
1.00	Moderate flattening
1.50	Severe clipping

At 0.92 V peak input, the expected output peak is $0.92 \times 7.35 = 6.76$ V. With VREF at 5.9 V, the output swings from $5.9 - 6.76 = -0.86$ V to $5.9 + 6.76 = 12.66$ V. The negative swing approaches ground and the positive swing exceeds the 12 V supply, which explains why clipping appears simultaneously on both peaks.

5.2.5 Passive Summing Network Performance

The passive summing network was tested by applying a 1 kHz signal to one input and checking for coupling at the other. No significant coupling was observed under the test conditions. A quantitative isolation measurement in dB was not performed.

Chapter 6

Discussion

6.1 Phase 1: Power Amplifier Performance

The measurements confirmed basic operation of the amplifier and speaker stage. The acoustic output was stronger in the mid-frequency range, which is consistent with the known behaviour of small full-range drivers without acoustic enclosures.

The 50 Hz hum was the primary unexpected result. Grounding turned out to affect system behaviour more than anticipated—most noise problems disappeared only after establishing a proper common ground reference. This is a well-known challenge in analog audio design that is easy to underestimate at the planning stage.

The weak low-frequency response came from the combination of the small driver size and the absence of an enclosure. Without one, the front and rear acoustic radiation partially cancel at low frequencies, reducing bass output.

6.2 Phase 2: Preamplifier Analysis

6.2.1 Biasing Network Stability

VREF showed approximately 10% deviation from the calculated value. The measured 5.9 V is still close to mid-supply and provided adequate headroom throughout testing. Moving to a soldered PCB would reduce breadboard-related effects and likely bring VREF closer to the calculated 6.53 V.

6.2.2 Gain Stage Performance

The measured gain of 7.35 versus theoretical 9 remains not fully explained. As discussed in Section 5.2.2, loading from the downstream summing network is a possible contributor, but a dedicated measurement with that network disconnected was not performed. The gain was sufficient for the input levels tested—clipping was not observed below 0.92 V peak input. The non-inverting configuration provides an effective input impedance of approximately 1 MΩ, dominated by the bias resistor.

6.2.3 Coupling and Filtering

With C1 = 10 μF and the 1 MΩ bias resistor:

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 10^6 \times 10 \times 10^{-6}} \approx 0.016 \text{ Hz} \tag{6.1}$$

This is well below 20 Hz, so no audible bass is attenuated at the input. For C3 (10 μF) with R8 (100 kΩ):

$$f_c = \frac{1}{2\pi \times 10^5 \times 10^{-5}} \approx 0.16 \text{ Hz} \tag{6.2}$$

Both coupling stages do not limit the audio bandwidth in the calculated high-pass response.

6.2.4 Passive Summing Analysis

The passive summing network introduces attenuation at the MONO_MIX node. The load seen by the guitar signal through R5 (10 kΩ) includes R8 (100 kΩ) and the amplifier input impedance in parallel, forming a voltage divider. A quantitative measurement of this attenuation was not performed, but the observed signal reduction between pin 1 and the MONO_MIX node is consistent with this loading.

6.3 Component Design and Justification

Each component was selected to satisfy specific engineering criteria. Table B.2 in Appendix B lists the actual values used. The following summarises the key reasoning for each.

6.3.1 Guitar Input (J2), AC Coupling (C1 = 10 μF), and Bias Resistor (1 MΩ)

C1 blocks DC from the guitar source, preventing disturbance of the op-amp bias. Combined with the 1 MΩ bias resistor, it forms a high-pass filter with $f_c \approx 0.016$ Hz—well below the audible range. The 1 MΩ resistor provides the high input impedance required by guitar pickups [1].

For AC guitar signals, the VREF node is approximately AC-grounded by C2. The pickup therefore sees an input load dominated by the 1 MΩ bias resistor. This high input impedance reduces loading on the passive guitar pickup and helps preserve signal amplitude and frequency response across the audio band.

6.3.2 VREF Divider (R3 = 46 kΩ, R4 = 55 kΩ) and Bypass (C2 = 22 μF)

R3 and R4 shift the audio signal from 0 V-centred to VREF-centred, making single-supply operation possible. The calculated VREF is 6.53 V, close to but not exactly mid-supply. Current through the divider:

$$I = \frac{12}{101000} \approx 119\ \mu\text{A}, \quad P \approx 1.4\ \text{mW} \tag{6.3}$$

Equal resistors would give exactly mid-supply VREF. The values 46 kΩ and 55 kΩ were the closest available that gave a VREF near mid-supply, since the original schematic used 100 kΩ/100 kΩ and stock differed. The resulting 6.5 V is close enough for this prototype. C2 filters supply noise on VREF with $f_c \approx 0.29$ Hz.

6.3.3 Op-Amp Gain Network (R6 = 80 kΩ, R7 = 10 kΩ)

Theoretical gain: $G = 1 + 80\text{k}/10\text{k} = 9$. Measured: 7.35. The clipping point at 0.92 V peak input ($0.92 \times 7.35 = 6.76$ V peak output) sets the upper usable input range for this gain setting.

6.3.4 Decoupling, Coupling, and Mixing Resistors

C4 (0.1 μF ceramic) provides local supply decoupling for the op-amp. C3 (10 μF) removes the VREF DC offset from the output. R8 (100 kΩ) defines the DC reference

at NODE_A after C3. R1 and R2 (4.7 kΩ each) combine stereo PC audio without shorting source outputs. R5 (10 kΩ) isolates the guitar path at the summing node.

6.4 Comparison with Project Plan

Table 6.1: Planned versus actual phase completion

Phase	Description	Planned Weeks	Status
0	Research and system design	1–3	Complete
1	Power amplifier and speaker	4–6	Complete
2	Guitar preamplifier	7–9	Complete
3	Digital effects	10–13	Partially complete (DAC and DSP verified; ADC failed)
4	Battery power and enclosure	14–17	Enclosure manufactured; battery not implemented
5	Testing and documentation	18–20	Partially completed through this report

Phases 1 and 2 took longer than planned due to breadboard instability, component delivery issues, and grounding problems that took time to diagnose. Several lessons came out of this: breadboard prototypes require more debugging time than estimated; component delivery risk should be managed by ordering earlier and identifying fallback parts in advance. Phase 3: DAC, delay, and reverb were all verified using internally generated test signals. The external oscillator (ACHL-24.576 MHz-EK) arrived and was installed, and all ADC clock signals were verified correct. However, both PCM1808 ADC modules from the same batch failed to produce output, likely due to a batch-level manufacturing defect. The full DSP signal chain could therefore not be completed. Phase 4: the enclosure was designed in Onshape and successfully 3D printed in PLA using FDM. The analogue signal chain was installed in the enclosure with the Visaton FRS 7 speaker. Battery power was not implemented.

6.5 Sustainability, Ethics, and Societal Aspects

6.5.1 Environmental Considerations

Building a custom replacement for a broken amplifier extends the useful life of components and avoids electronic waste. The Class-D topology offers significantly higher power efficiency (typically 85–95%) compared to Class-AB designs [4]. The 3D-printed enclosure uses PLA plastic. While PLA is sometimes described as compostable, proper disposal still requires industrial composting facilities; otherwise it contributes to plastic waste. A 2S Li-ion battery would require a battery management system and proper recycling at end of life.

6.5.2 Safety Considerations

The BTL topology requires care with oscilloscope probes: connecting a ground clip to either output terminal shorts it to earth ground through the probe. At the supply voltages used here, electrical shock risk is low, but speaker power should be kept within the driver's 8 W rating. Prolonged exposure to loud audio output may cause hearing damage.

6.5.3 Ethical Considerations

AI-based tools were used in this project for learning and report structuring. The use is disclosed in the Acknowledgements. The author takes full responsibility for all technical content. Accurate reporting of prototype limitations—battery not implemented, ADC not verified due to hardware failures—is important for honest scientific communication.

6.6 Sources of Error and Uncertainty

- **Breadboard power connections:** A loose VDD connection to the op-amp supply pin caused intermittent signal loss and noisy waveforms during testing. After soldering the connection, signal quality improved immediately. Critical power connections should be soldered even on breadboard prototypes.
- **Resistor tolerance:** Standard 5% resistors introduce up to approximately 10% error in ratios

- **Op-amp offset voltage:** TLC272 maximum offset voltage up to 10 mV [3] may cause a small DC error at the output
- **Multimeter accuracy:** Tenma 72-7732A, ±0.5% DC voltage accuracy
- **Oscilloscope probe loading:** 10 MΩ probe impedance may affect measurements at high-impedance nodes
- **Breadboard contact resistance:** Intermittent contacts introduce variability that would not be present in a soldered design

These uncertainty sources are typical of breadboard-based prototype work and should be kept in mind when interpreting the reported results.

6.7 Improvements and Future Work

6.7.1 Component and Circuit Improvements

- Replace TLC272 with OPA1678 for lower noise and offset
- Use 1% precision resistors in the gain network and VREF divider
- Add a variable gain stage to accommodate different pickup types
- Implement soft clipping using a diode network for improved sound quality at high input levels
- Measure gain directly at op-amp output with downstream network disconnected to characterise loading in isolation

6.7.2 Battery Power (Phase 4)

Portable operation requires a 2S Li-ion battery (7.4 V nominal, 8.4 V fully charged) with a boost converter to supply the TPA3116 at 12 V, or alternatively a 3S pack (11.1 V nominal). A Battery Management System (BMS) providing overcurrent, overcharge, and undervoltage protection is required for safe operation. A fuse and appropriate enclosure ventilation would also be needed.

6.7.3 Enclosure Manufacturing (Phase 4)

The enclosure designed in Onshape should be 3D printed at the CASE laboratory and tested for fit and acoustic properties. Speaker mounting orientation and internal volume both affect acoustic frequency response.

6.7.4 Phase 3: Full Digital Effects

The external oscillator was installed and all ADC clock signals were verified, but both PCM1808 modules tested failed to produce output. Remaining work includes sourcing PCM1808 modules from a different supplier or batch, verifying the full signal chain (guitar input $\rightarrow$ PCM1808 ADC $\rightarrow$ ESP32 $\rightarrow$ PCM5122 DAC $\rightarrow$ amplifier), and testing delay and reverb on real guitar input. An alternative ADC such as the PCM1865 could be considered.

Chapter 7

Conclusion

This project demonstrated the design and experimental verification of a prototype guitar amplifier through systematic incremental development. The analog preamplifier and Class-D amplifier stages were experimentally verified.

Phase 1 verified Class-D amplifier operation and identified grounding as the dominant noise source. Star grounding reduced the noise floor from approximately -20 dBV to -40 dBV. Phase 2 achieved a measured voltage gain of 7.35 (theoretical 9), with clipping first observed at 0.92 V peak input at 12 V supply. VREF was measured at 5.9 V (calculated 6.53 V with the actual 46 kΩ/55 kΩ divider).

Component values were selected based on specific engineering criteria—input impedance, gain, and power consumption—and verified through measurement where possible. Frequency response was confirmed qualitatively. The incremental breadboard methodology proved effective for managing complexity and catching problems early.

The enclosure was designed and manufactured. Battery integration and full Phase 3 ADC verification—blocked by hardware failures in both PCM1808 modules tested—remain as future work before the system can be considered a complete portable amplifier.

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Appendix A

Schematics and Circuit Diagrams

A.1 Phase 1: Power Amplifier Circuit

The Phase 1 circuit uses the TPA3116-based module with a 10 kΩ resistor from RIN to AGND. Signal from the function generator connects to RIN; 10 kΩ connects from RIN to AGND. Speaker connects between R+ and R-. No speaker terminal connects to ground.

A.2 Phase 2: Preamplifier Circuit

Figure A.1 shows the KiCad schematic with the actual implemented component values.

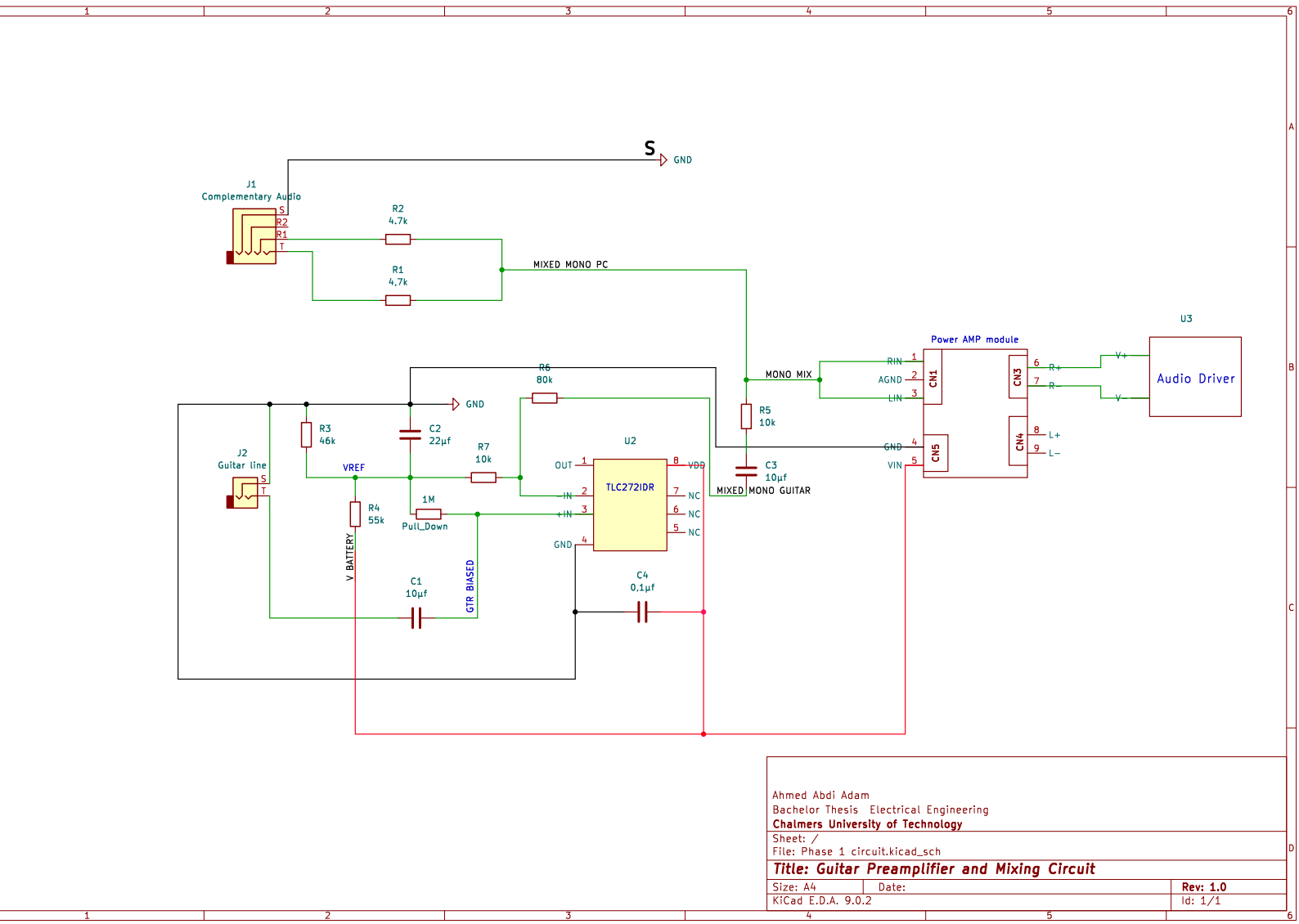

Figure A.1: Phase 2 preamplifier and mixing circuit schematic (KiCad). Actual implemented values: R3 = 46 kΩ, R4 = 55 kΩ, R6 = 80 kΩ, pull-down = 1 MΩ, U2 = TLC272IDR. See Table B.2 for full component list.

Appendix B

Component Values and Specifications

B.1 Phase 1 Components

Table B.1: Phase 1 components

Component	**Value**	**Notes**
Amplifier module	TPA3116D2-based	Nominally rated up to 2×50 W; operated at 12 V
Speaker	4 Ω, 8 W	Measured DCR ≈ 4.3 Ω
R_IN	10 kΩ	Input reference resistor
PSU	12 V, 1 A current limit	Tenma 72-8345A

B.2 Phase 2 Components

Table B.2: Phase 2 actual component values used in breadboard implementation

Component	**Actual Value**	**Notes**
U2 (op-amp)	TLC272IDR	Substitute used for all measurements; OPA1678 planned. On SOIC-8 adapter.
R1	4.7 kΩ	PC right channel to MONO_MIX
R2	4.7 kΩ	PC left channel to MONO_MIX
R3	46 kΩ	VREF divider upper (VCC to VREF node)
R4	55 kΩ	VREF divider lower (VREF node to GND)
R5	10 kΩ	Guitar path isolation
R6	80 kΩ	Op-amp feedback
R7	10 kΩ	Gain reference
R8	100 kΩ	NODE_A reference
Pull-down	1 MΩ	Guitar input impedance
C1	10 μF	Input AC coupling, electrolytic
C2	22 μF	VREF bypass (replaced after polarity issue)
C3	10 μF	Output AC coupling, electrolytic, positive to op-amp output side
C4	0.1 μF	Op-amp supply decoupling, ceramic
J1	TRRS 3.5 mm	Auxiliary stereo input
J2	TS 6.35 mm	Guitar input

Appendix C

Noise Measurements

Noise was measured at the power amplifier input (RIN to AGND) using oscilloscope AC coupling mode, 10× probe, 100 Hz bandwidth limit, RMS measurement.

- Before grounding fix: approximately −20 dBV RMS (dominated by 50 Hz hum)
- After star grounding and input reference resistor: approximately −40 dBV RMS (limited by oscilloscope noise floor)

Appendix D

Code and Firmware

D.1 Phase 3: Preliminary DSP Verification

The following code was verified on the Olimex ESP32-DevKit-LiPo with the PCM5122 DAC module using internally generated 440 Hz sine test signals. The guitar ADC (PCM1808) was not verified in this phase; all DSP testing used internally generated signals only.

D.1.1 Delay Effect

Listing D.1: Delay effect verified on ESP32 with PCM5122 DAC (internal test signal only)

```
#include "driver/i2s.h"
#include <math.h>

#define SAMPLE_RATE     44100
#define I2S_NUM         I2S_NUM_0
#define BCK_PIN         4
#define WS_PIN          5
#define DATA_OUT_PIN    13
#define DELAY_MS        350
#define FEEDBACK        0.5f
#define DELAY_SAMPLES   (SAMPLE_RATE * DELAY_MS / 1000)
```

```
float delay_buffer[DELAY_SAMPLES] = {0};
int delay_index = 0;

void setup_i2s() {
    i2s_config_t cfg = {
        .mode = (i2s_mode_t)(I2S_MODE_MASTER | I2S_MODE_TX),
        .sample_rate = SAMPLE_RATE,
        .bits_per_sample = I2S_BITS_PER_SAMPLE_16BIT,
        .channel_format = I2S_CHANNEL_FMT_RIGHT_LEFT,
        .communication_format = I2S_COMM_FORMAT_STAND_I2S,
        .intr_alloc_flags = ESP_INTR_FLAG_LEVEL1,
        .dma_buf_count = 8,
        .dma_buf_len = 64,
        .use_apll = false,
        .tx_desc_auto_clear = true,
        .fixed_mclk = 0
    };
    i2s_pin_config_t pins = {
        .mck_io_num = I2S_PIN_NO_CHANGE,
        .bck_io_num = BCK_PIN,
        .ws_io_num = WS_PIN,
        .data_out_num = DATA_OUT_PIN,
        .data_in_num = I2S_PIN_NO_CHANGE
    };
    i2s_driver_install(I2S_NUM, &cfg, 0, NULL);
    i2s_set_pin(I2S_NUM, &pins);
}

void loop() {
    static float phase = 0.0f;
    int16_t buf[128];
    for (int i = 0; i < 64; i++) {
        float input = sinf(phase) * 10000.0f;
        phase += 2.0f * M_PI * 440.0f / SAMPLE_RATE;
```

```
        if (phase > 2.0f * M_PI) phase -= 2.0f * M_PI;
        float delayed = delay_buffer[delay_index];
        float output = input + delayed * FEEDBACK;
        delay_buffer[delay_index] = output;
        delay_index = (delay_index + 1) % DELAY_SAMPLES;
        int16_t s = (int16_t)fmaxf(-32768, fminf(32767,
           output));
        buf[2*i] = s;
        buf[2*i+1] = s;
    }
    size_t written;
    i2s_write(I2S_NUM, buf, sizeof(buf), &written,
       portMAX_DELAY);
}
```

D.1.2 Reverb Effect (Schroeder)

Listing D.2: Schroeder reverb [6] verified on ESP32 with PCM5122 DAC (internal test signal only)

```
#include "driver/i2s.h"
#include <math.h>

#define SAMPLE_RATE 44100
#define I2S_NUM     I2S_NUM_0
#define BCK_PIN     4
#define WS_PIN      5
#define DATA_PIN    13

#define COMB1 1557
#define COMB2 1617
#define COMB3 1491
#define COMB4 1422
#define ALLPASS1 225
#define ALLPASS2 556
```

```
#define REVERB_GAIN 0.84f
#define AP_GAIN     0.5f

float comb1[COMB1]={}, comb2[COMB2]={}, comb3[COMB3]={},
   comb4[COMB4]={};
float ap1[ALLPASS1]={}, ap2[ALLPASS2]={};
int ci1=0,ci2=0,ci3=0,ci4=0,ai1=0,ai2=0;

float comb_f(float *buf, int *idx, int len, float in) {
    float out = buf[*idx];
    buf[*idx] = in + out * REVERB_GAIN;
    *idx = (*idx + 1) % len;
    return out;
}

float allpass_f(float *buf, int *idx, int len, float in) {
    float delayed = buf[*idx];
    float out = -in + delayed;
    buf[*idx] = in + delayed * AP_GAIN;
    *idx = (*idx + 1) % len;
    return out;
}

void setup_i2s() {
    i2s_config_t cfg = {
        .mode = (i2s_mode_t)(I2S_MODE_MASTER | I2S_MODE_TX),
        .sample_rate = SAMPLE_RATE,
        .bits_per_sample = I2S_BITS_PER_SAMPLE_16BIT,
        .channel_format = I2S_CHANNEL_FMT_RIGHT_LEFT,
        .communication_format = I2S_COMM_FORMAT_STAND_I2S,
        .intr_alloc_flags = ESP_INTR_FLAG_LEVEL1,
        .dma_buf_count = 8,
        .dma_buf_len = 64,
        .use_apll = false,
```

```
        .tx_desc_auto_clear = true,
        .fixed_mclk = 0
    };
    i2s_pin_config_t pins = {
        .mck_io_num = I2S_PIN_NO_CHANGE,
        .bck_io_num = BCK_PIN,
        .ws_io_num = WS_PIN,
        .data_out_num = DATA_PIN,
        .data_in_num = I2S_PIN_NO_CHANGE
    };
    i2s_driver_install(I2S_NUM, &cfg, 0, NULL);
    i2s_set_pin(I2S_NUM, &pins);
}

void loop() {
    static float phase = 0.0f;
    int16_t buf[128];
    for (int i = 0; i < 64; i++) {
        float input = sinf(phase) * 10000.0f;
        phase += 2.0f * M_PI * 440.0f / SAMPLE_RATE;
        if (phase > 2.0f * M_PI) phase -= 2.0f * M_PI;
        float rev = comb_f(comb1,&ci1,COMB1,input)
                  + comb_f(comb2,&ci2,COMB2,input)
                  + comb_f(comb3,&ci3,COMB3,input)
                  + comb_f(comb4,&ci4,COMB4,input);
        rev = allpass_f(ap1,&ai1,ALLPASS1,rev);
        rev = allpass_f(ap2,&ai2,ALLPASS2,rev);
        float mix = input * 0.5f + rev * 0.3f;
        int16_t s = (int16_t)fmaxf(-32768, fminf(32767, mix));
        buf[2*i] = s;
        buf[2*i+1] = s;
    }
    size_t written;
```

```
    i2s_write(I2S_NUM, buf, sizeof(buf), &written,
        portMAX_DELAY);
}
```