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Combined onboard charger and DC-DC converter design in a Plug-in Hybrid Vehicle

Master's Thesis in Electrical Power Engineering

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Department of Electric Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

MASTER'S THESIS 2018:NN

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Abstract

To enhance the power density by reducing the charging system's volume, this master thesis designed and optimized a combined onboard charger and DC-DC converter with a three-winding transformer for a plug-in hybrid vehicle platform.

The topology adopts a dual active full bridge (DAB) design as the DC-DC isolated converter in the OBC and a full-bridge DC-DC converter with current doubler and synchronous rectification for the 12V battery charging. In the project, these two different typologies were investigated and simulated in LTspice. Zero Voltage Switching (ZVS) has been implemented and its operation has been verified in order to decrease the switching losses. A three-port high frequency transformer is designed to keep a high power density. Power losses and efficiency are calculated and presented in this report. Moreover, the real component selection and the comparison related to efficiency, volume and cost are made between the new design topology with a three-port HF transformer and the existing conventional charging system.

The simulation, power losses and efficiency are analyzed of the nominal operating point in this project. The simulation result shows that the ZVS strategy is achieved successfully for efficiency improvement. The volume of the transformer has been minimized with the appropriate design of the core and windings. The power losses includes switching loss, conduction loss, core loss and copper loss in the transformer. For the DC/DC converter in the OBC, the efficiency can reach 94.8% at the nominal operating point and regarding the full-bridge DC/DC converter, the efficiency can reach 93.57% at the nominal operationg point. Compared with the single packages for the OBC and DC-DC component, the price saved is roughly about 613 Sek and the dimension saved is approximately 72 cm^3.

Keywords: On board charger, DC-DC converter, three winding transformer, plug-in hybrid vehicle.

Acknowledgements

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Last but not least, we are grateful to our parents for supporting us throughout all our studies at Chalmers. Their love and guidance are with us in whatever we pursue.

Mingzhi Xue and Jiaao Tong, Gothenburg, 2018

Table of Contents

Abbreviations

AC	Alternating Current
DAB	Dual active full bridge
DC	Direct Current
DC-DC	DC to DC Converter
HF	High frequency
HV	High Voltage
OBC	Onboard Charger
RMS	Root Mean Square
ZVS	Zero Voltage Switching

1

Introduction

1.1 Background

The ever more pressing topic of exhaust gas emission reductions leads the automotive industry to develop more environment friendly technologies. Besides, the fact that fossil fuels are being depleting also encourages the development of sustainable transportation. Hence, vehicle manufacturers intend to integrate hybrid power trains in conventional vehicles, and even to replace it with fully electrical ones. In addition, the hybrid vehicle has a higher efficiency and the possibility to regenerate the kinetic power to electric power for later use, which also makes the hybrid vehicle quite popular with customers.

Based on customer requirements and market expectations, a better performance and still a low cost hybrid vehicle is a logical step .The hybrid propulsion system is based on a complex systems of power electronic devices. Furthermore, the concept of power density of power electronic converters is most widely utilized to present and evaluate the performance. Therefore, the automotive industry requires a high power density of the power electronics as well as a low cost.

The converter volume has a significant impact on the power density. Besides, a small volume requirement allows a greater design freedom and a lower capital outlay in the building infrastructure[1]. Hence, it is accordingly necessary to think about package volume reduction.

There are several different charging system typologies that are known today. One common design is shown in Figure.1.1. It is indicated that that the onboard charger(OBC) and DC/DC converter are packaged separately. The OBC package is designed as the AC/DC together with a DC/DC converter to charge the high voltage batteries. The isolated buck DC-DC converter is designed in another package, which is fed by the battery and supplies the 12V power net needed for auxiliary purposes in a hybrid electric vehicle. The transformer for galvanic insulation is applied in both the OBC charger and DC/DC converter, which takes much space due to the usages of two packages. Therefore, one can consider to combine these two packages into a compact one and a three winding transformer will be used to transfer power, shown in Figure1.2. Consequently, the volume of the power electronic device has a potential to be lower due to the new combined transformer as well as the sharing of cooling system. In this thesis work, this thought will be discussed and the performance will be evaluated.

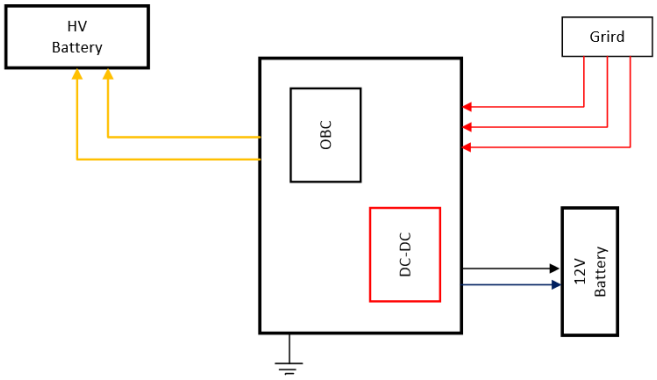

Figure 1.1: The existing architecture of the charging system with an extra 12V storage system.

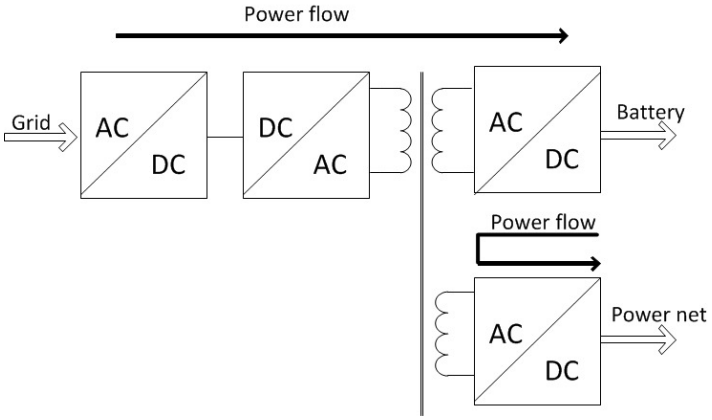

Figure 1.2: Design Overview.

1.2 Previous work

The previous work [5] investigated the full bridge with full wave rectification and full bridge with current synchronous rectification regarding ZVS implementation, transformer design and power losses calculation. The result shows the feasibility to investigate further for charging system in hybrid vehicle. Therefore, based on the previous work, a dual active bridge for the DC/DC part of OBC and a full-bridge DC-DC converter with current doubler and synchronous rectification for charging 12V power-net are investigated as well as a proper three-winding transformer design is implemented so as to achieve high power density for the charging system.

1.3 Purpose

The main objective of the thesis work is to design a combined on board charger and DCDC converter through using three-winding transformer for a plug-in hybrid vehicle to increase

the power density compared with the conventional topology. In order to integrate the system and keep high efficiency, the focus is on the converter topology and using a three-port HF transformer instead of two conventional transformers.

1.4 Sustainability and ethics aspects

We hereby declare the thesis work is carried out by ourselves under the guidance of our supervisor and examiner. The content, data and result are authentic, which is obtained by the logical and valid derivation and quotation. Efforts have been made to describe the work carefully so that it can be reproduced by readers.

The outcome of the project is targeted for hybrid and electrical automotive industry which is aiming to reduce air pollution. The thesis outcome reduces the existing design cost and losses and contributes to the product environmental friendly and sustainable development. We did not choose any component which includes non-desirable material and will not cause misery on earth.

2

Theory

2.1 Design overview

PHEVs charging system consists of an OBC for high voltage battery system and a DC-DC converter for low power system. In order to increase the power density and save space, the OBC could be combined with the DC-DC converter through an isolated three-winding transformer.

In normal case the OBC includes AC/DC boosting converter with PFC and DC-DC converter for high voltage battery system. In this design, the concentration will be the OBC DC-DC isolated converter combined with the 400-12V DC/DC converter for low power system.

As Figure1.2 shown ,there are two power flow paths, which is conducted by different typologies. Hence, these two typologies will be discussed separately.

2.2 Soft switching - Zero Voltage Switching

In all the pulse-width-modulated dc-to-dc and dc-to-ac converter typologies, the controllable switches are operated in a high frequency switch mode where they are required to turn on and turn off the entire load current during each switching. In such a switch-mode operation, the switches are subjected to high switching stresses and high switching power losses that increases linearly with the switching frequency. Another significant drawback of the switch-mode operation is the EMI produced due to large di/dt and dv/dt caused by a switch-mode operation[6]. However, in order to reduce the size and volume of the converter and hence to increase the power density, the high switching frequency operation mode is unavoidable.

Therefore, one can reduce the switching losses by turning on and off each converter MOSFET when either the switch voltage or current is zero. Ideally, if each switch changes its status when the voltage across it is zero, this will result in zero-voltage switching(ZVS)[6]. Consequently, the switching losses will be reduced largely. With the help of the MOSFET's junction capacitance and the reverse recovery diode, ZVS can be achieved in this master thesis work. It eliminates the switching loss as well as di/dt noise, which enables the converter to operate at a high switching frequency.

2.3 DC-DC part of OBC

The dual active bridge(DAB) is commonly proposed for HV applications in this research field. Its character is bidirectional power transfer, which is very suitable for high voltage battery charging system fed by a battery in driving mode. Besides, a high frequency isolated transformer is involved in the DAB, which can provide the isolation for safety as a charger in hybrid/electric vehicles. The topology of a dual active bridge is shown in Figure 2.1.

The converter consists of eight active switches which are placed on four legs as full bridge structures and a HF transformer. Four switches are located on the primary side and the other four are placed on the secondary side. Both sides are isolated by a HF transformer. Since the leakage inductance of the transformer and the parasitic capacitance of the active components can be utilized to achieve the ZVS soft switching technology with the combination of a proper converter topology and a suitable switching pattern. This can be utilized to minimize switching losses, which, in return, will increase the switching frequency and subsequently a reduce size and weight of the transformers and the passive components numbers.

The main merit of the DAB are the low number of passive components, the evenly shared currents in the switches, its soft switching properties and flexible control strategy. With the DAB converter topology, high power density is possible. [2][3]

2.3.1 Switching pattern

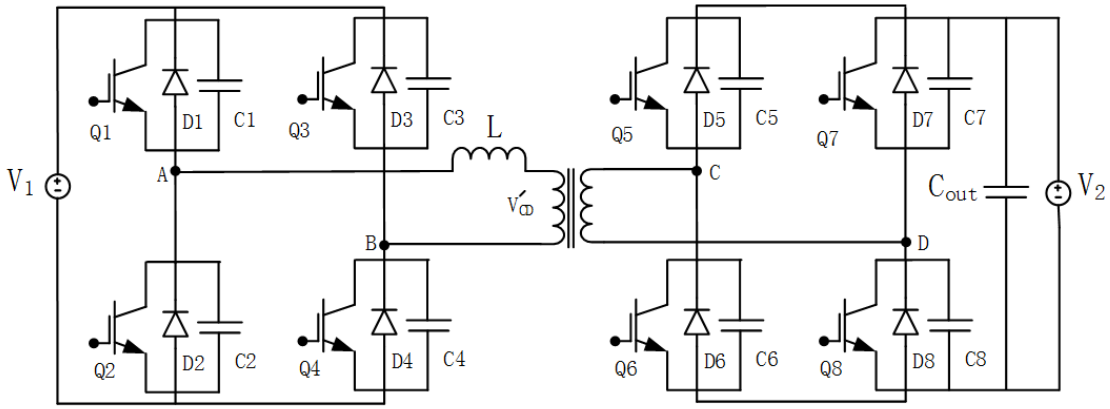

Figure 2.1: Dual active bridge topology schematic.

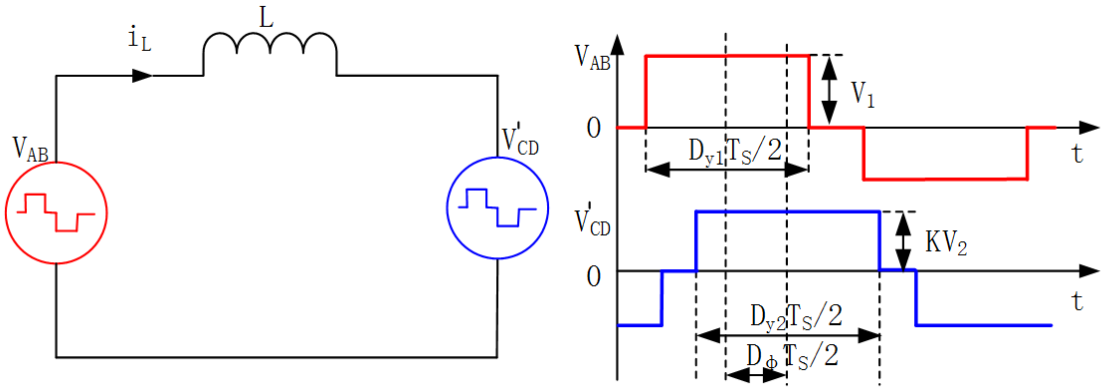

Figure 2.2: Simplified DAB circuit.

Redrawing the DAB converter as shown in Fig.3.1 and from the simplified schematic Fig.3.2 shown above, according to suitable control of the switches, two square voltage waves can be achieved on both sides of the transformer, V_{AB} and V_{CD}. V'_{CD} is the transferred voltage from the secondary side to the primary side. Energy passes through the inductance L between the two sources. Flexible control strategy can be achieved by adjusting the duty cycle of V_{AB}, the duty cycle of V'_{CD} and phase shift angle between V_{AB} and V'_{CD}. In this case, we define the voltage ratio $k = KV_2/V_1$. When $k \leqslant 1$, the converter transfers positive power but the converter transfers negative power when $k > 1$. For a charging system, $k \leqslant 1$ is applied for the positive power transfer. D_ϕ is defined as the duty cycle corresponding to the phase shift between V_{AB} and V_{CD}, while D_{y1} is the duty cycle of V_{AB}.

The most commonly used modulation method, phase shift modulation, operates the DAB with a constant frequency and with maximum duty cycles. The two switches in every arm just conduct 180°complementary and the diagonal switches keep on and off action simultaneously. It solely changes the phase shift angle to control the transferred power[8]. The main advantage of this pattern is its simplicity as only one variable need to be controlled. Basic on the phase shift switching modulation, adding another controllable variable, the duty cycle of the primary side. Considering this pattern, the two switches in every arm conduct 180°complementary. The two legs of the primary side adopt the phase shift pattern which means Q1 and Q2 leading Q3 and Q4. The duty cycle of the primary voltage V_{AB} can be controlled through the phase shift of this two arms. The diagonal switches on the secondary side turns on or off simultaneously. Consequently, the transferred power are adjusted using the phase shift angle between V_{AB} and V_{CD}. The great merits of this switching modulation are a wide range of soft switching and a smaller RMS currents using high frequency transformer compared with the phase shift modulation.[11]

2.3.2 Circuit operation

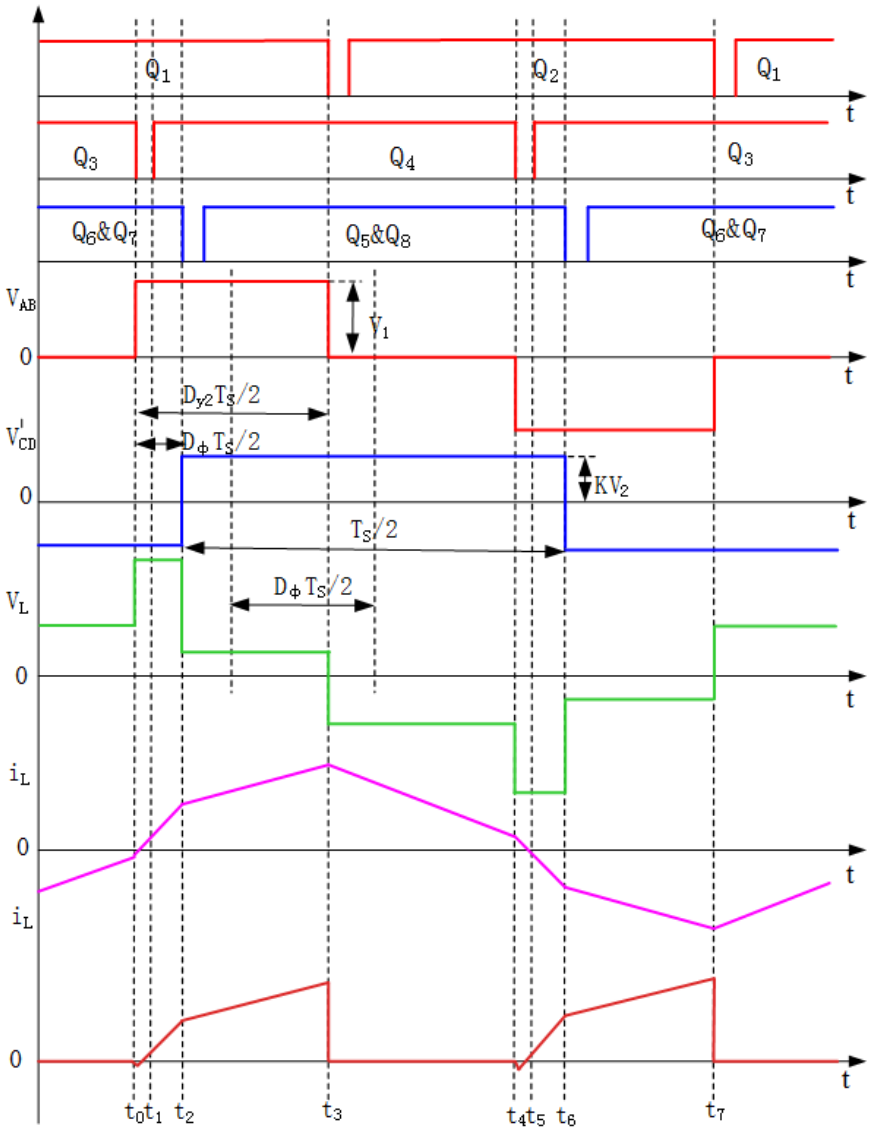

Figure 2.3: Gate signals and main waveforms of the DAB converter.

Figure 2.3 shows the gate control signals and main waveforms of a dual active full bridge converter. The operation of the DAB converter with ZVS in different time periods are shown from Figure 2.4 to Figure 2.8. The operation of the circuit is achieved by a proper turn on/off sequence of eight switches (Q1 to Q8). Moreover, there are an anti-parallel body diode and an output parasitic capacitance embedded inside the MOSFET which can realize the ZVS operation in consideration with the inductance. And the inductance is the sum of the leakage inductance and a passive external inductance.

Considering the blanking time between the upper and lower switches in each leg, which avoid short circuit and provide the time interval for ZVS operation, the duty cycle is slightly less than 50% for each switch. The converter operation is explained at the following part.

During a half switching cycle $[t_0, t_4]$, there are four switching instants that are shown from Figure 2.4 to Figure 2.8. Since the switching process is very short, the transient process is neglected to simplify the analysis.

Mode I: Initial condition t_0

Suppose that Q_1 and Q_3 are conducting before time instant t_0. The primary side current is negative flowing D_1 and Q_3. And the current in secondary side goes through D_6 and D_7. In this mode, the inductance L releases energy to the voltage source V_2. This process can be seen from Figure 2.4.

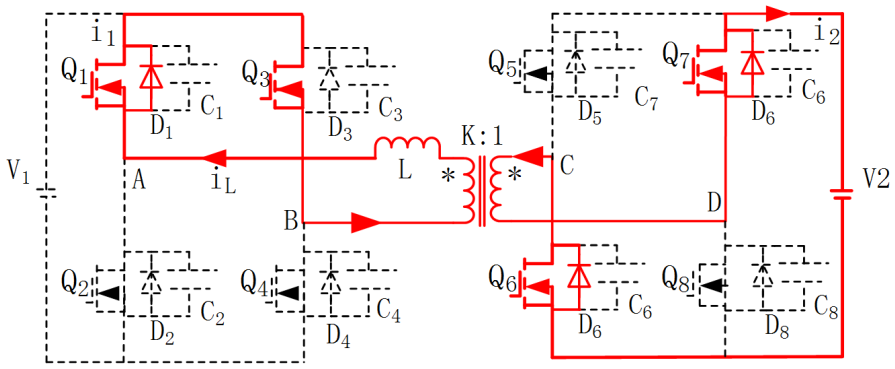

Figure 2.4: Operation of the DAB converter with ZVS at time t_0.

Mode II: Start of the right leg transition in primary side $[t_0, t_1]$

Q_3 is turned off at time instant t_0, C_3 is charged by i_L while C_4 is discharged. Due to the capacitance C_3 and C_4, Q_3 can be switched off with zero voltage. When the voltage of C_3 reaches V_1 and the voltage of C_4 decreases to zero, the body diode of Q_4 , D_4, will conduct naturally to turn on Q_4 with zero voltage. Now, $V_{AB} = V_1$, $V_{CD} = -V_2$ and $V_L = V_1 + KV_2$, so i_L increases with the slope

$$\frac{di_L}{dt} = \frac{V_1 + KV_2}{L} \tag{2.1}$$

At time instant t_1, i_L increases from minus to zero, meanwhile D_1, D_4, D_6 and D_7 will be turned off naturally.

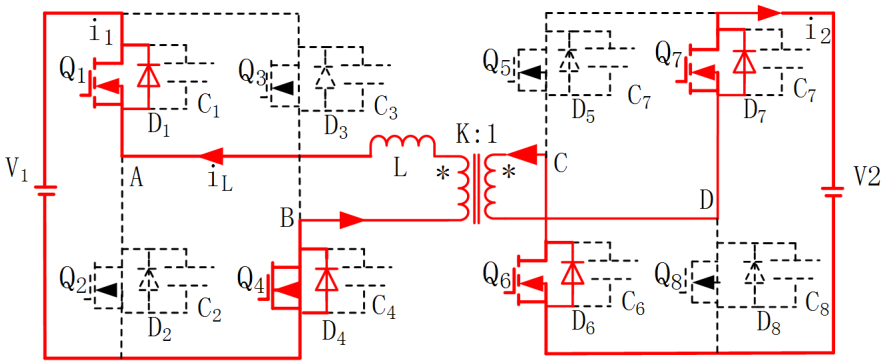

Figure 2.5: Operation of the DAB converter with ZVS at $[t_0, t_1]$.

Mode III: Completion of the right leg transition in primary side $[t_1, t_2]$

At time instant t_1, i_L becomes positive flowing through Q_1 and Q_4, so $V_{AB} = V_1$. Then the secondary side current runs through Q_6 and Q_7, which means $V_{CD} = -V_2$. So $V_L = V_1 + KV_2$ at this moment, i_L keeps increasing. In this mode, the power source V_1 and V_2 supply the energy to the inductance simultaneously.

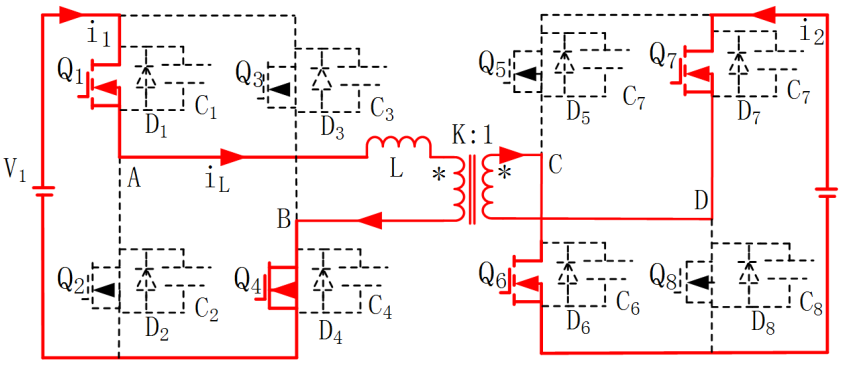

Figure 2.6: Operation of the DAB converter with ZVS at $[t_1, t_2]$.

Mode IV: Switching commutation in secondary side $[t_2, t_3]$

The switches Q_6 and Q_7 are turned off at t_2 and C_6 and C_7 are charged by i_L. At the same time, C_5 and C_8 are fully discharged. Because the voltage between the capacitance can not change instantly, Q_6 and Q_7 achieve turn off with zero voltage. When C_6 and C_7 are fully charged, which means the voltage of C_5 and C_8 reach zero. Then the anti-parallel diode will conduct automatically. Hence, Q_5 and Q_8 will be turned on with zero voltage. Meanwhile, $V_{AB} = V_1$, $V_{CD} = V_2$ and $V_L = V_1 - KV_2$. i_L still keeps increasing, but the increasing slop changes to

$$\frac{di_L}{dt} = \frac{V_1 - KV_2}{L} \tag{2.2}$$

In this mode, the inductance L releases energy to the source V_2.

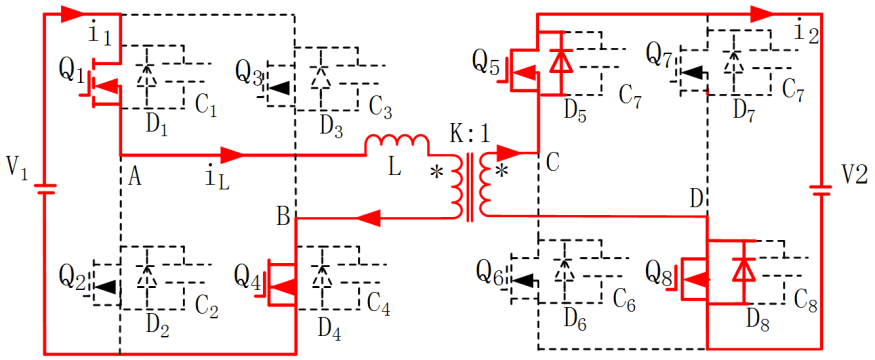

Figure 2.7: Operation of the DAB converter with ZVS at $[t_2, t_3]$.

Mode V: Start of the left transition in primary side $[t_3, t_4]$

Q_1 is turned off at time t_3, C_1 is charged by i_L and C_2 is discharged. At this moment, Q_1 can realize zero voltage turned-off. Once the voltage of C_1 increases to V_1 and C_2 is fully discharged, the anti-parallel diode of Q_2 will conduct and Q_2 can be turned on with zero voltage. Now $V_{AB} = 0, V_{CD} = V_2$, but i_L begins to decrease with a negative slop:

$$\frac{di_L}{dt} = \frac{-KV_2}{L} \tag{2.3}$$

After time instant t_4, the DAB converter will start to operate in another half circle, which is the similar operation explained above.

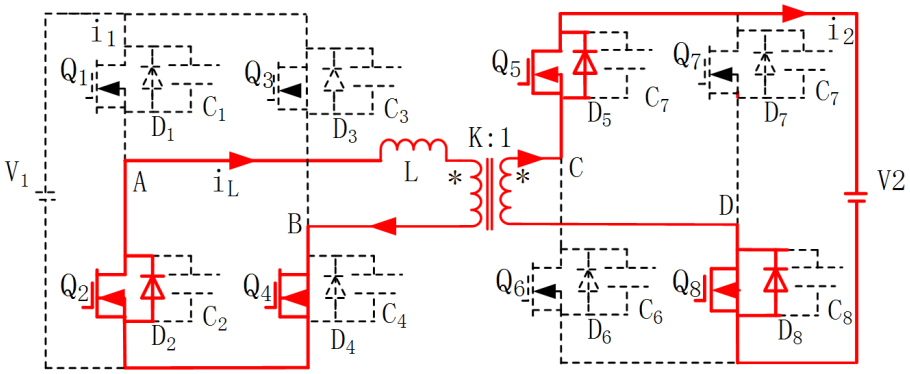

Figure 2.8: Operation of the DAB converter with ZVS at $[t_3, t_4]$.

Based on Fig2.3, the inductance current in one half cycle can be induced when $t_0 \leq t < t_2$

$$i_{(t)} = \frac{(1+k)V_1}{L}(t-t_0) - \frac{(D_{y1}+kD_{y1}+2kD_\phi-2k)V_1}{4Lf_s} \tag{2.4}$$

When $t_2 \leq t < t_3$, the inductance current can be calculated as

$$i_{(t)} = \frac{(1-k)V_1}{L}(t-t_2) - \frac{(k+2kD_\phi-1)V_1}{4Lf_s} \tag{2.5}$$

While $t_3 \leq t < t_4$, the expression of the inductance current becomes:

$$i_{(t)} = \frac{-kV_1}{L}(t-t_3) + \frac{(D_{y1}-kD_{y1}+2kD_\phi)V_1}{4Lf_s} \tag{2.6}$$

According to the Fig2.3 and [11], the input average power can be described as

$$P = \frac{kV_1^2}{8Lf_s}[1-(1-2D_\phi)^2-(1-D_{y1})^2] \tag{2.7}$$

The ability of power transfer is determined by D_ϕ and D_{y1}. The higher values of D_ϕ and D_{y1}, the higher power can transfer. When D_ϕ=1 and D_{y1}=0.5, the converter transfers the maximum power.

2.4 DC-DC

When the main 400V battery is going to charge the 13.8V Li-ion battery, the DC-DC will work to bring the voltage down. In this project, the DC-DC is designed as a full-bridge DC-DC converter with current doubler and synchronous rectification.

In this case, the secondary side of the dual active bridge, which is introduced in Section 2.3, will act as the full-bridge converter on the input side. At the output side, there are different available typologies that could be compared and selected from, full-wave and half full-wave rectification, full bridge rectifier and current doubler rectifier, etc. They are all able to work good for the scenario of low voltage and high current output. Among them, the current doubler(Fig.2.9) topology is first introduced and selected.

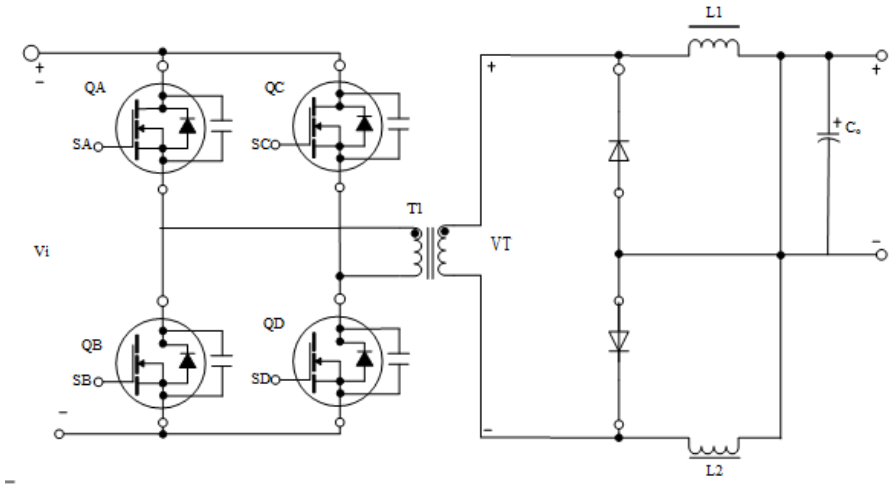

Figure 2.9: The topology of current doubler.

Compared to the most common used centre tapped full wave rectifier, the secondary side of the transformer only sees half of the output current with no center tapping needed. This makes the transformer to achieve a higher efficiency as well as an optimized and simplified structure. In contrast with the full wave rectifier, this structure only needs two diodes, not four. Instead, two inductors are applied. Although the number of the output filter inductors increases, it has a big advantage of reducing the size of each filter inductor[4][5]. In addition, the output ripple current is added together by the two inductor currents, which has a small current ripple as well as a fast response.

On the other hand, however, the diode voltage drops will be a high percentage of the output voltage. The loss in the rectifier diodes is quite high and hence limits the efficiency. Instead, synchronous rectification is a reasonable solution here. In terms of synchronous rectification, the MOSFETs will replace and behave as the diodes. When there is a need to turn on or turn off the diodes, the control signal SR1 and SR2 will be used to drive the MOSFET, which will make it possible to make the MOSFETs to work as diodes and realize rectification. The topology of a full bridge converter with a current doubler synchronous rectification of ideal components is shown in Figure.2.10.

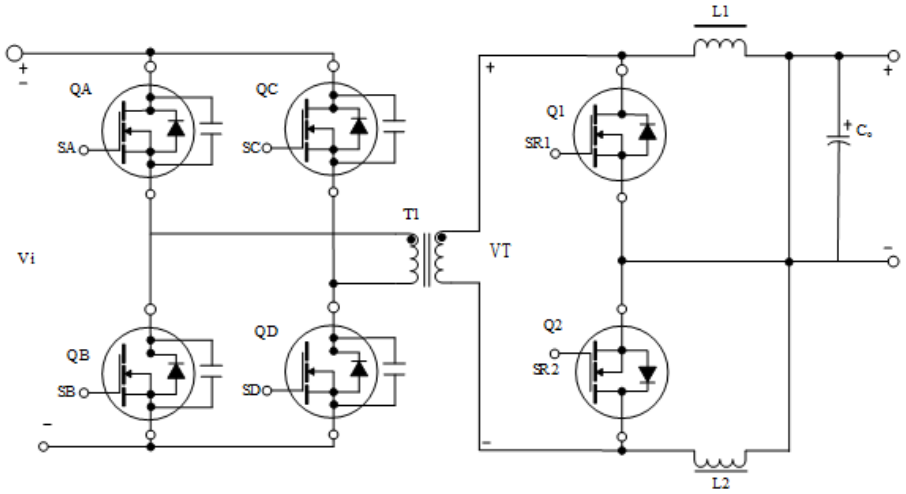

Figure 2.10: The full-bridge DC-DC converter with current doubler and synchronous rectifier.

2.4.1 DC-Dc switching pattern

The switching pattern of phase shift modulation, introduced in Section 2.3.1, is also a perfect widely used strategy to control the DC/DC converter. The switching pattern is shown in Figure2.11. Signals of SA,SB,SC,SD are used to control the MOSFETs on the transformer secondary side and SR1 as well as SR2 are the drive signal for the synchronous rectifier.

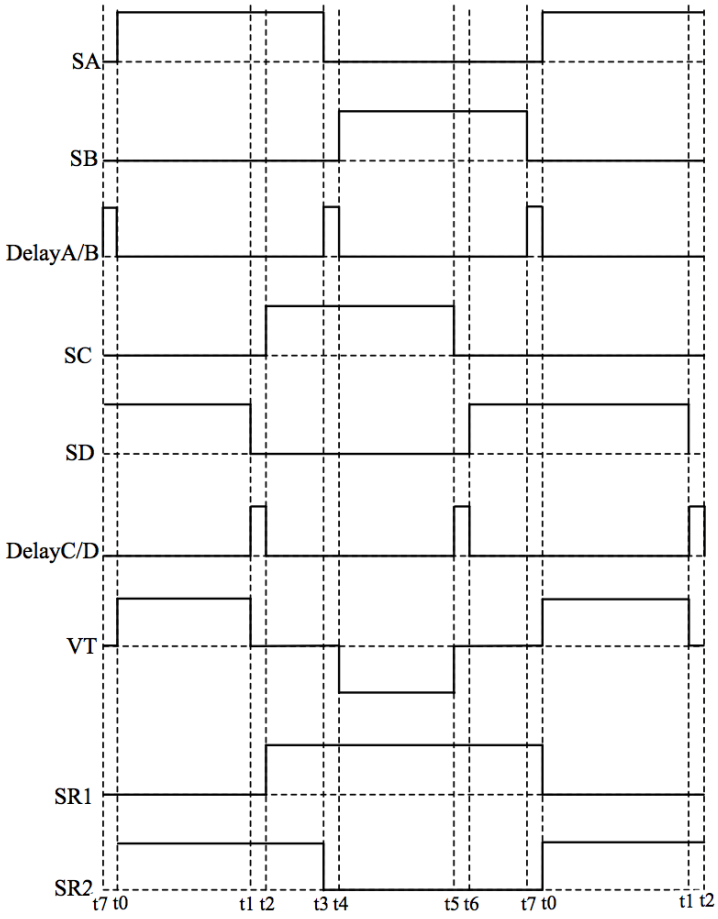

Figure 2.11: The switching pattern of Phase shift full bridge converter and current doubler.

For the DC-DC high voltage input side, the full bridge converter with phase shift strategy leads an almost 50% fixed-duty cycle to the four MOSFETs. Beside, there is a phase shift angle between the two leg driving signal, which is used to control the output voltage. There is a small blanking time between A/B and C/D, shown as Delay A/B and Delay C/D in Figure2.11 . This is to prevent the MOSFETs on the same leg from turning on simultaneously, which will lead to a short circuit and a destruction of the MOSFETs[7]. Besides, it will also work enable Zero Voltage Switching.

The low voltage output voltage of this topology will act as a buck converter. The MOSFETs will turn on and off to control the power transferred from the HV side. When the transfer voltage VT is positive, Q1 is turned off and Q2 is on. When VT is negative, Q1 is on and Q2 is turned off.

In terms of ZVS, the transformer leakage inductance will work together with the MOSFETs parasitic capacitance to realize soft switching of QA, QB, QC and QD. As the secondary side, the filter inductance and the parasitic capacitance of synchronous rectifiers will achieve ZVS.

2.4.2 Circuit operation

The circuit operation can be divided into eight time intervals. The switching analysis of the low power charging path will be discussed here following the control strategy shown in Figure2.11. To be specific, the $400V$ is input of the secondary transformer winding and $13.8V$ is the output of the tertiary side. And only the secondary and tertiary windings of the transformer will be described in the following schematics.

- **Timeframe** $t_0 - t_1$

  The first time interval operation schematic is shown in Fig.2.12.

  At the beginning time t_0 on the secondary side, QD has already turned on. The voltage over MOSFET QA is zero and QA starts to turn on as well. Hence the secondary current is flowing through Q1, transformer T1 side and QD. The power transfers from the secondary side to tertiary side. VT is positive.

  On the tertiary side, SR1 is off and SR2 is in on state. MOSFET Q2 will conduct and take all the flowing current so no current will flows through MOSFET Q1. The currents in L1 and L2 will flow in the same direction but two different paths. The current flowing through L1 will keep increasing due to the force transformer voltage VT. But L2 current will decrease with the freewheeling stored energy in L2.

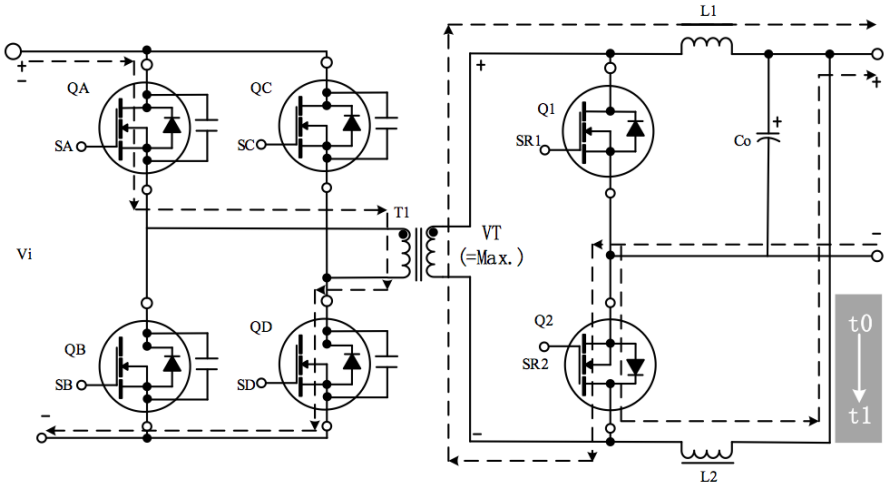

Figure 2.12: Schematic operation at time interval $t_0 - t_1$.

- **Timeframe** $t_1 - t_2$

  The operation schematic in this time interval is shown in Fig.2.13.

  In this designed topology, there will be a resonant inductance L_r on the secondary side, which results from the leakage inductance of the transformer. It will keep the current in transformer secondary winding flowing in the same direction. At t_1, QD is turned off. The stored energy in resonant inductance will force transformer current I_p to keep flowing of its value at t_1. The current will start to discharge the MOSFET

output capacitance the C_{OSS} of QC and charge C_{OSS} of QD and as shown in Fig.2.13. If I_p is adequate , the drain voltage of QD, and source voltage of QC, will resonate from Vi,max to zero. When they reach zero, the current I_p stops flowing through the C_{OSS} of QD. It turns on the body diode of QC and I_p keeps flowing[7].

Meanwhile on the tertiary side at the time instant t_1, the forced voltage on the secondary side is off and transfers voltage changes from the maximum value to zero. In this short time period, V_{DS} of Q1 reaches zero voltage and the body diode of Q1 will turn on. Since the secondary current Ip keeps almost the same value, the tertiary transformer side current will have almost the same value as at t_1. Therefore, the current of body diode Q1 will start at zero current and increase slowly. The diode current through Q1 will continue to flow through L1 as the third path.

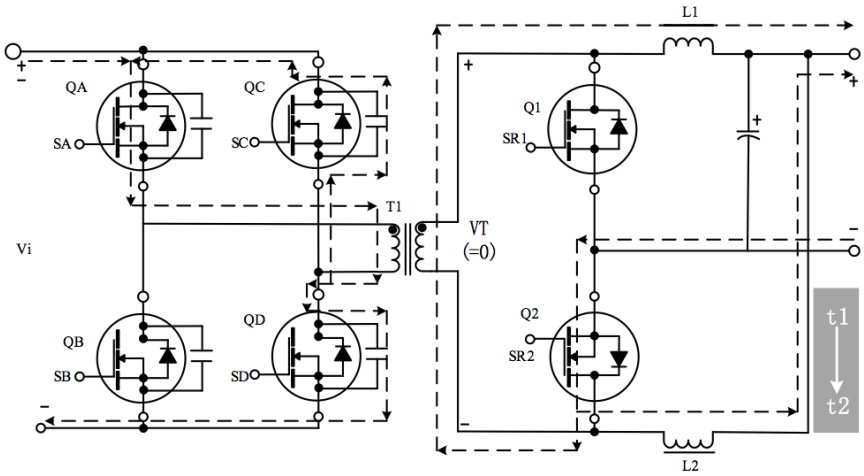

Figure 2.13: Schematic operation at time interval $t_1 - t_2$.

- **Timeframe** $t_2 - t_3$

  The operation schematic in this time interval is shown in Fig.2.14

  At t_2, QA is still on and QC starts to turn on. The current still flows through QA, however the current path through QC will changed form the the QC body diode to QC MOSFET As shown on the secondary side, the current will flow by QA, T1, and QC.

  On the tertiary side at time instant t_2 , SR1 turns the MOSFET Q1 on. Since the body diode of Q1 is already turned on, V_{DS} of Q1 is zero. zero voltage switching will be achieved during this turn on period. The third charging path will change from flowing through the Q1 body diode to the MOSFET Q1 instead. The other two charging path will be exactly the same within the timeframe $t_1 - t_2$.

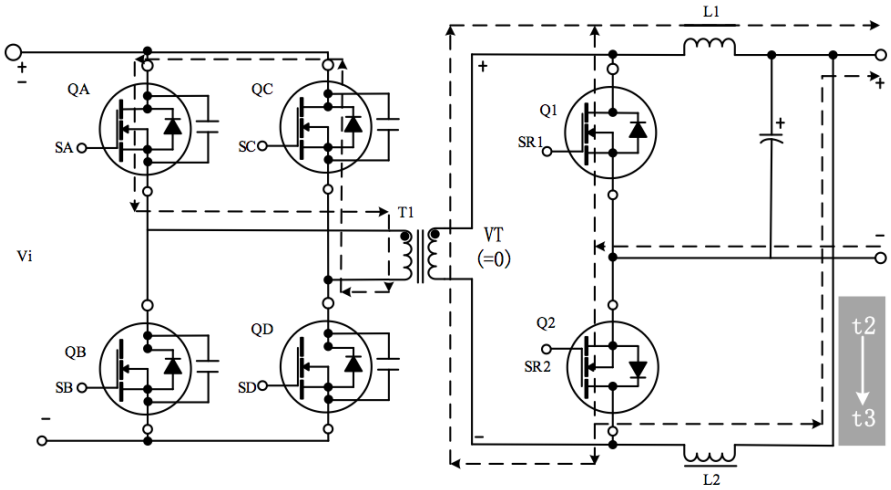

Figure 2.14: Schematic operation at time interval $t_2 - t_3$.

- **Timeframe** $t_3 - t_4$

  The operation schematic in this time interval is shown in Fig.2.15

  At time t_3, QA turns off. Similarly as in time period $t_1 - t_2$, the stored energy in the leakage inductance Lr will force I_p to keep flowing with its value at t_3, which will charge QA C_{OSS} however discharge QB C_{OSS} as shown in Fig.2.15. If I_p is adequate, the QA source voltage will resonate from Vi,max to zero. The ZVS transition will finish. After the QB drain voltage reach Vi,max, the current I_p stops flowing through the C_{OSS}. Instead the current turns into the QB body diode on and keeps flowing.

  At t_3 with ZVS, the QA source voltage is resonated from the maximum to zero voltage. In this period, the QB V_{DS} reaches to value zero therefore the body diode is turned on. The secondary current I_p still keeps the similar value, hence tertiary side current is almost the same as the current value at t_1. Therefore, the current of the body diode Q2 will take all the current flowing the MOSFET Q2 at t_3. The current path through MOSFET Q2 is shifted to the Q2 body diode. The other two paths are the same with the timeframe $t_2 - t_3$.

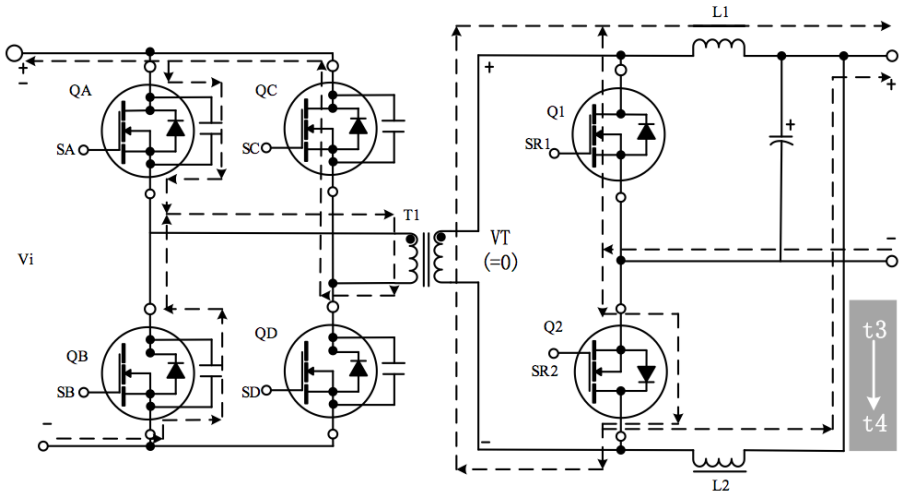

Figure 2.15: Schematic operation at time interval $t_3 - t_4$.

- **Timeframe** $t_4 - t_5$

  The operation schematic in this time interval is shown in Fig.2.16.

  At $t_4 - t_5$, QA and QD are off. QB is turned on together with the QC on state. The transformer secondary side current is flowing through QC, the transformer winding as well as QB as shown in Fig.2.15. The power transfers from the transformer secondary side to the tertiary side and will generate a negative VT as shown in Figure2.11.

  This time period is quite similar with the process in timeframe $t_0 - t_1$. On the tertiary side, SR1 is already on and SR2 is off. No current will flow through Q2 and all the transfer current is passing through Q1. The current will be separated into the two paths trough L2 and L3. The current flowing through the L2 will keep increasing due to the negative force transformer voltage VT. However the L1 current will decrease with the freewheeling stored energy in L1.

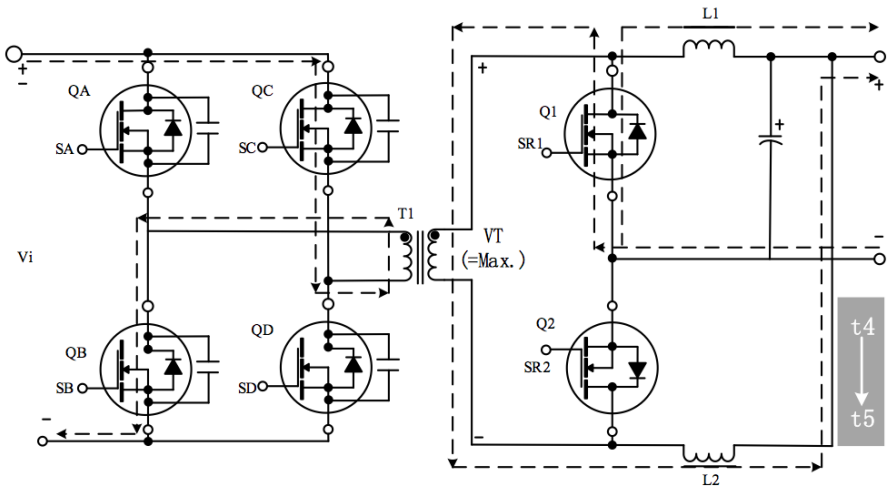

Figure 2.16: Schematic operation at time interval $t_4 - t_5$.

- **Timeframe** $t_5 - t_6$

  The operation schematic in this time interval is shown in Fig.2.17.

  At t_5, QC turns off and the other MOSFETs keep the same states. The stored energy of Lr forces Ip to keep flowing with its value at t5, which will lead to a start of charging the QC C_{OSS} and discharge QD C_{OSS}. If I_p is adequate as mentioned before, the voltage of the drain of QD, or the source of QC, will resonate from Vi, max to zero to achieve ZVS. After realizing ZVS, the current Ip stops flowing through the C_{oss} instead the QD body diode is turned on and Ip still keeps flowing through it.

  At t_5, the forced voltage VT will change to zero and the energy stops flowing now. Since V_{DS} of Q2 is reaching zero voltage in this period and the Q2 body diode is on. At the secondary side the current keeps almost the same value, the current of the tertiary side transformer is almost the same value as at t_5. As a result, the body diode current Q2 will increase slowly from zero. Together with the two existing current paths in the time period $t_4 - t_5$, the current through the Q2 diode and L2 behave as the third path.

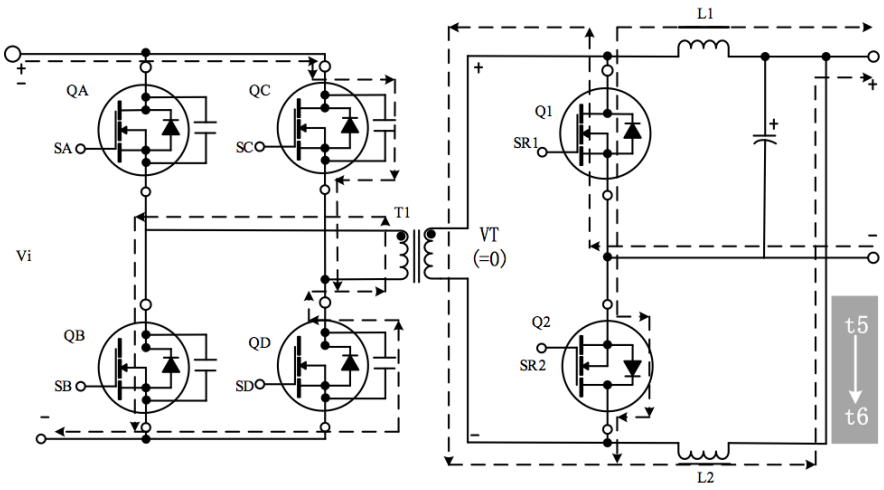

Figure 2.17: Schematic operation at time interval $t_5 - t_6$.

- **Timeframe** $t_6 - t_7$

  At t_6, QD starts to turn on. The secondary current will shift the current to the QD MOSFET from the body diode. As shown in Fig.2.18, the current keeps flowing through QB, the transformer, and QD with almost the same value.

  On the tertiary side, SR2 turns the MOSFET Q2 on. Since the Q2 body diode is on previously, the V_{DS} of Q2 is zero. ZVS occurs in the turn-on switching of Q2. Now the current is passing by MOSFET Q2 instead of the body diode. These other two current approaches are the same as mentioned for the time period $t_5 - t_6$.

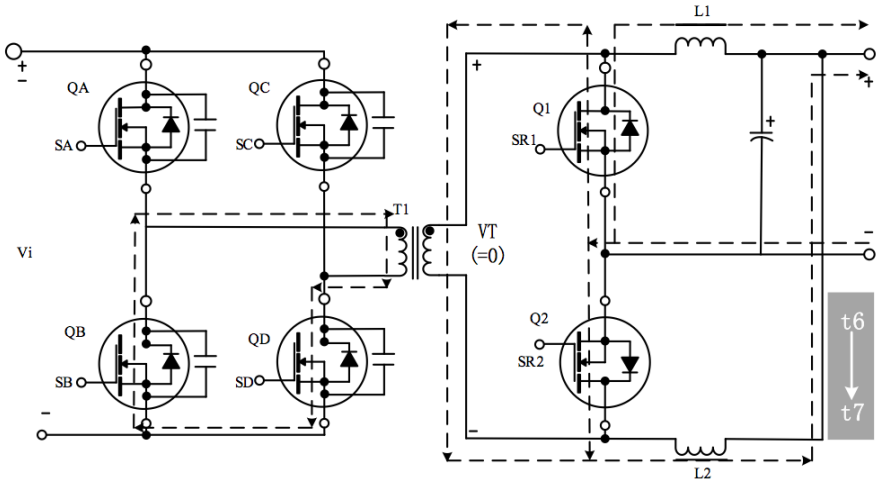

Figure 2.18: Schematic operation at time interval $t_6 - t_7$.

- **Timeframe** $t_7 - t_0$

  $t_7 - t_0$ is the last period of the repeated charging sequence. QB is off at t_7. The leakage inductance stored energy forces the current to still flow with its value at t_7, which will start to discharge QA C_{OSS} and charge QB C_{OSS} as shown in Fig.2.19. If I_p is adequate, the voltage of the drain of QB, or the source of QA, will resonate from zero to Vi, max. After the voltage of the drain of QB, or the source of QA, reaches Vi, max, the current I_p stops flowing through the C_{OSS}, instead turns on the body diode of QA and continues to flow.

  At t_7, the voltage of the QA source or QB source is resonated from the maximum value to zero voltage. In this short time, V_{DS} of QB will reach zero voltage and the body diode will turn on. Since the secondary side current keeps almost the same value, the transformer tertiary side is the same of the value at t_7. As a result, the body diode of Q1 will take all the current of the Q1 MOSFET at t_7. The charging path changed from the MOSFET Q1 to the body diode of Q1. And the other two current paths are the same as those in the time period of $t_6 - t_7$.

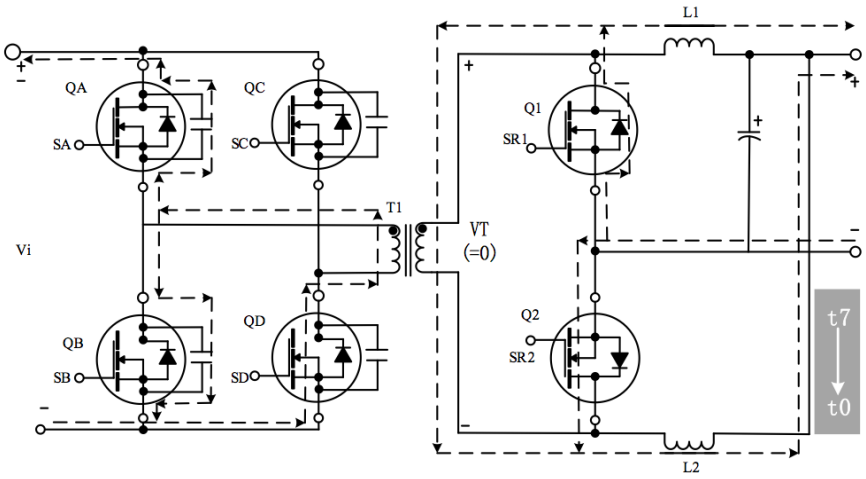

Figure 2.19: Schematic operation at time interval $t_7 - t_0$.

2.5 Transformer

The transformer plays a significant role in the converter design. On one hand, it has the function to transfer power, change voltage as well as make the isolation. On the other hand, it affects a lot of the converter volume and efficiency. Especially in this thesis' case, the three winding transformer will combine the OBC and DC-DC converter together to reduce volume. The inductive coupling between the primary and secondary windings can transfer the energy from the grid to power the HV battery. In addition to that, a third winding is added. By the inductive coupling between the secondary and tertiary side, it brings the high battery voltage down to the 12V load at the output for supplying auxiliary network loads. In this thesis work, the three winding transformer will be designed accordingly for the rated voltage and current. Also it aims to achieve higher efficiency with the new transformer structure.

The three winding transformer losses need to be considered carefully. The losses in a transformer are core loss and copper losses. The core loss strongly depends on the material that is chosen for the transformer core, which could be basically called hysteresis loss and eddy currents loss. In order to calculate core loss, the Steinmetz equation is introduced here.

$$P_v = k f_{sw}^a (\triangle B_{max})^b \tag{2.8}$$

where P_v is time average power loss per unit volume, f is switching frequency in kHz A and B is the peak flux density in T. K, a, b are material parameters. Hence, the total core losses can be decided as

$$P_{core} = P_v V_e \tag{2.9}$$

where V_e is the core volume.

Copper loss refers the losses generated when the current flows through the copper wires. When the three winding transformer is working, only two sides are active, we can calculate the copper losses of the OBC and separately.

First, one must determine the total resistance of the copper wires. Since the length of one turn could be found in the core shape datasheet, the total length of the copper wires can be defined with the help of turn numbers.

$$\begin{aligned} Lpri, winding &= L_{turn} N_1; \\ Lsec, winding &= L_{turn} N_2; \\ Lter, winding &= L_{turn} N_3; \end{aligned} \tag{2.10}$$

Secondly, the resistance of copper wires can be calculated.

$$\begin{aligned} R_1 &= \frac{\rho_{cu} Lpri, winding}{A_{1,bundle}}; \\ R_2 &= \frac{\rho_{cu} Lsec, winding}{A_{2,bundle}}; \\ R_3 &= \frac{\rho_{cu} Lter, winding}{A_{3,bundle}}; \end{aligned} \tag{2.11}$$

where ρ_{cu} is the copper resistivity. ρ_{cu} is temperature related. Usually, ρ_{cu} is $1.7 * 10^{-8} \Omega m$ in normal temperature. When the transformer is working, however, the temperature is much higher than 25°C. Hence °C is set to $2.02 * 10^{-8} \Omega m$ according to N87 datasheet.

The copper losses for OBC and DcDc can be quantified by the following expression.

$$\begin{aligned} P_{cu,highpower} &= R_1 I_{1,rms}^2 + R_2 I_{1,rms}^2; \\ P_{cu,lowpower} &= R_2 I_{22,rms}^2 + R_3 I_{3,rms}^2 \end{aligned} \tag{2.12}$$

Eventually, the maximum power dissipated in the transformer is figured out as

$$P_{total,OBC} = P_{core,OBC} + P_{cu,OBC} \tag{2.13}$$

$$P_{total,DcDc} = P_{core,DcDc} + P_{cu,DcDc} \tag{2.14}$$

2.6 Semiconductor losses determination

When talking about the semiconductor losses, it usually refers to switching and conduction losses. When the semiconductor is turned on and off, the losses is called switching losses. When it is conducting, conduction losses occur. The semiconductor voltage and current waveforms during one conduction period are plotted in Fig.2.20

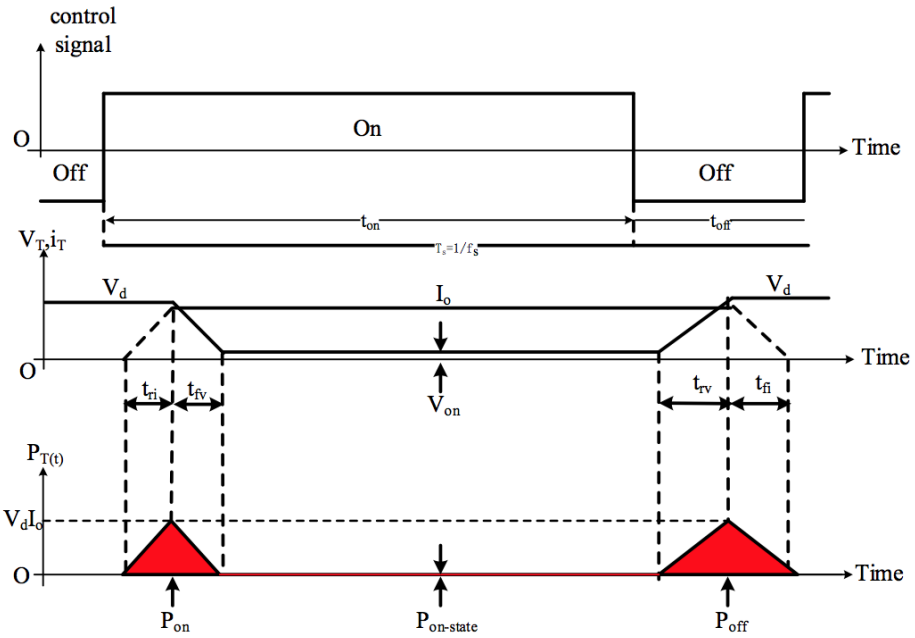

Figure 2.20: Semiconductor losses.

2.6.1 Switching losses

When the control signal is set to ON, it starts with turn on losses. As Fig.2.20 indicates, the voltage decrease from the max value to zero voltage and the current increase from zero to max voltage. One triangle is formed and marked red to show the power over the switch when turning on. t_{ri} is the rise time and t_{fv} is the turn on delay time. V_d is the voltage between gate d and s when the MOSFET turning on and I_0 is the current. Consequently the turn on losses is

$$P_{on} = V_d I_0 \frac{t_{ri} + t_{fv}}{2} f_s \tag{2.15}$$

As the turn off process, t_{fi} is the fall time and t_{rv} is the turn off delay. Similarly the turn off losses could be found as

$$P_{on} = V_d I_0 \frac{t_{fi} + t_{rv}}{2} f_s \tag{2.16}$$

2.6.2 Conduction losses

When the MOSFET is conducting, it will behave as a resister, which will lead to conduction losses. The conduction losses could roughly be calculated as

$$P_{on-state} = R_{don} I^2_{on(rms)} \tag{2.17}$$

Among them, R_{don} is the on-state resistance and the value could be easily got from the MOSFET datesheet. $I_{on(rms)}$ is the calculated RMS current during conduction.

In reality, however, there is one body diode in anti - parallel with the MOSFET in the switch module. It will the carry reverse polarity current. Besides, the diode usually starts conducting before the MOSFET turning on to prepare the zero voltage switching. Due to the forward voltage drop on the diode when the MOSFET is on-state, the conduction losses can be found,

$$V_{on-state} = V_{sd} + R_{don} I_{on(rms)} \tag{2.18}$$

$$\begin{aligned} P_{on-state} &= \frac{1}{T_s} \int_0^{DT_s} ion(V_{sd} + R_{don} I_{on}) dt \\ &= \frac{V_{sd}}{T_s} \int_0^{DT_s} i_{on} dt + \frac{R_{don}}{T_s} \int_0^{DT_s} i_{on}^2 dt \\ &= V_{sd} I_{on(avg)} + R_{don} I_{on(rms)}^2 \end{aligned} \tag{2.19}$$

For MOSFET V_{sd} is the forward voltage drop and can be found on the datesheet.$I_{on(avg)}$ is the calculated average current during conduction.

2.7 Topology overview

Figure.2.21 indicates the topology of the design which consists of the DC/DC part of OBC and DC/DC converter for low power charging system. In order to reduce the volume, the DC/DC for 12V battery charging is intended to integrate to the OBC part with a isolated three-winding transformer which is a replacement of two conventional transformers.

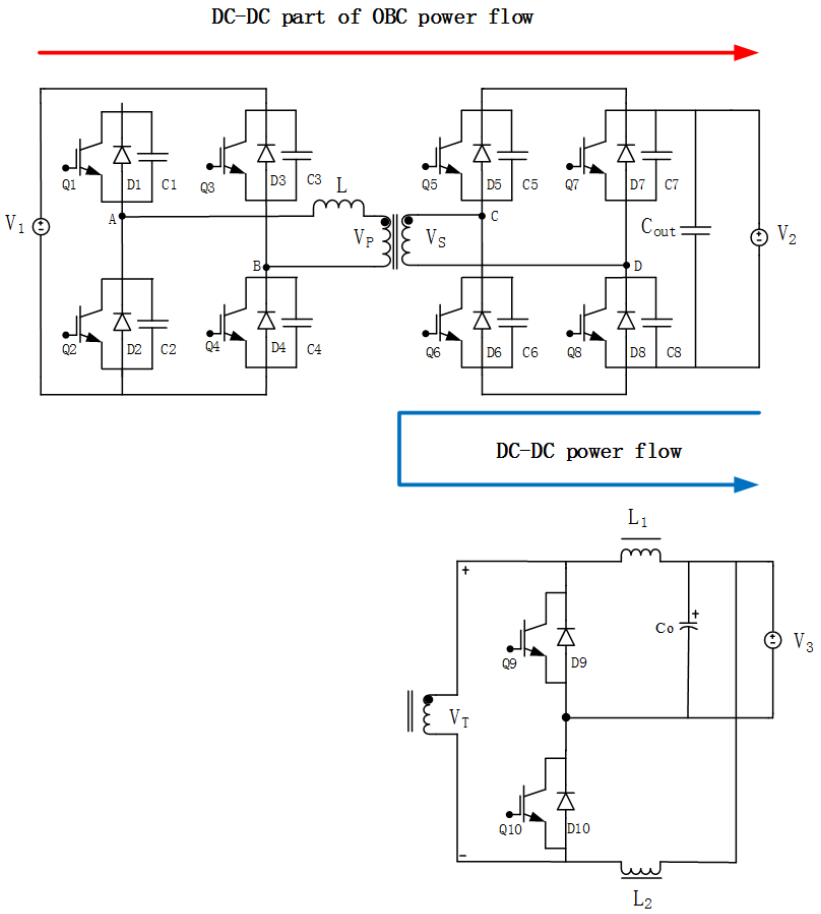

Figure 2.21: The topology of the combined OBC and DC-DC converter.

3

Case set up

3.1 Specification

As this thesis work has defined, the specifications for these two charging paths are shown in Table 3.1 and 3.2.

Table 3.1: Specifications of the high power charging path

Input AC phase voltage from grid V_i	$110V - 240V$
Maximum value of the input current from the grid	$16A$
AC line frequency	$50Hz$
Output power	$3.6kW$
Output dc voltage	$250V - 400V$
Output voltage ripple	Less than 2V(peak to peak)
Maximum output current	$11A$
Switching frequency of the DC-DC stage,	$100kHz$
Efficiency	over 94%

Table 3.2: Specifications of the low power charging path

Input dc voltage range,V_i	$330V - 420V$
Output power	$2.5KW$
Output dc voltage,V_o	$10V - 16V$
Output voltage ripple	peak to peak around $4\% - 5\%$
Output current	$182A$
Switching frequency, f_s	$100kHz$
Efficiency	over 90%

3.2 Passive components selection

3.2.1 DC-DC part of OBC resonance inductance selection

The leakage inductance add the external inductance L for ZVS achievement can be derived by the minimum principle of I_{Lrms_max}. The target is to decrease the losses by finding out a suitable inductance value which is corresponding to the optimized lower RMS current. According to the principle of DAB, the energy is transferred by the inductance between the power source and battery, the value of the inductance determines the ability of the power transfer. Hence, the minimum value of the maximum power transfer must be large than the rated power.

$$k_{min}\frac{V_1^2}{8Lf_s} = 0.66 \times \frac{400^2}{8 \times L \times 10^5} \geq 3600 \tag{3.1}$$

$$\Rightarrow L \leqslant 36.67\mu H \tag{3.2}$$

There is a relation between the inductance L and the maximum rms value of the inductance current I_{Lrms_max}. This can be observed from Fig3.1, where there is an optimized L making I_{Lrms_max} to be the minimum value, which means $L = 21.966\mu H$ and $I_{Lrms\_max} = 16.147A$. The inductance value is used for realizing the ZVS operation with the parasitic output capacitance of the semiconductor.

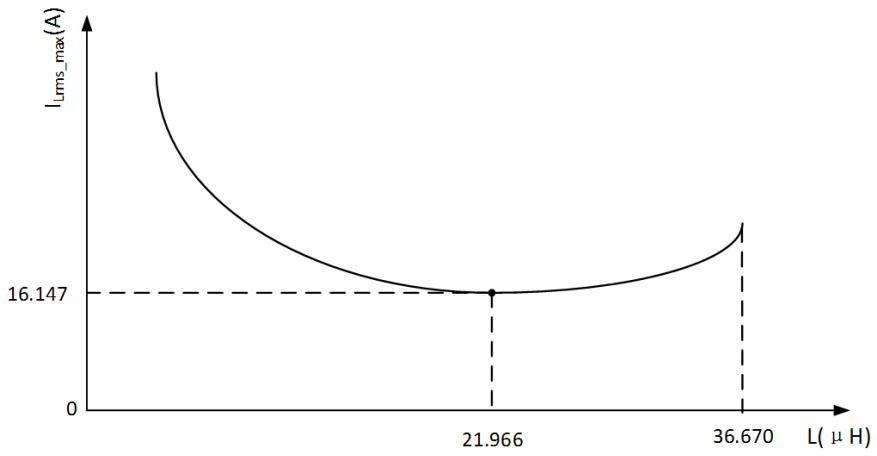

Figure 3.1: The waveform of I_{Lrms_max} corresponding with L.

3.2.2 DC-DC Passive components selection

The filter inductance play an important role in the current doubler design. It mainly affects the output current ripple. The output current I_0 is the sum up of the current flowing these two inductance I_{L1} and $I_{L1}(I_0 = I_{L1} + I_{L2})$. Hence the filter current will cancel some ripple. Here a cancel coefficient K is set to present the relationship between Δi_0 and Δi_L. Δi_0 is the output current ripple and Δi_L is the inductance current ripple.

$$\Delta i_0 = K\Delta i_L \tag{3.3}$$

where,

$$\Delta i_0 = \frac{(1-D)TV_0}{L_0} \tag{3.4}$$

$$\Delta i_L = \frac{(1-\frac{D}{2})TV_0}{L_0} \tag{3.5}$$

As a result, one can calculate,

$$K = \frac{\Delta i_0}{\Delta i_L} = \frac{1-D}{1-\frac{D}{2}} \tag{3.6}$$

$$\Delta i_0 = (1-D)\frac{V_0}{2L_f f_s} \tag{3.7}$$

Consequently, when $D = 1$, the out put current ripple will be zero. To decrease the filter inductance, the best situation is to let D to be near 1.

In this design, the duty cycle of DC/DC converter at the rated voltage is

$$D = \frac{2V_0 N}{V_{in}} = 0.64 \tag{3.8}$$

The cancel coefficient K is

$$K = \frac{1-D}{1-D/2} = \frac{1-0.64}{1-\frac{0.64}{2}} = 0.53 \tag{3.9}$$

According to the max current ripple and K, the output inductor ripple can be calculated as

$$\Delta i_L = \frac{\Delta i_0}{K} = 33.7A \tag{3.10}$$

Accordingly, the output filter inductor is

$$L_f = L_1 = L_2 = \frac{V_0(1-\frac{D}{2})}{\Delta i_L f_s} = 2.8\mu H \tag{3.11}$$

The output filter capacitance C_f mainly affects the output voltage ripple. If the filter capacitance is quite small, there be large voltage ripple. By comparison, the large output capacitance will lead to a big package volume. It is of great importance to choose the appropriate capacitance. The following relation must be fulfilled as

$$C_f = \frac{V_0}{8L_f(2f_s)^2\Delta V_{opp}}(1-\frac{V_0}{V_{in}/n}) \tag{3.12}$$

The output capacitance is selected to $200\mu F$

3.3 Operation frequency

High frequency power conversion systems are attracting more and more attentions in industry for high power density, reduced weight, and low noise without compromising efficiency, cost, and reliability[10]. To study the suitable operation frequency, the losses and the volume of the transformer have been investigated under different frequency. Since the losses in the transformer increases obviously with a nearly saturated flux density under 100kHz, and the switching loss of the converter rises rapidly above 100kHz. In this case, 100kHz is chosen as the switching frequency.

3.4 Component selection

3.4.1 Semiconductor selection

The transistor as switch plays a crucial role in the charging system with respect to switching speed and power loss. Nowadays, IGBTs and MOSFETs are widely used in electrical systems for PHEVs. For the low switching frequency(less than 50kHz) and high rated voltage, the IGBT is probably the best choice. But for the higher switching frequency, the MOSFET is better than the IGBT. According to the design specification, the operating frequency is 100kHz and voltage range is about 10V to 400V. So, the best transistor is probably the MOSFET in this supply range.

For the high power charging path, the withstanding voltage across the transistor on the primary side of DAB is equal to the input voltage $V_1 = 400V$, the voltage of the secondary side for the transistor is the upper limit of the battery voltage $400V$. The peak current is of the transistor on the primary side is about 24A based on calculation from the (2.6). For choosing the appropriate rating for the semiconductors, the voltage and current safety margin should be kept for the transistors. So the IPW65R048CFDA from Infineon is chosen for being the semiconductors on the primary side.

The IPW65R048CFDA from Infineon is an automotive qualified technology with a integrated fast body diode on the market. Its rated voltage reaches 650V which meets the suitable safety margin. And from the data sheet, the maximum conduction current is $63.3A$ at $25\ ^\circ C$ and $40A$ at $100\ ^\circ C$.

The same procedure is carried out on the secondary side. Since the withstanding voltage of the MOSFET is also 400V and the turns ratio is 0.8, which means that the current is almost the same as the primary current. So the IPW65R048CFDA from Infineon is selected for both the primary and secondary sides in high power charging path.

Still the same procedure is conducted for the MOSFETs used for the tertiary winding side, but the ratings are different. The peak voltage they need to stand is $40V$. For the peak current, the number is approximately $200A$. According to the procedure mentioned before, IRFP2907 is selected. IRFP2907 is an automotive MOSFET from International Rectifier. It is designed for 42 volts automotive electrical systems. Its rated voltage can reach to $75V$ and the maximum conduction current is $209A$.

3.5 Transformer design

The three winding transformer design plays an important role in this master thesis. This part will go through the transformer design procedure and how to choose the best transformer according to the transformer losses and its working flux density.

3.5.1 Turns ratio determination

To determine the turns ratio of the three windings transformer, the turns ratios between $N1/N2$ and $N2/N3$ needs to be figured out separately, then the general relationship could be found.

When the input voltage stays at a lower level, the transformer could still make the output voltage stay at the rated value. To start with the high power charging path, the voltage of the secondary side is as V_T. The maximum duty cycle on the secondary side is D_{smax}. Hence, the minimum voltage should be

$$V_{smin} = \frac{V_T}{D_{smax}} \tag{3.13}$$

The turn ratio is determined as

$$\frac{N_1}{N_2} = \frac{V_{in}}{V_{smin}} \tag{3.14}$$

Similarly, the turns ratio of $\frac{N_2}{N_3}$ can be settled using the same procedure.

3.5.2 Core Design

Nowadays, a lot of magnetic materials and structures are widely used in industry. They differ by losses per unit, prices, recommended operational frequency, magnetic properties, density etc. There are three main groups of magnetic core used today. They are ferrite cores, metal alloy tape-wound cores and powdered metal cores. Among them, ferrite cores, are selected due to their standard working high frequency ability. Ferrites have been known for a long time. They are ceramic materials which mostly consist of iron oxide with such additives as oxides or carbonates of manganese and zinc or nickel and zinc. A ferrite core has the feature of a low coercivity. Hence they are named as "soft ferrites" which means the material's magnetization can easily reverse direction instead of dissipating much energy (hysteresis losses). Due to the different iron oxide contents, the ferrite core has different types such as N82, N87, N92 and so on.

When the core material is decided, a core shape must be decided. One important condition is that the window area of the transformer must be large enough to fit the three windings together inside. Here the E series is choose due to its large window area, Besides, the winding is also expected to have a larger contact with the air, which will be a benefit for cooling. To be specific, EE, EC, ETD are all belong to E series cores. Among them, ETD core is selected since its dimension is optimized for a better transformer efficiency. The one turn length of ETD is smaller than that of EE and EC core. So the winding resistance is minimized. Consequently, copper losses will be less and it will lead to a lower temperature raise.

Basing on the products provided by the supplier of TDK, the ETD core has two different ferrite materials. One is N87 and the other is N97. N87 is the standard transformer material when the transformer is working under 500kHz. Due to its lower price and lower losses, N87 is a better choice. It is ferrite core with base material of MnZn. The peak flux density it can withstand is 0.39T.

A conventional design procedure is defining the number of turns, calculating flux levels and checking whether they fit in the core. When determining the turns number according to the turns ratio, one must make sure the core would not be saturated since the number of primary turns also affects the peak flux density $\hat{B}_{core}$ in the core. As a result, it can start the primary turn number determination based on the working flux with help of Faraday's Law,

$$e(t) = N\frac{d\phi}{dt}A_m \tag{3.15}$$

$$\Rightarrow V(t) = N\frac{dB}{dt}A_w \tag{3.16}$$

$$B = \hat{B}\cos(wt) \Rightarrow V_1(t) = N_1 A_w \frac{d\hat{B}}{dt}\cos(\omega t) \tag{3.17}$$

$$\Rightarrow V_1 = N_1 A_w \omega B \sin(\omega t) \tag{3.18}$$

$$\Rightarrow V_1 = N_1 A_w \omega B_{core} \tag{3.19}$$

Since the magnetic flux can be decided by

$$\phi = A_w \hat{B}_{core} \tag{3.20}$$

To explain, V_1 is the primary side voltage which is varying with time. A_w is the core effective area and $\frac{d\phi}{dt}$ is the time derivative of the magnetic flux in the core.

Combining 3.20 and 3.17, the following relation is found

$$\int_0^{DT_s} V_1 dt = N_1 A_w \int_{-B_{core}}^{B_{core}} dB \tag{3.21}$$

When there is an active power transfer through the transformer, it will generate the voltage V_1 applied over the primary side. Besides, this voltage will create the flux density in the transformer, which will be changing from negative to positive peak flux density every period.

In 3.21, it can be seen that the flux density highly depends on the input voltage applied on the transformer. In other words, if the duty cycle DT_S is changing, the peak flux density in the core $\hat{B}_{core}$ or N_1 will also be changing accordingly. To define the appropriate transformer core, the maximum input voltage and the maximum duty is considered. Hence the turn can be found by the expression

$$N_1 = \frac{V_{d,max} D_{max} T_s}{2 A_m \hat{B}_{core}} \tag{3.22}$$

If the number of turn is determined, the equation can be also used to calculate the peak flux density.

$$\hat{B}_{core} = \frac{V_{d,max} D_{max} T_s}{2 A_m N_1} \tag{3.23}$$

3.5.3 Winding Design

To calculate the cross - sectional area of the wiring, the RMS current values when the three winding transformer working at the nominal load needs to be calculated first. Due to the operational high frequency in the charging system, Litz wire is suggested as to increase the conductor area while maintaining a low skin effect as well as low proximity losses. Tens, hundreds, or more strands of small-gauge insulated copper wire are bundled together, and are externally connected in parallel. These strands are twisted, or transposed, such that each strand passes equally through each position inside and on the surface of the bundle. This prevents the circulation of high-frequency currents between strands. To be effective, the diameter of the strands should be sufficiently less than one skin depth. Also, it should be pointed out that the Litz wire bundle itself is composed of multiple layers.[9]

Considering the thermal issue in this design, the current density is chosen as 4.5 A/mm^2. Next, the cross-section of each winding can be calculated based on the RMS current and the current density,

$$A_{bundle} = \frac{I_{RMS}}{J} \tag{3.24}$$

where A_{bundle} is the total area of each winding and J is the current density with the value of 4.5 A/mm^2.

In general, the maximum single wire diameter should be smaller or equal to nearly a third of skin depth,

$$d = \frac{1}{3}\delta \tag{3.25}$$

d is the diameter of one single wire and the skin depth $\delta = \frac{7.5}{\sqrt{f}} = 0.2377mm$ at $T = 100°$.

Now the number of strands in each winding can be determined by

$$A_{strand} = \frac{A_{bundle}}{\pi r^2} \tag{3.26}$$

where r is the radius of the single wire.

Finally, using the data information from the Litz wire supplier called Elektrisola to check which series of Litz wire matches the design according to the calculation above. In this design, the copper fill factor is assumed to be $K_{cu} = 0.45$. Then the winding area equation related with K_{cu} is achieved.

$$A_{winding} = \frac{A_{1,bundle} N_1 + A_{2,bundle} N_2 + A_{3,bundle} N_3}{K_{cu}} \tag{3.27}$$

where the $A_{winding}$ is the window area of the core and N_1, N_2, N_3 are the transformer turns.

4

Results and analysis

4.1 Topology simulation results

The total topology with selected MOSFETs is shown in Fig.4.1.

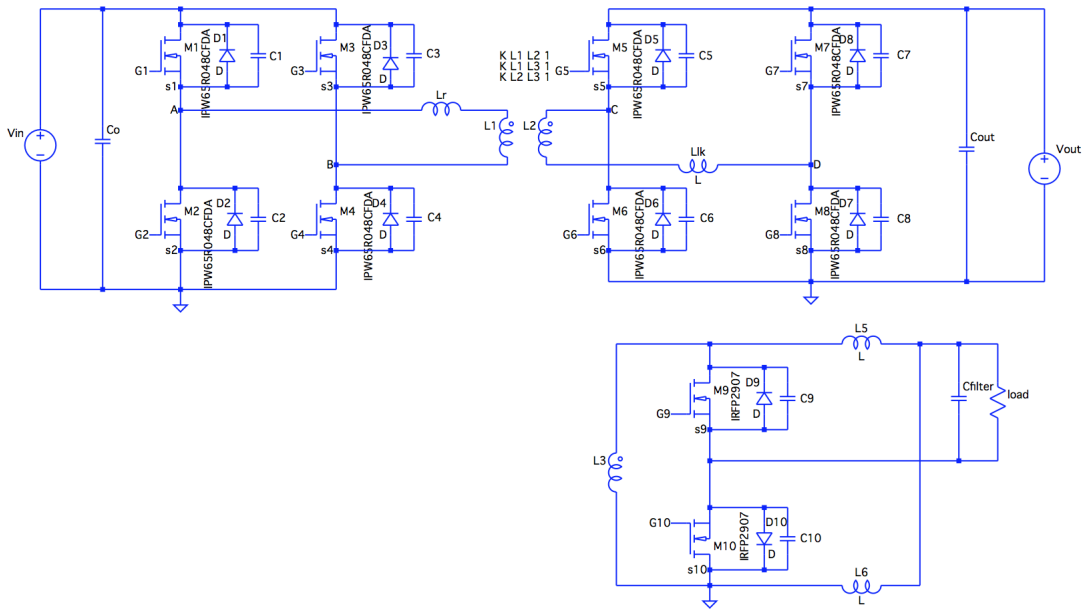

Figure 4.1: Dual active bridge converter and current doubler synchronous rectification.

In this section, the high power charging path with a dual active bridge structure and the low power charging path with current doubler topology will investigated separately. Both of the models are set up and simulated in LTspice. The parameters of the components are taken from the data sheets that were mentioned before. And the MOSFET's model are also taken from the Infenon supplier. In this model, MOSFETs are defined by the on-state resistance $R_{DS(on)}$, the forward voltage drop V_f, the parasitic output capacitance and the embedded body diode.

4.1.1 OBC charging path simulation and analysis

For the high power charging path, the simulation results of the Dual active bridge converter are presented. On the primary side, one voltage source with $400V$ acts the output of the interleaved boost converter and on the secondary side, a voltage source with a series resistance is used to imitate the battery model in simulation. To decrease the oscillation, the turn-off pure capacitive snubber circuit is added in the design.

The simulation setup is according to the one introduced to Chapter 3.3.1. The duty cycle of each switch is selected to be less than 50% so as to achieve zero voltage operation during the switching transient. The drive signal for the switches are marked in blue colour and the voltage waveform over each switch is shown as red colour in simulation. According to the simulation and the obtained waveforms, ZVS is successfully achieved both on the primary side and the secondary side, which are shown from Figure 4.2 to Figure 4.7. It can be clearly seen that the switch voltage for each switch goes up after the gate signal reaches zero during turn-on transition and the switch voltage decreases to zero before the gate signal increases during a turn-off interval. To realize the soft switching operation, the transistor is modeled with an anti parallel diode, a parasitic capacitance, and the sum of leakage inductance with an external inductance.

For instance on the primary side, when the switch Q1 turns off, the inductor current will charge the parasitic capacitance C1 and discharge the parasitic capacitance C2 of Q2 until the voltage of C2 reaches zero. Then the current will flow through the body diode D2. After that, the switch Q2 can be turned on at zero voltage and the inductor current will freewheel both though the switch and the diode until the current changes into the positive direction.

The other switches operate followed the same principle that explained in detail on chapter 3.3.1. To achieve ZVS operation, the stored energy in the inductor must be large enough to fully charge and discharge the parasitic capacitance from zero to the switch voltage and vice verse.

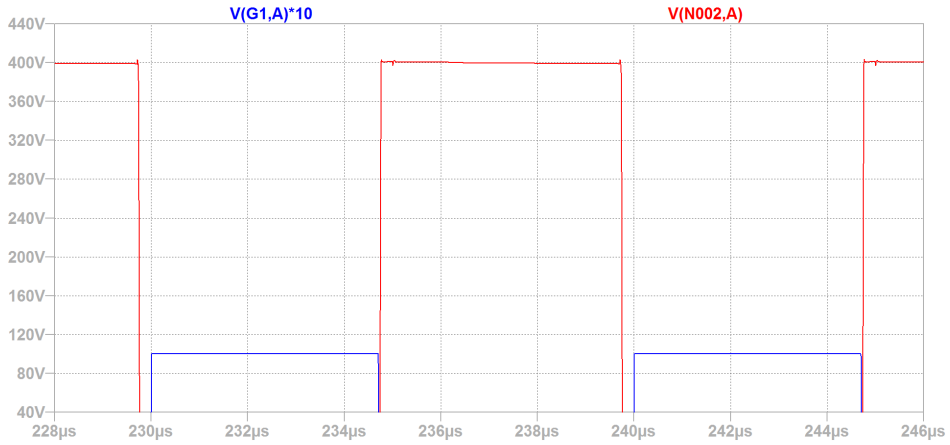

Figure 4.2: ZVS switching for transistor Q1 of DAB.

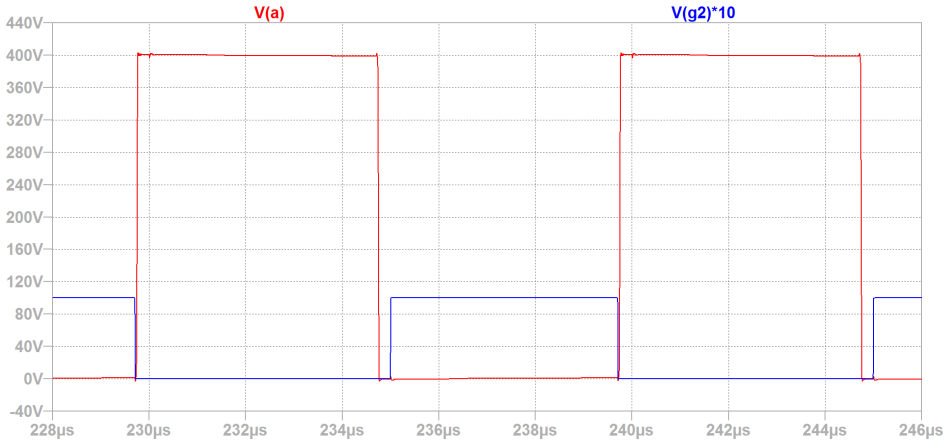

Figure 4.3: ZVS switching for transistor Q2 of DAB.

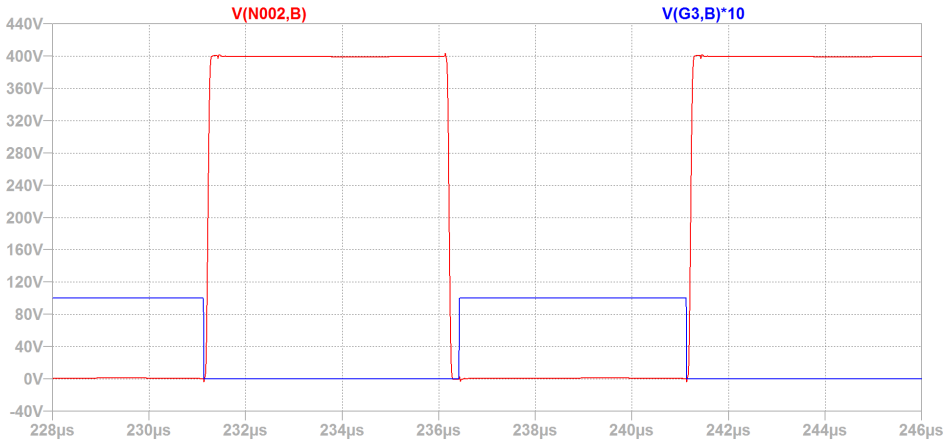

Figure 4.4: ZVS switching for transistor Q3 of DAB.

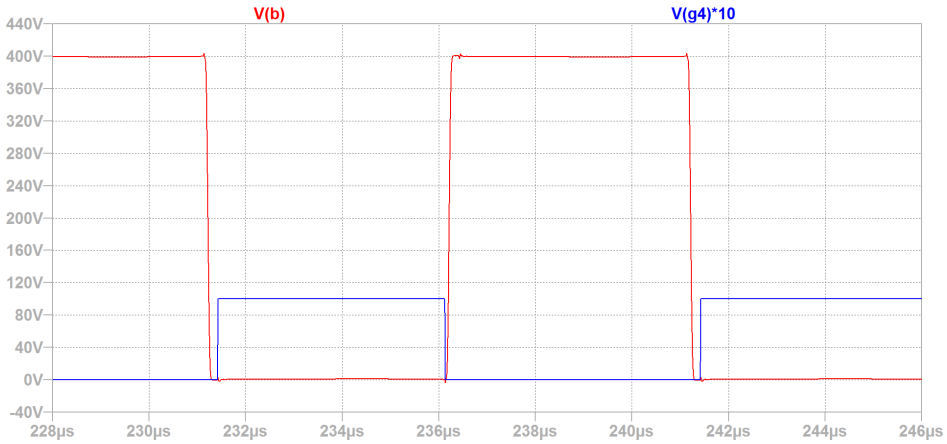

Figure 4.5: ZVS switching for transistor Q4 of DAB.

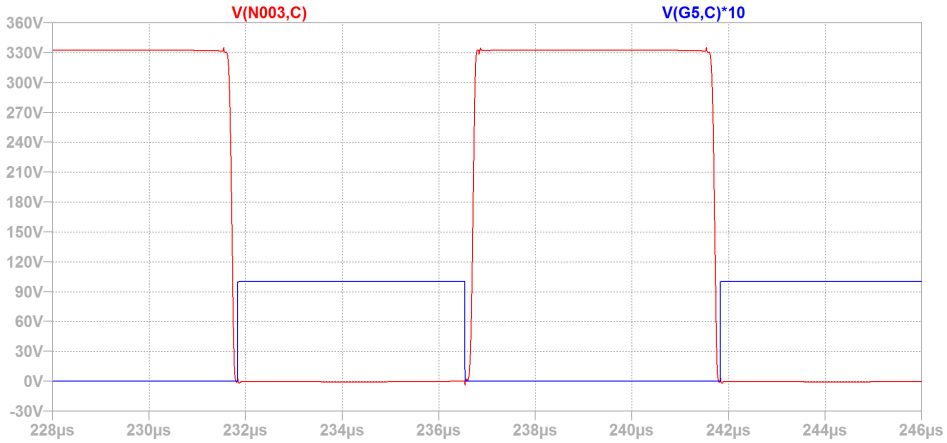

Figure 4.6: ZVS switching for transistors Q5 and Q8 of DAB.

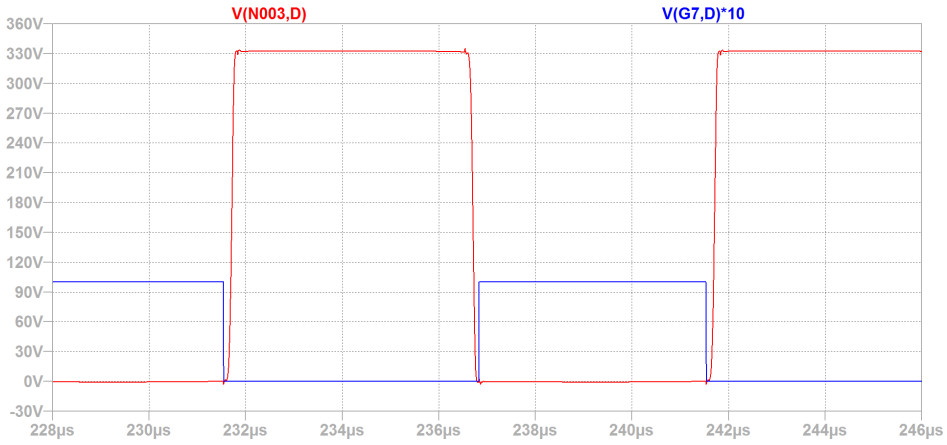

Figure 4.7: ZVS switching for transistors Q6 and Q7 of DAB.

Figure 4.8 and Figure 4.9 show the simulation results of the transformer voltages on primary and secondary side. Based on the phase-shift control, the inner phase-shift ratio on the primary side is adding to expand the ZVS range. In this switching pattern, the voltage on the primary side is becoming a three-level waveform while the voltage on the secondary side is a two-level square waveform. During the time intervals of the zero voltage of the three-level waveform, the back-flow power is zero which means the circuiting power decreases.

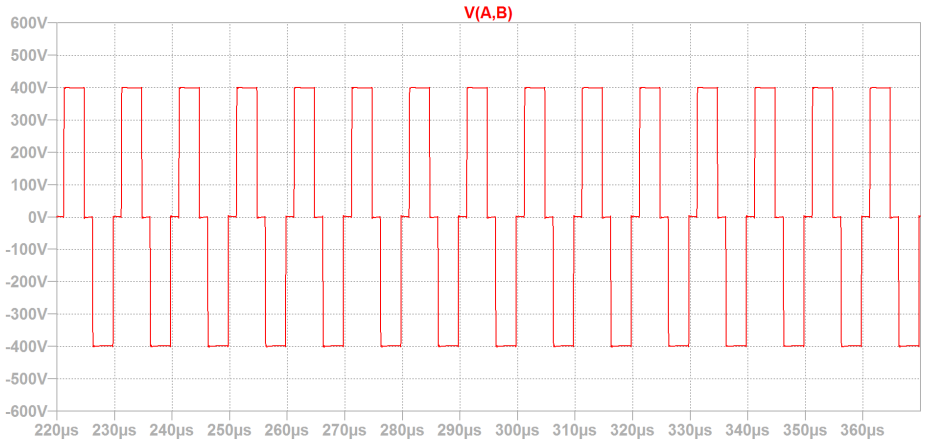

Figure 4.8: The voltage on the primary side of the transformer in DAB.

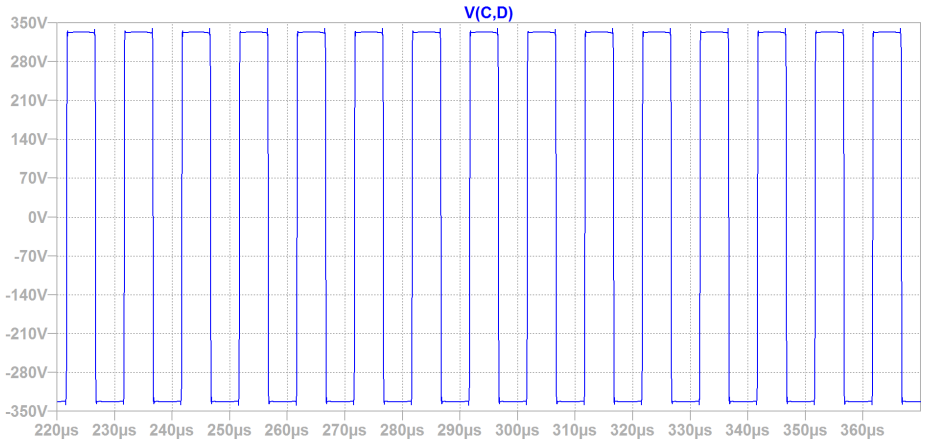

Figure 4.9: The voltage on the secondary side of the transformer in DAB.

The output voltage and output current are shown in Figure 4.10, and from the simulation result it can be seen that, the voltage ripple is less than 2V due to the output filter.

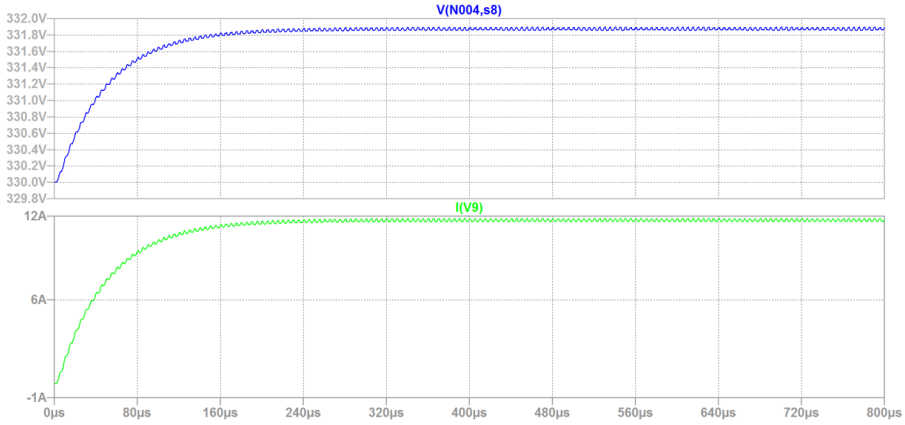

Figure 4.10: The output voltage and current of the OBC.

4.1.2 DC-DC topology simulation and analysis

For the DC-DC phase - shift full bridge converter and current doubler synchronous rectifier topology, the simulation parameters is set according to the Chapter.3.2.2. In this chapter, the simulation results and waveform will be covered and analyzed.

First, the drive signal for the four switches on the secondary side is set according to Fig.2.11. The waveform is shown in Fig.4.11. The blue and magenta are the drive signal for QA and QB. And red and green are to drive MOSFET QC and QD.

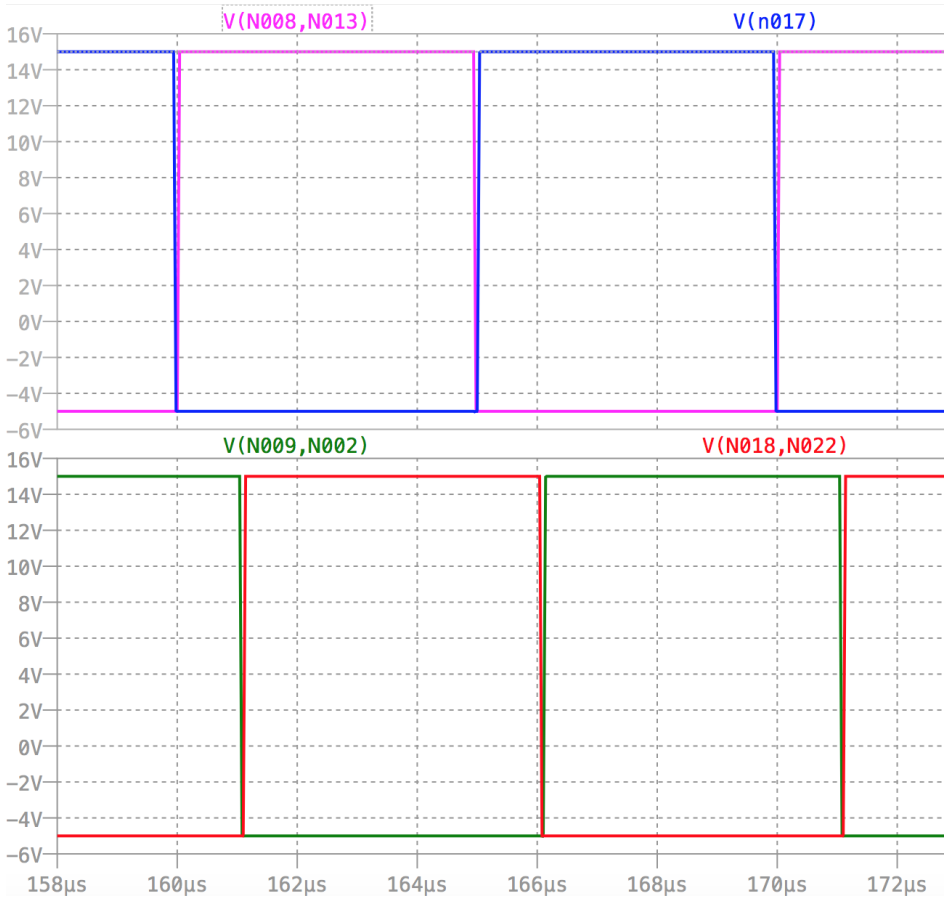

Figure 4.11: Drive signal for MOSFETs .

It can be seen that a switching frequency of $100kHz$ is applied ($T = 10\mu s$). The duty cycle is chosen to be slightly lower than 50%. Therefore, the blanking time between the switches has the ability to prevent short-circuit of one leg. There is also a phase shift between leg A/B and leg C/D. This will help to control the transformer primary side voltage.

The voltage and current behavior analysis is shown in Fig.4.12. In subfig 3, the green line refers to the transformer secondary side voltage and the purple refers to the current. It is seen that when MOSFET QA and QD are both conducting, the transformer will transfer the positive voltage from the secondary side to the tertiary side displayed as the positive green voltage around $330V$. Similarly, when QB and QC are conducting, it will transfer the negative voltage to the tertiary side as the $-330V$ transformer primary output voltage. With

the energy flowing, the current will increase doing the non-zero voltage period. When QA and QC, or QB and QD are conducting, as the phase shift happens, there will be no power flowing through the transformer. It is indicated as the zero voltage in the 4.12. The current is decreasing in the same time period.

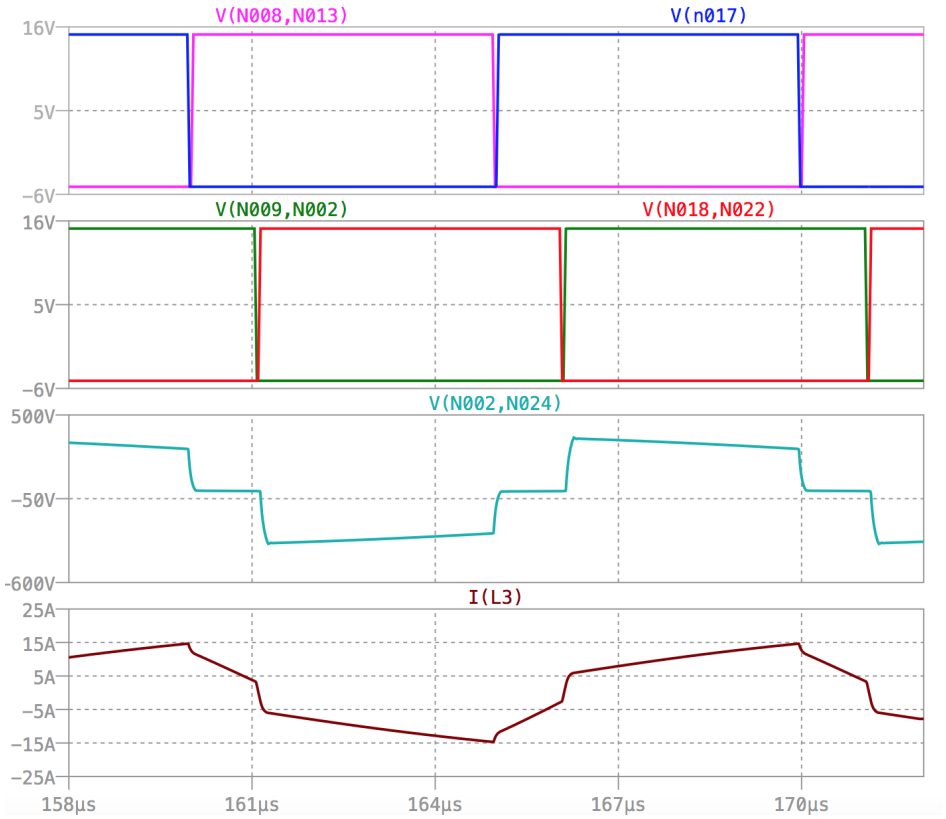

Figure 4.12: Voltage and current behavior analysis in the secondary transformer side .

Regarding the ZVS achievement on the DC-DC full bridge converter, it is found to work very well using simulation. The operation can be seen from Fig.4.13 - 4.14. The blue curve is the gate-source voltage and red is drain source voltage. For each MOSFET, it is clearly shown that when U_{ds} has already reached zero, U_{gs} would begin to rise. There is no overlap and ZVS is achieved, which reduces the full bridge switching losses.

Figure 4.13: MOSFET QA zero voltage switching.

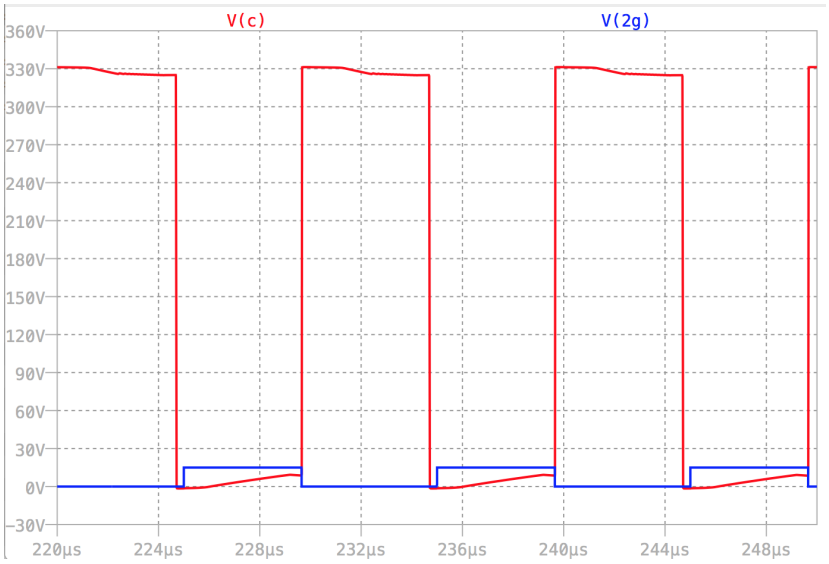

Figure 4.14: MOSFET QA zero voltage switching.

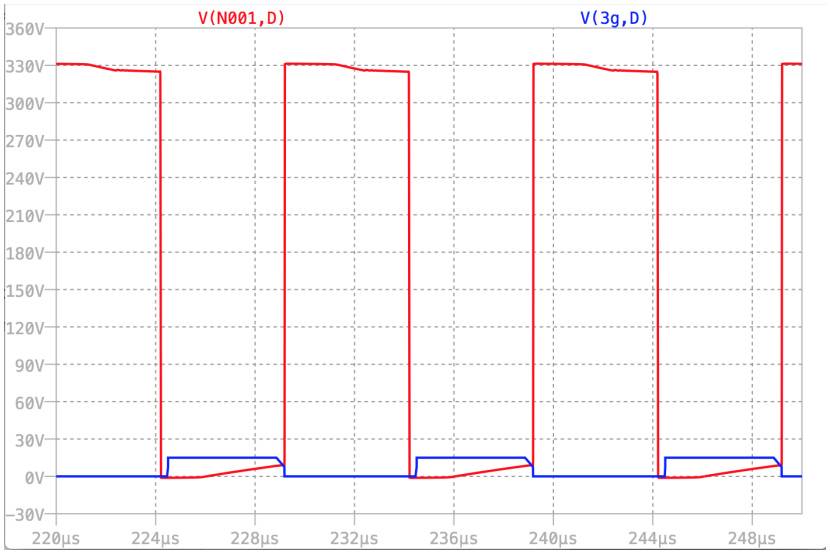

Figure 4.15: MOSFET QA zero voltage switching.

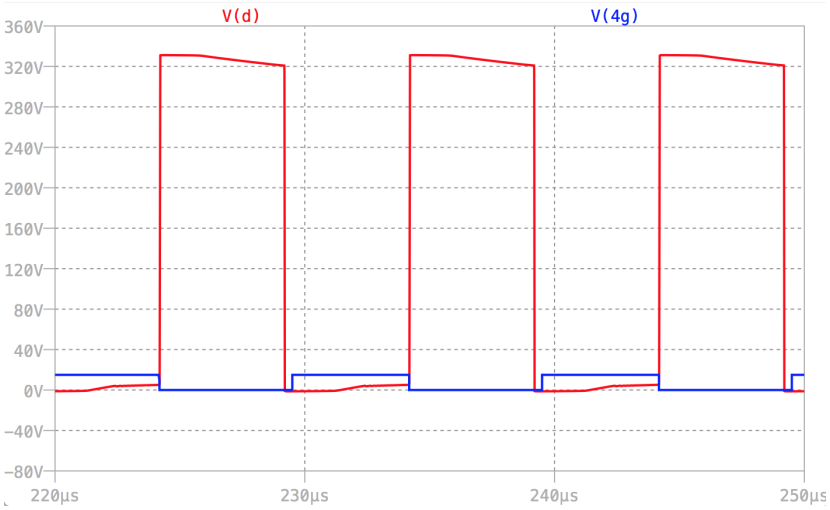

Figure 4.16: MOSFET QA zero voltage switching.

The synchronous rectification current doubler topology is implemented on the third side of the three winding transformer. The signal operation to SR1 and SR2 are shown in Fig.4.17. The green curve stands for the drive signal of MOSFET SR1 and the red curve is for the drive signal of MOSFET SR2. The synchronous rectifier behaves by following the power transferred from the transformer primary side. It can be seen that when transformer voltage is positive, MOSFET SR1 is turned off. By contrast, if VT is negative, MOSFET SR2 is turned off.

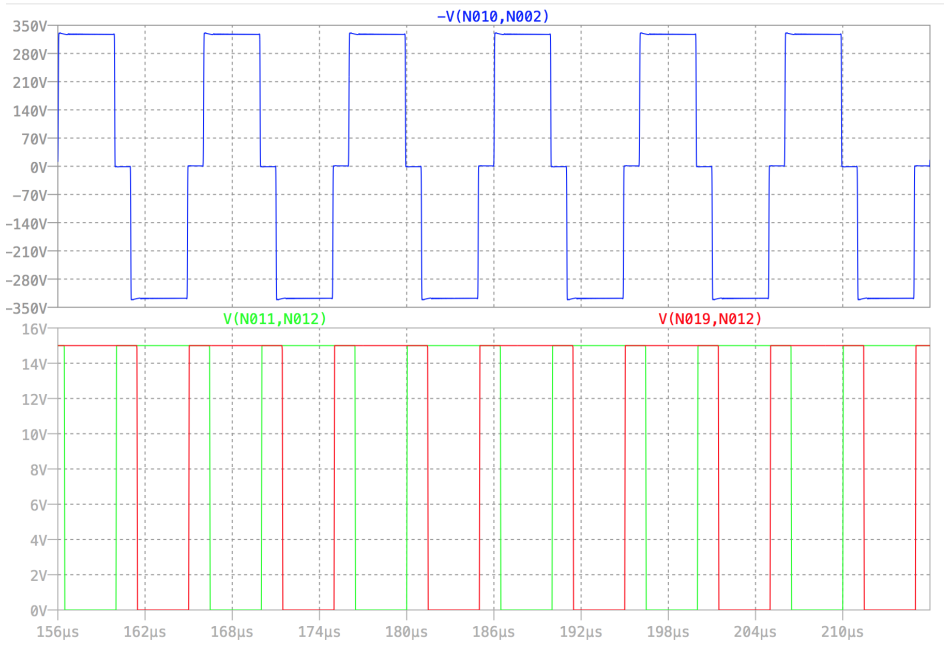

Figure 4.17: Drive signal for MOSFETs on the tertiary side .

Fig.4.18 is the current analysis on the tertiary winding. The red and blue curve stand for the current flowing the inductors and the green one is the output current. Each filter inductor will pass half of the output current with ripples. These ripple will be reduced after they add together and flow as the output current with much more smooth current around 180A. The lower limit value of output current is 169A and the high peak value is 187A, which meets the design of 10% current ripple.

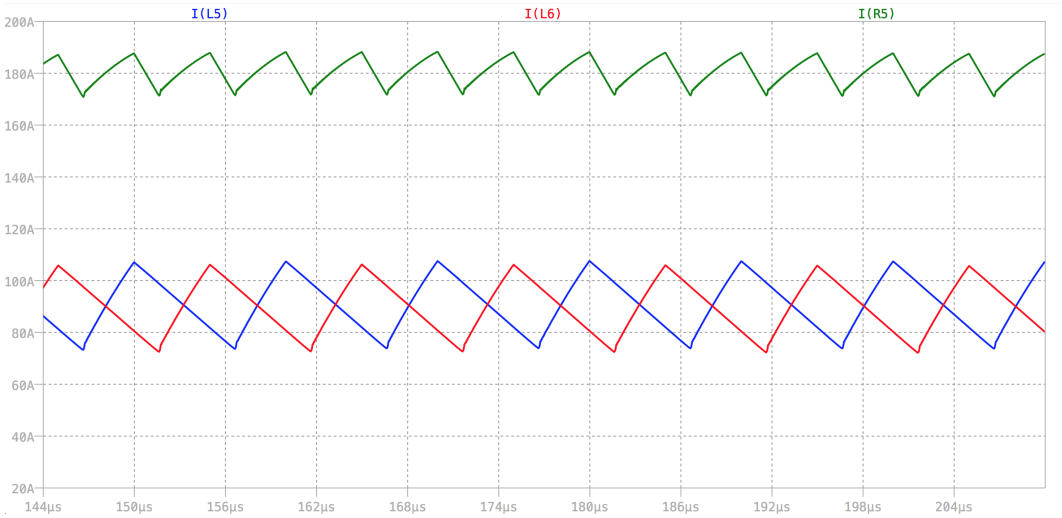

Figure 4.18: Current flowing through inductors.

Fig.4.19 shows the output voltage curve. It is indicated that the output voltage will increase when the DC-DC starts converting. When the DC-DC operates in a stable state, the output voltage is about 13.7V with a low ripple.

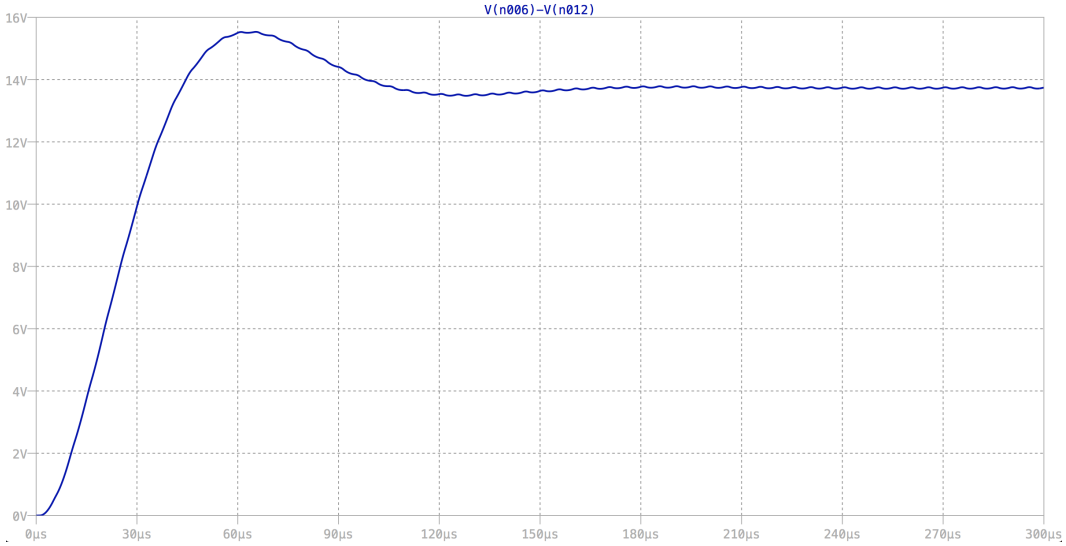

Figure 4.19: Output voltage.

4.2 Transformer selection

Transformer design and selection are keys to this thesis. In this chapter, the focus will be on the core and winding design. The two-winding transformer for the OBC and DC-DC will be discussed first, and then finally a three winding transformer will be introduced and compared.

4.2.1 Turns determination

In this section, the core of the winging transformer and the is selected based on the working flux, the transformer losses and whether the winding can fit the window area. According to the turns ratio decided before, $\frac{N1}{N2} = 0.8$ and $\frac{N2}{N3} = 7.7$, seven turns groups are chosen and will be further discussed here in Table 4.1.

Table 4.1: Available three winding transformer turns

N1	6	12	18	25	31	37	43
N2	8	15	23	31	39	46	54
N3	1	2	3	4	5	6	7

4.2.2 Core design

4.2.2.1 OBC isolated transformer

Based on the introduce in Chapter 3.6.2, the peak flux density is first calculated according to 3.30. The peak flux density in different cores as a function of the primary turn number for OBC is shown as below.

		B[T]						
Core Type	Aw[mm^3]	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	76	1.8268	0.91338	0.60892	0.43842	0.35357	0.29623	0.2549
ETD 34/17/11	97.1	1.4298	0.7149	0.4766	0.34315	0.27673	0.23186	0.19951
ETD 39/20/13	125	1.1107	0.55533	0.37022	0.26656	0.21497	0.18011	0.15498
ETD 44/ 22/15	173	0.8025	0.40125	0.2675	0.1926	0.15532	0.13014	0.11198
ETD 49/25/16	211	0.65798	0.32899	0.21933	0.15791	0.12735	0.1067	0.091811
ETD 54/28/19	280	0.49583	0.24792	0.16528	0.119	0.095968	0.080405	0.069186
ETD 59/31/22	69	0.37726	0.18863	0.12575	0.090543	0.073019	0.061178	0.052642

Figure 4.20: Peak flux density in different cores as a function of primary number of turns at $100kHz$ for OBC path.

For the ETD cores series, there are seven types in total with different dimensions. A_w stands for effective core area for each ETD core type. From the calculation result, it is seen that each cell represents the peak magnetic flux magnitude formed in the cores with respect to the seven turn groups. Since the maximum flux density of a N87 ferrite is $0.39T$, the tables compare

the formed peak flux density with this flux density limit and the cell colour represents the suitability. The cell with red indicates exceeding the saturated value and the green shows lower than it. Therefore, the green marked cells have the potential for being a choice.

Continuinga with the winding design, Fig. 4.21 shows whether the winding could fit in the core window area. The values are positive meaning that the winding size is smaller than the bobbin and could fit in. By contrast, negative values indicate that the winding will not be applicable for the transform bobbin. Combined with the values from the Fig.4.20, consequently, the green marked cells are potentially suitable to work on.

Core Type	Area differece [mm^2]						
	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	93.733	-0.26667	-100.53	-209.16	-309.42	-403.42	-503.69
ETD 34/17/11	143.73	49.733	-50.533	-159.16	-259.42	-353.42	-453.69
ETD 39/20/13	255.73	161.73	61.467	-47.156	-147.42	-241.42	-341.69
ETD 44/ 22/15	325.73	231.73	131.47	22.844	-77.422	-171.42	-271.69
ETD 49/25/16	445.73	351.73	251.47	142.84	42.578	-51.422	-151.69
ETD 54/28/19	531.73	437.73	337.47	228.84	128.58	34.578	-65.689
ETD 59/31/22	631.73	537.73	437.47	328.84	228.58	134.58	34.311

Figure 4.21: Differences between the core window area and the windings area.

To get a better transformer efficiency, the transformer core loss and copper loss are calculated and presented in Fig. 4.22 and Fig. 4.23 to help with the selection, where V_e presents the effective magnetic volume in cm^3 and L_n stands for the average length for one turn in mm.

Core Type		P_core [W]						
	Ve[cm^3]	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	5.35	1127.7	185.99	64.813	27.588	15.77	9.9551	6.7352
ETD 34/17/11	7.63	850.53	140.29	48.885	20.808	11.894	7.5086	5.08
ETD 39/20/13	11.5	664.77	109.65	38.208	16.264	9.2965	5.8686	3.9705
ETD 44/ 22/15	17.8	442.01	72.905	25.405	10.814	6.1814	3.9022	2.64
ETD 49/25/16	24.1	357.12	58.903	20.526	8.7371	4.9943	3.1527	2.133
ETD 54/28/19	35.6	252.8	41.696	14.53	6.1848	3.5353	2.2317	1.5099
ETD 59/31/22	51.2	178.65	29.466	10.268	4.3707	2.4984	1.5771	1.067

Figure 4.22: OBC transformer core losses.

Core Type		Pcu [W]						
	ln[mm]	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	52.8	0.85455	1.6599	2.5144	3.4458	4.3004	5.1057	5.9603
ETD 34/17/11	60.5	0.97917	1.902	2.8811	3.9483	4.9275	5.8503	6.8295
ETD 39/20/13	69	1.1167	2.1692	3.2859	4.5031	5.6198	6.6723	7.789
ETD 44/ 22/15	77.7	1.2575	2.4427	3.7002	5.0708	6.3284	7.5135	8.7711
ETD 49/25/16	86	1.3919	2.7036	4.0955	5.6125	7.0044	8.3161	9.708
ETD 54/28/19	96	1.5537	3.018	4.5717	6.2651	7.8189	9.2831	10.837
ETD 59/31/22	106.1	1.7172	3.3355	5.0527	6.9243	8.6415	10.26	11.977

Figure 4.23: OBC transformer copper losses.

Usually the least total losses design is preferred. When the losses will not make too much difference, prefer to have the core with smaller dimension and windings with less turns to

save the cost and reduce volume. Compared the losses difference, it is seen that core type ETD 54/28/19 with the winding of $N1 = 25$ and $N2 = 31$ has the roughly equal core and copper losses. The size of ETD 54/28/19 is 54 x 56 x 22 mm and it consists of two pieces. The final total losses are the transformer is $12.45W$ shows in Fig. 4.24 with a efficiency of 99.65%.

	Ptotal [W]						
Core Type	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	1128.5	187.65	67.327	31.034	20.07	15.061	12.695
ETD 34/17/11	851.51	142.19	51.766	24.757	16.822	13.359	11.91
ETD 39/20/13	665.88	111.81	41.494	20.767	14.916	12.541	11.759
ETD 44/ 22/15	443.27	75.348	29.105	15.885	12.51	11.416	11.411
ETD 49/25/16	358.52	61.607	24.621	14.35	11.999	11.469	11.841
ETD 54/28/19	254.35	44.714	19.102	12.45	11.354	11.515	12.347
ETD 59/31/22	180.37	32.802	15.321	11.295	11.14	11.837	13.044

Figure 4.24: OBC transformer total losses.

4.2.2.2 DC-DC isolated transformer

Similar as the OBC transformer introduced in Chapter 4.2.2.1, the peak flux density in different cores as a function of the turn number for the DC-DC is shown as below. To easily look up the ratio relationship in Table 4.1, the primary turn number is still used for reference and indication. The possible choices after flux density calculation are marked as green cells.

		B[T]						
Core Type	Aw[mm^3]	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	76	1.6118	0.85965	0.56064	0.41596	0.33063	0.28032	0.23879
ETD 34/17/11	97.1	1.2616	0.67285	0.43881	0.32557	0.25879	0.21941	0.1869
ETD 39/20/13	125	0.98	0.52267	0.34087	0.2529	0.20103	0.17043	0.14519
ETD 44/ 22/15	173	0.70809	0.37765	0.24629	0.18273	0.14525	0.12315	0.1049
ETD 49/25/16	211	0.58057	0.30964	0.20194	0.14982	0.11909	0.10097	0.08601
ETD 54/28/19	280	0.4375	0.23333	0.15217	0.1129	0.089744	0.076087	0.064815
ETD 59/31/22	69	0.33288	0.17754	0.11578	0.085905	0.068283	0.057892	0.049316

Figure 4.25: Peak flux density in different cores as a function of primary number of turns at $100kHz$ for DC-DC path.

After checking the area fitting of the transformer window and windings, the possible selection are marked with the colour green and the discarded options are filtered with red in Fig.4.26.

Core Type	Area differece [mm^2]						
	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	67.328	-51.301	-177.97	-304.65	-431.32	-549.95	-676.62
ETD 34/17/11	117.33	-1.3013	-127.97	-254.65	-381.32	-499.95	-626.62
ETD 39/20/13	229.33	110.7	-15.973	-142.65	-269.32	-387.95	-514.62
ETD 44/ 22/15	299.33	180.7	54.027	-72.645	-199.32	-317.95	-444.62
ETD 49/25/16	419.33	300.7	174.03	47.355	-79.317	-197.95	-324.62
ETD 54/28/19	505.33	386.7	260.03	133.35	6.6827	-111.95	-238.62
ETD 59/31/22	605.33	486.7	360.03	233.35	106.68	-11.947	-138.62

Figure 4.26: Differences between the core window area and the windings area.

The calculated DC-DC transformer losses are shown in Fig.4.27 and Fig.4.28 respectively. Based on the same design concept introduced, the ETD 59/31/22 core is selected due to the least losses difference as well as a reasonable total losses. ETD 59/31/22 core size is 59 x 62 x 22 mm and contains two pieces. The two winding ratios are 31: 4. With a transformer core loss of 3.8121W and copper loss of 9.7739W, the DC-DC transformer will have a total loss of 13.586W and achieve an efficiency of 99.62% at rate power working point.

Core Type		P_core [W]						
	Ve[cm^3]	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	5.35	814.41	158.87	52.286	24.062	13.247	8.624	5.684
ETD 34/17/11	7.63	614.27	119.83	39.437	18.149	9.9914	6.5047	4.2872
ETD 39/20/13	11.5	480.11	93.656	30.823	14.185	7.8092	5.084	3.3508
ETD 44/ 22/15	17.8	319.23	62.274	20.495	9.4319	5.1925	3.3804	2.228
ETD 49/25/16	24.1	257.92	50.314	16.559	7.6205	4.1952	2.7312	1.8001
ETD 54/28/19	35.6	182.58	35.616	11.722	5.3944	2.9697	1.9333	1.2743
ETD 59/31/22	51.2	129.02	25.169	8.2835	3.8121	2.0986	1.3663	0.9005

Figure 4.27: DC-DC transformer core losses.

Core Type		Pcu [W]						
	ln[mm]	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	52.8	1.2358	2.3923	3.6281	4.8639	6.0997	7.2562	8.492
ETD 34/17/11	60.5	1.416	2.7412	4.1572	5.5732	6.9892	8.3144	9.7304
ETD 39/20/13	69	1.615	3.1263	4.7413	6.3562	7.9712	9.4826	11.098
ETD 44/ 22/15	77.7	1.8186	3.5205	5.3391	7.1577	8.9763	10.678	12.497
ETD 49/25/16	86	2.0128	3.8966	5.9094	7.9223	9.9351	11.819	13.832
ETD 54/28/19	96	2.2469	4.3497	6.5966	8.8435	11.09	13.193	15.44
ETD 59/31/22	106.1	2.4833	4.8073	7.2906	9.7739	12.257	14.581	17.064

Figure 4.28: DC-DC transformer copper losses.

Core Type	Ptotal [W]						
	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	815.65	161.26	55.914	28.926	19.346	15.88	14.176
ETD 34/17/11	615.69	122.57	43.594	23.722	16.981	14.819	14.018
ETD 39/20/13	481.72	96.782	35.565	20.541	15.78	14.567	14.448
ETD 44/ 22/15	321.05	65.794	25.834	16.59	14.169	14.059	14.725
ETD 49/25/16	259.94	54.21	22.468	15.543	14.13	14.55	15.632
ETD 54/28/19	184.82	39.965	18.318	14.238	14.06	15.126	16.714
ETD 59/31/22	131.51	29.976	15.574	13.586	14.356	15.947	17.965

Figure 4.29: DC-DC transformer total losses.

4.2.2.3 Three winding transformer

The same procedure will be conducted here. Since the three winding will not be working at the same time, the the flux density will still be calculated separately as OBC and DC-DC in the same working scenario. Therefore the result shows in Fig. 4.20 and 4.25 can be used for this investigation.

Regarding the window area calculation, now the third winding is introduced and the possible choices are shown in Figure. 4.30. Now the choices are reduced, and fewer cells could fit its winding in the core window area.

Core Type	Area differece [mm^2]						
	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	18.569	-148.82	-324.25	-507.72	-683.15	-850.54	-1026
ETD 34/17/11	68.569	-98.819	-274.25	-457.72	-633.15	-800.54	-975.97
ETD 39/20/13	180.57	13.181	-162.25	-345.72	-521.15	-688.54	-863.97
ETD 44/ 22/15	250.57	83.181	-92.249	-275.72	-451.15	-618.54	-793.97
ETD 49/25/16	370.57	203.18	27.751	-155.72	-331.15	-498.54	-673.97
ETD 54/28/19	456.57	289.18	113.75	-69.723	-245.15	-412.54	-587.97
ETD 59/31/22	556.57	389.18	213.75	30.277	-145.15	-312.54	-487.97

Figure 4.30: Differences between the core window area and total three windings area.

With the flux density limit shows in Fig. 4.20 and 4.25, a new figure is obtained, presented in Fig. 4.30. The choices are restricted in only these 8 groups.

Core Type	Area differece [mm^2]						
	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	18.569	-148.82	-324.25	-507.72	-683.15	-850.54	-1026
ETD 34/17/11	68.569	-98.819	-274.25	-457.72	-633.15	-800.54	-975.97
ETD 39/20/13	180.57	13.181	-162.25	-345.72	-521.15	-688.54	-863.97
ETD 44/ 22/15	250.57	83.181	-92.249	-275.72	-451.15	-618.54	-793.97
ETD 49/25/16	370.57	203.18	27.751	-155.72	-331.15	-498.54	-673.97
ETD 54/28/19	456.57	289.18	113.75	-69.723	-245.15	-412.54	-587.97
ETD 59/31/22	556.57	389.18	213.75	30.277	-145.15	-312.54	-487.97

Figure 4.31: Differences between the core window area and total three windings area.

Since when the OBC and the DC-DC are working, the RMS current will be the same as in the previous scenario, the copper losses will be the same as in the previous discussion. To have least total losses, the core ETD 60/31/22 is selected with three winding turns set as 25/31/4. It has the largest dimension in this ETD core series and the transformer will be 60 x 62 x 22 mm and consists of two ETD core pieces.

When the primary and secondary winding of the three winding transformer are in operation in the on board charger, the total losses is 11.295W marked in Fig.4.32 and the efficiency is 99.67%. When the secondary and tertiary winding are transferring as DC-DC, the total losses is approximately 13.586W marked in Fig.4.33 with and efficiency of 99.45%.

	Ptotal [W]						
Core Type	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	1128.5	187.65	67.327	31.034	20.07	15.061	12.695
ETD 34/17/11	851.51	142.19	51.766	24.757	16.822	13.359	11.91
ETD 39/20/13	665.88	111.81	41.494	20.767	14.916	12.541	11.759
ETD 44/ 22/15	443.27	75.348	29.105	15.885	12.51	11.416	11.411
ETD 49/25/16	358.52	61.607	24.621	14.35	11.999	11.469	11.841
ETD 54/28/19	254.35	44.714	19.102	12.45	11.354	11.515	12.347
ETD 59/31/22	180.37	32.802	15.321	11.295	11.14	11.837	13.044

Figure 4.32: Total losses for OBC.

	Ptotal [W]						
Core Type	N1 = 6	N1 = 12	N1 = 18	N1 = 25	N1 = 31	N1 = 37	N1 = 43
ETD 29/16/10	815.65	161.26	55.914	28.926	19.346	15.88	14.176
ETD 34/17/11	615.69	122.57	43.594	23.722	16.981	14.819	14.018
ETD 39/20/13	481.72	96.782	35.565	20.541	15.78	14.567	14.448
ETD 44/ 22/15	321.05	65.794	25.834	16.59	14.169	14.059	14.725
ETD 49/25/16	259.94	54.21	22.468	15.543	14.13	14.55	15.632
ETD 54/28/19	184.82	39.965	18.318	14.238	14.06	15.126	16.714
ETD 59/31/22	131.51	29.976	15.574	13.586	14.356	15.947	17.965

Figure 4.33: Total losses for DC-DC.

4.2.3 Winding

4.2.3.1 OBC transformer

To design and choose the Litz wire as introduced in Chapter 3.4.2, the two winding transformer used in on board charger is now conducted. A brief calculated winding bundle area and strands number in each bundle for OBC transformer is shown in Table.4.4

Table 4.2: OBC transformer winding calculation

	I_{RMS}	A_{bundle}	N_{Strand}	Litz type	Litz length
Primary turn	$16.14A$	$3.59mm^2$	714	4 bundle 180 strands	$2.40m$
Secondary turn	$16A$	$3.56mm^2$	708	4 bundle 180 strands	$2.96m$

With the result presented, the Litz wire could be selected from the supplier *Elektrisola*. Finally the OBC transformer winding is constructed by four bundles. Each bundle will have 180 strands inside and the cross section area of each bundle is $0.9048mm^2$. Based on the core type ETD 54/28/19 and the winding of 25: 31 turns, the total length of four bundle Litz wire will be $5.36m$.

4.2.3.2 DC-DC transformer

Following the same approach, the strands number in each bundle for DcDc transformer is calculated as $N_{Strand,pri} = 304$, $N_{Strand,sec} = 2785$. The primary winding is designed to be five bundles and each bundle has 60 strands. The bundle cross section area is $0.3016mm^2$. The five bundles of Litz wire with 600 strands in each bundle and of the cross section area $3.0159mm^2$ is utilized for the secondary winding. To fit the transformer core of the ETD 59/31/22 and winding turns of 31:4, $3.29m$ five bundle 60 strands Litz wire and $0.42m$ five bundle 600 strands Litz wire are needed.

Table 4.3: DcDc transformer winding calculation

	I_{RMS}	A_{bundle}	N_{Strand}	Litz type	Litz length
Primary turn	$8.30A$	$1.85mm^2$	307	5 bundle 60 strands	$3.29m$
Secondary turn	$64A$	$14.20mm^2$	2785	5 bundle 600 strands	$0.42m$

4.2.3.3 Three winding transformer

As the three winding transformer, the calculation for each winding shall take the RMS current scenario into consideration as the table below. For the primary and secondary winding, the Litz wire used for OBC transformer will still be applicable here. The total length for four bundle 180 strands will be $4.93m$ long. In addition, a $0.42m$ long 5 bundle 600 strands Litz will conduct for the tertiary winding.

Table 4.4: Three transformer winding calculation

	I_{RMS}	A_{bundle}	N_{Strand}	Litz type	Litz length
Primary turn	$17A$	$3.77mm^2$	750	4 bundle 180 strands	$2.65m$
Secondary turn	$16A$	$3.56mm^2$	708	4 bundle 180 strands	$2.28m$
Tertiary turn	$64A$	$14.20mm^2$	2785	5 bundle 600 strands	$0.42m$

To compare the combined design with the signal OBC and DC-DC package, it is easily verified that the the winded Litz length reduce a lot. A $0.43m$-long 4 bundle 180 strands is reduced and and no 5 bundle 60 strands Litz wire is needed.

4.3 Semiconductor losses

4.3.1 Semiconductor losses for OBC

The transistor losses normally consist of switching loss and conduction loss, which are calculated using the equations mentioned in previous chapter.

Fig.4.34 shows the switching transition for Q2. The navy wave is the voltage over the transistor, the red wave represents the total current flowing through the MOSFET module and the bluish one is the gate signal. For instance, before switch Q2 turns on, the capacitor discharges the energy through the inductor, so the current goes down with the decreased voltage, which can be observed from Fig.4.34. After the voltage decreases to zero, the current flows in the anti-parallel body diode, thus, switch Q2 can be turned on with zero voltage. When the gate signal is triggered, the MOSFET turns on, but the current flows both through the MOSFET and the body diode according to the direction of the current. In Fig.4.34, only if the current becomes positive, the MOSFET itself will conduct all current. Consequently, to simplify the analysis and calculation, the switching conduction loss and the body diode will be calculated together as conduction loss.

For simply analysis, the flowing current whatever its direction, is regarded as the current going through MOSFET after the gate signal is triggered. Moreover, from the simulation result it can be seen, ZVS operation is fully achieved for all switches in the OBC. Thus, the semiconductor losses only consist of the transient loss caused by the body diode during the blanking time and the conduction loss by switch itself.

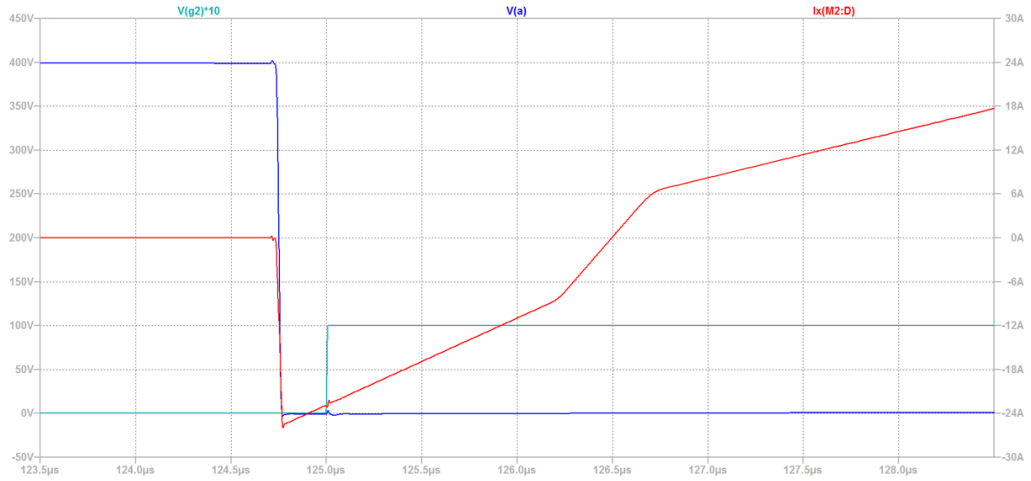

Figure 4.34: The key waveforms for switch Q2 in DAB.

Figure.4.35 displays the current waveforms for each switch in one cycle. It is obviously seen the half cycle starts from t_0 and ends at t_4.

According to the theoretical waves and the simulation results, the current on the typical point, such as I_{t_0}, I_{t_1}, I_{t_2}, I_{t_3} and I_{t_4} can be calculated by (4.1) to (4.2) . Then different piecewise

functions reflect the current waves which can be constructed in Matlab to calculate the typical current values. Finally, the value of average current and rms current can be derived by Matlab.

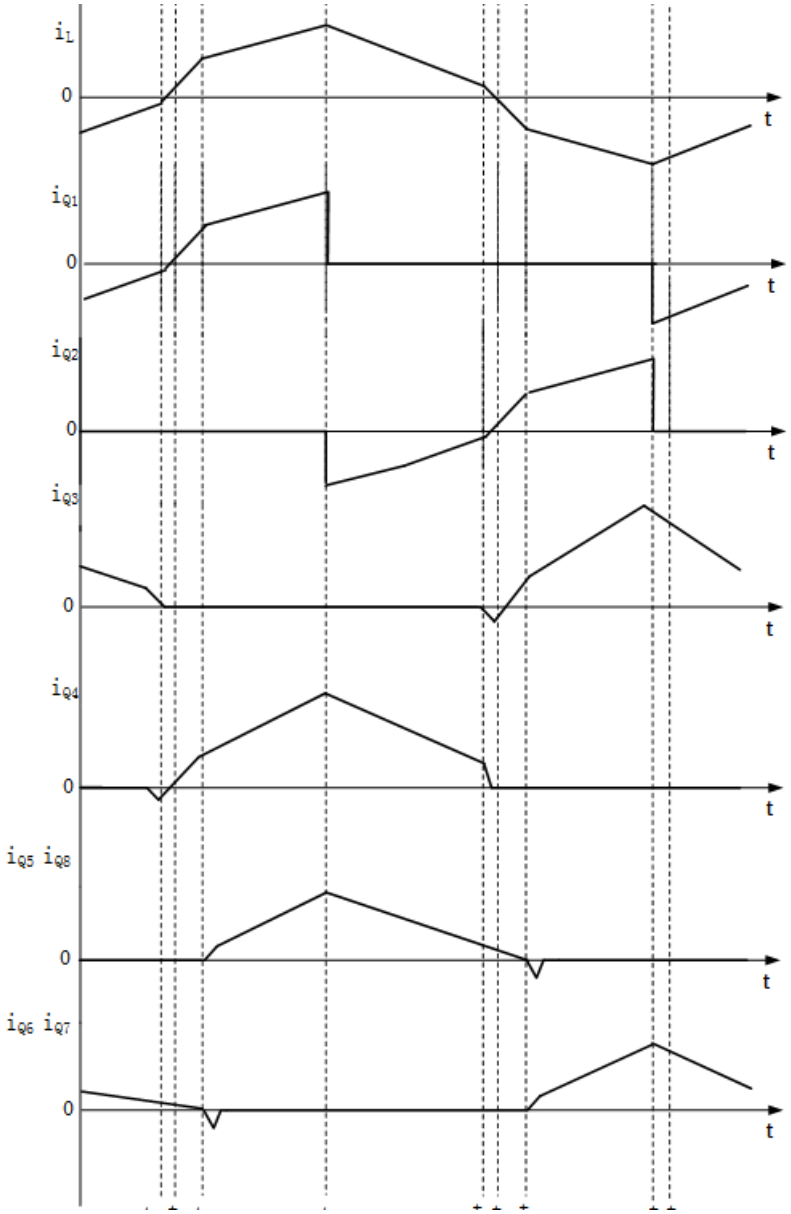

Figure 4.35: The current waveforms for each switch.

- **Time interval between t_0 to t_2:**

$$i_{(t)} = \frac{(1+k)V_1}{L}(t-t_0) - \frac{(D_{y1}+kD_{y1}+2kD_{\phi}-2k)V_1}{4Lf_s} \tag{4.1}$$

- **Time interval between t_2 to t_3:**

$$i_{(t)} = \frac{(1-k)V_1}{L}(t-t_2) + \frac{(k+2D_\phi - 1)V_1}{4Lf_s} \tag{4.2}$$

- **Time interval between t_3 to t_4**:

$$i_{(t)} = \frac{-kV_1}{L}(t-t_3) + \frac{(D_{y1} - kD_{y1} + 2kD_\phi)V_1}{4Lf_s} \tag{4.3}$$

Based on the analysis of Chapter 2.3.2, regarding switch Q_1, during blanking time before turning on, the current flows through the body diode during one period. Then the current will run through Q_1 itself when it is on. Here is the analysis procedure in detail for one period from t_0 to t_8 .

- **Time interval between t_0 to t_2**:

Q1 is on status and the switch current is negative from t_0 and reaches zero at t_0 then flows in positive direction, thus I_{t_0} = -7.48A according to (4.1).

- **Time interval between t_2 to t_3**:

The current flows positive through Q1 in this period. According to (4.1) and (4.2), the instant current at t_2 and t_3 can be calculated as I_{t_2} = 4.92A and I_{t_3} = 24.54A.

- **Time interval between t_3 to t_7**:

Q1 snaps off during this period, therefore, the current is zero.

- **Time interval between t_7 to t_8**:

From t_7, Q1 starts up for another half cycle operation. During the blanking time between t_7 and t_8, the current flows through the body diode of Q1 reversely. From the figure can be seen, $I_{t_7} = -I_{t_3}$. Hence, $I_{t_7} = -24.54A$ and $I_{t_8} = -20.8A$.

- **Time interval between t_8 to t_0**:

The current is still negative through Q1 and the current wave from t_7 to t_0 is symmetric with the current in the figure from t_3 to t_4.

Then these current values are imported to Matlab and the average current and rms current can be finalized. Consequently, the semiconductor losses for Q_1 is calculated as

$$P_{on-state-Q1} = V_{sd}I_{on(avg)} + R_{don}I^2_{on(rms)} =$$

$$0.9V \cdot 22.67A + 0.043\Omega \cdot (3.8^2A + 15.78^2A + 14.14^2A) \approx 40W$$

R_{don} is the on-state Resistance of MOSFET and is chosen with the value of 0.043Ω under 25° based on the MOSFET IPW65R048CFDA specification in this case.

As the current wave of Q2 is symmetrical and there is only a half cycle phase shift compared to Q1, therefore, the semiconductor losses is the same as Q1. Other switches follow the same

analyzing procedure with the similar operational mechanism. The waves of Q3 and Q4 are symmetric with 180° phase shift. Therefore, the semiconductor losses for Q3 and Q4 are

$$P_{on-state-Q3Q4} = V_{sd}I_{on(avg)} + R_{don}I^2_{on(rms)}$$
$$= 0.9V \cdot 3.74A + 0.043\Omega \cdot (2.82^2A + 13.77^2A + 16.75^2A) \approx 24W$$

On the secondary side, the two switches in each arm are conducting 180° complementary and the diagonal switches operates simultaneously. So the waveforms of Q5 and Q8 are identical and the waveforms of Q6 and Q7 are only 180° phase shifted compared to Q5 and Q8. The current value on the secondary side is proportional to the primary side current with the value of transformer turns ratio. Therefore, according to the theoretical current waveforms and simulation, the power losses of each switch can be defined.

$$P_{on-state-sec} = V_{sd}I_{on(avg)} + R_{don}I^2_{on(rms)}$$
$$= 0.9V \cdot 2A + 0.043\Omega \cdot (12.62^2A + 13.4^2A) \approx 16.5W$$

Consequently, the semiconductor power losses for OBC can be calculated as

$$P_{on-state-tot} = 2P_{on-state-Q1} + 2P_{on-state-Q3Q4} + 4P_{on-state-sec}$$
$$= 2 \cdot 40W + 2 \cdot 24W + 4 \cdot 16.5W = 194W$$

4.3.2 Semiconductor losses for DC-DC

4.3.2.1 DcDc full bridge topology semiconductor losses

As the simulation result shows in Chap. 4.1.2, zero voltage switching is well achieved for the four MOSFETs on DC-DC full bridge. It is clear that the conduction losses will be the main dominant part. Based on (2.18) introduced, the conduction loss for one MOSFET can be found to be

$$P_{on-state} = V_{sd} I_{on(avg)} + R_{don} I^2_{on(rms)} = 7.8W$$

Regardless of the switching losses due to good result of ZVS, the total semiconductor losses of the DC-DC full bridge in one period is

$$P_{tot,sec} = 4 * P_{on-state} = 31.4W$$

4.3.2.2 DC-DC current doubler topology semiconductor losses

To calculate the semiconductor losses in the DC-DC output topology synchronous rectifier losses, the conduction process in one cycle could be divide into the following four periods in specific as shown in Fig 4.36. Combined with the simulation result shown in Fig.4.18 and Fig.4.19, the losses will be calculated in the following part.

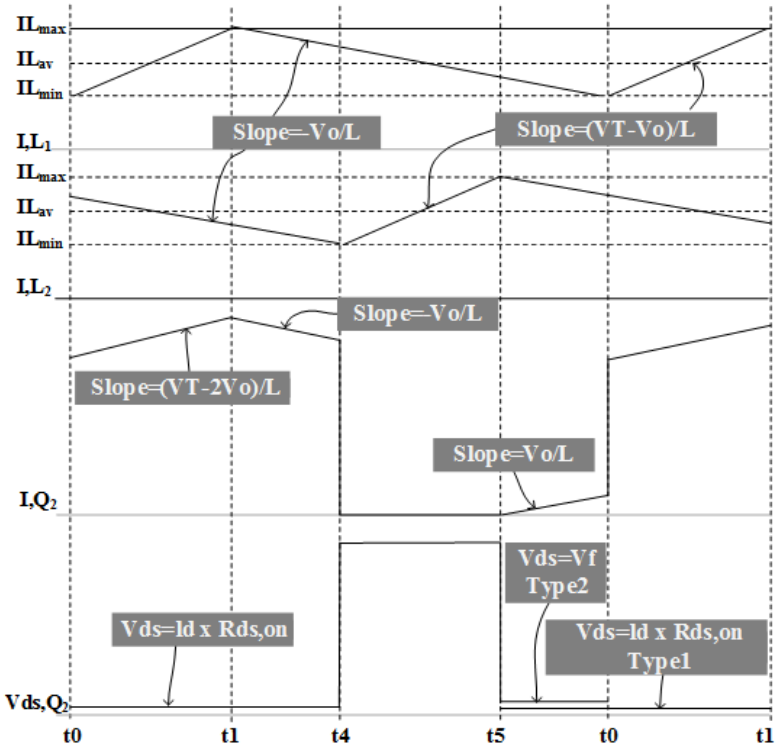

Figure 4.36: Losses analysis of synchronous rectifier.

- **Timeframe** $t_0 - t_1$

$$I_{d(avg)} = I_{L_{av}} + I_{L_{av}} = 2I_{L_{av}} = I_o \tag{4.4}$$

$$V_{DS} = R_{don} I_{d(avg)} = R_{don} I_o \tag{4.5}$$

$$P_{d1} = \frac{DT_s}{T_s} I_{d(avg)} V_{DS} = DR_{don} I_o^2 = 0.36 \cdot 3.6 \cdot 10^{-3} \cdot 180^2 = 41.9W \tag{4.6}$$

- **Timeframe** $t_1 - t_4$

The losses in this period is calculated as

$$I_{d(avg)} = I_o + T_s(\frac{V_o}{4L} - \frac{DV_o}{2L}) \tag{4.7}$$

$$V_{DS} = R_{don} I_{d(avg)} = R_{don}[I_o + T_s(\frac{V_o}{4L} - \frac{DV_o}{2L})] \tag{4.8}$$

As a result the loss is

$$P_{d2} = \frac{(0.5-D)T_s}{T_s} I_{d(avg)} V_{DS} \tag{4.9}$$

$$= (0.5-D)R_{don}[I_o + T_s(\frac{V_o}{4L} - \frac{DV_o}{2L})]^2$$

$$= (0.5-0.36) \cdot 3.6 \cdot 10^{-3} \cdot [180 + 10^{-5}(\frac{13.5}{4 \cdot 2.8 \cdot 10^{-6}} - \frac{0.36 \cdot 13.5}{2 \cdot 2.8 \cdot 10^{-6}})]^2 = 16.9W$$

- **Timeframe** $t_4 - t_5$

In this time period, the losses the the MOSFET turn off losses. According to2.6.1, it is calculated

$$P_{d3} = P_{on} = V_d I_0 \frac{t_{fi} + t_{rv}}{2} f_s$$

$$= 13.5 \cdot 180/2 \cdot \frac{(130+130) \cdot 10^{-6}}{2} \cdot 10^5 = 1.6W$$

- **Timeframe** $t_5 - t_0$

$$I_{d(avg)} = T_s(\frac{V_o}{4L} - \frac{DV_o}{2L}) \tag{4.10}$$

$$V_{DS} = R_{don} I_{d(avg)} = R_{don} T_s(\frac{V_o}{4L} - \frac{DV_o}{2L}) \tag{4.11}$$

As the result, the loss is calculate

$$P_{d4} = \frac{(0.5-D)T_s}{T_s} I_d V_{DS} = (0.5-D)R_{don}[T_s(\frac{V_o}{4L} - \frac{DV_o}{2L})]^2 \tag{4.12}$$

$$= (0.5 - 0.36) \cdot 3.6 \cdot 10^{-3} \cdot [10^{-5}(\frac{13.5}{4 \cdot 2.8 \cdot 10^{-6}} - \frac{0.36 \cdot 13.5}{2 \cdot 2.8 \cdot 10^{-6}})]^2 = 0.05W$$

Based on the above calculation for one MOSFET in one conduction period, the total DC-DC current doubler loss during one conduction could be get as

$$P_{tot,ter} = 2 * (P_{d1} + P_{d2} + P_{d3} + P_{d4}) = 120.45W \tag{4.13}$$

4.4 Efficiency

4.4.1 Efficiency of OBC path

The efficiency of the DAB is evaluated using real transistor model from Infineon and calculated in nominal operation point which means the output voltage is the nominal voltage of the battery with the value of $330V$.

In full load condition, the output power is around $3.750kW$ in steady state. The semiconductor losses with $194W$ and the transformer losses with $12.45W$ are calculated from previous section. Hence, the efficiency at nominal point of the high power charging path is 94.8%.

4.4.2 Efficiency of DC-DC path

The DC-DC loss can be obtained from the previous calculation. It is conducted based on the theoretical analysis and the LTspice simulation waveform. In the full load condition with an input power of $2.5kW$, the total losses will be $160.67W$ and achieve an efficiency of 93.57%. The output power will be $2.34kW$

$$P_{total} = P_{tot,sec} + P_{trans} + P_{tot,ter} = 31.4 + 8.82 + 120.45 = 160.67W$$

4.5 Design comparison

A simple transformer comparison is made in Fig.4.37 based on efficiency, component price as well as the rough transformer volume. It is shown that the efficiency reduces a little with the three winding transformer conducting for the OBC. The volume is reduced a lot since one one ETD 59/31/22 core will be used. In terms of the component price, based on the local RS component online shop and E-bay, three winding transformer is much more cost effective by reducing about 35%.

		OBC	DcDc	Combined OBC and DcDc	Comparison Result
Efficiency		99.65%	99.45%	OBC 99.67% DcDc 99.45%	Increased
Price/kr	**Core**	89.79	123.68	123.68	215.93
	Liz wire	214	175.75	291.7	
	Coil former	28.03	34.06	34.06	
	Total	331.82	333.49	449.38	
Volume/cm^3		71.2	102.4	102.4	71.2

Figure 4.37: Transformer comparison.

Based on the comparison above, a further general cost of the power electronic devices are listed. On one hand, the new design reduces the package dimension. On the other hand, the total cost of the key component is much lower. It eliminates one transformer core. More importantly, only ten MOSFETs are used instead of total fourteen MOSFET working on two PCBs, which makes the combined OBC and DC-DC much more promising and cost effective. In an rough summary, it could saves about 613 Sek for the new combined package design.

	Transformer		MOSFET	
OBC	Two winding	332 Sek	8 * IPW65R048CFDA	792 Sek
DC - DC	Two winding	334 Sek	4 * IPW65R048CFDA 2 * IRFP2907	508 Sek
OBC & DC-DC	Three winding	449 Sek	8 * IPW65R048CFDA 2 * IRFP2907	904 Sek

Figure 4.38: Device pricing.

5

Conclusion

5.1 Results from present work

The target of this thesis work is fulfilled successfully. The OBC and DC-DC converter topology are selected, implemented and simulated with the software LTspice. The topology performance is also investigated. In general, the switching pattern of ZVS and phase shift control strategy is well applied to control the MOSFETs for OBC and DC-DC. The switching losses and noise is greatly decreased. To be specific,

- The dual active bridge is applied on the OBC converter. Power from the grid will flow through to charge the HV battery. Since the secondary side of this full bridge is bi-directional, the secondary side will work as the input side of DC-DC converter to charge the 12V battery.
- The DC-DC functionality is achieved as the full bridge converter uses the needed components from the DAB secondary side and current doubler with synchronous rectification. The inductance is selected to lower the current ripple.
- The power losses for each topology is also involved. It meets the original design target.

The isolated OBC and DC-DC transformer is designed as the reference. To compare, a three winding transformer structure including the core and winding is introduced and carried out in detail. It is clearly indicated that the combined three winding transformer could transfer power for the DC-DC and OBC with approximately the same efficiency. More advanced, the volume and cost consequences of components are assessed roughly. The results shows that the dimension is reduced in a big step. Hence it is feasible to combine the OBC and the DC-DC converter design in one package to enhance the power density.

5.2 Future Work

To continue with this thesis work, a few topics could be carried out:

- Replace MOSFITs with alternative semiconductors devices in simulations, i.e. GaN and SiC
- Design the dynamic controller to control and drive the MOSFET gate signal.

- Design and test a PCB board and verify the simulated results on the real converter.
- Investigate the converter's performance in different working loads as well as for different frequencies .
- The insulation of AC charger during driving mode and the isolation of DC-DC converter during grid charging mode need to be solved by suitable control.

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