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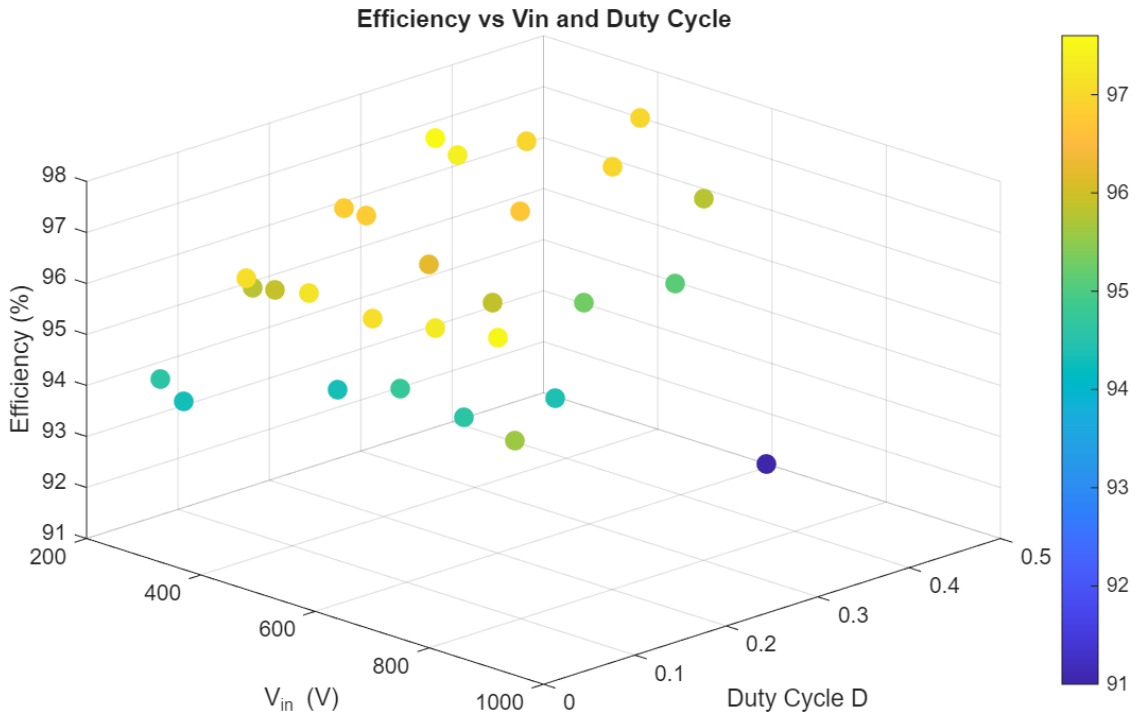

Design of HV to LV DC/DC converter using resonant topology

Master's Thesis in Sustainable Electric Power Engineering and Electromobility

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Design of HV to LV DC/DC Converter Using Resonant Topology
Utilising First Harmonic Approximation to design and evaluate the performance of the converter
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Cover:Efficiency plot of the converter

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Abstract

The increasing demand for high-voltage electric vehicle architectures requires efficient power converters. Additionally, the increasing adoption of 800 V battery architectures alongside conventional 400 V systems has increased the requirements placed on the high-voltage to low-voltage (HV-LV) DC-DC converter. Hence, a wider variation in battery voltage requires converters with a wide input-voltage range while maintaining high efficiency, compact size, and low voltage stress on the components. This thesis presents the design and evaluation of a 9 kW isolated HV-LV DC-DC converter based on a Stacked Half-Bridge (SHB) LLC resonant topology, designed to operate over an input-voltage range of 330–950 V while providing a regulated low-voltage output.

The proposed converter uses the LLC resonant tank together with the SHB structure to achieve the required wide voltage-gain range. The large variation in input voltage would otherwise require a conventional LLC converter to operate over a wide gain range, potentially increasing the required operating frequency range or requiring additional conversion stages. The SHB structure provides an additional voltage gain, allowing the required conversion ratio to be achieved over the 330–950 V input range. At the same time, the LLC resonant tank enables soft-switching operation, while the SHB structure reduces the voltage stress across the primary-side switches. The converter design includes the development of the LLC resonant tank, high-frequency transformer, resonant inductor, modulation strategy, and control structure. First Harmonic Approximation (FHA) was employed for resonant tank design, and detailed loss models were implemented in MATLAB/Simulink to evaluate converter performance under practical operating conditions.

Several capacitor-voltage balancing techniques were investigated, and an interleaved PWM modulation strategy was selected due to its improved balancing performance. Simulation results demonstrate that the proposed converter achieves the required voltage conversion over the specified operating range while maintaining capacitor-voltage balance and high efficiency. A maximum efficiency of 97.2% was obtained under nominal operating conditions. From the results, it can be concluded that the SHB LLC converter is a promising solution for wide-input-voltage automotive DC-DC conversion applications. It offers high efficiency, reduced component stress and increased voltage gain range of the converter.

Keywords: HV-LV DC-DC converter, LLC resonant converter, Stacked Half-bridge Converter, Electric Vehicles, Zero-voltage switching,Voltage Balancing, Transformer Design, Resonant Topology, Power Electronics

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Sareena Gouse Vaddinakatti,
Gothenburg, August 2026

List of Acronyms

AC	Alternating Current
BCM	Boundary Conduction Mode
CC	Constant Current
CV	Constant Voltage
DC	Direct Current
EV	Electric Vehicle
FB	Full Bridge
FHA	First Harmonic Approximation
HB	Half Bridge
HV	High Voltage
IPOP	Input-Parallel Output-Parallel
IPOS	Input-Parallel Output-Series
ISOP	Input-Series Output-Parallel
ISOS	Input-Series Output-Series
LLC	Inductor-Inductor-Capacitor Resonant Converter
LV	Low Voltage
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PWM	Pulse Width Modulation
RMS	Root Mean Square
SHB	Stacked Half Bridge
SiC	Silicon Carbide
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ESR	Equivalent Series Resistance
MLT	Mean Length Per Turn
L_r	Resonant inductance
N	Primary to secondary turns ratio
L_m	Magnetizing inductance
C_r	Resonant capacitance
R_{ac}	Equivalent AC load resistance
f_s	Switching frequency

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1
Introduction

The latest Volvo car models use an 800V battery, whereas previous models oper ated with a 400V system. This increase in voltage allows for higher power delivery and efficiency, but it also necessitates a reliable HV to LV power converter to supply auxiliary loads with a wide range of voltage. LLC resonant converters are chosen for this application due to their high efficiency, ability to achieve zero voltage switching (ZVS), and compact size, for a high power density design. Additionally, it uses a stacked half bridge for providing extra gain for the converter. This project aims to design a HV to LV power converter that meets the performance requirements, optimizes thermal and electrical characteristics, and integrates control strategies and modulation techniques. The design is fully automated to reduce redesign time and simple for multi-objective optimization techniques in order to achieve high efficiency and power density converter.

1.1 Related Work

In recent years, LLC has been a major part of Power converters where efficiency is the utmost priority due to its Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) capability. These are operated at high frequencies to achieve high power density in electric vehicle chargers, DC-DC converters, photovoltaic cells, wireless power transfer, etc. [1]. Among various resonant converter topologies, the full-bridge and half-bridge are the most common topologies used in the power converters. But these come with a limitation that we cannot have a wide voltage range and high voltage stress in full bridge LLC converter[2]. To overcome these challenges, a novel topology has emerged providing wider voltage range due to the additional gain range provided by the stacked half bridge. This also has an additional benefit of lower voltage stress at the switches due to its additional switches in series[2]. However, this comes with the challenge of capacitor voltage balancing because of the dividing capacitors at the input of the converter. This challenge can be overcome by various solutions like diode clamping, addition of flying capacitor, etc.[4]. But this would require additional components in the board. Hence this project focuses on balancing the voltage using different modulation techniques to make it more efficient.

1.2 Purpose and Goal

The purpose of this project is to develop a high-efficiency single-stage DC-DC converter capable of operating over a wide input voltage range of 330–950 V. By elim-

inating the need for an additional power conversion stage, the proposed topology reduces system complexity, component count, cost, and packaging space, making it well suited for automotive applications. The project also aims to achieve high efficiency while maintaining a simple and effective control strategy. The goal of this project is to design and evaluate a 9 kW single-stage DC-DC converter and verify its performance over the specified operating range. The work includes the design of the high-frequency transformer and resonant inductor, selection of suitable semiconductor devices and passive components, and assessment of the converter's efficiency under different operating conditions, including the effects of temperature and component tolerances.
A detailed loss analysis is carried out using MATLAB/Simulink in combination with analytical calculations. The simulations provide the voltage and current waveforms required to estimate conduction and switching losses, while component parasitics obtained from manufacturers' datasheets are incorporated to model practical operating conditions. The analysis also verifies the achievement of zero-voltage switching (ZVS) across the operating range and evaluates the overall converter efficiency.

1.3 Limitation

The primary limitation of this work is that the proposed converter was evaluated solely through simulation and was not implemented in hardware. Consequently, practical effects such as manufacturing tolerances, component parasitics, electromagnetic interference, measurement uncertainties, and control implementation challenges could not be experimentally verified. Due to the time constraints of the project, it was also not possible to perform a direct comparison between the proposed converter and the company's existing converter hardware. Therefore, the performance improvements predicted by the simulation results remain subject to experimental validation. Furthermore, several non-ideal effects including detailed gate-driver behaviour, dead-time mismatches, and additional losses associated with practical hardware implementation, were not explicitly included in the simulation model. These factors may influence the converter performance and should be investigated in future work.

2

Converter Topology

The system specifications require the design of a 9 kW isolated HV-LV DC-DC converter. Instead of implementing a single 9 kW converter, a modular architecture consisting of two identical 4.5 kW converter modules was selected. A modular approach offers several advantages, including improved thermal management, reduced electrical and thermal stress on individual components, easier maintenance, and increased system scalability. Furthermore, the failure of a single module does not necessarily result in complete system shutdown, thereby improving the overall reliability of the converter.

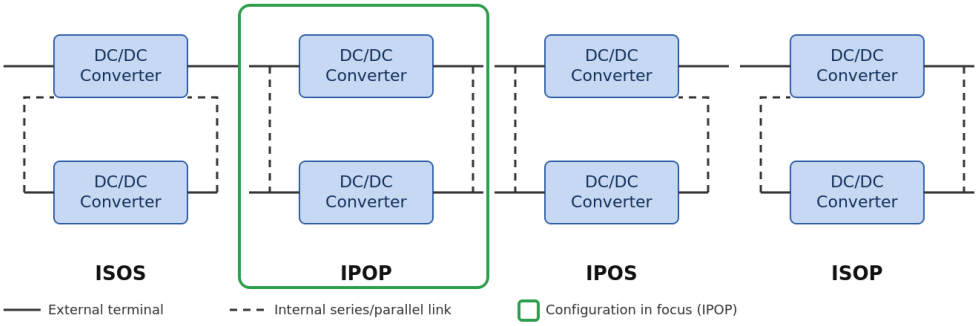


Figure 2.1: Modular isolated DC–DC converter interconnection configurations: Input-Series Output-Series (ISOS), Input-Parallel Output-Parallel (IPOP), Input-Parallel Output-Series (IPOS), and Input-Series Output-Parallel (ISOP).

Several interconnection configurations can be adopted for modular isolated DC-DC converters, including Input-Parallel Output-Parallel (IPOP), Input-Series Output-Series (ISOS), Input-Parallel Output-Series (IPOS), and Input-Series Output-Parallel (ISOP). These configurations are illustrated in Fig 2.1. Each topology offers different advantages in terms of voltage and current sharing, component stress, control complexity, scalability and fault tolerance. In this project, the IPOP topology is selected for the initial investigation due to its ability to distribute the output current between parallel converter modules, thereby reducing conduction losses, improving thermal management, and enhancing system reliability. Since the converter modules share both the input voltage and output current, the current handled by each module is approximately half of the total system current. This reduces conduction losses, distributes thermal loading between the modules, and improves fault tolerance, as

one converter can continue operating if the other becomes unavailable. However, parallel operation introduces challenges related to current sharing and circulating currents between the modules, requiring an appropriate control strategy to ensure stable operation.

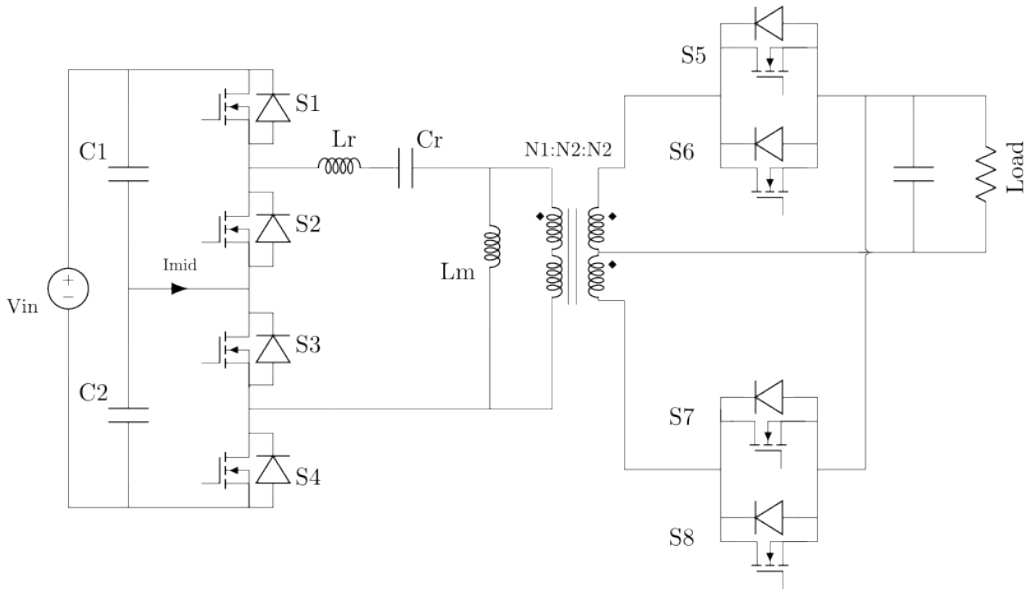


Figure 2.2: Stacked Half Bridge LLC converter

For the DC-DC conversion stage, a stacked half-bridge (SHB) LLC resonant converter is employed as shown in Fig 2.2. While conventional high-voltage conversion often requires multiple power conversion stages to achieve the required voltage conversion ratio, the proposed SHB LLC converter performs the conversion in a single stage, reducing the number of passive and active components, minimizing conversion losses, and simplifying the overall control architecture. In addition, the LLC resonant tank enables Zero Voltage Switching (ZVS) over a wide operating range, resulting in reduced switching losses, higher efficiency, and improved power density. The stacked half-bridge structure also provides increased voltage gain while reducing the voltage stress across the switching devices, making it well suited for high-voltage automotive applications. This converter has four major parts which will be discussed in the later section which are stacked half bridge, LLC tank, transformer and rectifier. Practically, the transformer is a part of LLC tank but is separated for a clear understanding of the operation of the converter in this project.

3

Theory

This chapter presents the theoretical background required for the design and analysis of the proposed converter. The operating principles of the LLC resonant converter, stacked half-bridge topology, voltage-balancing mechanism, rectification stage, magnetic component design, and converter loss mechanisms are discussed. The presented theory provides the foundation for the component sizing, control strategy and design methodology described in the subsequent chapters.

3.1 LLC Resonant Converter

Resonant converters utilise resonant tanks in order to reduce the switching losses and provide a gain to the signals. This is achieved because of the presence of its inductive and capacitive elements. The value of the voltage gain varies with different frequencies due to its change in the impedance of its components.

The gain of the resonant tank depends on the value of its components, the input frequency and the value of the load at the output. This gain characteristic can be divided into three operating regions to explain its different behaviour during the change of the parameters stated above.

$$G_{\mathrm{LLC}} = \frac{m f_n^2}{\sqrt{\left[(m+1)f_n^2 - 1\right]^2 + m^2 Q^2 f_n^2 \left(f_n^2 - 1\right)^2}} \tag{3.1}$$

$$R_{ac} = \frac{8N^2}{\pi^2} R_{dc}. \tag{3.2}$$

Table 3.1: Parameters used in the LLC voltage gain equation.

Symbol	Name	Definition
Q	Quality factor	$Q = \frac{\sqrt{L_r/C_r}}{R_{\text{ac}}}$
m	Inductance ratio	$m = \frac{L_m}{L_r}$
f_n	Normalized frequency	$f_n = \frac{f_s}{f_r}$
f_r	Resonant frequency	$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$

3.1.1 Operation of the Converter Below Resonant Frequency

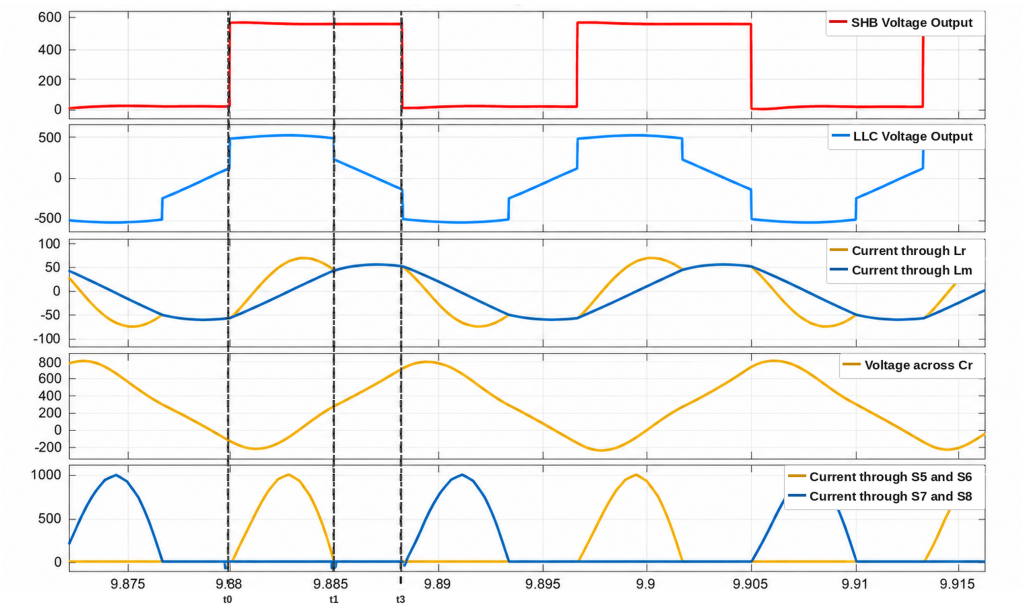


Figure 3.1: Voltage and current waveforms below Resonant Frequency

The operation of the converter below the resonant frequency is divided into two intervals, as illustrated in Fig. 3.1.

3.1.1.1 Interval I (t_0–t_1)

At $t = t_0$, switches S_1 and S_4 are turned on, applying the input voltage across the resonant tank. At the beginning of this interval, the resonant inductor current (I_{Lr}) is negative due to the energy stored during the previous switching cycle. Since an inductor resists sudden changes in current, the current increases gradually toward the positive direction.

During this interval, the resonant capacitor is charged, while the magnetizing current (I_{Lm}) increases approximately linearly because the transformer primary is excited by the applied voltage. The secondary-side rectifier conducts, transferring power from the primary side to the output.As the resonant current decreases, it eventually becomes equal to the magnetizing current:

$$I_{Lr} = I_{Lm} \tag{3.3}$$

At this instant, the secondary current becomes zero because the transformer current available for power transfer is zero. Consequently, the secondary-side rectifier turns off naturally, and no power is transferred to the output during this interval. The resonant tank continues to oscillate, with the circulating current confined to the primary side.

3.1.1.2 Interval II (t_1–t_3)

At $t = t_2$, switches S_1 and S_4 are turned off. After the required dead time, switches S_2 and S_3 are turned on, reversing the voltage applied across the resonant tank.

As a result, the resonant inductor current decreases, crosses zero, and increases in the negative direction. The resonant capacitor begins discharging and then charging with the opposite polarity, while the magnetizing current also reverses its direction. Once the magnitude of the resonant current exceeds the magnetizing current, the secondary rectifier conducts again, and power transfer resumes. After this half cycle,the converter operation is symmetrical to Interval I, with all currents and voltages having opposite polarity. Energy is transferred from the input source to the output until the resonant current again becomes equal to the magnetizing current. After this condition is reached, the next switching cycle begins.

3.1.2 Operation of the Converter at Resonant Frequency

At resonance, the switching frequency is equal to the resonant frequency of the LLC tank,

$$f_s = f_r. \tag{3.4}$$

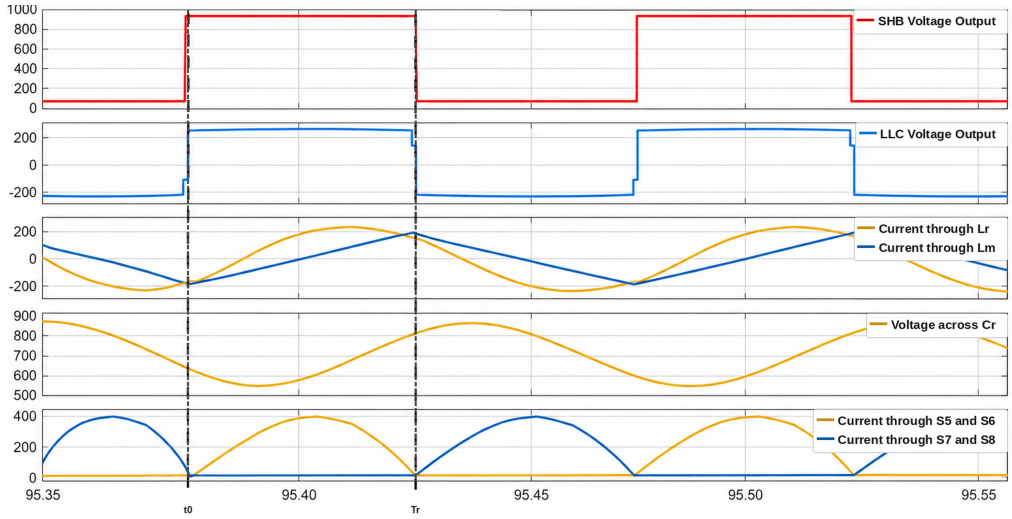


Figure 3.2: Voltage and current waveforms at Resonant Frequency

At this operating point, the inductive reactance of the resonant inductor L_r and the capacitive reactance of the resonant capacitor C_r are equal in magnitude and cancel each other. Consequently, the resonant tank exhibits its minimum impedance, resulting in maximum power transfer from the source to the load. Due to the reduced reactive power circulation, the converter operates with high efficiency. The gain of the LLC converter at resonance is approximately unity,

$$G_{LLC} = 1. \tag{3.5}$$

Fig. 3.2 illustrates the waveforms of the LLC converter operating at the resonant frequency. It can be observed that the resonant tank current is approximately in phase with the applied tank voltage. In contrast to below-resonance operation, the discontinuous conduction interval disappears and the transformer remains continuously involved in energy transfer throughout the switching cycle. The operation can be analysed using two significant instants, namely t_0 and T_r, where T_r is the resonant period given by

$$T_r = \frac{1}{f_r}. \tag{3.6}$$

3.1.2.1 Operation at $t = t_0$

At $t = t_0$, the resonant current and magnetizing current become equal,

$$I_{Lr} = I_{Lm}. \tag{3.7}$$

At this instant, the secondary current reaches zero and the rectifier current ceases conduction momentarily. No current is transferred to the secondary winding; however, unlike below-resonance operation, the secondary current does not remain zero for an extended duration. Instead, the current immediately reverses direction as the resonant current continues its sinusoidal oscillation. This operating point represents

the boundary between continuous and discontinuous conduction. Therefore, the LLC converter is said to operate at the boundary conduction mode (BCM) when the switching frequency is equal to the resonant frequency.

3.1.2.2 Operation at $t = T_r$

At $t = T_r$, the resonant current reaches the next zero crossing and the same boundary-conduction condition occurs with opposite polarity. The resonant current, magnetizing current and secondary current reverse direction, maintaining symmetrical operation between the positive and negative half cycles. Since the secondary current only touches zero instantaneously before changing direction, continuous power transfer is maintained throughout the switching period. The resonant current remains nearly sinusoidal and in phase with the applied voltage, resulting in lower conduction losses and improved converter efficiency. Compared with operation below resonance, the circulating current is reduced, the discontinuous conduction interval is eliminated, and maximum power transfer is achieved. Consequently, resonance is often considered to be the optimal operating point of the LLC resonant converter.

3.1.3 Operation of the Converter Above Resonant Frequency

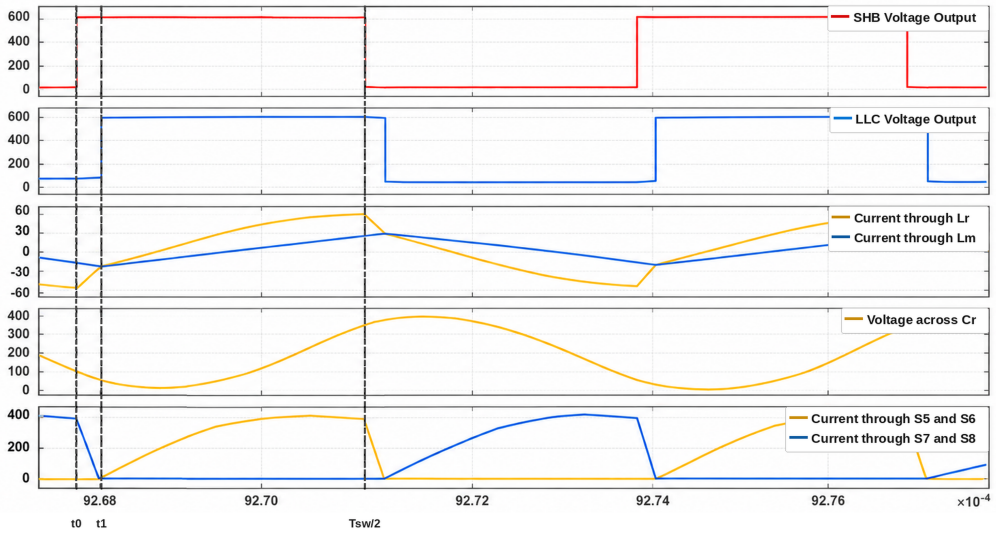


Figure 3.3: Voltage and current waveforms above Resonant Frequency

When the switching frequency is higher than the resonant frequency ($f_s > f_r$), the LLC converter operates above resonance. As shown in Fig. 3.3, the polarity of the voltage applied to the LLC resonant tank reverses before the resonant half-period is completed. Consequently, the primary switches experience higher turn-off losses when compared to operation at the resonant frequency. In this operating region, the voltage gain of the LLC converter is lower than that at resonance. Therefore, this

mode of operation is typically utilised when the input voltage is high and a lower voltage gain is required from the LLC resonant tank.

3.1.4 Soft Switching

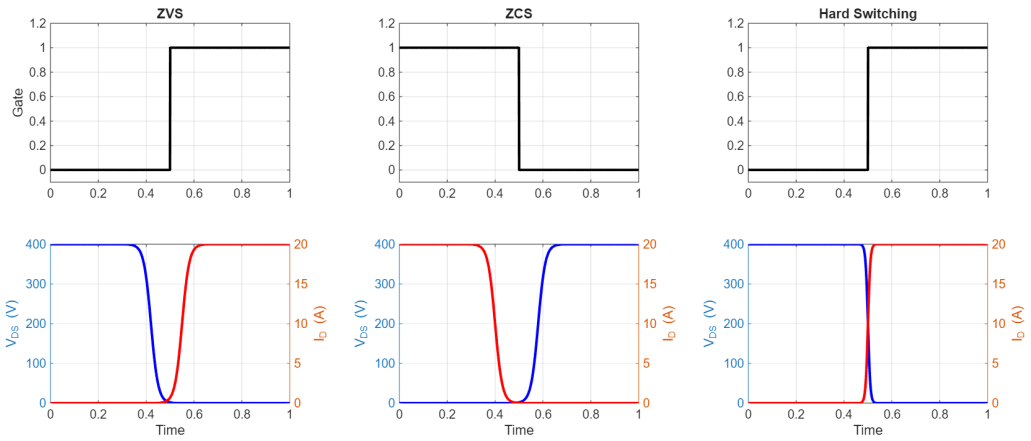


Figure 3.4: Switching Techniques

3.1.4.1 Zero Voltage Switching (ZVS)

Every MOSFET has an inherent output capacitance due to its physical structure. Because of this capacitance, a voltage may still be present across the device even when the gate signal is turned off and the MOSFET is in the off-state. Zero Voltage Switching (ZVS) is a soft-switching technique in which the MOSFET is turned on only after the voltage across the device has been reduced to nearly zero ($V_{DS} \approx 0$).By ensuring that the drain-to-source voltage and switch current do not overlap significantly during the turn-on transition, ZVS greatly reduces switching losses. This improves converter efficiency, reduces device stress, and minimizes electromagnetic interference compared with conventional hard-switching operation.
The LLC resonant converter naturally supports ZVS operation due to its resonant characteristics, allowing it to achieve higher efficiency than hard-switched converters. However, successful ZVS operation requires two important conditions to be satisfied. First, the converter must operate in the inductive region, where the resonant current lags behind the applied voltage. This phase relationship is essential because it allows the resonant current to charge and discharge the MOSFET output capacitances before the switching transition occurs.
Second, the resonant current and magnetizing current must provide sufficient energy during the dead time to completely discharge the parasitic output capacitances of the MOSFETs. Once the voltage across the switch has been reduced to zero, the MOSFET can be turned on with minimal turn-on loss.
Therefore, proper control of the resonant operating point and ensuring adequate circulating energy are critical for maintaining reliable ZVS operation in an LLC converter.

The effect of ZVS can be observed in Fig. 3.4, where the voltage across the MOSFET falls to zero before the application of the gate pulse. Under this condition, the switch is turned on with negligible turn-on loss, resulting in high-efficiency operation. In contrast, Fig. 3.4 illustrates a hard-switching condition, where the MOSFET is turned on while a significant voltage is still present across the device. Consequently, simultaneous voltage and current overlap during the switching transition leads to increased switching losses and reduced converter efficiency. Since the voltage at the input is high, it is necessary to have ZVS at the primary switches in the converter to reduce the turn on losses of the switches

3.1.4.2 Zero Current Switching (ZCS)

In an LLC resonant converter, the secondary-side devices operate under ZCS conditions for the majority of the operating range. This is because the resonant current naturally decreases to zero before commutation occurs. Consequently, the secondary current is approximately zero at the switching instant, resulting in negligible turn-off losses.

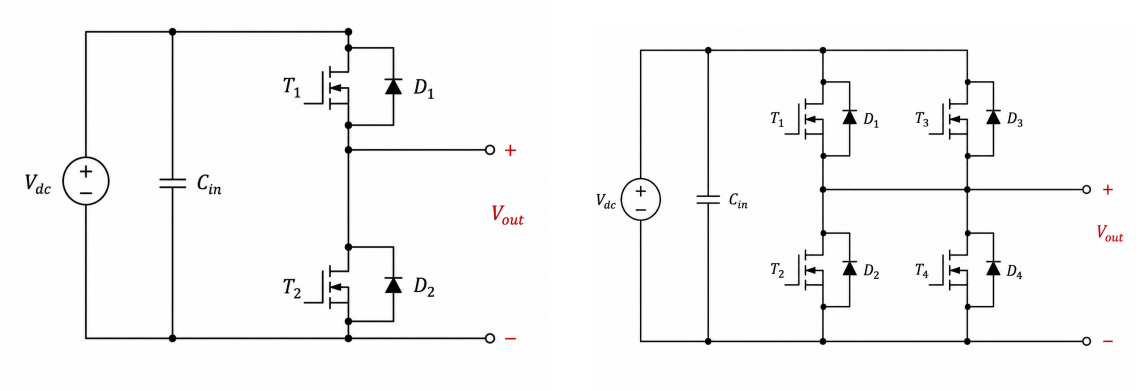
Furthermore, the converter employs synchronous rectification on the secondary side, where MOSFETs replace conventional rectifier diodes. Since the current through the synchronous rectifiers naturally falls to zero before commutation, the switching losses are significantly reduced. In addition, if body diodes conduct during the commutation process, the associated reverse-recovery losses are minimal because the current is already close to zero.

As shown in Fig. 3.1, Fig. 3.2 and Fig. 3.3, the current through the secondary-side synchronous rectifiers naturally falls to zero before commutation. This results in ZCS operation and significantly reduces switching losses. Such a reduction in losses is particularly beneficial on the secondary side of the converter, where relatively high current levels are present.

3.2 Bridge Topologies for LLC Converters

The LLC resonant tank requires a high-frequency pulsed voltage excitation, which is typically generated by a bridge converter connected between the DC source and the resonant tank. The bridge converts the DC voltage supplied by the battery into a high-frequency square-wave voltage that excites the LLC network.

The most common bridge topologies used in LLC converters are the Full-Bridge (FB) and Half-Bridge (HB) configurations. The selection of a suitable topology depends on several factors, including the voltage stress across the switching devices, the output voltage magnitude produced by the bridge, the converter power rating, and the overall component count. In the following sections, the operating principles of the Full-Bridge, Half-Bridge, and Stacked Half-Bridge topologies are discussed. The effect of each topology on the voltage applied to the LLC tank and the resulting gain characteristics are also presented.



(a) Half Bridge **(b)** Full Bridge

Figure 3.5: Comparison of converter topologies.

In this thesis, a Stacked Half-Bridge (SHB) topology is employed. Unlike the conventional Half-Bridge and Full-Bridge configurations, the SHB topology is capable of generating three voltage levels through appropriate modulation strategies. As a result, it offers increased flexibility in controlling the voltage applied to the LLC tank while reducing the voltage stress on individual switching devices. Due to these advantages, the SHB topology has recently attracted considerable attention in the field of power electronics.

3.2.1 Half-Bridge Converter

Fig. 3.5(a) shows the Half-Bridge (HB) converter. The inverter consists of two active switches, T_1 and T_2, together with their anti-parallel diodes D_1 and D_2. When T_1 is turned on, current flows through the upper switch and the lower diode, completing the current path. Similarly, when T_2 is turned on, current flows through the lower switch and the upper diode.
A blocking capacitor is commonly connected at the input of the transformer to prevent the presence of a DC component in the transformer voltage, thereby avoiding transformer saturation. The output voltage applied to the LLC resonant tank varies between $+V_{dc}/2$ and $-V_{dc}/2$. Consequently, only half of the input DC voltage is applied to the resonant tank. The voltage stress across each switching device is equal to V_{dc}. The Half-Bridge topology is widely used due to its simple structure and low component count. However, since only half of the DC bus voltage is applied to the LLC tank, a higher transformer turns ratio is generally required compared to a Full-Bridge converter.

3.2.2 Full-Bridge Converter

Fig. 3.5 (b) shows the Full-Bridge (FB) converter. The topology consists of four switches arranged in two bridge legs. By alternately switching the diagonal pairs of devices, a square-wave voltage is generated across the LLC resonant tank.
The output voltage applied to the resonant tank varies between $+V_{dc}$ and $-V_{dc}$. Therefore, the Full-Bridge converter applies the entire DC-link voltage across the

LLC tank, resulting in a bridge gain that is twice that of the Half-Bridge topology. The voltage stress across each switch is equal to V_{dc}. Due to the higher output voltage capability, the Full-Bridge topology is commonly employed in high-power applications. However, it requires four active switches and a more complex gate-drive arrangement than the Half-Bridge converter.
Both the Half-Bridge and Full-Bridge topologies generate only two voltage levels at their output. In contrast, SHB topology is capable of producing three different voltage levels. This additional degree of freedom provides increased flexibility in controlling the voltage applied to the LLC resonant tank and extends the operating range of the converter.

3.2.3 Stacked Half-Bridge Converter

The Stacked Half-Bridge (SHB) converter utilises four active switches and offers reduced voltage stress across each switching device compared to the conventional Half-Bridge and Full-Bridge topologies. As shown in Fig. 2.2, the input DC-link capacitor is divided into two series-connected capacitors, creating a midpoint voltage. As a result, the voltage stress across each switch is limited to approximately $V_{dc}/2$. To prevent a short circuit across the DC-link capacitors, switches S_1 and S_2 are operated in a complementary manner. Similarly, switches S_3 and S_4 are also operated complementarily. This ensures proper voltage sharing and safe converter operation.
A major advantage of the SHB topology is its ability to generate multiple output-voltage levels through appropriate switching-state selection. This additional degree of freedom increases control flexibility and extends the achievable operating range of the converter. The switching combinations and corresponding output voltage levels are summarised in Table 3.2.
Although the SHB topology offers significant advantages, it introduces additional control complexity. The presence of split DC-link capacitors requires capacitor voltage balancing to ensure that each capacitor maintains approximately half of the input voltage.

Table 3.2: Output voltage levels of the SHB converter.

Switches ON	Output Voltage
S_1, S_4	V_{dc}
S_1, S_3 or S_2, S_4	$V_{dc}/2$
S_2, S_3	0

Table 3.3 provides a comparison between the Half-Bridge (HB), Full-Bridge (FB), and Stacked Half-Bridge (SHB) topologies. It can be observed that the SHB topology offers an additional voltage level while simultaneously reducing the voltage stress across the switching devices. Although the control complexity is increased, the additional degree of freedom provided by the third voltage level enables improved control of the LLC resonant converter.
For this reason, the SHB topology was selected for this thesis. The reduced voltage stress across the switching devices makes the topology suitable for high-voltage battery applications. In addition, the presence of an extra voltage level provides greater

Table 3.3: Comparison of bridge topologies used in LLC converters.

Parameter	HB	FB	SHB
Number of switches	2	4	4
Number of voltage levels	2	2	3
Voltage stress per switch	V_{dc}	V_{dc}	$V_{dc}/2$
Gain variation	0–0.5	0–1	0–0.5
Control complexity	Low	Medium	High

flexibility in controlling the voltage applied to the LLC resonant tank. Consequently, the converter can accommodate a wider input-voltage variation while maintaining the required output-voltage regulation and gain characteristics.

3.2.4 Voltage Balancing

The voltages across the split DC-link capacitors are affected by the switching states, gate-signal timing, and non-ideal characteristics of the converter components. Small mismatches in the gate-signal timing can cause one capacitor to charge while the other discharges during each switching period. In particular, even a small gate-signal delay can result in significant capacitor-voltage imbalance under symmetric modulation. The imbalance may also become more pronounced at higher switching frequencies because the same absolute timing error represents a larger fraction of the switching period. Mismatches in capacitance and equivalent series resistance (ESR) can also produce transient voltage imbalance, although their effect on the steady-state imbalance may be limited. [4]
The capacitor-voltage imbalance affects the voltage distribution across the switching devices and can increase the voltage stress on individual devices. Therefore, an effective balancing method is required to maintain safe and reliable operation of the SHB LLC converter.
The switching states of the SHB converter can be classified according to the neutral-point current I_{mid}, the resonant current direction and the conducting switches. When switches S_1 and S_4 are on, or when switches S_2 and S_3 are on, I_{mid} is ideally zero. Consequently, these states do not change the DC-link capacitor voltages. In contrast, when switches S_1 and S_3, or switches S_2 and S_4, are on, a neutral-point current can flow and charge one capacitor while discharging the other.
For equal DC-link capacitances, the capacitor currents satisfy $I_{C1} = -I_{C2}$. When $I_{mid} > 0$, the top capacitor C_1 is charged and the bottom capacitor C_2 is discharged. Conversely, when $_{mid} < 0$, C_1 is discharged and C_2 is charged. When $I_{mid} = 0$, the capacitor-voltage difference is ideally unaffected. The voltage difference can therefore be expressed as

$$V_{\text{diff}} = V_{C1} - V_{C2} = \int \frac{i_{NP}}{C}\, dt, \qquad C = C_1 = C_2. \tag{3.8}$$

Hence, capacitor-voltage balancing is achieved by controlling the direction and duration of the neutral-point current through the modulation strategy. In interleaved modulation technique, phase-shift control can be implemented and the duty cycles of

the relevant switching states can be adjusted to control the duration of the positive or negative neutral-point current. [5]

3.2.5 Rectifier Topologies for LLC Converter

Since the output of the transformer is an AC voltage, a rectifier is required to convert it into a DC voltage suitable for the load. The characteristics of the selected synchronous rectifier MOSFET, including the on-state resistance used in the loss calculations, were obtained from the manufacturer datasheet [8]. There are multiple rectifier topologies that can be used in LLC converters, including the half-wave rectifier, full-bridge rectifier, and centre-tapped full-wave rectifier. The converter considered in this thesis employs a centre-tapped full-wave rectifier. Therefore, only this rectifier topology is discussed in detail.
The centre-tapped full-wave rectifier utilises two rectifying devices connected at the ends of the centre-tapped secondary winding of the transformer, with its centre terminal connected to the load.
Fig. 2.2 shows the SHB with centre-tapped full-wave rectifier.The operation of the centre-tapped full-wave rectifier can be divided into two intervals. During the positive half-cycle of the transformer secondary voltage, one rectifying device conducts. During the negative half-cycle, the other rectifying device conducts. In both cases, the output current flows in the same direction through the load, thereby producing a DC output voltage with ripple which is later filtered by an output capacitor.
Additionally, synchronous rectification is used in this rectifier to reduce conduction losses. In conventional rectification, the diode conducts when its forward biased by the voltage applied across it. In synchronous rectification, the current path through the diode is replaced by a MOSFET, which provides a lower resistance current path due to its lower on-state resistance. When the appropriate voltage polarity is detected, the MOSFET gate signal is applied, allowing the MOSFET to conduct and reducing the conduction losses compared with diode operation. Proper dead time between the MOSFET gate signals is required to prevent reverse current conduction and cross conduction between the MOSFETs. . Since MOSFETs generally exhibit lower conduction losses than diodes at the same operating point, they improve the efficiency of the rectifier. Different methods of synchronous rectification control can be implemented where the gate signal of the MOSFETs in the rectifiers turns them on based on the voltage across them. This can be done in two ways: self-driven or externally driven [6]. This topic is beyond the scope of this thesis hence it is not covered in detail. But the synchronous rectification was utilised in the simulations to extract the values of losses.

3.2.6 Design of Transformer

The transformer in an LLC converter provides galvanic isolation and voltage transformation between the primary and secondary sides. In addition, the transformer magnetising inductance contributes directly to the operation of the LLC resonant tank. The transformer design therefore requires careful selection of the core area, air-gap length, winding arrangement and conductor sizing.

3.2.6.1 Core Area Determination

The transformer core is designed using Faraday's law of electromagnetic induction. The voltage induced across the winding is given by

$$V = N\frac{d\Phi}{dt} \tag{3.9}$$

where V is the winding voltage, N is the number of turns and Φ is the magnetic flux. The magnetic flux is related to the flux density by

$$\Phi = BA_e \tag{3.10}$$

where B is the flux density and A_e is the effective core area. Substituting into Faraday's law gives

$$V = NA_e\frac{dB}{dt} \tag{3.11}$$

For square-wave excitation, the maximum flux density can be approximated by

$$B_{\max} = \frac{VD}{2NA_ef} \tag{3.12}$$

where D is the duty cycle and f is the switching frequency. Rearranging,

$$A_e = \frac{VD}{2NB_{\max}f} \tag{3.13}$$

This equation is used to determine the minimum effective core area required to avoid saturation.

3.2.6.2 Magnetizing Inductance

The magnetising inductance is determined from the magnetic reluctance of the magnetic circuit according to

$$L_m = \frac{N^2}{\mathcal{R}} \tag{3.14}$$

where $\mathcal{R}$ is the total reluctance. The total reluctance consists of the core reluctance and the air-gap reluctance,

$$\mathcal{R} = \mathcal{R}_c + \mathcal{R}_g \tag{3.15}$$

The core reluctance is

$$\mathcal{R}_c = \frac{l_e}{\mu_0\mu_rA_e} \tag{3.16}$$

and the air-gap reluctance is

$$\mathcal{R}_g = \frac{g}{\mu_0A_e} \tag{3.17}$$

where l_e is the effective magnetic path length and g is the air-gap length. The magnetising inductance is therefore

$$L_m = \frac{\mu_0A_eN^2}{g + \frac{l_e}{\mu_r}} \tag{3.18}$$

For gapped ferrite components,

$$g \gg \frac{l_e}{\mu_r} \tag{3.19}$$

and therefore the air gap primarily determines the magnetising inductance.

3.2.6.3 Magnetizing Current

The magnetising reactance is

$$X_m = \omega L_m \tag{3.20}$$

where

$$\omega = 2\pi f \tag{3.21}$$

The corresponding magnetising current is

$$I_m = \frac{V}{X_m} \tag{3.22}$$

or

$$I_m = \frac{V}{\omega L_m} \tag{3.23}$$

Increasing the magnetising inductance reduces the magnetising current and therefore reduces circulating current within the LLC converter.

3.2.6.4 Window Area Requirement

The conductor area required by a winding is

$$A_{Cu} = \frac{I_{RMS}}{J} \tag{3.24}$$

where I_{RMS} is the RMS winding current and J is the current density. The total copper area is

$$A_{Cu,total} = \sum \frac{I_{RMS}}{J}. \tag{3.25}$$

The minimum window area required is

$$A_w = \frac{A_{Cu,total}}{K_u} \tag{3.26}$$

where K_u is the window utilisation factor.

3.2.6.5 Winding Design

The winding design must account for both DC resistance and the increase in AC resistance caused by high-frequency effects.

3.2.6.5.1 Skin Effect When alternating current flows through a conductor, the current tends to concentrate near the conductor surface. This phenomenon is known as skin effect. The skin depth is given by

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}} \tag{3.27}$$

where σ is the conductivity of the conductor. The ratio between conductor diameter and skin depth is

$$\xi = \frac{d}{\sqrt{2}\delta}. \tag{3.28}$$

The DC resistance is

$$R_{DC} = \frac{4}{\sigma \pi d^2}. \tag{3.29}$$

The skin-effect loss can be estimated as

$$P_s = R_{DC} F_R(f) i^2 \tag{3.30}$$

where $F_R(f)$ is the AC-to-DC resistance factor.

3.2.6.5.2 Proximity Effect The proximity effect arises due to magnetic fields generated by neighbouring conductors. These fields alter the current distribution within a conductor, thereby increasing the AC resistance. Techniques such as conductor spacing, interleaving and the use of Litz wire are commonly employed to minimise proximity-effect losses.

3.2.6.6 Leakage Inductance

The transformer leakage inductance arises due to magnetic flux that links only one winding and not the other. Unlike the magnetising inductance, the leakage inductance is mainly determined by the winding arrangement and spacing between the primary and secondary windings. The leakage inductance can be related to the coupling coefficient by

$$L_{lk} = L_m \left(\frac{1-k}{k} \right) \tag{3.31}$$

where k is the coupling coefficient. The coupling coefficient of practical high-frequency transformers typically lies between 0.95 and 0.99. The transformer leakage inductance may contribute to the required resonant inductance of the LLC tank.

3.2.7 Design of the Resonant Inductor

The LLC converter requires a resonant inductance connected in series with the resonant capacitor. The required inductance may be realised entirely using an external inductor or by combining transformer leakage inductance with an external resonant inductor.
The design of the resonant inductor follows principles similar to those used for transformer magnetic design. The required inductance is determined from the LLC

resonant tank parameters, after which the core geometry, air-gap length, number of turns and conductor dimensions are selected to satisfy the electrical and thermal requirements.
Since the resonant inductor operates at high frequency, the winding design must also consider skin effect and proximity effect in order to minimise AC copper losses. The detailed equations used for the magnetic and winding design are identical to those presented in the transformer design section and are therefore not repeated here.

3.2.8 Power Losses in the Converter

To design an efficient converter, it is essential to understand the losses associated with each component. Accurate loss estimation enables informed design decisions and assists in the selection of suitable components and cooling methods.
The major loss contributors in the converter include semiconductor losses, transformer core losses, winding losses, and passive component losses. These losses are primarily dependent on the voltage and current stresses experienced by the individual components during operation.
Thermal considerations also play an important role in converter design. Component temperature affects material properties such as semiconductor on-state resistance, magnetic core characteristics, and conductor resistance. Consequently, the losses of the converter are strongly influenced by its operating temperature.
The following sections describe the major loss mechanisms considered in this work and present the equations used to account for the non-ideal behaviour of practical components.

3.2.8.1 MOSFET Losses

Silicon Carbide (SiC) MOSFETs are employed on the primary side of the converter due to their suitability for high-voltage and high-frequency applications. The total MOSFET power loss consists of two main components: switching loss and conduction loss.
The switching loss occurs during the turn-on and turn-off transitions of the device, when both voltage and current are simultaneously present across the MOSFET. In LLC converters, these losses can be significantly reduced by operating under Zero Voltage Switching (ZVS) conditions.
The switching loss can be expressed as

$$P_{sw} = f_s(E_{on} + E_{off}), \tag{3.32}$$

where f_s is the switching frequency, E_{on} is the turn-on energy loss, and E_{off} is the turn-off energy loss.
The conduction loss is caused by the finite on-state resistance of the MOSFET, $R_{DS(on)}$. This loss is given by

$$P_{cond} = I_{rms}^2 R_{DS(on)}, \tag{3.33}$$

where I_{rms} is the RMS current flowing through the device.

The values of E_{on}, E_{off} and $R_{DS(on)}$ were obtained from the selected SiC MOSFET datasheet [9].

3.2.8.2 Diode Losses

When a diode is forward biased, a voltage drop exists across the PN junction. As a result, power is dissipated during conduction. The conduction loss of the diode can be expressed as

$$P_{D,cond} = V_F I_{avg}, \tag{3.34}$$

where V_F is the forward voltage drop of the diode and I_{avg} is the average current flowing through the device.
Another significant loss mechanism in a diode is the reverse-recovery loss. This loss occurs when a conducting diode becomes reverse biased and the stored charge within the junction must be removed before the device regains its blocking capability.
In LLC converters, reverse-recovery losses are minimised because the secondary-side rectifiers operate under near-ZCS conditions. However, reverse recovery may still occur if ZCS is not achieved or if non-ideal commutation conditions are present.
The reverse-recovery loss can be expressed as

$$P_{rr} = Q_{rr} V_R f_s, \tag{3.35}$$

where Q_{rr} is the reverse-recovery charge, V_R is the reverse voltage across the device, and f_s is the switching frequency.
The total diode loss is obtained by summing the conduction and reverse-recovery losses,

$$P_D = P_{D,cond} + P_{rr}. \tag{3.36}$$

The calculated power loss is then used for the thermal analysis of the device. The junction temperature can be estimated using the thermal resistance model,

$$T_j = T_c + P_D \left(R_{jc} + R_{cc}\right) \tag{3.37}$$

where T_j is the junction temperature, T_c is the coolant temperature, P_D is the power dissipated by the device, R_{jc} is the thermal resistance from the junction to the case, and R_{cc} is the thermal resistance from the case to the coolant.
The device temperature influences the electrical characteristics of the semiconductor. For example, the forward voltage drop of a diode and the on-state resistance of a MOSFET vary with temperature. Therefore, these parameters are updated iteratively until the calculated temperature converges to a steady-state value.

3.2.8.3 Core Losses

Core losses occur in magnetic materials when exposed to an alternating magnetic field. These losses include hysteresis losses and eddy-current losses, both increasing with operating frequency and flux density. The core loss is commonly estimated using the Steinmetz equation

$$P_{core} = k f^{\alpha} B^{\beta} V_{core}, \tag{3.38}$$

where k, α, and β are Steinmetz coefficients that depend on the core material and are typically obtained from manufacturer data. f is the operating frequency, B is the peak flux density, and V_{core} is the core volume.
Hence, the selection of a suitable core material and operating flux density is important for achieving high converter efficiency.

3.2.8.4 Winding Losses

Winding losses result from the resistive losses in the winding conductors. At high frequencies, the AC resistance becomes greater than the DC resistance due to the skin effect and proximity effect. Consequently, the winding losses increase with operating frequency.
The winding loss can be expressed as

$$P_{cu} = I_{rms}^2 R_{AC}, \tag{3.39}$$

where I_{rms} is the RMS current through the winding and R_{AC} is the effective AC resistance of the conductor.
The AC resistance can be related to the DC resistance by

$$R_{AC} = F_R(f) R_{DC}, \tag{3.40}$$

where $F_R(f)$ is the frequency-dependent resistance factor that accounts for the skin-effect and proximity-effect losses.
Consequently, the winding design, conductor dimensions, and operating frequency must be carefully selected to minimise copper losses in high-frequency magnetic components.
This chapter presented the theoretical background required for the design of the proposed SHB LLC converter. The operating principles of the LLC resonant tank, voltage balancing mechanism, rectification stage, transformer design, resonant inductor design, and converter loss model were discussed. The presented theory forms the basis for the component sizing and design methodology described in the next chapter.

4

Design Requirements

The converter is intended for an automotive high-voltage to low-voltage DC-DC conversion application. The main electrical and thermal requirements are summarised below.

4.1 High-Voltage Side Requirements

The converter shall operate from a high-voltage DC bus with the following voltage limits:

- Minimum operating voltage: 330 V
- Minimum voltage for full-power operation: 350 V
- Maximum voltage for full-power operation: 920 V
- Maximum operating voltage: 950 V
- Withstand voltage: 1050 V

Derating of the output power is permitted between 330 V and 350 V, and between 920 V and 950 V.

4.2 Low-Voltage Side Requirements

The converter output voltage range is specified as:

- Output voltage range: 6 V – 16 V
- Nominal output voltage: 15 V

The output operating strategy is defined as follows:

- Between 15 V and 16 V, the converter operates in constant-power mode.
- Below 15 V, the converter operates in current-limited mode.

4.3 Power Requirements

The converter shall satisfy the following power requirements:

- Continuous output power: 6 kW
- Peak output power: 9 kW
- Peak-power duration: 1.5 s

4.4 Thermal Requirements

The thermal design of the converter shall comply with the following cooling constraint:

- Maximum coolant temperature: 65°C

5

Converter Design

5.1 LLC Parameter Design

The selected converter topology consists of three gain stages that collectively determine the overall voltage conversion ratio. The first stage is the Stacked Half-Bridge (SHB), which can generate multiple voltage levels and therefore provides a variable gain between 0.25 and 0.5. The second stage is the LLC resonant tank, whose gain varies as a function of switching frequency and resonant tank parameters. The final stage is the high-frequency transformer, which provides a fixed voltage gain determined by the transformer turns ratio. The overall converter gain can therefore be expressed as

$$G_{\text{conv}} = G_{\text{SHB}} G_{\text{LLC}} \frac{N_s}{N_p} \tag{5.1}$$

where G_{SHB} is the gain contributed by the stacked half-bridge stage, G_{LLC} is the LLC resonant tank gain, and N_p/N_s represents the transformer voltage gain determined by the transformer turns ratio.
The maximum and minimum converter gains were determined from the specified input and output voltage limits according to

$$G_{\max} = \frac{V_{o,\max}}{V_{in,\min}} \tag{5.2}$$

$$G_{\min} = \frac{V_{o,\min}}{V_{in,\max}} \tag{5.3}$$

The required LLC gain was subsequently obtained after accounting for the gain provided by both the SHB stage and the transformer. Since the SHB can operate at gains of 0.25 and 0.5, the LLC resonant tank must compensate for the remaining conversion ratio. The maximum LLC gain is required when the SHB operates at a gain of 0.25, whereas the minimum LLC gain is required when the SHB operates at a gain of 0.5. Different transformer turns ratios were investigated in order to determine the most suitable operating region for the LLC resonant tank. For each candidate turns ratio, the required LLC gain range, average gain, gain variation and equivalent AC load resistance were evaluated. The minimum and maximum values of the output resistance were determined from the specified operating power range. These values were subsequently converted into equivalent AC load resistances using the first harmonic approximation,

$$R_{ac} = \frac{8n^2}{\pi^2} R_{dc} \tag{5.4}$$

where $n = N_p/N_s$ is the transformer turns ratio. Table 5.1 summarises the investigated transformer turns ratios and the corresponding LLC gain requirements.

Table 5.1: Transformer Ratio and LLC Gain Characteristics

$\mathbf{N_p/N_s}$	$G_{\min}$	$G_{\max}$	G_{avg}	ΔG	$R_{\text{ac,min}}$
7	0.68	1.36	1.02	0.68	0.79
8	0.23	1.75	0.99	1.52	1.31
9	0.11	1.75	0.93	1.63	1.31
10	0.25	1.94	1.10	1.69	1.62
11	0.13	1.94	1.03	1.81	1.62
15	0.38	1.45	0.92	1.08	3.65
16	0.40	1.55	0.98	1.15	4.15
17	0.43	1.65	1.04	1.22	4.69
18	0.21	1.65	0.93	1.43	4.69
19	0.23	1.75	0.99	1.52	5.25
20	0.24	1.84	1.04	1.60	5.85
21	0.25	1.94	1.10	1.69	6.48

As shown in Table 5.1, low transformer turns ratios result in small values of R_{ac}, leading to high quality factor requirements at maximum load. Although a turns ratio of 7 exhibited the smallest gain variation, the corresponding LLC tank operated at an unfavourably high quality factor and therefore did not satisfy the design objectives. Higher turns ratios produced larger values of R_{ac} and consequently reduced the required quality factor. The turns ratios of 15 and 16 were identified as the most suitable candidates as both provided acceptable gain characteristics, moderate gain variation and practical values of equivalent AC load resistance. Initially, a turns ratio of 16 was selected as the preferred electrical design solution due to its slightly lower required quality factor. However, subsequent transformer design investigations showed that the 15-turn configuration resulted in a more favourable magnetic design by reducing the required core area and air-gap length while maintaining acceptable LLC gain characteristics. Consequently, a transformer turns ratio of 15 was selected for the final converter design.

Following the transformer ratio selection, the LLC resonant tank parameters were determined using the First Harmonic Approximation (FHA). The minimum and maximum values of R_{ac} were calculated over the complete operating range of the converter. The maximum value of R_{ac} corresponded to the light-load operating condition. A light-load power level of 50 W was assumed for output voltages between 13 V and 16 V. This operating point represents a practical charging condition in which the auxiliary battery is fully charged and the load demand is minimal. Using the required gain range together with the calculated values of $R_{ac,min}$ and $R_{ac,max}$, the quality factor

$$Q = \frac{\omega_r L_r}{R_{ac}} \tag{5.5}$$

and inductance ratio

$$m = \frac{L_m}{L_r} \tag{5.6}$$

were varied to obtain suitable gain characteristics. The design objective was to maximise the achievable quality factor while maintaining the inductance ratio within the recommended range of 4 to 7. The LLC gain equation derived in Chapter 3 was used to generate the corresponding gain curves. After evaluating multiple combinations of Q and m, the resonant tank parameters were selected such that the required gain range was satisfied while maximising the magnetising inductance and minimising the resonant capacitance. The final selected resonant tank parameters are summarised in Table 5.2.

Table 5.2: Selected LLC Resonant Tank Parameters

Parameter	Value
C_r	498 nF
L_r	5.08 μH
L_m	28.46 μH

5.2 Transformer Design

Following the LLC resonant tank design, the transformer was designed to satisfy the electrical requirements imposed by the converter while maintaining acceptable flux density, magnetising inductance and air-gap length.
The transformer design was based on the specifications obtained from the LLC design stage. The resonant tank design resulted in a required magnetising inductance of 28.46 μH and a resonant frequency of 100 kHz. The transformer was implemented using a DMR95 ferrite EE core[7].
Although a transformer turns ratio of 16:1:1 was initially identified as a suitable candidate during the LLC gain analysis, subsequent magnetic design investigations demonstrated that both the 15:1:1 and 16:1:1 solutions satisfied the required LLC gain characteristics. Therefore, the final turns selection was based on magnetic design constraints, including flux density, effective core area and air-gap length.
To ensure that the transformer was designed for the worst-case magnetic stress condition, the maximum value of the volt-second term was identified over the entire converter operating range. Since the transformer flux density is proportional to the applied volt-seconds, the critical operating point corresponds to the maximum value of

$$\frac{VD}{f_{sw}} \tag{5.7}$$

where V is the transformer primary voltage, D is the bridge duty factor and f_{sw} is the switching frequency.
The highest volt-second condition was observed at:

- Primary voltage, $V = 810$ V
- SHB gain, $D = 0.25$
- Switching frequency, $f_{sw} = 70.22$ kHz

resulting in

$$\left(\frac{VD}{f_{sw}}\right)_{\max} = 2.88 \times 10^{-3} Vs \tag{5.8}$$

This operating point produces the maximum transformer flux density and was therefore used as the basis for the magnetic design.
The effective core area was calculated using the core area expression presented in (3.17). Several maximum flux-density limits were investigated in order to evaluate the trade-off between core size and air-gap length.
Initially, a conservative flux-density limit of 0.1 T was considered. Although this resulted in low magnetic loading of the ferrite core, the corresponding effective core area was found to be excessively large. According to (3.22), increasing the effective core area also increases the achievable magnetising inductance, thereby requiring a larger air gap in order to maintain the specified value of L_m.
Since large air gaps increase magnetic fringing effects and complicate practical implementation, several candidate designs were investigated. For each design, the effective core area was calculated using (3.17) and the corresponding air-gap requirement was calculated using (3.22).
The resulting comparison is presented in Table 5.3.

Table 5.3: Comparison of candidate transformer designs

$B_{\max}$ **(T)**	A_e **(mm^2)**	**Gap (mm)**
0.10	862	8.5
0.20	432	4.3
0.25	345	3.43
0.3	287	2.86

As shown in Table 5.3, reducing the operating flux density significantly increases the required effective core area. Although this reduces magnetic loading of the ferrite material, it also requires a substantially larger air gap in order to achieve the specified magnetising inductance.
The design corresponding to a flux density of 0.1 T required an air gap approaching 10 mm. Such an air gap was considered impractical due to excessive fringing flux and increased difficulty in transformer implementation. Similarly, the 0.2 T and 0.25 T designs required air gaps exceeding the preferred design limit of approximately 4 mm.
Conversely, increasing the allowable flux density reduces the required core area and consequently reduces the required air-gap length. However, excessive flux densities reduce the available saturation margin of the ferrite material and increase core losses.
A maximum operating flux density of approximately 0.284 T was therefore selected as the most suitable compromise between core size, saturation margin and air-gap length. This operating point represents the worst-case magnetic loading condition and was therefore selected as the basis for the transformer design. Under normal operating conditions, the converter is expected to operate at lower magnetic stress levels due to the action of the control system. This resulted in an effective core area of 307 mm^2 and an air-gap length of 3 mm, satisfying the imposed maximum air-gap constraint while maintaining sufficient separation from the ferrite saturation region.
A comparison between the 15-turn and 16-turn transformer designs was subsequently performed. Although the 16-turn solution satisfied the electrical requirements of the LLC converter, the resulting magnetic design required either a larger effective core

area or a larger air gap to maintain an acceptable operating flux density. As the air gap is directly proportional to the square of the number of turns.
The 15-turn solution provided a more favourable compromise between flux density, effective core area and air-gap length while preserving the desired LLC gain characteristic. Consequently, 15 primary turns were selected for the final transformer design.
After determining the core geometry, the required winding window area was evaluated using (3.24) to (3.26). The maximum primary winding RMS current obtained from simulation was 24 A. Each half of the centre-tapped secondary winding carried a maximum of 100.84 A RMS.
The required conductor cross-sectional areas were calculated from the RMS winding currents and the selected current density. The total required copper area was then used together with the window utilisation factor to determine the minimum window area.
A window area of 210.25 mm^2 was selected, resulting in

$$\frac{A_w}{k_w} = \frac{210.25}{324} = 0.649 \tag{5.9}$$

which provides adequate space for the primary winding, centre-tapped secondary winding, insulation requirements and practical manufacturing tolerances.
The transformer employed a centre-tapped secondary winding consisting of one turn per secondary half winding. Consequently, the transformer turns ratio was selected as

$$N_p : N_s = 15 : 1 : 1 \tag{5.10}$$

where the secondary winding was implemented as a centre-tapped configuration to facilitate output rectification.
The final transformer design parameters are summarised in Table 5.4.

Table 5.4: Final transformer design parameters

Parameter	Value
Core Type	EE
Core Material	DMR95
Primary Turns (N_p)	15
Secondary Turns (N_s)	1 + 1
Effective Magnetic Path Length (l_e)	200 mm
Magnetising Inductance (L_m)	28.46 μH
Effective Core Area (A_e)	324 mm^2
Window Area (A_w)	210.25 mm^2
Peak Flux Density ($B_{\max}$)	0.284 T
Current Density (J)	4 A/mm^2
Air-Gap Length	3.2 mm
Primary RMS Current	24 A
Secondary RMS Current (per winding)	100.84 A

The selected transformer design represents a compromise between saturation margin, core volume, air-gap length and manufacturability. By selecting a peak flux density

of approximately 0.284 T, the required effective core area and air-gap length were significantly reduced while maintaining adequate distance from the saturation limit of the DMR95 ferrite material. The final design therefore satisfies the electrical and magnetic requirements of the proposed stacked half-bridge LLC converter.
The final transformer design therefore represents the outcome of a multi-objective trade-off between LLC gain requirements, flux density, magnetising inductance, effective core area and air-gap length. Although the initial electrical design favoured a 16:1:1 turns ratio, the final magnetic design demonstrated that a 15:1:1 transformer provided a more practical implementation with lower core area and reduced air-gap requirements while maintaining the required converter gain characteristics.

5.2.1 Winding Design

The transformer windings were designed based on the maximum operating frequency of 300 kHz. At this frequency, skin-effect losses become significant and must therefore be considered during conductor selection. The skin depth was calculated using (3.31), resulting in a skin depth of approximately 0.12 mm for copper.
The required conductor cross-sectional area for each winding was determined using (3.24) based on the RMS current obtained from MATLAB simulation and an allowable current density of 4 A/mm^2. Due to the relatively high operating frequency, a Litz-wire conductor was selected for the primary winding to minimise AC resistance caused by skin effect. For the secondary winding, copper foil conductors were selected because of the significantly higher RMS current and single-turn winding configuration.
The winding design parameters obtained using (3.24) to (3.26) together with the skin-effect considerations of (3.31) and (3.32) are summarised in Table 5.5.

Table 5.5: Transformer winding design parameters

Parameter	**Primary Winding**	**Secondary Winding**
Operating Frequency	300 kHz	300 kHz
RMS Current	24 A	100.84 A
Current Density	4 A/mm^2	4 A/mm^2
Required Copper Area	6.00 mm^2	25.21 mm^2
Skin Depth (Cu)	0.12 mm	0.12 mm
Selected Conductor	Litz Wire	Copper Foil
Strand/Foil Size	0.2 mm	0.1 mm × 18.3 mm
Area per Strand/Foil	0.0314 mm^2	1.8 mm^2
Required Parallel Conductors	200 strands	14 foils
Turns	15	1 + 1
Mean Length Per Turn	76.6 mm	76.6 mm
Total Conductor Length	1.149 m	0.0766 m
DC Resistance (R_{DC})	3.15 mΩ	0.052 mΩ

Although the calculated DC resistance of the primary winding is 3.15 mΩ, an effective resistance of approximately 31 mΩ was used in the loss model to account for interconnection resistance, termination resistance, solder joints, and additional AC

resistance effects. Similarly, an additional resistance contribution was included for the secondary-side conductors. Similarly 1.5mΩ was assumed for each secondary winding. The total copper area required for the transformer was calculated as

$$A_{Cu,total} = A_{Cu,p} + 2A_{Cu,s} = 56.42 \text{ mm}^2 \tag{5.11}$$

where the secondary winding consists of two centre-tapped sections. Using the selected window area of 219.6 mm^2, the overall window utilisation factor obtained from (3.26) is

$$K_u = \frac{A_{Cu,total}}{A_w} = \frac{56.42}{219.6} = 0.26 \tag{5.12}$$

corresponding to an overall fill factor of approximately 25.7%. For the selected Litz-wire construction, a packing factor of 0.6 was assumed. The corresponding primary winding bundle area is therefore

$$A_{bundle} = \frac{6}{0.6} = 10 \text{ mm}^2 \tag{5.13}$$

which remains well within the available window area. Consequently, the selected winding arrangement satisfies the geometric constraints of the transformer design.
The primary winding consists of 15 turns implemented using 200 strands of Litz wire. The total conductor length is estimated using the mean length per turn (MLT),

$$l_{cond} = N \times MLT = 1.149 \text{ m} \tag{5.14}$$

The total copper cross-sectional area is

$$A = 200 \times 0.0314 = 6.28 \text{ mm}^2. \tag{5.15}$$

The DC resistance of the primary winding is therefore

$$R_{DC} = \rho \frac{l_{cond}}{A} = 3.15 \text{ m}\Omega, \tag{5.16}$$

where $\rho = 1.724 \times 10^{-8}\ \Omega \cdot m$ is the resistivity of copper.
The secondary winding consists of one turn implemented using 14 parallel copper foils. The total conductor cross-sectional area is

$$A = 14 \times 1.83 = 25.62 \text{ mm}^2. \tag{5.17}$$

Using the mean length per turn of 76.6 mm, the conductor length is

$$l_{cond} = 76.6 \text{ mm} = 0.0766 \text{ m}. \tag{5.18}$$

The DC resistance of the secondary winding is therefore

$$R_{DC} = \rho \frac{l_{cond}}{A} = 0.0515 \text{ m}\Omega. \tag{5.19}$$

Although the calculated copper resistance is 3.15 mΩ, additional interconnection resistance, solder joints, termination resistance and AC resistance effects increase the effective winding resistance used in the loss calculation to approximately 31mΩ.

5.2.2 Leakage Inductance Estimation

At this stage of the design, the detailed transformer winding arrangement has not yet been finalised. Consequently, an exact calculation of the transformer leakage inductance is not possible since it depends strongly on the winding layout, spacing between windings, insulation thickness, and interleaving strategy.
For the first design iteration, the transformer leakage inductance is estimated using a typical coupling coefficient for high-frequency ferrite transformers. A coupling coefficient between 0.95 and 0.99 is commonly reported for well-coupled power transformers. Therefore, an average value of

$$k = 0.97 \tag{5.20}$$

is assumed for the initial design iteration.
The transformer leakage inductance is related to the coupling coefficient by

$$L_{lk} = L_m \left(\frac{1-k}{k} \right) \tag{5.21}$$

where L_m is the transformer magnetising inductance.
The estimated transformer leakage inductance is

$$L_{lk} = 0.88\ \mu H. \tag{5.22}$$

Since the transformer leakage inductance contributes to the resonant inductance, the required external resonant inductance is

$$L_{ext} = L_r - L_{lk} \tag{5.23}$$

Therefore, for the first design iteration, the transformer leakage inductance is assumed to be approximately 0.88 μH and an external resonant inductor of approximately 4.2 μH is required to achieve the desired resonant inductance.
The assumed coupling coefficient is consistent with typical values reported for well-coupled high-frequency ferrite transformers in power electronic applications [10].
The estimated leakage inductance is used only for the first design iteration. The final value depends on the winding layout and should be verified experimentally.

5.3 Resonant Inductor Design

The LLC resonant tank requires a total resonant inductance of 5.08 μH. Based on the leakage inductance estimation presented in the previous section, approximately 0.88 μH is provided by the transformer leakage inductance. Therefore, an external resonant inductor of approximately 4.2 μH is required.
The resonant inductor was designed using the maximum resonant-tank current obtained from simulation. A DMR95 ferrite EE core was selected to satisfy the inductance, current and thermal requirements while maintaining adequate saturation margin.
The core area, number of turns and air-gap length were determined using the inductor design equations presented in Chapter 3. A maximum flux density of 0.3 T was

selected to ensure sufficient margin from ferrite saturation, while an air-gap length of approximately 3 mm was used to achieve the required inductance.
Due to the maximum operating frequency of 300 kHz, a Litz-wire conductor was selected to minimise AC resistance caused by skin-effect and proximity-effect losses. The final resonant inductor design parameters are summarised in Table 5.6.

Table 5.6: Resonant inductor design parameters

Parameter	Value
Core Type	EE
Core Material	DMR95
Inductance (L_r)	4.2 μH
Effective Core Area (A_e)	200 mm^2
Effective Path Length (l_e)	200 mm
Number of Turns (N)	7
Air-Gap Length (g)	3 mm
Peak Flux Density ($B_{\max}$)	0.3 T
RMS Current	24 A
Peak Current	60 A
Conductor Type	Litz Wire
Litz Construction	200 $\times$ 0.2 mm
Maximum Frequency	300 kHz
Stored Energy	7.56 mJ

The resulting resonant inductor satisfies the required inductance, current density and current ratings while maintaining an acceptable flux density and a practical air-gap length. The selected Litz-wire conductor minimizes high-frequency winding losses, making the design suitable for operation over the full converter frequency range. EE-core geometry was selected for the resonant inductor design. The effective core area, magnetic path length and air-gap dimensions of this core were subsequently used in the design calculations presented in this section.

5.4 Modulation Techniques

The proposed converter employs a Stacked Half-Bridge (SHB) topology, which is capable of generating three different output voltage levels. This additional degree of freedom enables the voltage applied to the LLC resonant tank to be controlled using both voltage-level selection and frequency modulation. The SHB converter can operate in three different modes:

- **Mode 1**: The output voltage varies between 0 and V_{dc}.
- **Mode 2**: The output voltage varies between 0 and $V_{dc}/2$.
- **Mode 3**: Hybrid operation, where the output voltage can take the values 0, $V_{dc}/2$, and V_{dc}.

The required output voltage level is generated by appropriate switching of the four active devices in the SHB converter. The switching combinations and their corresponding output voltage levels are summarised in Table 5.7.

Table 5.7: SHB switching states and output voltage levels

State	S1	S2	S3	S4	V_o
1	1	0	0	1	V_{dc}
2	1	0	1	0	$V_{dc}/2$
3	0	1	0	1	$V_{dc}/2$
4	0	1	1	0	0

In Mode 1, switches S_1 and S_4 are enabled, producing the maximum bridge output voltage of V_{dc}. In Mode 2, either the switching combination (S_1, S_3) or (S_2, S_4) is activated, resulting in an output voltage of $V_{dc}/2$. In Mode 3, the converter alternates between the available voltage states to generate a hybrid output waveform containing the voltage levels 0, $V_{dc}/2$, and V_{dc}. Since the LLC resonant tank predominantly responds to the fundamental component of the bridge voltage, the fundamental harmonic magnitude of each operating mode can be obtained from the Fourier series representation of the corresponding waveform. The resulting fundamental voltage magnitudes are summarised in Table 5.8.

Table 5.8: Fundamental voltage components of SHB operating modes

Mode	$V_{1,\text{peak}}$	$V_{1,\text{rms}}$
Mode 1	$\frac{2V_{dc}}{\pi}$	$\frac{\sqrt{2}V_{dc}}{\pi}$
Mode 2	$\frac{V_{dc}}{\pi}$	$\frac{V_{dc}}{\sqrt{2}\pi}$
Mode 3	$\frac{V_{dc}}{\pi} < V_{1,\text{peak}} < \frac{2V_{dc}}{\pi}$	$\frac{V_{dc}}{\sqrt{2}\pi} < V_{1,\text{rms}} < \frac{\sqrt{2}V_{dc}}{\pi}$

Mode 3 forms the basis of the proposed modulation strategy. By varying the duration of the individual voltage levels, the fundamental voltage applied to the LLC tank can be continuously adjusted while simultaneously providing a mechanism for balancing the voltages across the input capacitors. By selecting the appropriate voltage level, the SHB topology reduces the gain requirement imposed on the LLC resonant tank and extends the operating range of the converter. The selection of the operating mode depends on the required LLC gain and the capacitor-voltage balancing requirements. The adopted modulation strategy is discussed in the following section.

5.4.1 Capacitor Voltage Balancing

The stacked half-bridge converter employs two series-connected DC-link capacitors, C_1 and C_2, which ideally share the input voltage equally. In Mode 1 operation, where the bridge voltage alternates between 0 and V_{dc}, neither capacitor is individually involved in the power-transfer process. Consequently, the average charge stored in the capacitors remains unchanged and no significant voltage imbalance is observed. In contrast, capacitor-voltage imbalance becomes a concern whenever the

intermediate voltage level $V_{dc}/2$ is utilised. According to Table 5.7, the intermediate voltage level is generated using either State 2 or State 3. During these states, the resonant current flows through only one of the two DC-link capacitors, causing one capacitor to be charged while the other is discharged. In State 2, capacitor C_1 is charged, whereas in State 3, capacitor C_2 is charged. Consequently, the average capacitor currents are directly influenced by the frequency and duration of occurrence of these switching states. If the utilisation of States 2 and 3 is not properly balanced, the capacitor voltages gradually diverge, producing unequal voltage stress across the converter switches. To investigate the balancing behaviour of the proposed converter, five modulation strategies were evaluated.

5.4.1.1 Modulation Strategy 1

The first modulation strategy corresponds to Mode 2 operation, where the output voltage alternates between 0 and $V_{dc}/2$ using States 2 and 4. The resulting waveforms are shown in Fig. 5.1. Since only one capacitor participates in the charging and discharging process, capacitor C_2 continuously loses charge and its voltage gradually decreases. This causes severe capacitor-voltage imbalance and eventually prevents normal converter operation. Therefore, this modulation strategy was rejected.

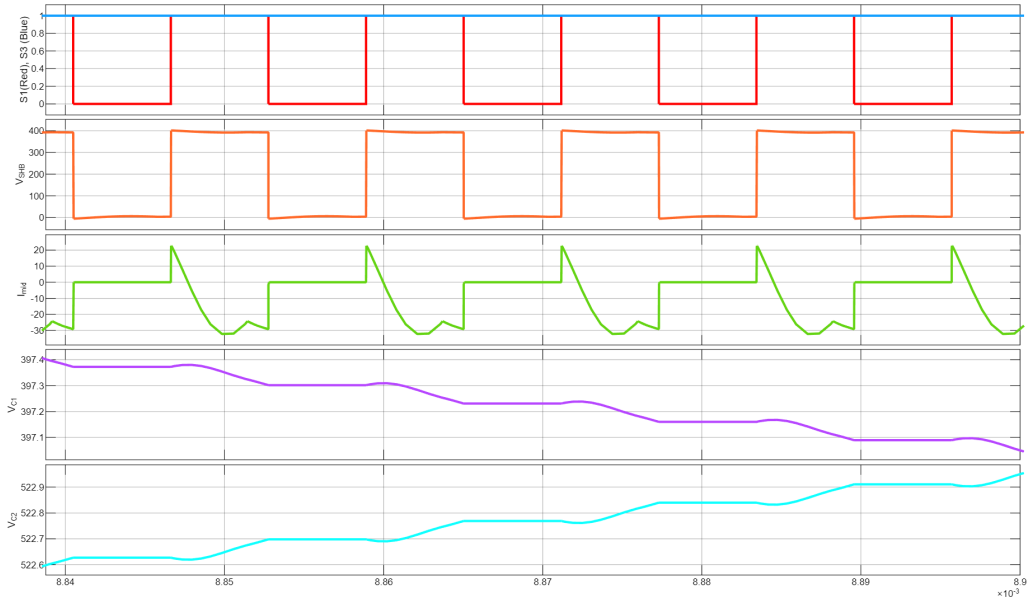


Figure 5.1: Modulation Strategy 1 waveforms

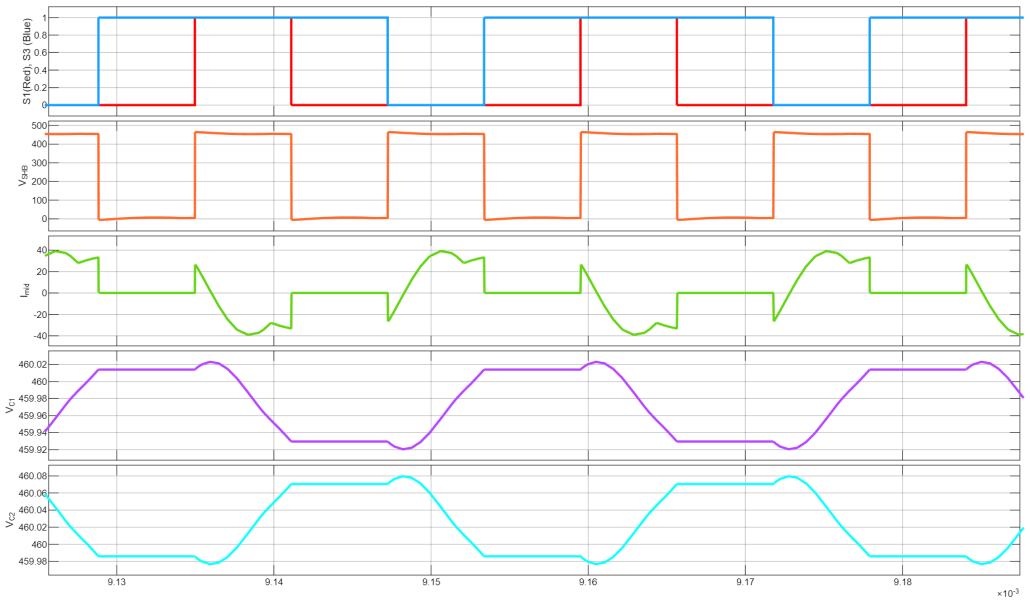


Figure 5.2: Modulation Strategy 2 waveforms

5.4.1.2 Modulation Strategy 2

In the second strategy, States 2 and 3 are alternately used to generate the $V_{dc}/2$ voltage level. Since State 2 primarily charges C_1, while State 3 primarily charges C_2, the two capacitors are utilized more evenly. As shown in Fig. 5.2, the voltage imbalance is significantly reduced. However, a noticeable voltage offset still exists between the capacitor voltages. Additionally, the ON durations of the switches are not identical, which may result in unequal power losses and increased thermal stress in two of the four switches. This uneven thermal loading can lead to faster device aging and reduced switch lifetime.

5.4.1.3 Modulation Strategy 3

The third case investigates hybrid operation, where all switching states are utilised to generate a three-level output waveform. Although both intermediate voltage states are used, the capacitor voltages do not remain balanced, as shown in Fig. 5.3. This is because the resonant current decreases during the second occurrence of the $V_{dc}/2$ level, resulting in unequal charge transfer between the capacitors.

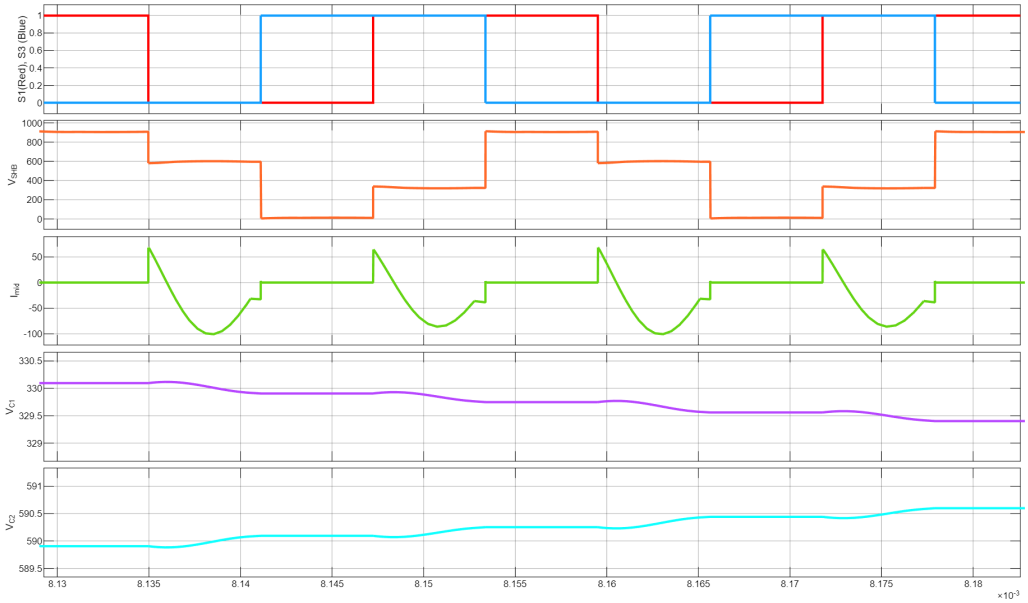


Figure 5.3: Modulation Strategy 3 waveforms

5.4.1.4 Modulation Strategy 4

A simplified hybrid modulation strategy was also investigated, where only one intermediate state is used to generate the $V_{dc}/2$ level. This results in unequal utilisation of the two capacitors and a voltage difference develops between them as shown in Fig. 5.4. The imbalance becomes more pronounced as the switching frequency decreases. Therefore, this approach was not suitable for the proposed converter.

5.4.1.5 Modulation Strategy 5-Interleaved

To overcome the limitations of the previous methods, an interleaved modulation strategy was implemented [5]. During one switching cycle, the $V_{dc}/2$ level is generated using S_1 and S_3, while during the next switching cycle it is generated using S_2 and S_4. By alternating the capacitor utilised in each cycle, the average charge transfer through C_1 and C_2 becomes nearly equal. Simulation results confirm that the capacitor voltages remain balanced, and therefore this technique was selected for the final converter implementation. The capacitor-voltage waveforms obtained using the interleaved modulation strategy are shown in Appendix Fig A.5 and demonstrate successful voltage balancing between the two DC-link capacitors.

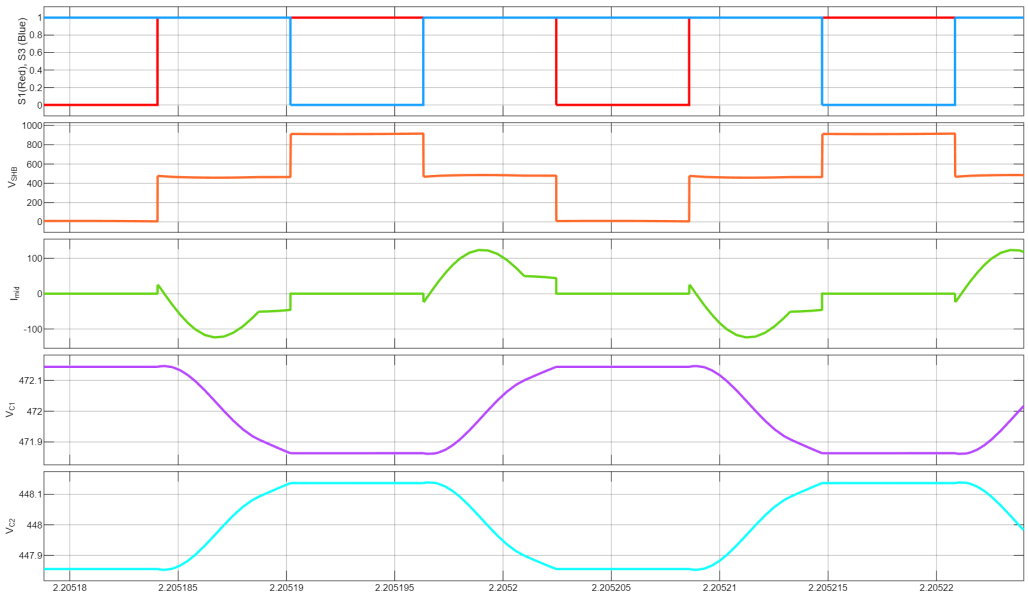


Figure 5.4: Strategy 4 waveforms

5.4.2 Implementation of the Interleaved PWM Strategy

The interleaved PWM strategy is implemented by comparing a high-frequency triangular carrier waveform with a square-wave modulation signal. The triangular waveform varies between -1 and 1, whereas the modulation signal varies between 0 and 1.

The comparison between the carrier waveform and the modulation signal generates the gate pulses for switches S_1 and S_3. The complementary gate signals required for switches S_2 and S_4 are subsequently generated while maintaining the required dead time.

Fig. 5.5 illustrates the triangular carrier waveform, modulation signal and the resulting gate pulses generated by the PWM modulator.

The proposed modulation method provides three independent control variables that can be used to regulate the converter operation.

- **Switching Frequency** :The switching frequency is used to control the gain of the LLC resonant tank. Changing the frequency modifies the operating point on the LLC gain curve and therefore regulates the output voltage.
- **Duty factor** :The duty factor controls the effective gain produced by the SHB converter. This parameter is adjusted by varying the magnitude of the modulation signal. Here, a parameter D is utilised to define the on-time of Switch S3 during its first half of the interleaved switching period
- **Phase Shift** :The phase shift is used to achieve capacitor-voltage balancing. By modifying the relative phase between the carrier waveform and modulation signal, the charging and discharging intervals of capacitors C_1 and C_2 can be controlled.

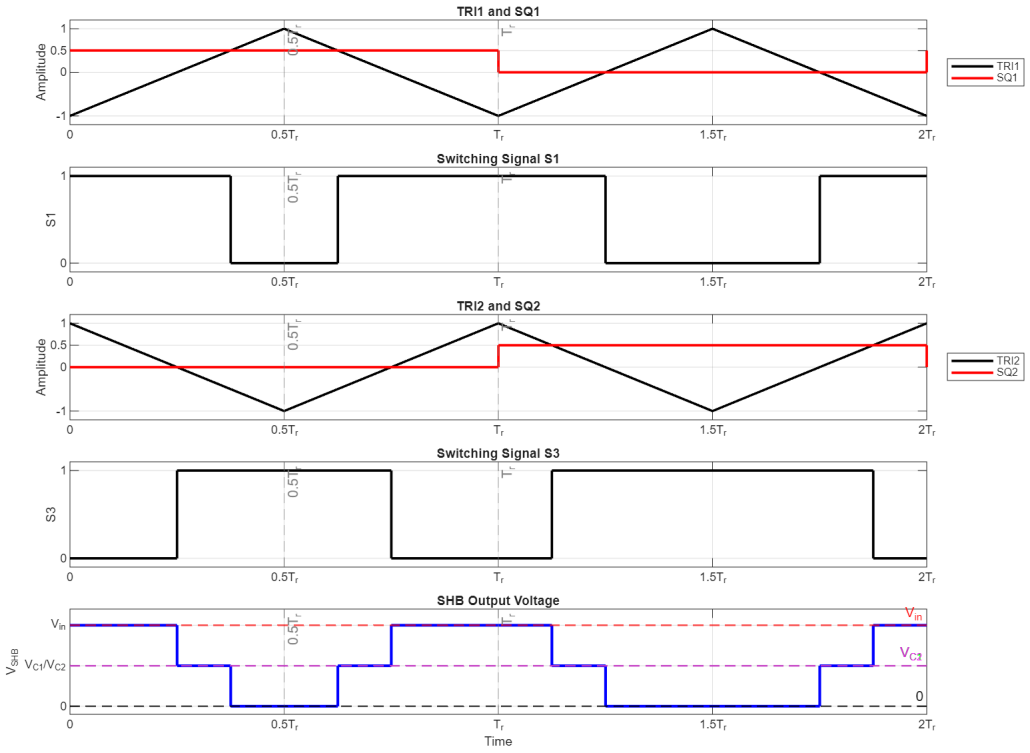


Figure 5.5: Implementation of Interleaved Switching

5.4.3 Controller Structure

The proposed controller requires three voltage measurements and one current measurement in order to regulate the converter and maintain capacitor-voltage balance. The measured quantities are

- Input voltage, V_{in},
- Lower capacitor voltage, V_{C2},
- Output voltage, V_o,
- Output current, I_o.

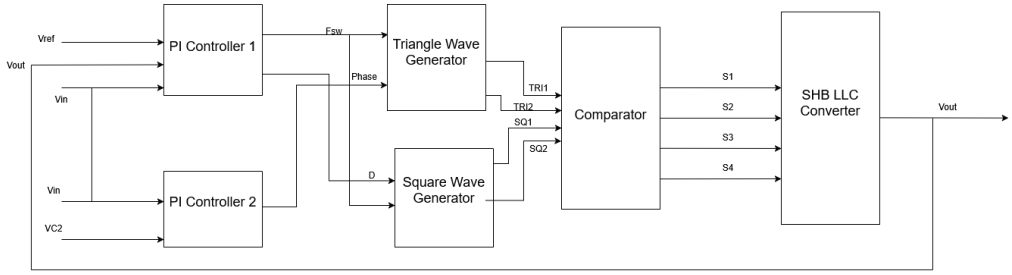


Figure 5.6: Constant Voltage Control System Implementation

The output-voltage and output-current measurements are used to implement the

required constant-current (CC) and constant-voltage (CV) charging modes. Meanwhile, the capacitor-voltage measurement is used by the balancing controller to maintain equal voltage sharing between the two DC-link capacitors. Fig. 5.6 shows the overall control structure employed in the proposed converter. Although the proposed controller structure supports both constant-current (CC) and constant-voltage (CV) operation, only the CV control mode was implemented and evaluated within the scope of this thesis.

6

Results and Discussion

This chapter presents the simulation results of the proposed Stacked Half-Bridge LLC converter. The converter performance was evaluated over the complete operating range by varying the input voltage, output current and SHB duty factor. The investigation focuses on converter efficiency, power losses, thermal performance, capacitor voltage balancing and overall converter operation.

6.1 Evaluation Conditions

The converter was evaluated under the operating conditions specified in Chapter 4. The investigated operating variables are summarised below.

- Input voltage: 330 V – 950 V
- Output voltage: 15 V
- Output current: 3.3 A – 300 A
- SHB duty factor: 0 – 0.5

For each operating point, the following quantities were evaluated:

- Converter efficiency
- Semiconductor losses
- Magnetic losses
- Total converter losses
- Junction temperatures of the HV switches

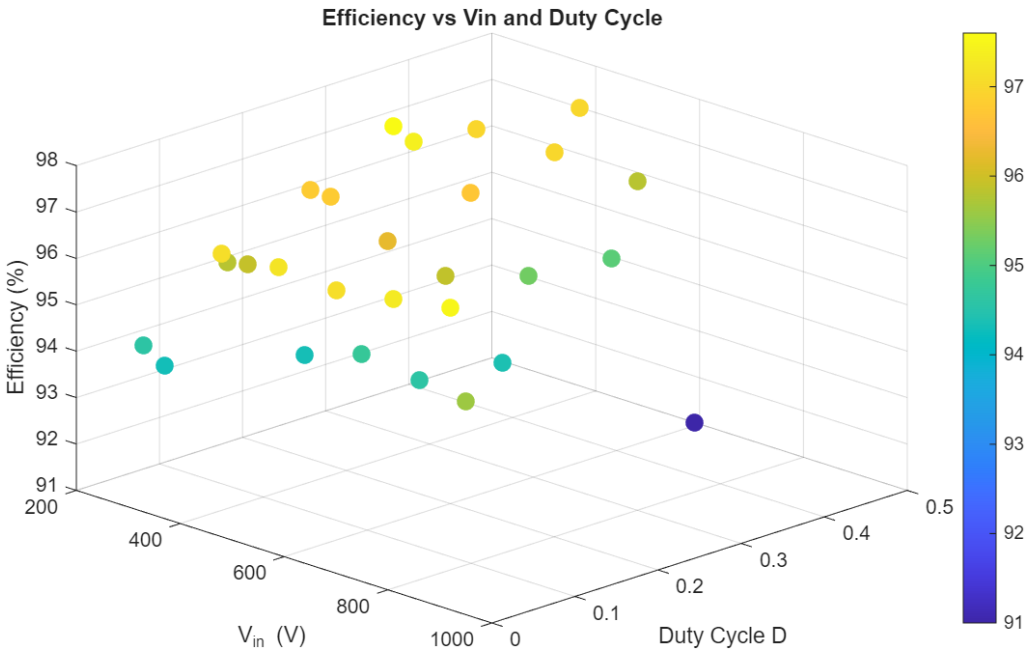


Figure 6.1: Converter efficiency as a function of input voltage and duty factor.

6.2 Influence of Input Voltage

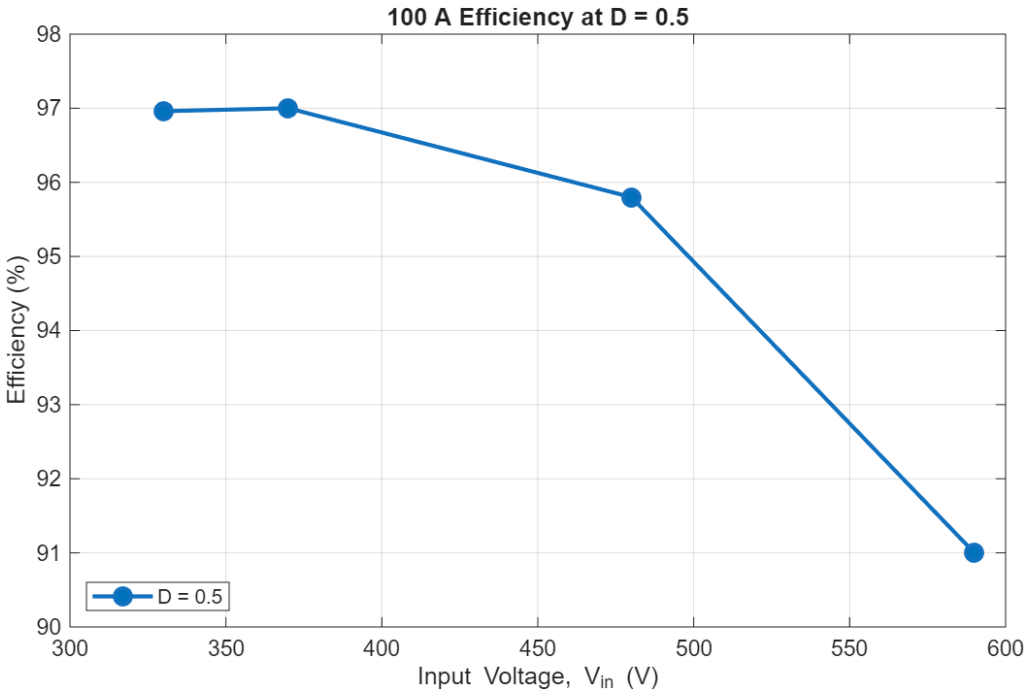


Figure 6.2: Converter efficiency as a function of input voltage.

As shown in Fig. 6.2, the converter maintains high efficiency throughout the investigated input-voltage range. At low input voltages, a higher LLC gain is required and the converter therefore operates closer to resonance at lower switching frequencies. As the input voltage increases, the LLC gain requirement decreases and the converter operates at higher switching frequencies. The increased switching frequency leads to higher switching losses in the primary-side MOSFETs as well as increased magnetic losses in the transformer and resonant inductor. Consequently, the overall converter efficiency decreases slightly at higher input voltages. The reduction becomes more pronounced above approximately 450 V, where frequency-dependent losses begin to dominate the total loss profile.

6.3 Converter Losses

Figure 6.3 shows the variation of total converter losses with input voltage at 100A output current. The total converter losses increase with increasing input voltage.

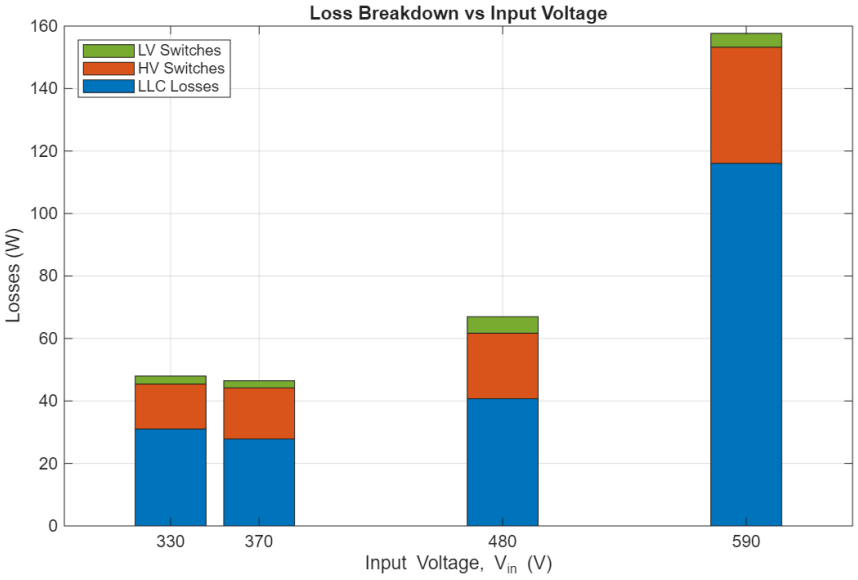


Figure 6.3: Total converter losses as a function of input voltage.

This is mainly due to higher switching losses in the primary-side MOSFETs caused by the increased voltage stress and operating frequency. Furthermore, the magnetic losses of the LLC resonant tank rise significantly because core losses are strongly dependent on both flux density and frequency, as described by the Steinmetz equation. As a result, the transformer and resonant inductor contribute an increasing share of the total converter losses at higher input voltages.

6.4 Influence of Output Current

Fig. 6.4 shows the converter efficiency as a function of output current at 810V and D=0.

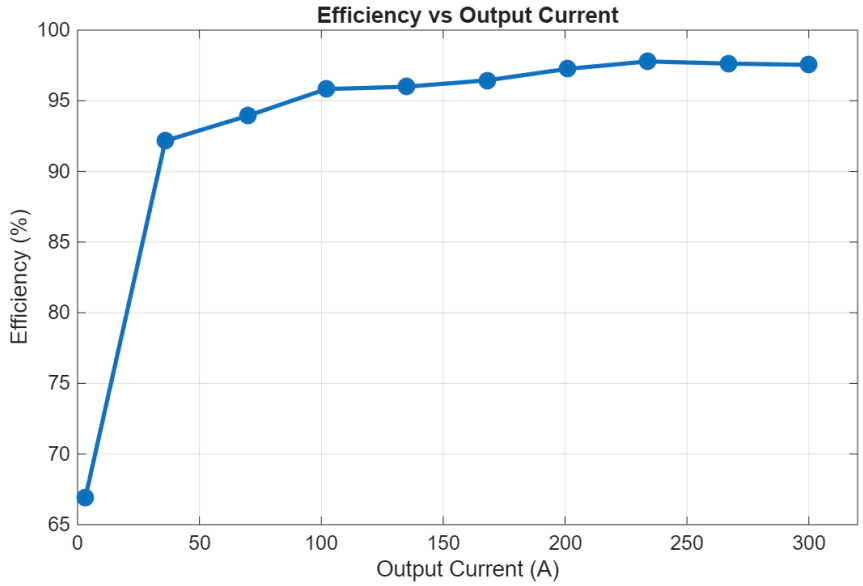


Figure 6.4: Total converter efficiency as a function of output current at 810V.

At low output currents, fixed losses such as magnetic losses and switching losses represent a significant proportion of the transferred power. Consequently, the efficiency is reduced. As the output current increases, the fixed losses become less significant relative to the output power and the efficiency improves. At the highest load currents, conduction losses become dominant and limit further efficiency improvement.

6.5 Influence of SHB Duty Factor

Figure 6.5 illustrates the influence of SHB duty factor on converter efficiency at 590V and 100A.
The SHB duty factor directly influences the gain contribution of the stacked half-bridge stage and therefore affects the operating point of the LLC resonant tank. The highest efficiency is achieved at D = 0, where the converter operates with reduced switching frequency (half that required when D > 0) and lower switching losses. As the duty factor increases, the LLC converter must operate at higher switching frequencies to maintain output-voltage regulation. The resulting increase in switching and magnetic losses causes a gradual reduction in converter efficiency.

6.6 Thermal Performance

The thermal performance of the primary-side switches was evaluated using the calculated semiconductor losses and device thermal models. Figure 6.6 illustrates the variation of primary-side switch temperature under different output current values. The switch temperature follows the same trend observed in the converter loss calculations. The highest temperatures occur under operating conditions where the converter experiences the greatest conduction and switching losses. Nevertheless,

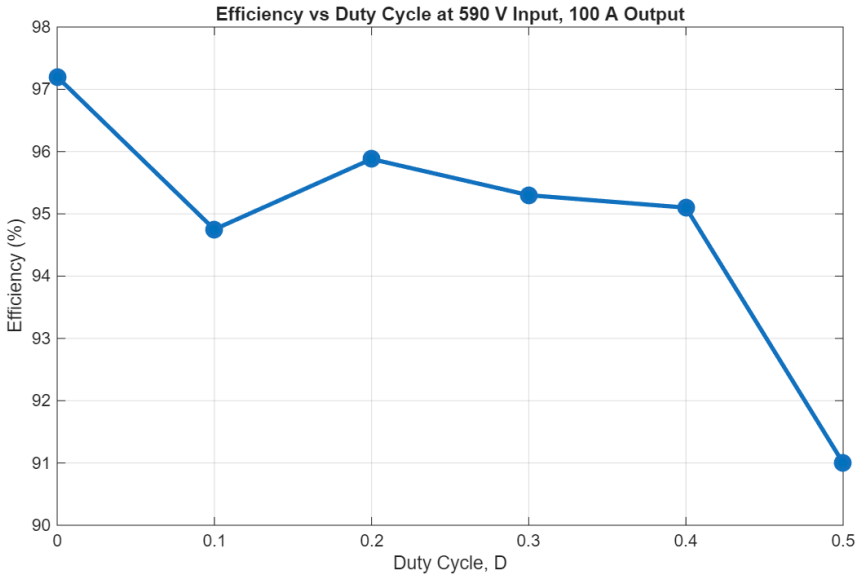


Figure 6.5: Converter efficiency as a function of SHB duty factor.

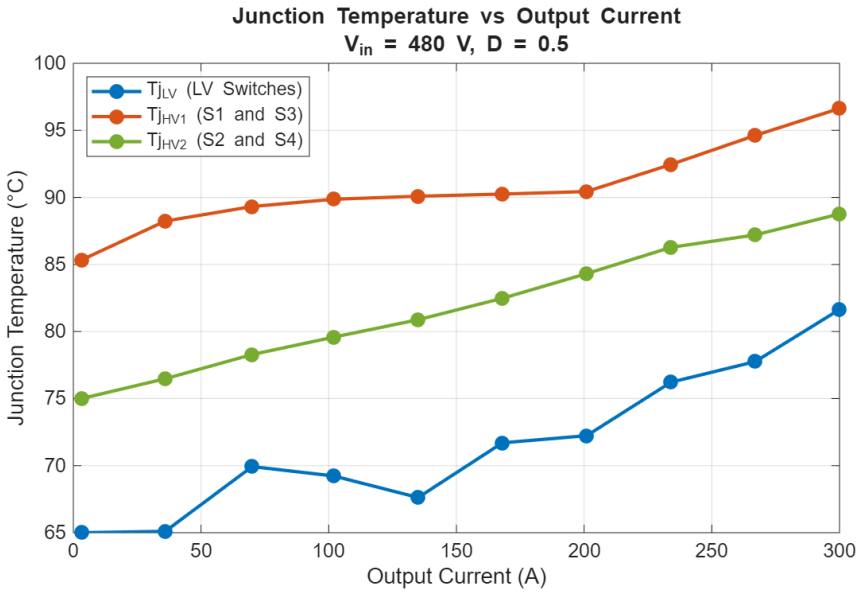


Figure 6.6: Primary-side switch temperature.

the calculated temperatures remain within the allowable operating limits of the selected semiconductor devices [8] and [9].

6.7 Resonant Inductor Magnetic Performance

Although the converter operated correctly over most of the investigated operating range, the resonant inductor was found to operate close to the saturation limit under certain low-frequency, high-current operating conditions. Figure 6.7 shows the resonant-inductor flux density under this operating condition.
The highest flux-density values were observed when the converter operated at high

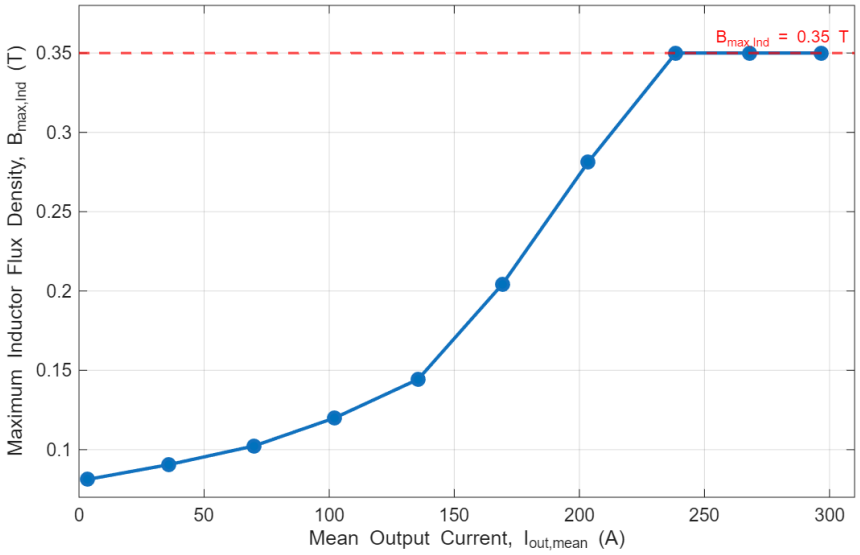


Figure 6.7: Resonant-inductor flux density during low-frequency, high-current operation.

gain, requiring lower switching frequencies and increased resonant current. Under these conditions, the magnetic loading of the resonant inductor increased significantly, causing the peak flux density to approach the saturation limit of the selected ferrite material. Although magnetic saturation was not observed throughout the entire operating range, the results indicate that the resonant inductor represents one of the most critical magnetic components during high-gain operation. Additional optimisation of the resonant-inductor design may therefore be considered in a future design iteration.

6.8 Summary of Results

The simulation results demonstrated that the proposed SHB LLC converter is capable of satisfying the specified operating requirements over a wide input voltage range. The converter successfully regulated the output voltage while operating from 330 V to 950 V and delivering output currents up to 300 A. The combination of SHB duty-ratio control and LLC frequency modulation provided sufficient gain variation to satisfy the converter requirements throughout the investigated operating range. A maximum calculated efficiency of 97.2% was achieved. The high efficiency was primarily attributed to the resonant operation of the LLC tank and the reduction of switching losses. However, the reported efficiency values are expected to be slightly optimistic since gate-driver losses, capacitor ESR losses and additional harmonic core losses were not included in the loss model. The interleaved PWM strategy successfully maintained capacitor-voltage balance and prevented unequal voltage stress across the switching devices. Among the five investigated modulation techniques, the interleaved approach provided the best balancing performance and was therefore selected for the final converter implementation. Thermal analysis indicated that the temperatures of the high-voltage switches remained within the al-

lowable operating limits over the investigated operating range. The main limitation observed during the evaluation was the increase in resonant-inductor flux density under low-frequency, high-current operating conditions. Under these circumstances, the magnetic flux approached the saturation limit of the selected ferrite material. Consequently, further investigation and optimisation of the resonant-inductor and the transformer design is recommended for future work.

7
Conclusion

This thesis presented the design and evaluation of a stacked half-bridge (SHB) LLC resonant converter for high-voltage to low-voltage DC-DC conversion in automotive applications. The converter was designed to operate over a wide input-voltage range while maintaining a regulated low-voltage output and high efficiency. The proposed architecture combines the advantages of the SHB topology and the LLC resonant converter. The SHB stage provides an additional degree of freedom through duty-ratio control, reducing the gain requirement imposed on the LLC resonant tank and extending the converter operating range. The LLC resonant tank enables high-efficiency operation through soft-switching techniques and reduced switching losses. The complete converter design was developed using a systematic methodology. The LLC resonant tank parameters were determined using first harmonic approximation analysis, followed by the design of the high-frequency transformer, resonant inductor, modulation strategy and control structure. An interleaved PWM modulation technique was investigated and selected due to its superior capacitor-voltage balancing performance. Simulation results demonstrated that the converter satisfies the specified input-voltage range and output-current requirements. The selected modulation strategy successfully maintained balanced voltages across the split DC-link capacitors, thereby reducing unequal voltage stress on the switching devices. The converter also achieved a maximum calculated efficiency of 97.2%. Although the converter operated satisfactorily over most of the investigated operating range, elevated resonant-inductor flux density was observed during certain low-frequency and high-current operating conditions. This behaviour indicates that the magnetic design of the resonant inductor may require further investigation and optimisation in future work. Overall, the results demonstrate that the proposed SHB LLC converter is a viable solution for wide-input-voltage automotive DC-DC conversion applications, providing high efficiency, effective capacitor-voltage balancing and a wide operating range.

7.1 Future Work

Future work should focus on:

- Optimisation of resonant-inductor operation under low-frequency, high-current conditions.
- Inclusion of dead-time effects and gate-driver non-idealities in the simulation model.
- Verification of zero-voltage switching at light load conditions.

- Optimisation of the magnetic components to improve power density and reduce volume.
- Proper tuning of the PI controllers in the control system.
- Experimental validation of the proposed converter.
- Comparison with the existing converter.

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A

Appendix 1

This appendix includes the voltages across the two input capacitors for the different modulation strategies investigated.

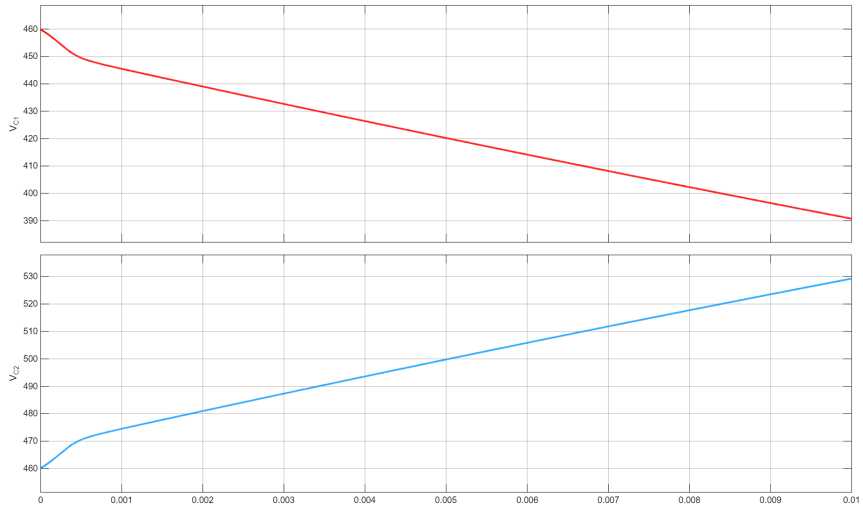

Figure A.1: Voltage Across C1 and C2 during the switching with strategy 1

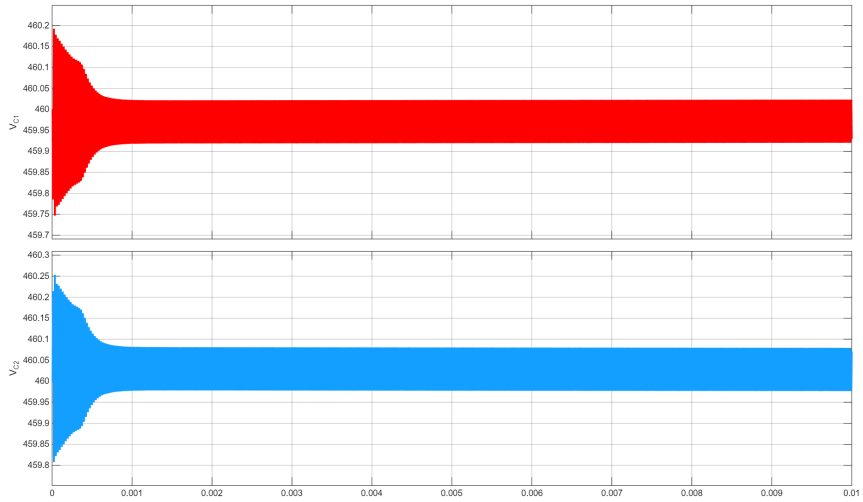

Figure A.2: Voltage Across C1 and C2 during the switching with strategy 2

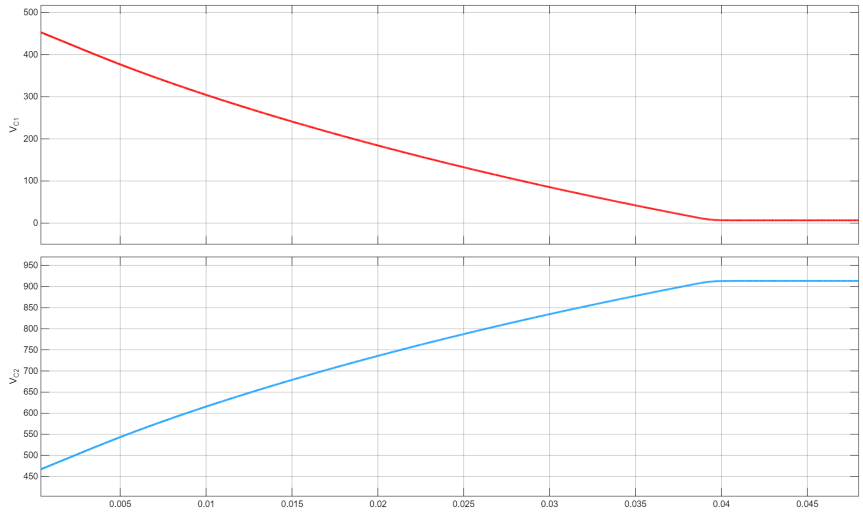

Figure A.3: Voltage Across C1 and C2 during the switching with strategy 3

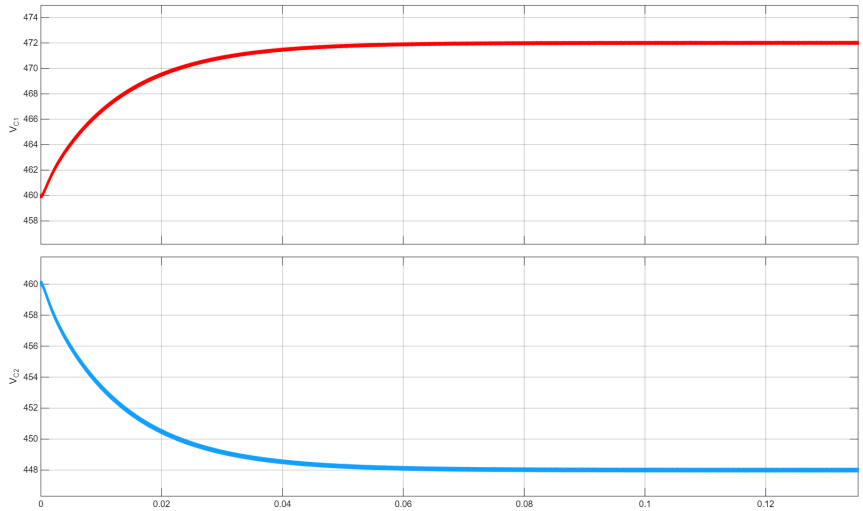

Figure A.4: Voltage Across C1 and C2 during the switching with strategy 4

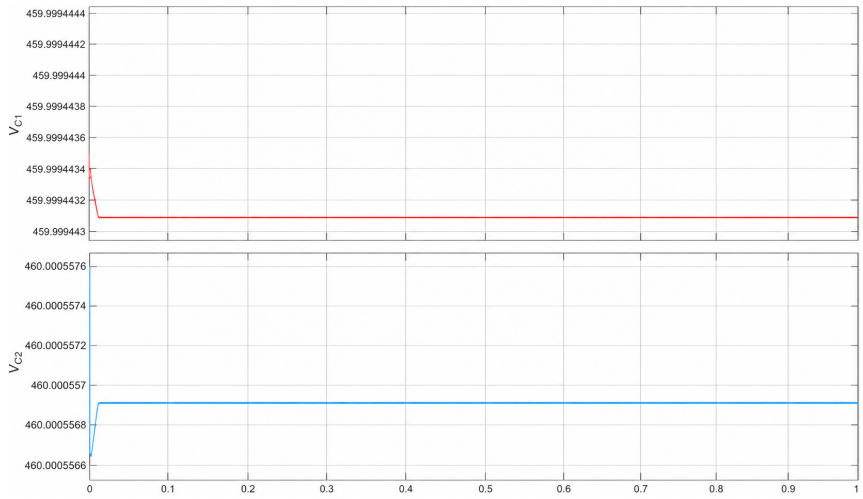

Figure A.5: Voltage Across C1 and C2 during the switching with strategy 5

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