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A FPGA-based 5 Gbit/s D-QPSK Modem

Master of Science Thesis

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Master Thesis:

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Abstract:

E-band (71-76 GHz and 81-86 GHz) is permitted worldwide for ultra high capacity point-to-point (P2P) communications. The 10 GHz spectrum represents by far the widest bandwidth ever allocated for radio P2P links, enabling fibre-like transmission with data rates of gigabit per second (Gbps) and greater that are difficult to reach using the bandwidth-limited, lower microwave frequency bands.

The goal of this project is to develop a Differential Quadrature Phase Shift Keying (D-QPSK) modem supporting 5 Gbps (Gigabits per second) data rate transmission. A 2.5 Gbps field-programmable gate array (FPGA)-based modem had been designed and verified previously. This modem was built using FPGA and microwave components, in which the FPGA is programmed to generate a D-QPSK signal and the microwave components perform the up-and down-conversion between baseband and intermediate frequency (IF) signal. However, it is not a trivial task at all to upgrade the modem to 5 Gbps, since there are severe limitations with the FPGA solution to support the required data rate.

In this thesis, a prefix parallel layer (PPL) algorithm is proposed to increase the speed of differential coding process. This algorithm can be implemented in a FPGA and it is capable for processing data rate of 5 Gbps and higher. In addition, the demodulator structure is simplified, which also raise the capability of detecting higher data rate D-QPSK signal.

The 5 Gbps D-QPSK is tested the in lab environment and at the end of the project the system has successfully achieved error-free transmission. However, improvements in several aspects are needed to turn this proof-of-concept experiment into prototype for products.

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1 Introduction

1.1 Project background

Data traffic in mobile network is increasing rapidly. In attempt to meet the capacity of mobile backhaul required by LTE (Long-Term Evaluation, a 4G technology), LTE-Advanced and beyond, research activities are going on within Ericsson Research for solutions that are future-proven and offer capacity up to 10 Gbps. Nowadays 60% of the world's base stations are connected using microwave links today. Ericsson's microwave radios nowadays are using conventional bands of 7-42 GHz with a typical capacity of 340 Mbps per radio per channel.

E-band and 120 GHz solutions are under development for their large bandwidth availability (10 GHz @ E-band and >15 GHz@120 GHz). [1] Table 1 shows the relationship between the bandwidth and modulation in ideal case and it can be seen that with a larger bandwidth it is possible to apply low order modulations to achieve high data rate.

Bandwidth (GHz) vs. Capacity (Gbps)

Available Bandwidth (GHz)		2.5	5	10
Maximum Capacity (Gbps)	BPSK	1.25	2.5	5
	QPSK	2.5	5	10
	16 QAM	5	10	20

Table 1. The Capacity of different modulations on 2.5 GHz to 10 GHz bandwidth [1]

The system will be tested for both 2.5 Gbps and 5 Gbps data rate. Figure 1 shows Ericsson's research activity in E-band radio links. The goal is to reach 10 Gbps capacity using 16QAM. This thesis project is a mid-step towards the final goal, where 5 Gbps data rate is to be achieved using D-QPSK.

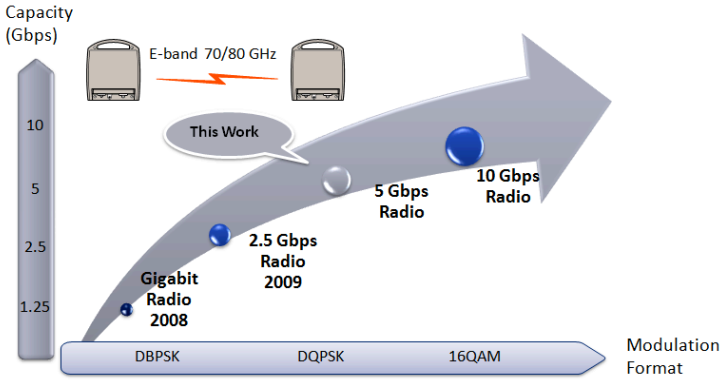


Figure 1. Ericsson's research activity in E-band radio links

1.2 Project Outline

The tasks of the project are as follows:

1. A basic D-QPSK modulation system designed for 2.5 Gbps was implemented on Altera Stratix® II board. Complete the ongoing design test on 2.5 Gbps system.
2. Modify the algorithm and structure toward 5 Gbps and even 10 Gbps.
    a. Use Quartus II (software design platform provide by Altera) to build up the transmitter and receiver; test FPGA performance on high data rate.
    b. Design a new algorithm for D-QPSK coding to support 5 Gbps data rate.
    c. Combine transceivers and coding blocks together on a single FPGA to produce correct D-QPSK coded signal for testing and demodulation.
    d. Use microwave components to modulate and demodulate signal and send back to the same FPGA receiver block.
    e. Test and modify the complete system.

The new design should be implemented on a Stratix® IV board which was available to the project at the time.

1.3 Thesis Report Outline

The first section is the introduction, including the project background and outline.

In section 2 and 3, the fundamental concepts of this project will be discussed. In section 2, I will discuss why use D-QPSK as modulation and introduce its coding rules. In section 3, the fundamental information of the FPGAs will be addressed, and then the two FPGA boards which are used in the project will be explained in details.

Section 4 is the most important part: section 4.1 contains the modulator's architecture and how FPGA works as a modulator; in section 4.2 the D-QPSK coding algorithm will be discussed, this section will explain the structure for the coder block in the system; section 4.3 is about the demodulator, the demodulator is constructed by using microwave components, figures of the structure can be find in this section.

All the test results will be issued in section 5, including time domain and frequency domain measurements, and follows by a short discussion in section 6.

2 D-QPSK Modulation Fundamental

2.1 Why D-QPSK?

Differential Quadrature Phase Shift Keying (D-QPSK) has a very important advantage: it does not require carrier recovery. [2] The detection operation for differentially encoded data is done by comparing the recent symbol with the preceded symbol.

Figure 2 and Figure 3 show the difference between QPSK and D-QPSK. For QPSK, as in Figure 2, the signal information is represented by the phase difference between the modulated signal and the original carrier signal, which means, at the receiving side, the system needs to know the correct carrier phase for demodulation. For D-QPSK, as in Figure 3, the signal information is represented by the phase difference between the current and the previous symbol, with a differential per-coder added to the transmitting side. The receiver can demodulate the signal without carrier recovery.

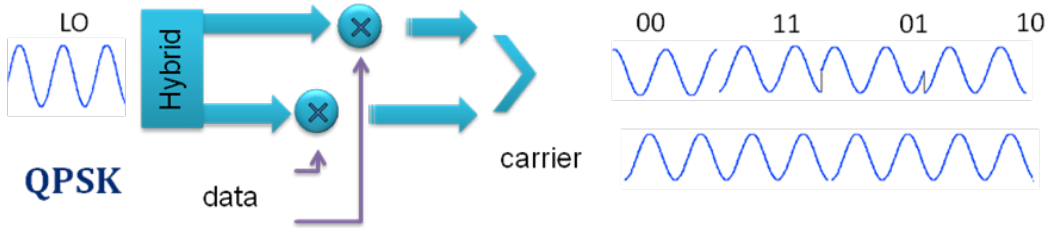


Figure 2. QPSK modulation, demodulation requires carrier information

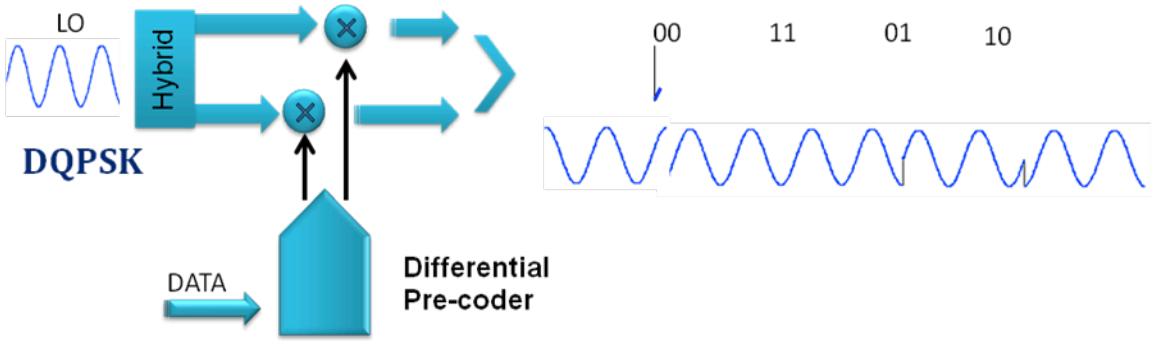


Figure 3. D-QPSK modulation, no carrier information is needed at demodulation

2.2 D-QPSK coding rule

input	I	Q	Δφ
00	I(k-1)	Q(k-1)	180°
01	Q(k-1)	I(k-1)	90°
10	Q(k-1)	$\overline{I(k-1)}$	270°
11	I(k-1)	Q(k-1)	0°

Table 2. D-QPSK coding rule used in programming

The D-QPSK coding rule used in the programming is listed in Table 2. This coding rule is to map each 2 input bits onto phase shift, as shown in Figure 4**Error! Reference source not found.** For example, if input signal is 00, according to coding rule, the phased difference is 180°. This mean if the last symbol for example is 11, input 00 will give a 180°rotate, then the coded output will be 00. The right side of Figure 4 shows how D-QPSK is represented as constellation points. At the receiver side, the decision lines separate I and Q signals at +45°and -45°.[2][3]

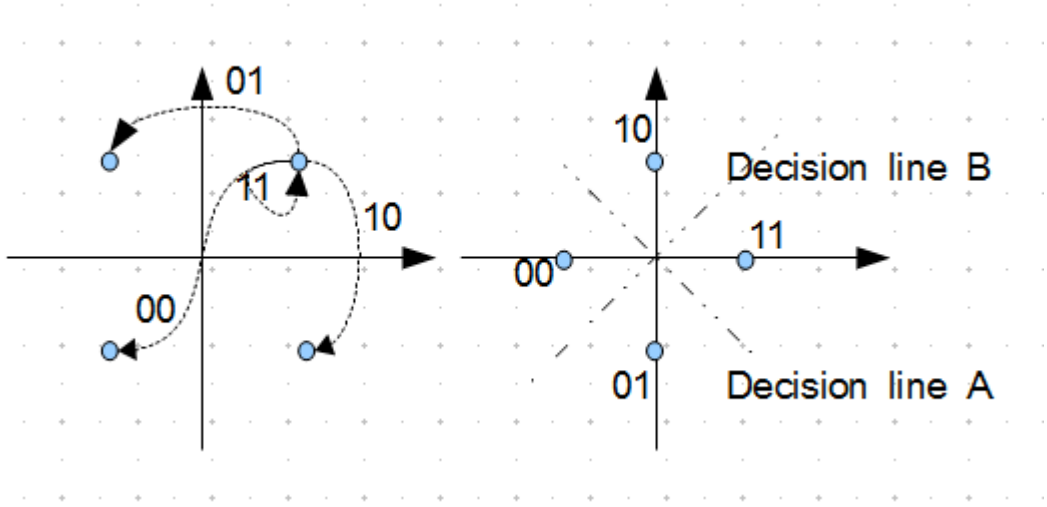


Figure 4. D-QPSK coding rule and constellation

3 Field- Programmable Gate Array (FPGA)

3.1 FPGA-based implementation introduction

FPGA stands for Field-programmable gate array. FPGA has rich resources as prebuilt logic blocks and programmable routing resources. By programming, one actually re-routing the connectivity of all the available prebuilt logic blocks, thus a FPGA can be used for different functionality. [4] This procedure is achieved by the help of computer-aided design tool, which translate a HDL (hardware-description language) code into the routing map of FPGA built-in blocks. The tool also generates a configuration file or bit-stream that contains information on how the components should be wired. With the development of CAD tools, now, one can not only using HDL code, but also using graphic interfacing or even C code to implement logic function over a FPGA.

FPGAs are widely used across all industries, because it combines the best parts of ASICs and processor-based systems. It is much easier to debug and modify the design, which reduces the risk to implement function over hardware platform, which is achieved by developing customized ASIC. As a result, FPGA is suitable for researching and early phase product development.

3.2 FPGA with high speed interface

FPGA is mainly used for heavy signal processing tasks; the convention interface over an FPGA is used for control and connecting different digital data bus. The maximum data rate for a general FPGA is 1.2 Gbps, which is using a LVDS (Low-voltage differential signaling) standard interface.

However, recently the speed of data bus is increasing dramatically, for instance, SATA (Serial Advanced Technology Attachment) can support data rate up to 6 Gbps. To supporting the need of these applications Altera published their first FPGA family with integrated transceivers in 2001. [4] A production line of Altera's FPGA with integrated transceivers is shown in Table. 3.

DEVICE	SEMICONDUCTOR PROCESS	CHANNEL NUMBERS	MAXIMUM DATA RATE (GBPS)
Stratix V GT	28 nm	66	28
Stratix V GX	28 nm	66	12.5
Stratix IV GT	40 nm	48	11.3
Stratix IV GX	40 nm	48	8.5
HardCopy IV GX	40 nm	36	6.5
Arria II GZ	40 nm	24	6.375

Table 3. Altera production line with multi- Gbps interface [5]

3.3 FPGA Kits used in this project

In this project, commercial development kits are used to perform prove-of-concept test. Two different development kits are used in this thesis work as shown in Figure 5 and Figure 6.

Kit	Stratix II GX Transceiver Signal Integrity Development Board	Stratix IV GX Transceiver Signal Integrity Development Board
FPGA model	Stratix II GX EP2SGX90EF	Stratix IV GX EP4SGX230KF40C2N
Foot Print	1152 pin BGA	1152 pin BGA
Clock	On-board 25MHz and 156.25MHz clock oscillators	On-board clock oscillators: 50 MHz, 100 MHz, 156.25 MHz, 312.5 MHz, 425.0 MHz
High Speed transceiver	Six full-duplex transceiver channels routed to SMA connectors	Eight full-duplex transceiver channels routed to SMA connectors
Maximum data rate	6.375 Gbps	8.5 Gbps

Table 4. Comparison of the two development kits used in the project [6 - 9]



Figure 5. Stratix II GX Transceiver Signal Integrity Development Board (copy from Altera Stratix II GX Edition Reference Manual) [6]

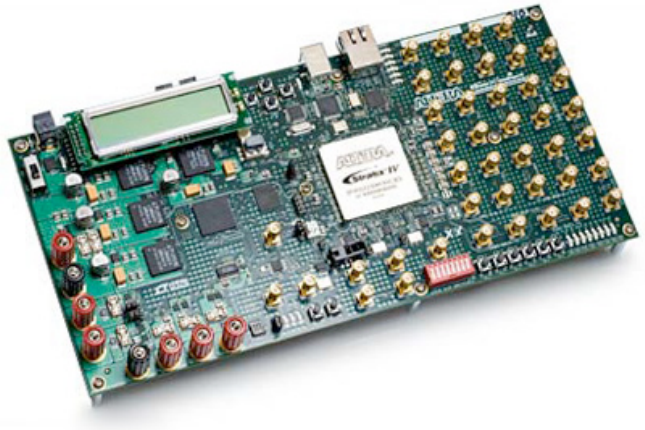


Figure 6. Stratix IV GX Transceiver Signal Integrity Development Board (copy from Altera Stratix IV GX Edition Reference Manual) [7]

3.4 Development workflow

In this project, various design techniques are used, including algorithm simulation, algorithm programming, FPGA based implementation and lab measurement and verification. Different tool are used in different stage of development:

1. Matlab is used for algorithm simulation and parameter optimization.
2. FPGA related programming and debugging are made within Altera's quartus II development environment. We used verilog language to program FPGA, quartus can take this code and convert this into a netlist file and a bit stream file.
3. Another tool Modelsim is used to simulate the behavior of FPGA. This tool can take the netlist file from quartus II, then you are allowed to edit the input waveform of the FPGA, Modelsim can generate output waveform, according to this the functionality of FPGA implementation can be verified.
4. Last step in the workflow is set-up hardware testbench, real signal is input and output can be monitored by either oscilloscope or you can use a tool, LogicTap, to monitor the internal register of the running FPGA. LogicTap cannot display all the data in real-time, instead, it can capture data within certain time period. The trigger condition to start capturing can be configured.

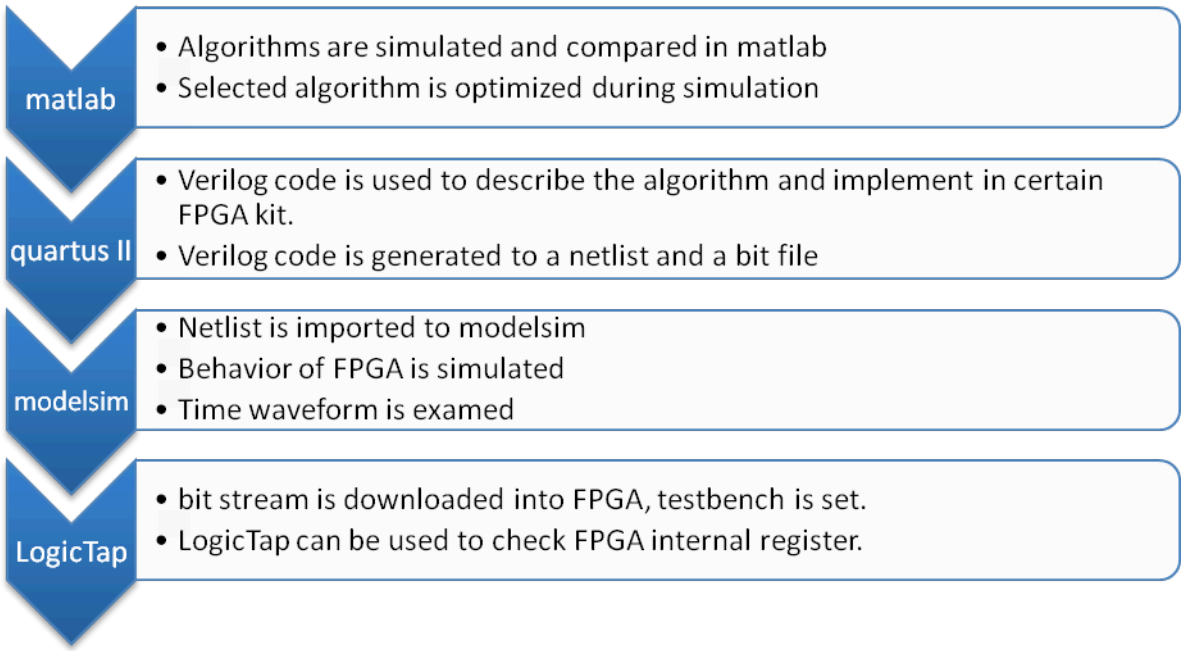


Figure 7. FPGA design workflow we used in this project

The project design workflow is shown in Figure 7, if any error or unpredicted behavior is observed in a step, one need to go back to the previous step, find the cause of the error and revise that. This process repeats until FPGA generates correct output in really hardware test.

4 Modem Implementation

4.1 Modulator

4.1.1 Conventional modulator architecture

A conventional D-QPSK modulator architecture is shown in Figure 8.
A 5 Gbps data stream is first input into a 1:2 DeMUX. A differential coder is needed to produce the coded I and Q according to the coding rule given in Table 1. Also, the differential coder requires a feedback loop to give last symbol's I and Q information.

The differential coder operates at a speed of 2.5 GHz and produce 2.5 Baud coded I and Q signal. Two XOR gates manufactured by Inphi, which work up to 13 Gbps, are used as mixers. A 90° hybrid converts the single-ended oscillator signal into two outputs of 90° out of phase. By combining the outputs of the mixers, the modulated D-QPSK signal is produced at a carrier of 11.5 GHz

To make all the functions above to work at 5 Gbps, there are three main challenges. First the 1:2 DeMUX at this operating speed is not available on the market; second, four signals: two pares of differential signals $I, \bar{I}$ and $Q, \bar{Q}$ all need to be delay a symbol period and fed back to the differential coder by using delay lines. An example of such delay line is shown in Figure 9 furthermore, all these delay lines have to be exactly symmetrical; third, there is no such component of differential coder available on the market, either. Thus, other architecture is desirable in order to build up a D-QPSK modulator at this data-rate.

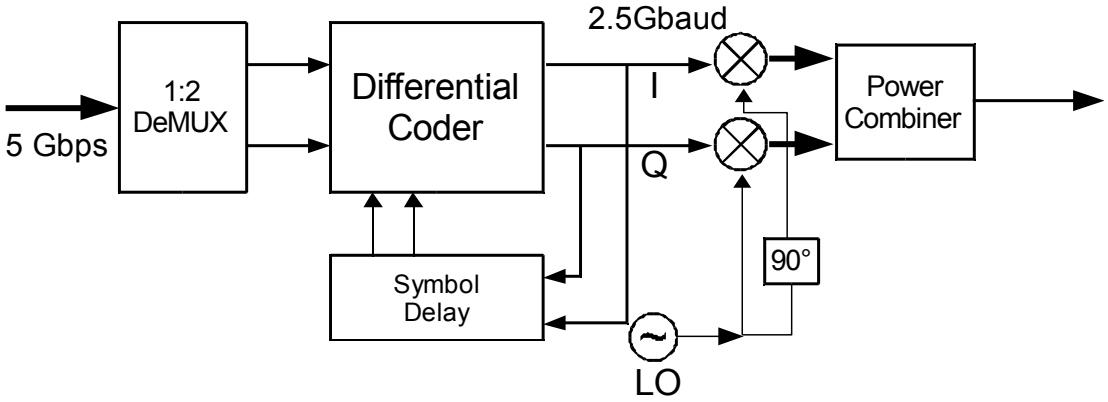


Figure 8. Conventional D-QPSK modulator architecture of a 5 Gbps system [11]

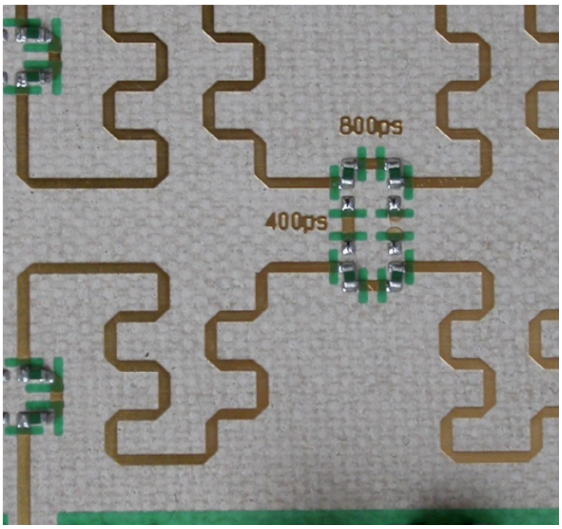


Figure 9. An example of one delay line design

4.1.2 FPGA based Modulator

By utilizing newly emerged FPGA as we mentioned in section 3.1 with I/Os support data rate up to 5 Gbps, it is possible to build a FPGA-based modulator for high data rate application. In this project the FPGA is mainly acting as the pre-coder. A FPGA can perform logic operations at rates up to 500MHz, which is still not as fast as the data-rate in our case. However, by using a structure as depicts in Figure 10, the FPGA can process 5 Gbps data by using a 250MHz internal clock. The signal is first split into 20-bit-width bus by using a FPGA internal DeMUX, the bus data rate is only 250MHz. Then an internal block is used for differential coding operation and then two 10-bit-width signals are output at the same rate. By using MUX, the FPGA rebuild the coded I and Q channel signal (each runs at 2.5 Gsps (Giga-symbols per second)). The details of the coding algorithm will be explained in section 4.2.

4.2 D-QPSK Coding Algorithm

4.2.1 Previous coding algorithm

A 2.5 Gbps D-QPSK modem has been presented in [12]. The ROM based coding algorithm used in that system is shown as in Figure 11. A 1:16 DeMux is used which produce a 16-bit-width data bus at a rate of 156.25MHz.
All the possible coded output of this 16-bit input data is programmed and stored in the ROM. By this, with each 16-bit-width bus input the coder simply checks the look up table in the ROM and gives out the output. The coding function depends also on the status of last symbol, thus, two different ROMs are used, each of them assumed a difference last symbol status. The last symbol register memorizes the real output symbols and controls the switch to chose the right output to be transferred to the 8:1 MUX.

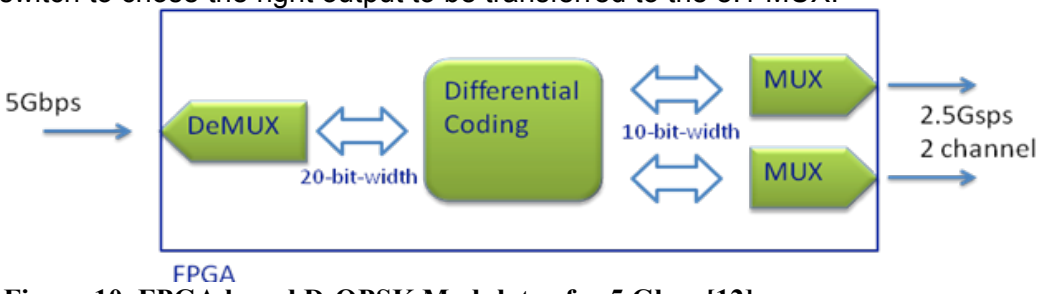


Figure 10. FPGA based D-QPSK Modulator for 5 Gbps [12]

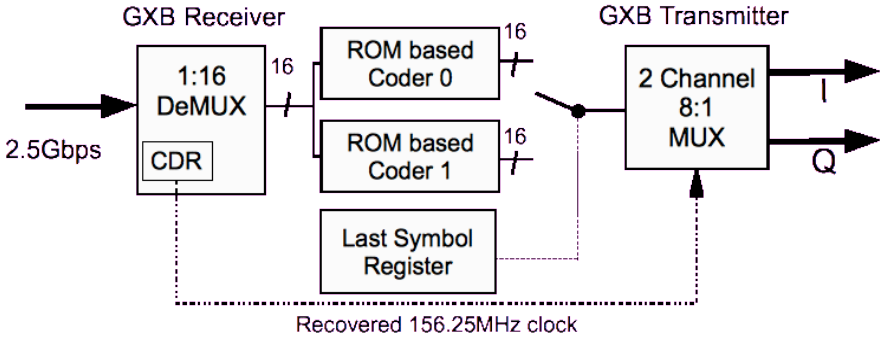


Figure 11. D-QPSK Coder structure for 2.5 Gbps system (copy from [12])

In order for the structure above to support a 5 Gbps system, a straightforward modification results in the version as shown in Figure 13. First, the DeMUX block has been changed from 1:16 to 1:20 in order to support the higher data rate to run on the FPGA, and second, the 2 channel MUX has been changed from 8:1 to 10:1.

4.2.1.1 Limitation

Unfortunately, the design shown in Figure 12 has a serious limitation. When the width of the data bus is increased from 16 to 20, the FPGA ROM can no longer support the large look up table. The ROM size has to be at least 2^{22} (2^{20} for input bits and 2^{2} for last symbol) in order to store a lookup table for 20-bits-wideth bus. The Altera Stratix IV GX board used in this project has a maximum ROM size of 2^{18}. [8][10] Therefore the old ROM based coder is no longer applicable for the system and a new algorithm is needed.

4.2.2 Improved algorithm

From the D-QPSK coding rule (as shown in Table 2), the information of the data is carried in the phase difference between the current and last symbol.
For the coding block 20-bit input data & last symbol position are known, the new algorithm needs to calculate 10 output symbols. The calculation can be expressed mathematically as [1]:
The phase of the k-th symbol is:

$$\phi_k = \phi_{\text{int}} + \sum_{i=0}^{k} \Delta\phi_i \qquad (1)$$

Where $\Delta\phi_i$ is the incremental phase according to the input data, which has been shown Table 2, and ϕ_{int} is the phase of last symbol. The input of the coder is 20 bits input data, a 'data-to-phase' block converts these input into a set of incremental phases $\left[\Delta\phi_0, \Delta\phi_1, \ldots, \Delta\phi_9\right]$. The phase accumulation is separately operated in different layers, which called prefix parallel layers (PPL). [13][14] The output of the second last layer (N-1 layer) is $\left[\Delta\phi_0, \sum_{i=0}^{1}\Delta\phi_i, \ldots, \sum_{i=0}^{9}\Delta\phi_i\right]$ and ϕ_{int} is added in the final layer. The output of layers is the accumulated phase information, which are converted back to I and Q expression in the block of 'phase-to-IQ' .
Then the coding will be look like in Figure 13.

The structure of parallel prefix layer is depicted in Figure 14. Each layer has input from the top, and the result output at the bottom. The solid line represents that the result is directly taken from the input and the dashed line indicates that the result is the sum of two input values. The number at the bottom represents the index of the result, for instance, the 6th node of layer1 has an index of [3:6], which means that the output at this node is $\sum_{i=3}^{6}\Delta\phi_i$. And this result will add with the result of [1:3] from the 3rd node in the next layer, and then produce a result of [1:6] as the final output. It only takes 3 layers to

produce the sum $\sum_{i=1}^{6} \Delta\phi_i$, the reason is that this PPL structure can share part of the calculation result with other nodes. In this structure, it only takes $\lceil \log_2(N/2) + 1 \rceil$ layers for calculating N outputs. [15]

Also, the layers are fully synchronized at a clock rate of $1/N$ data rate, which minimizes the risk of facing 'race condition' problem when the data rate is increased further.

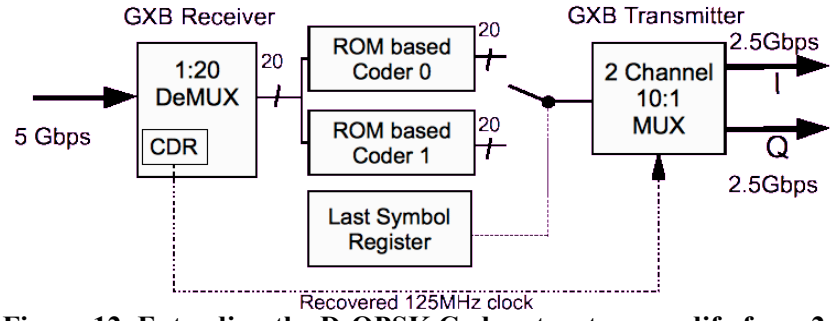


Figure 12. Extending the D-QPSK Coder structure modify from 2.5 Gbps to 5 Gbps

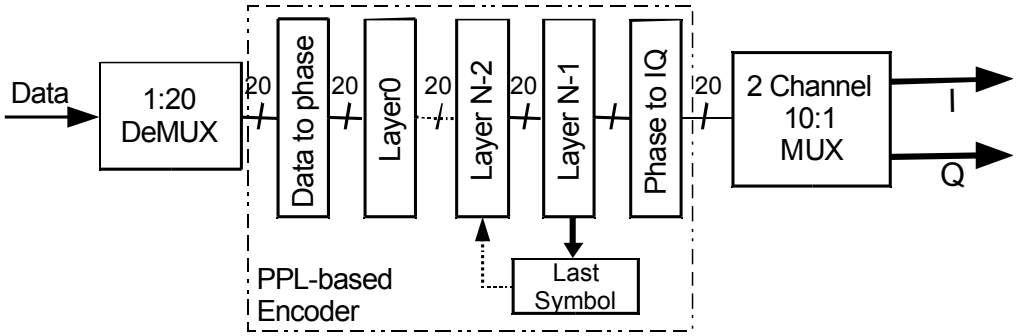


Figure 13. D-QPSK coding for 5 Gbps

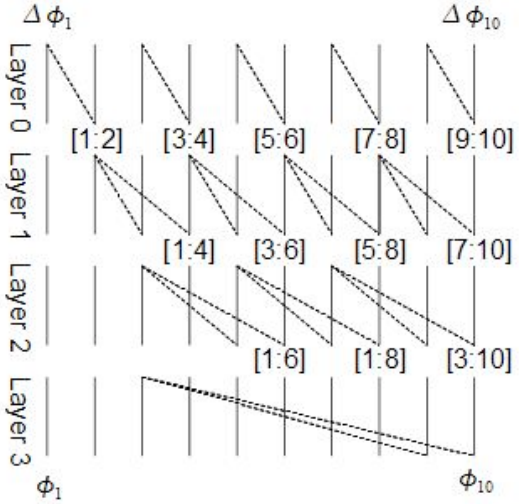


Figure 14. 10-symbol parallel prefix layer (PPL)

4.3 Demodulator

4.3.1 Demodulator architecture

The structure of the 2.5 Gbps D-QPSK demodulator is shown in Figure 15. [12] The IF signal is input from the left side of the figure, which is split into two branches by a power splitter. Each of these branches recovers one bit from each input symbol. In the upper branch, a mixer and a low pass filter (LPF) form a phase detector, where phase difference between one symbol period delayed IF signal and a 45° phased shifted IF signal is detected. A bit is recovered after the LPF. The lower branch has identical structure except that a -45° phase shifter is used, thus another bit is recovered from the input. These two recovered bits are combined by a 2-to-1 MUX which is implemented in the FPGA.

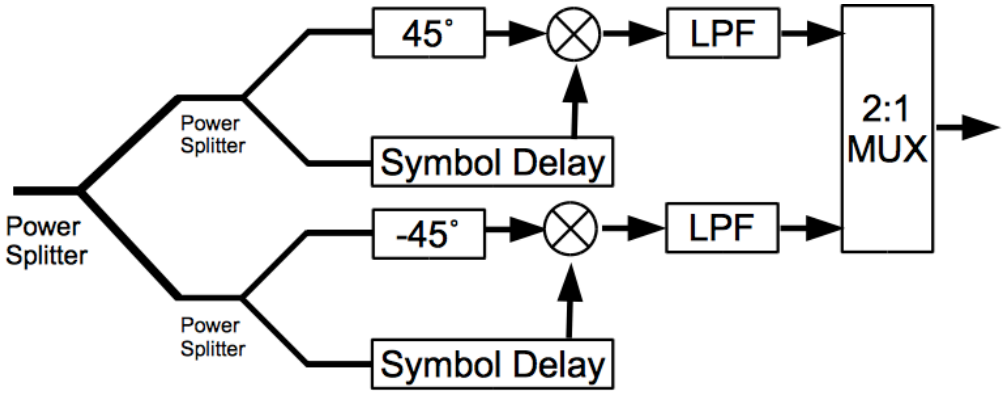


Figure 15. Demodulator architecture

4.3.2 Limitation for upgrading to 5 Gbps

Theoretically, the structure works for 5 Gbps, given that the LPF and symbol delay path are updated accordingly. However, hardware implementation is hard to achieve in practice:

1. The symbol delay should be exactly 400ps, which makes the design of a single physical line difficult and even harder to keep two such lines identical in length.
2. This structure has four parameters that are tunable: two adjustable phase shifter and two delay elements. From configuration point of view, the higher the data rate, the less the tolerance the demodulator can take, which poses tough requirements not only on hardware design but also on the manual operation to meet the accuracy.

4.3.3 Improved demodulator structure

The improved demodulator structure is depicted in Figure 16. This structure using a 90° coupler and ensures the phase difference between the two inputs to the mixers to be 90° out of phase. By coincidence, the 45° phase shifter itself has a propagation delay of about 400ps which is the required one symbol delay. Therefore, there is only one tunable component used in this structure.[12]

4.3.4 FPGA based 2:1 MUX

The demodulator comprises of a 2:1 MUX, which is not available from the market. Thus, this functionality is implemented in the same FPGA used for the pre-coder implement. [3][12]

Figure 17 shows the 2:1 MUX structure inside the FPGA. FPGA built-in DeMUX (1:10) and MUX (20:1) are used to handle Gbps data streams. An interleave block is used to deal with the order arrangement of the 2:1 function.

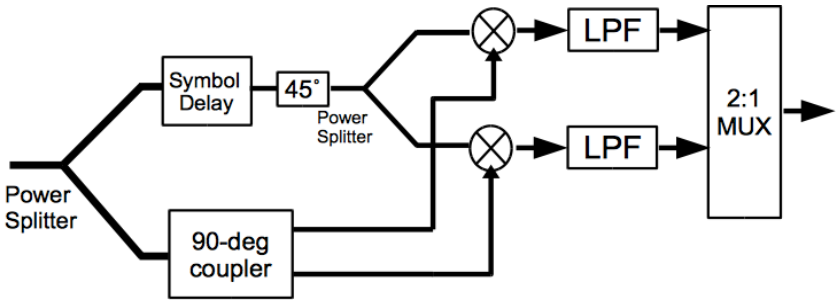


Figure 16. Demodulator architecture

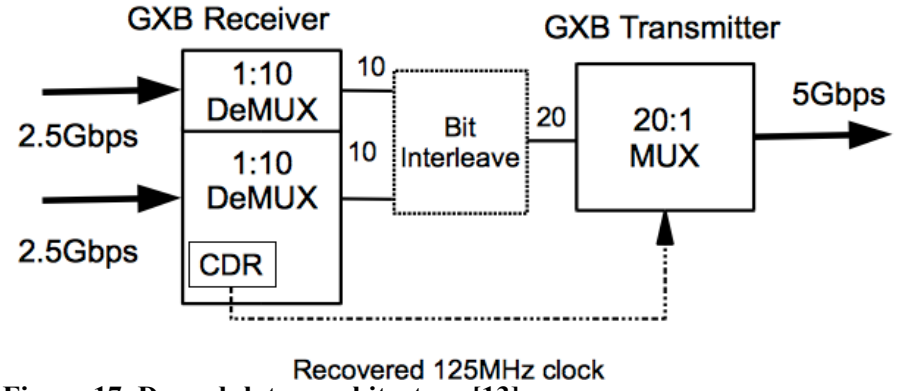


Figure 17. Demodulator architecture [13]

5 Test Result

5.1 Test bench setup

As in Figure 18, a pattern generator is used as data source, which is the input to the FPGA based modem. The coded I and Q output from the FPGA are fed to two mixers where the data are modulated onto a carrier of 11.5 GHz which is called intermediate frequency (IF). Choosing such an IF so the modem could be usable with the E-band transceivers. The final goal of this project is to apply the tested modem to build up a 5 Gbps E-band (71-76 GHz and 81-86 GHz) radio link.

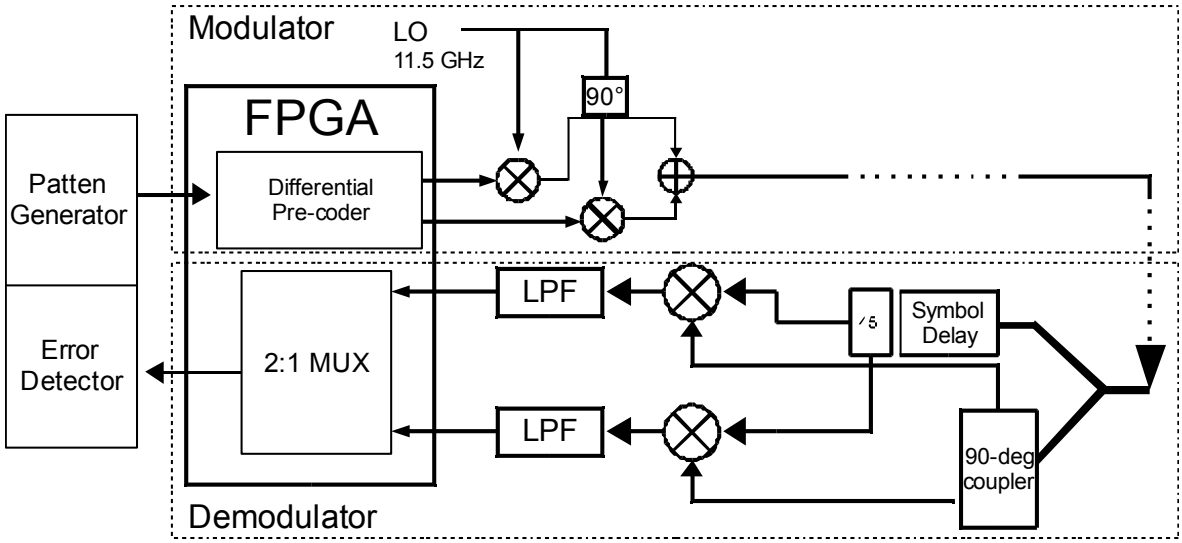


Figure 18. Test bench setup block diagram

Figure 19 shows how the test bench is setup in Ericsson's lab. All components are fixed on a metal board and are interconnected with co-axial RF cables. They are:

1. Two phase shifters, tuned to provide 90 degree phase difference between the two local oscillator input paths to the mixers.
2. High speed XOR gates manufactured by Inphi, used as mixers. The coded I and Q and the LO signals from 1 are input into these mixers. The outputs of these mixers are combined together which is the IF output of the modulator.
3. Variable gain IF amplifier.
4. Two voltage controlled phase shifters, two power splitters and two mechanically tunable cables, all together to provide the required one symbol delay and the phase shifter in the demodulator part.
5. Low-pass filter with 2 GHz bandwidth.

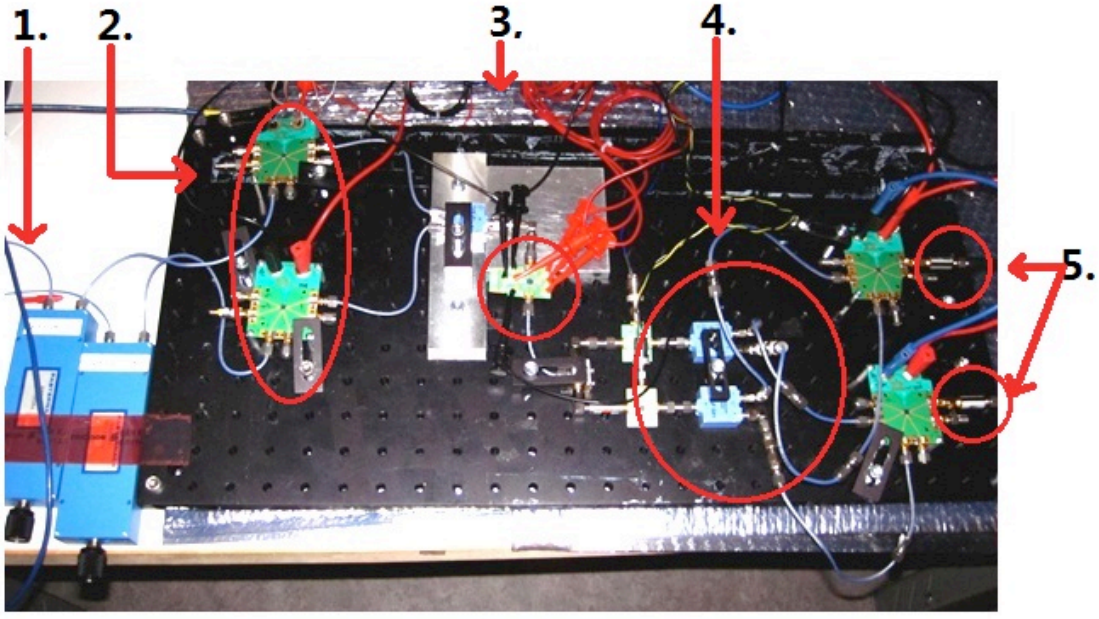


Figure 19. Test bench setup in the lab test

5.2 Time domain measurement

5.2.1 FPGA output signal quality

An important question for high speed data stream, however, is the signal quality. The quality of signal can be defined as both threshold margin and phase margin as shown in Figure 20. The threshold margin is the voltage difference between the highest and lowest value of the threshold voltage, when decision error rate is within a certain limit. The phase margin is defined as the range of the decision timing, in which the decision error rate is within the limit. The join of the threshold margin and the phase margin is described as an “eye”, the bigger the eye opens the better signal quality we get.

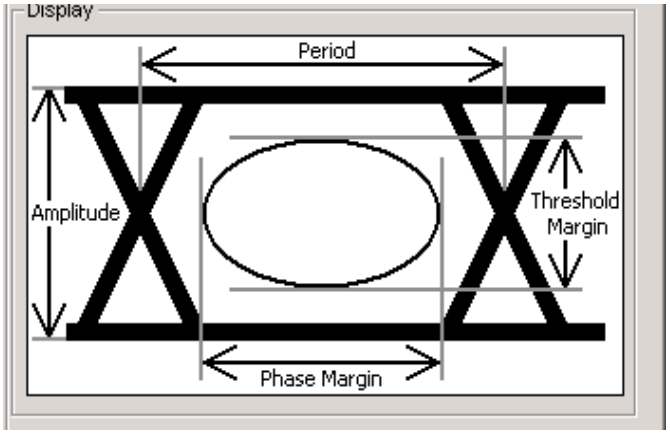


Figure 20. Eye diagram with phase margin

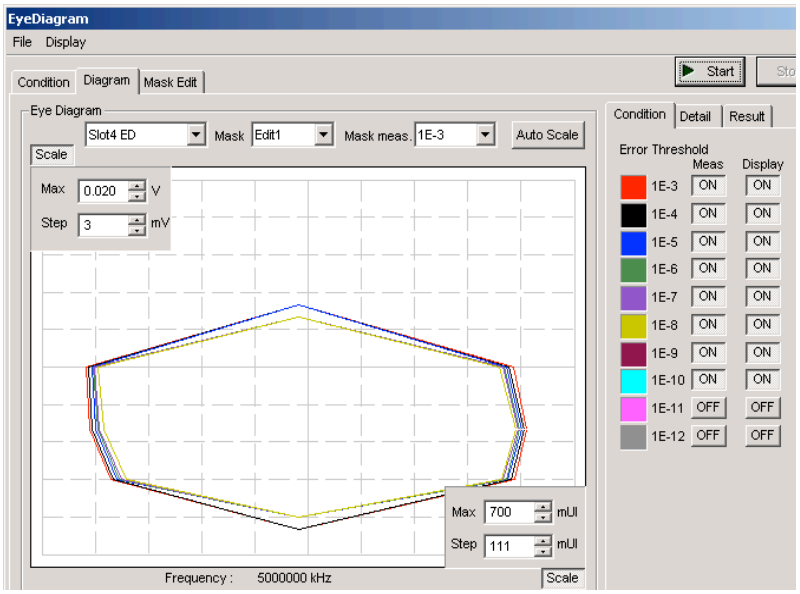


Figure 21. BER test result for FPGA pass-through 5Gps signal

The FPGA is programmed to pass-through 5 Gbps data. It receives data from the bit error rate tester (BERT) testing instrument, and its output is fed back to the instrument. The threshold and phase margin are tested simultaneously. For certain BER, the eye diagram of the phase margin and the voltage margin are shown in curves with different colors in Figure 21. The test result of this FPGA is presented below, where the margin difference for different BER is small, which indicates good signal quality.

The high speed data stream is created based on FPGA internal digital phase lock loop (DPLL). The DPLL has limited phase noise performance, which results in larger jitter of the output data after FPGA. Bathtub test is carried out to measure the jitter of the output [16]. It is show in Figure 22 that the definite jitter (DJ) is 41.12mUI and the random jitter (RJ) is 9.19mUI (milli-Unit-Interval). This means that the jitter performance is mainly limited by DJ which is related to the hardware architecture of high speed interface of the FPGA.

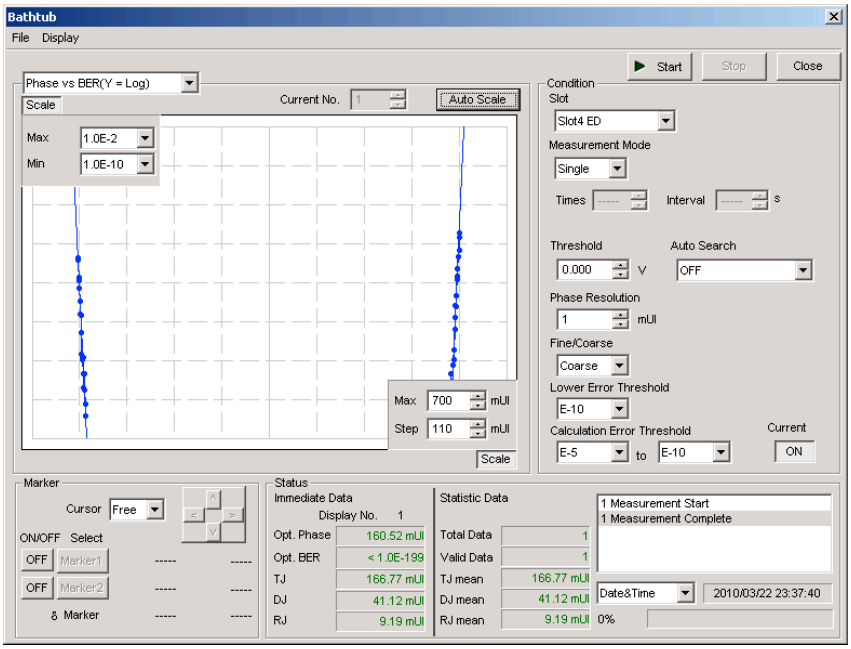


Figure 22. Jitter result for FPGA pass-through

Figure 23 shows the eye diagrams for 5 Gbps data from the pattern generator (upper diagram) and the output of the FPGA (lower diagram). The signal quality of the two data stream looks equally good.

5.2.2 The waveform of the demodulator

The eye diagram of the demodulator output is shown in Figure 24. By tuning the delay element in the demodulator, the eye diagram can be further optimized.

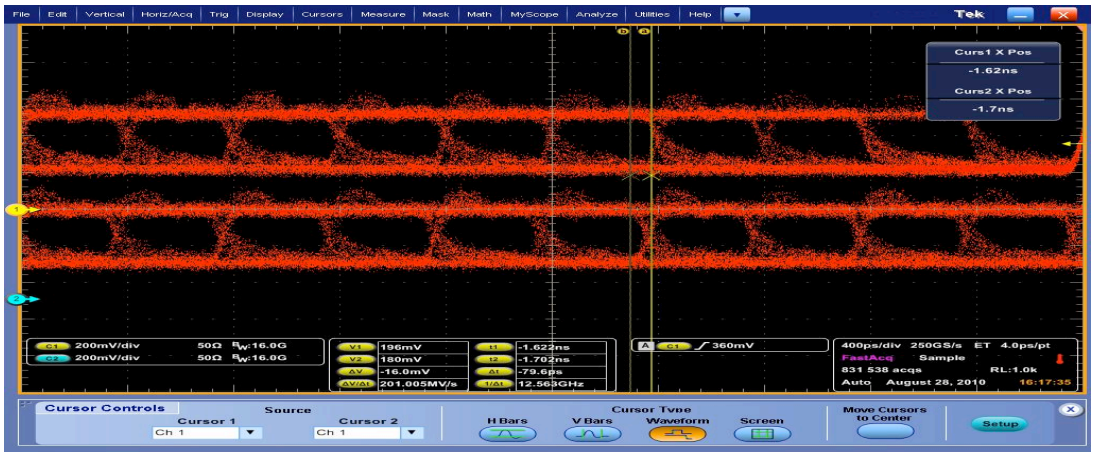


Figure 23. The output waveform from the FPGA

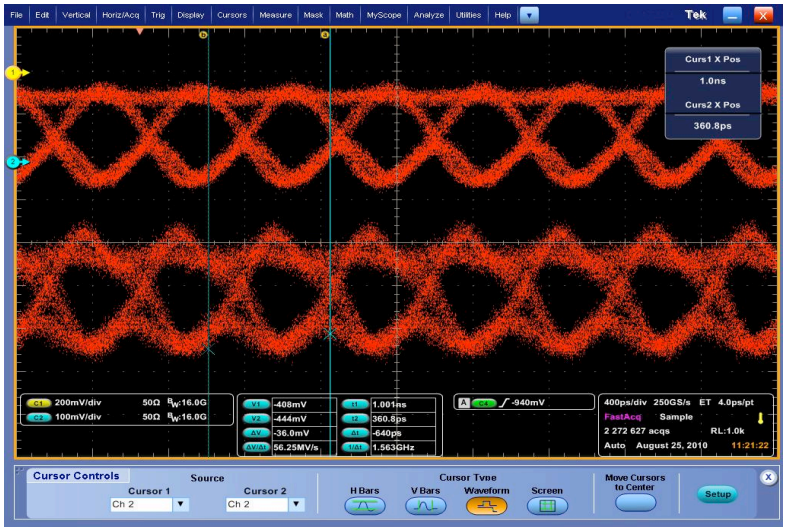


Figure 24. Demodulated signal

5.3 Frequency domain measurement

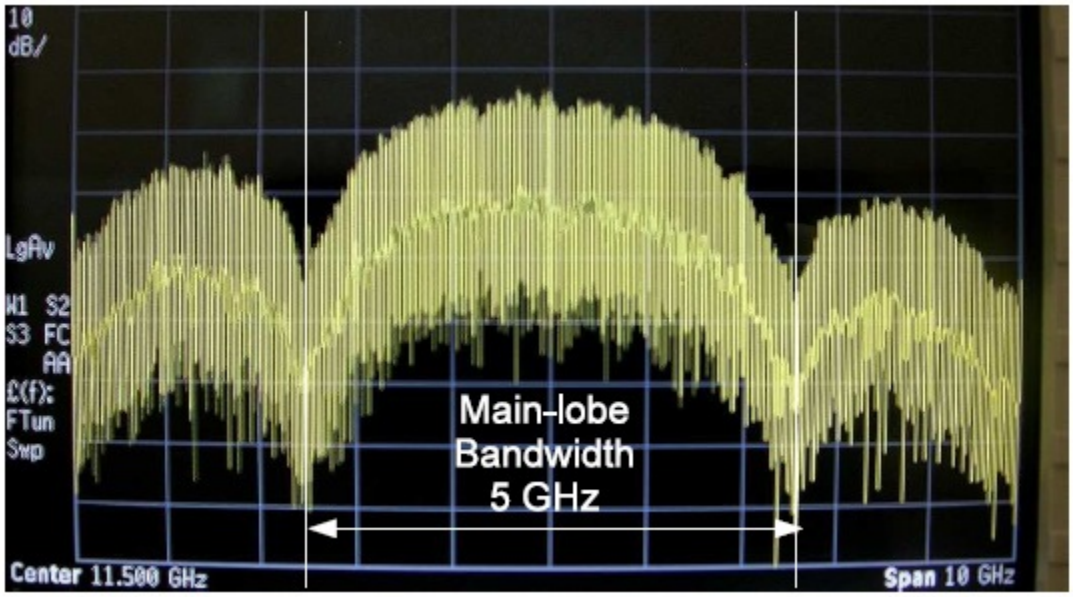


Figure 25. The spectrum of 5 Gbps D-QPSK data modulated at 11.5 GHz carrier

As shown in Figure 25 the main-lobe of the 5 Gbps D-QPSK data double side band signal occupies 5 GHz band width around 11.5 GHz (the IF carrier).

5.4 The FPGA resources utilization

FPGA Resource Utilization			
Resource Type	2.5 Gbit/s Modem	This work	Total Available
Combinational ALUTs	143	880	182,440
Dedicated logic registers	211	1,019	182,440
Total block memory bits	4,096	1,024	4,520,448
Power Consumption	4.8W	5.2W	

Table 5. The FPGA resource utilization

In Table 5, the resource utilization for 5 Gbps is compared with the 2.5 Gbps modem [12]. Because of the optimized PPL algorithm, the usage of the block memory is reduced by 75%. Although the usage of the arithmetic look-up table (ALUT) and the dedicated logic registers are increased, the resource used in this work is still a small part of the total resource available. The power consumption is slightly increased, due mainly to the fact that the MUX and the DeMUX run at a faster speed now.

6 Discussion

A FPGA-based 5 Gbps D-QPSK modem is implemented by using evaluation boards and discrete microwave components. The test shows that error free transmission at this data rate can be achieved with the solution proposed in this work. The current work is a proof-of-concept experiment. Several issues need to be resolved in order to make the system robust:

1. System performance is really sensitive to the analog part of the modem, especially the delay elements and the phase shifter. So a dedicated PCB design is desired.
2. Currently the data is fed from a BERT. In reality, the data is often provided from fiber based on SONET standard. Thus optical interface and protocol framer/de-framer should be implemented in the FPGA as well
3. There is no need for carrier recovery in non-coherent detection; however, data clock recovery (DCR) is needed for clock alignment with the output 5 Gbps serial data.

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