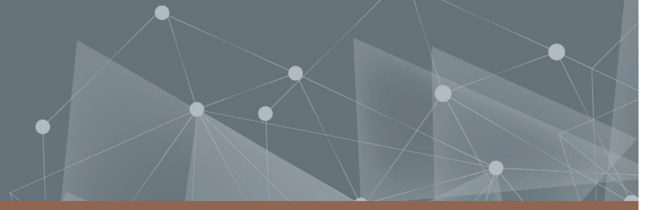
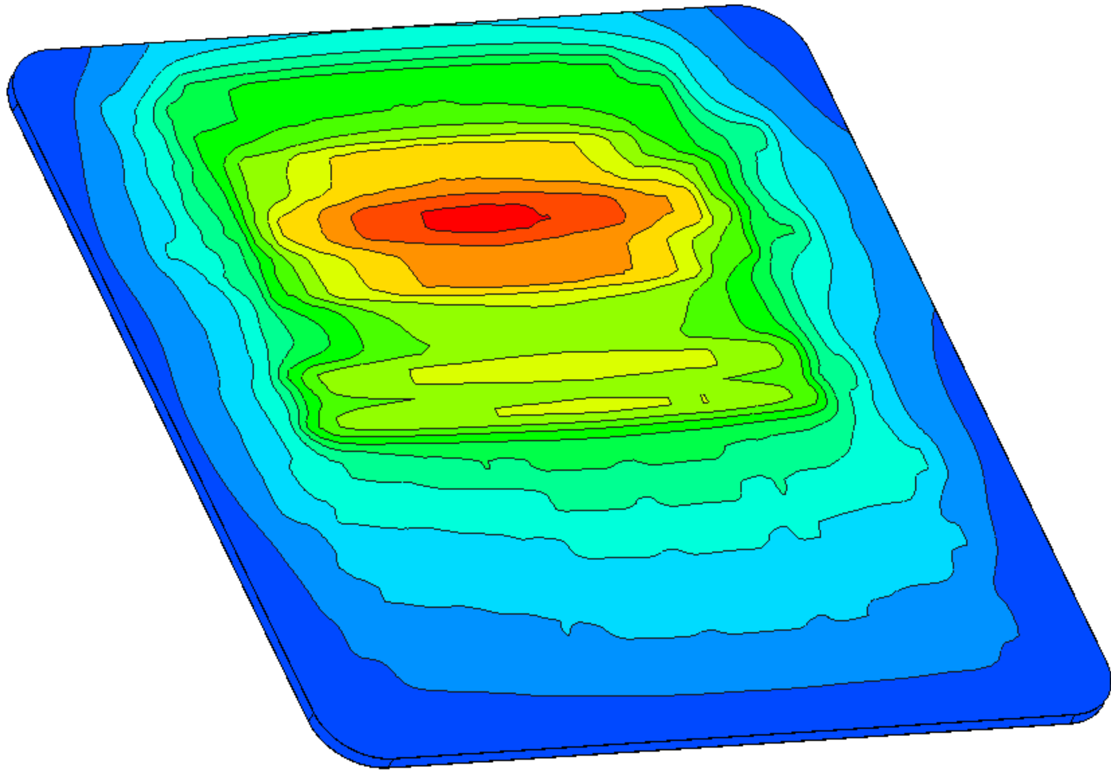
CHALMERS
UNIVERSITY OF TECHNOLOGY





Power and signal integrity of printed circuit boards

Predicting real-world performance of copper interconnections using simulations

Master of Science Thesis

David Einarsson

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2025
www.chalmers.se

Master's thesis 2025

Power and signal integrity of printed circuit boards

Predicting real-world performance of copper interconnections using simulations

David Einarsson

Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
Gothenburg, Sweden 2025

Power and signal integrity of printed circuit boards
Predicting real-world performance of copper interconnections using simulations
David Einarsson

© David Einarsson, 2025.

Master's Thesis 2025
Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology
SE-412 96 Gothenburg
Sweden
Telephone +46 (0)31-772 1000

Cover: Temperature plot of the DC IR printed circuit board simulated in Ansys SIwave.

Gothenburg, Sweden 2025

Power and signal integrity of printed circuit boards
Predicting real-world performance of copper interconnections using simulations
David Einarsson
Department of Electrical Engineering
Division of Electric Power Engineering
Chalmers University of Technology

Abstract

Printed circuit board (PCB) design is a complex process with small tolerances. A single fault could cause a malfunction of the complete system, requiring a costly redesign to regain a functional product. Introducing simulation tools in the design process could help identify problems with the PCB early in the design, reducing the need for physical prototypes, thus saving cost and reducing the environmental impact. This thesis investigates how different layouts affect the performance of the PCB in three key areas, including thermal behavior, power integrity (PI) and signal integrity (SI). Different design options were evaluated using simulations, which were later compared to measurements on physical boards. The simulated temperature and voltage drop of the PCB matched well with the measured values. In comparison, the impedance simulations had greater deviations from the measured values, where the differences were greater for power delivery networks compared to transmission lines. However, the impedance simulations of alternative designs gave a good visualization of the differences between the designs, which agreed with the general differences captured by the measurements. Some scenarios, including close decoupling placement and far-end crosstalk, were harder for the simulation to accurately predict. While stripline transmission lines and near-end crosstalk were easier to simulate. Changing the design of copper interconnects in the layout played a big role in deciding the final performance of the PCB, concerning thermal behavior, PI and SI. Utilizing simulation software in the design process allows for a good comparison between design alternatives, without the need to order a prototype. However, exact values of a certain design could be harder for the simulation to accurately estimate.

Keywords: PCB, SI, PI, simulation, layout, crosstalk, impedance, thermal, decoupling, transmission lines.

Acknowledgements

I would like to thank my supervisor, Ayşen Özcan and my manager, Pär Karlsson, at Volvo Cars for their continuous support and guidance. Thank you for entrusting me with the opportunity to write my thesis at Volvo Cars on an interesting subject.

Secondly, I would like to thank my supervisor and examiner, Torbjörn Thiringer, at Chalmers for giving me direction when I felt lost, as well as providing insightful feedback on how I could improve the thesis.

Thirdly, I would like to thank the team Inverter CPL and Mech. & PCBA at Volvo Cars for making me feel included and making my time at Volvo Cars more enjoyable. Thank you for all the help, fika, and activities.

Lastly, I would like to thank Volvo Cars for their financial support and all the fantastic people at Volvo Cars who have helped me throughout my master's thesis and made me feel welcome.

David Einarsson
Gothenburg, Sweden, 2025

List of Acronyms

Below is the list of acronyms that have been used throughout this thesis, listed in alphabetical order:

EMI	Electromagnetic interference
IC	Integrated circuit
PCB	Printed circuit board
PDN	Power delivery network
PI	Power integrity
SI	Signal integrity
VNA	Vector network analyzer
VRM	Voltage regulator module

Contents

Abstract **v**

Acknowledgements **vii**

List of Acronyms **ix**

1 Introduction **1**
- 1.1 Background 1
  - 1.1.1 Ethics and sustainability 1
- 1.2 Previous work 2
- 1.3 Purpose 2

2 Theory **3**
- 2.1 PCB stack-up 3
  - 2.1.1 PCB material characteristics 3
  - 2.1.2 Copper 4
  - 2.1.3 Planes 4
- 2.2 Traces 5
  - 2.2.1 Temperature and resistance 5
  - 2.2.2 Transmission lines 6
  - 2.2.3 Crosstalk 8
  - 2.2.4 Vias 9
- 2.3 S-parameters 10
  - 2.3.1 Vector network analyzer 10
- 2.4 PDN target impedance 11

3 Case set-up **15**
- 3.1 PCB set-up 15
  - 3.1.1 DC IR test board 16
  - 3.1.2 PDN test board 18
  - 3.1.3 SI test board 20
- 3.2 Simulation set-up 22
  - 3.2.1 DC IR simulation 22
  - 3.2.2 PDN simulation 22
  - 3.2.3 SI simulation 23
- 3.3 Hardware measurements 23
  - 3.3.1 DC IR measurements 23

3.3.2 PDN measurements 25
3.3.3 SI measurement 26

4 DC IR **27**
4.1 Simulation results 27
4.2 Hardware results 29

5 PDNs **35**
5.1 Simulation results 35
5.2 Hardware results 39

6 SI **45**
6.1 Simulation results 45
6.2 Hardware results 48

7 Conclusion **55**
7.1 Results from present work 55
7.2 Future work 56

A DC IR simulation figures **I**

1

Introduction

1.1 Background

Printed circuit boards (PCBs) are getting increasingly more complex, with smaller sizes, higher signal density, and higher switching frequencies [1]. Trace widths and clearances decrease to cope with the demand of higher signal density, which reduces the tolerances of the PCB. The higher frequencies further worsen the problems with decreased tolerances, leading to potential malfunctions of systems [2]. A redesign of the PCB is usually the only option to get a functional board, once a malfunction is identified [2]. The redesign process is costly and increases the time to market of the new product, which is detrimental to staying competitive [2].

Incorporating simulation tools in the design process is essential in improving the time and cost effectiveness of the whole process [1]. Signal integrity (SI) and power integrity (PI) are important design parameters that need to be verified before going into production. Accurately predicting the behavior of traces improves the quality of the PCB and increases the chance of getting it right the first time [2, 3].

Guidelines and best practices are commonly applied to achieve certain SI and PI performance [3]. Two areas where there are many misconceptions regarding the best practice are with decoupling capacitors and the thermal behavior of traces, including vias [3, 4, 5]

1.1.1 Ethics and sustainability

Utilizing simulations to gain additional information about the PCB could enhance the design process by improving the quality and reliability of the final product [6]. Increased reliability would improve the safety of critical devices by reducing the number of early faults. The sustainability of the devices would also increase with increased reliability, since the devices do not need to be replaced as often.

The PCB production process is associated with high energy usage, high resource expenditure, and the usage of hazardous chemicals [7]. Increasing the chance of a first successful device would reduce the number of prototypes needed to be ordered, thus reducing the waste and improving the sustainability. The lower amount of prototypes would also decrease the need for transportation, decreasing the CO2

emissions further.

PCBs are and will for a long time be extremely essential in the progress towards greener technology and are a cornerstone in enabling new technology, which would help the world move towards the UN Sustainable Development Goals [8, 9, 10]. Simulations could help serve the shift towards new technologies, by enabling a decreased time to market for new products, speeding up the transition towards more sustainable technologies.

1.2 Previous work

How simulation tools can be used to evaluate the layout of a PCB is something that has been studied in the literature. The crosstalk of the PCB can be scanned using simulations to get an overview of the layout and identify potential issues with the design [11]. SI can be further analyzed to check the simulated impedances of traces as well as the time domain response [12].

PI can also be evaluated by the placement of different decoupling capacitors, and then simulate the impedance of the power delivery network (PDN), which consists of the voltage regulator module (VRM), the power trace/area and finally the decoupling capacitors [13]. Moreover, could the thermal properties of the PCB also be simulated [14, 15]. The whole PCB is simulated to determine the overall temperature of the PCB and identify hot spots.

However, what is missing is a focus on the copper interconnects of the PCB, including traces, planes and vias. Where both SI, PI and thermal properties of different design options are evaluated in simulation and verified on the actual board. Understanding how different sizes, layer placements and transitions of copper interconnects affect the final performance of the PCB could increase the chance of a successful first design.

1.3 Purpose

The purpose of this thesis is to investigate the effect that layout has on different performance areas applicable to a traction inverter PCB. The focus will be on the copper interconnects on the PCB, where thermal behavior, PI and SI will be investigated. Simulations will be utilized to evaluate the performance of different copper interconnect designs, which will be compared to measurements on produced boards.

This thesis aims to study the following questions:

- How well do the simulations of the design correspond to the measurements of the produced PCBs?
- What options does the layout designer have to improve the thermal behavior, PI or SI of the PCB, and how effective are those?

2

Theory

2.1 PCB stack-up

PCB stack-ups come in many different variants. The PCB can be classified into three categories: single layer, double layer or multi-layer [16]. The PCB design engineer chooses the suitable number of layers based on the design complexity, regarding signal density, electromagnetic interference (EMI), SI, cost, and et cetera [16, 4].

To build the layers, the board fabricators typically purchase basic board material covered with copper foil [5]. The board material is the dielectric, which is formed by pressing layers of filler and resin under heat to form the insulating material [1]. The PCB will have different characteristics, depending on the combination of filler and resin used [1].

2.1.1 PCB material characteristics

There are many different dielectrics, with different characteristics that could be used in the stack-up of the PCB [17]. The most common category is FR4, however there are options within that category as well [17].

The dielectric has a relative permittivity (ε_r) often referred to as the dielectric constant. The dielectric constant determines the capacitive parasitics of the PCB and is an important parameter in the design. The value of the dielectric constant could, as an example range from 2.8 to 4.5 [1].

The dielectric also conducts heat in the PCB. The heat can spread in two directions, parallel to each plane or perpendicular, going from top to bottom. To characterize the thermal properties of a material, the thermal conductivity coefficient is used. The thermal conductivity of the material should be specified in each direction, since board materials are usually anisotropic, meaning they conduct heat better in one direction than in the other. A typical range for thermal conductivity coefficients of dielectrics is 0.3 to 0.8 W/mK [5].

2.1.2 Copper

There are two common methods for producing the copper foil, either by electrodeposition or rolled to the correct thickness [5, 1]. The electrodeposited method uses voltage to attract positive copper ions to the cathode, where the copper foil is produced. The cathode is rotating and the copper foil thickness is controlled by the rotation speed of the cathode [5, 1]. The rolled copper foils are produced by rolling copper between a series of rollers, where each pair of rollers flattens the copper and decreases the thickness [5].

There are some differences between the different processes. The surface roughness of electrodeposited copper is greater than that of rolled copper. However, the resistivity of rolled copper is higher than electrodeposited copper [5, 1]. There are some variations in the foil produced from each method, but the thickness tolerance is usually within 10% [5].

Copper foils that will constitute the inner layers of the PCB will go through an etching process where the trace network is mapped onto each copper foil [17]. Once each inner layer has been etched, the basic board materials are bonded together to form the complete PCB. The holes of the PCB are then drilled for through-hole components and vias [5, 1].

The next step is copper buildup on traces and holes. The plating procedure can be done in two ways, either pattern plating or panel plating [5, 1]. Pattern plating applies photoresist to the regions that should not be plated with copper and allows the copper to build up a layer on the exposed surfaces. Panel plating plates the whole PCB, producing an extra copper layer over the entire copper foil.

The trace network is etched out after the additional copper has been deposited, producing more copper waste in the panel plating process. Once the final etching process is done, is the outer copper protected from oxidation using a solder mask and surface finish of the exposed pads [1, 17].

The final result of each method is a plated copper layer sitting above the copper foil for the outer layers. The plating process does not have the same tolerance as for the copper foil [5]. There has been evidence that the plating thickness can vary across the board, with differences up to 50% not being uncommon [5].

2.1.3 Planes

A common design choice is the usage of planes in the layer stack-up. The plane is a solid region of copper that usually encompasses the whole layer [1, 16, 4]. Ground- or power planes are common in the PCB, since they act as EMI shielding, reducing the radiated emissions of the PCB [1, 3]. Placing the planes closer to signal layers allows the signals to have a stable reference that acts as a small capacitance for the signals [16]. This is further utilized by placing the power and ground plane adjacent to each other to improve the capacitance between the layers [3, 17]. The parallel

capacitance between the two planes is calculated as

$$C_{pp} = \varepsilon_0 \frac{\varepsilon_r A}{d} \tag{2.1}$$

where C_{pp} [F] is the capacitance between the planes, ε_0 is the vacuum permittivity at 8.85×10^{-12} F/m, ε_r is the relative permittivity of the board material, A [m^2] is the area of the power and ground planes and d [m] is the distance between the power and ground planes [3].

2.2 Traces

Traces are copper pathways etched out of the copper foil to form networks connecting different components on the PCB [5]. A single trace acts as a wire conducting current from one point to another.

2.2.1 Temperature and resistance

The resistance associated with a trace is calculated accordingly to

$$R = \frac{\rho L}{A} \tag{2.2}$$

where ρ [Ω m] is the resistivity of the material, L [m] is the length of the trace and A [m^2] is the cross sectional area of the trace [5]. The resistivity of copper foil (ρ_{copper}) is in the range of 1.62×10^{-8} to 1.74×10^{-8} Ω m depending on production method, measured at a temperature of 20 °C [5, 1].

Hinted by the above statement is that resistivity has a temperature dependency, which could be represented by the thermal coefficient of resistivity (α) [5]. The thermal coefficient of resistivity is derived from

$$\alpha = \frac{\frac{\Delta\rho}{\rho}}{\Delta T} \tag{2.3}$$

where T [K] is the temperature of the material [5]. The calculation of ρ at a specific temperature is done by

$$\rho(T) = \rho(T_0)(1 + \alpha_0(T - T_0)) \tag{2.4}$$

where T_0 is the temperature reference of ρ, which in this case is 20 °C [5]. The thermal coefficient of resistivity is also defined at a reference temperature, denoted as α_0. For copper the thermal coefficient of resistivity (α_{copper}) at 20 °C is 4×10^{-3} K^{-1} [5]. Using (2.2) with (2.4), assuming the ratio between trace length (L) and trace cross section (A) to be constant with temperature, gives

$$R(T) = R(T_0)(1 + \alpha_0(T - T_0)) \tag{2.5}$$

where the resistance now has a temperature dependency. Equation (2.5) could also be rearranged into the following form

$$T - T_0 = \frac{1}{\alpha_0}(\frac{R(T)}{R(T_0)} - 1) \tag{2.6}$$

where the temperature change could be calculated from the change in resistance. This allows the average temperature of the trace to be deduced from the measurement of the voltage drop between two points for a given current level, and applying Ohm's law to get the resistance. The first measurement needs to be done at the reference level, and then each new measurement can be compared to the reference level.

How the temperature changes with different parameters is described by

$$\Delta T \propto \frac{I^2 R}{W + Th} \tag{2.7}$$

where I [A] is the trace current, R [Ω] is the trace resistance, W [m] is the trace width and Th [m] is the trace thickness [5]. Furthermore, there is a time constant before the temperature reaches a steady value. The time needed for the temperature to stabilize is usually in the range of 6 to 15 minutes [5].

Having a plane underneath the trace improves the thermal performance, since the plane acts as a heat sink, effectively spreading the heat throughout the PCB [5]. Even if the trace is not directly connected to the plane by a thermal via, will the heat still spread down to the plane from the thermal conductivity of the dielectric [5].

The effect trace corners have on the thermal performance of the trace is minimal [5]. One misconception is that the temperature must be higher, since the current density is higher on the inside of the corner. However, the cross-sectional area of the corner is bigger if the corners are not rounded and kept at a constant width. The bigger cross area lowers the resistance, thus the effect of increased current density is somewhat canceled by the effect of reduced resistance.

There are some small temperature differences inside the corner area, which comes from the fact that the cooling of each side of the corner is different [5]. The outer turn of the trace has more contact with other board material than the inside turn has, resulting in the outer turn region running cooler than the inner turn region. The temperature difference of the corner area compared to the straight trace is minimal overall [5].

2.2.2 Transmission lines

At higher frequencies, the trace starts to behave as a transmission line conducting electromagnetic waves [17]. An important attribute of the transmission line is the characteristic impedance Z_0 [1, 17]. The characteristic impedance depends on the

parasitics of the trace and is calculated as

$$Z_0 = \sqrt{\frac{L}{C}} \tag{2.8}$$

where L [H] is the parasitic inductance and C [F] is the parasitic capacitance [1]. The parasitics of the trace and thus the characteristic impedance are determined by the geometry of the PCB [1, 17]. There are two common ways to design transmission lines, either microstrip or stripline [1, 17].

A microstrip is a trace that is placed on one of the outer layers, with the adjacent inner layer being a ground plane [1, 17]. The characteristic impedance can be estimated using

$$Z_0 = \Big(\frac{\mathrm{X}}{\sqrt{\varepsilon_r + 1.41}}\Big) ln\Big(\frac{5.98H}{0.8W + T}\Big) \tag{2.9}$$

where Z_0 [Ω] is the characteristic impedance, X is a constant depending on the trace width, ε_r is the relative permeability of the dielectric, H [m] is the distance to the ground plane, W [m] is the width of the trace and T [m] is the thickness of the trace [18]. X is equal to 79 for trace widths between 5 and 15 mils (0.127 to 0.381 mm), and 87 for trace widths between 15 and 25 mils (0.381 to 0.635 mm) [18].

The microstrip is commonly coated with solder mask when placed on the outer layer. The solder mask has a dielectric constant that differs from air, which has an impact on the impedance of the trace [1]. If the coating thickness is small, the impedance change will be negligible, otherwise it may change the impedance by several ohms [18].

By comparison, the stripline is routed on the inner layer with two adjacent ground planes, one above and one below [1, 17]. The planes could either be located at the same distance from the trace, creating a symmetrical stripline, or at different distances, creating an asymmetrical stripline [1].

The equation for determining the impedance for a symmetrical stripline is

$$Z_0 = \Big(\frac{60}{\sqrt{\varepsilon_r}}\Big) ln\Big(\frac{1.9B}{0.8W + T}\Big) \tag{2.10}$$

where Z_0 [Ω] is the characteristic impedance, ε_r is the relative permeability of the dielectric, B [m] is the distance between the two ground planes, W [m] is the width of the trace and T [m] is the thickness of the trace [18].

Equations (2.10) and (2.9) are only approximations to determine the impedance. The finished PCB can be analyzed using simulation tools that include the whole geometry of the stackup, with traces, to determine the characteristic impedance. An electromagnetic field solver is typically used to get a more accurate result in calculating the width needed for a certain characteristic impedance [19].

Matching the characteristic impedance of the transmission line to the source/receiver of the circuit is an important concept that needs to be followed to minimize the

reflections caused between different regions [1]. When the impedance is matched within the circuit, the energy flows without any disturbances, allowing the right information/power to be transferred to the receiver [1].

How much impact an impedance mismatch has, depends on the length of the trace in relation to the wavelength of the frequency [1]. Many rules of thumb are used to calculate a critical length where the trace should be regarded as a transmission line. However, best practice would be to design the trace to match the impedance over the frequency range of interest, instead of relying on critical lengths [20].

$50\,\Omega$ is commonly used for the characteristic impedance of single-ended traces [19, 1]. The $50\,\Omega$ value stems from the early use of coaxial cables, where it was optimal to design the coaxial cable with a characteristic impedance of $50\,\Omega$ [19]. The other systems needed to follow the $50\,\Omega$ standard to minimize impedance mismatch, once the cable was designed for $50\,\Omega$ [19].

There are advantages and disadvantages of designing with a higher impedance than $50\,\Omega$. Higher impedance allows for the design of smaller traces, thus enabling the designer to increase the interconnect density [19]. However, higher impedance can result in more crosstalk between traces, with more emissions and greater EMI sensitivity [19, 1].

2.2.3 Crosstalk

Crosstalk is the interference created from an activated signal, the aggressor, which is coupled to the victim signal either through inductive coupling or capacitive coupling [1, 21]. The voltage interference on the victim line is divided into two categories, near-end and far-end [21]. Near-end is at the source end, at the start of the trace, while far end is at the end of the trace, at the receiver [21].

For two nearby traces, the capacitive and inductive coupling can be represented in matrix form as

$$\mathbf{L}^{CM} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \quad \mathbf{C}^{CM} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \tag{2.11}$$

where L_{11} and L_{22} are the inductance for trace 1 and trace 2, L_{12} and L_{21} is the mutual inductance between the traces, C_{11} and C_{22} is the capacitance to the ground plane for trace 1 and trace 2, and C_{12} and C_{21} is the mutual capacitance between the traces [21]. The capacitance and inductance matrices are usually determined from an electromagnetic field solver that uses the geometry and materials to calculate the values [21].

The inductive- (K_L) and capacitive (K_C) coupling coefficients can then be determined as

$$K_L = \sqrt{\tfrac{L_{12}L_{21}}{L_{11}L_{22}}} \quad K_C = \sqrt{\tfrac{C_{12}C_{21}}{C_{11}C_{22}}} \tag{2.12}$$

which are then used to determine the para- (K_B) and tele-cross-talk (K_F) coefficients as

$$K_B = \tfrac{K_L+K_C}{4} \quad K_F = \tfrac{K_L-K_C}{2} T_p D_{coupled} \tag{2.13}$$

where T_P [s] is the average propagation time of the signal and $D_{coupled}$ [mm] is the coupled length [21].

The near-end crosstalk voltage (V_{Next}) could then be determined as

$$V_{Next} = K_B\Big(V_1(t) - V_1(t - 2T_P D_{coupled})\Big) \tag{2.14}$$

and the far-end crosstalk voltage (V_{Fext}) as

$$V_{Fext} = -K_F \frac{d\Big(V_1(t - T_p Dcoupled)\Big)}{dt} \tag{2.15}$$

where $V_1(t)$ [V] is the applied voltage on the aggressor line [21]. Analyzing (2.14) shows that the near-end crosstalk is dependent on the inductive and capacitive coupling as well as the aggressor voltage level. In comparison, the far-end crosstalk has the same dependencies with the added dependence on the coupled length as well as the rise time of the aggressor signal.

Both inductive and capacitive coupling depend on the distance between the signals, thus the effect could be diminished by increasing the separation between the signals [21]. Another method to decrease the crosstalk between signals is to introduce a ground line between the signals, thus reducing the impedance to ground and effectively directing away the disturbance [4, 17]. However, this would also impact the characteristic impedance of the trace, which would affect the reflections caused at each end, potentially leading to more radiation of disturbances of the aggressor trace [21].

2.2.4 Vias

Vias are used to transition between different layers on the PCB. The most common type of via is a plated through-hole via [1]. The plated through-hole via is manufactured by drilling a hole and plating the hole with copper (Section 2.1.2). Connection pads are placed on the desired layers, enabling current to travel from one connection pad, through the copper-plated hole, to the other connection pad [1].

Vias have resistance that can be calculated accordingly to (2.2) [5]. However, the via length compared to the total trace length is usually short, thus the resistance of the via is negligible in the overall picture [5].

Leading current through the vias creates heat. However, the via temperature is not only determined by the current flowing through it, but also by how each end of the via is connected to the trace [5]. The vias will be cooled by the traces if the conducting area of the traces is bigger than the conducting area of the connected vias. The opposite is also true, where the via could act as a heat sink for thin traces [5].

Vias also have inductive and capacitive parasitics that need to be included for high-frequency analysis [3]. Potential SI and PI issues might arise if the parasitics are neglected. An electromagnetic field solver can be used to simulate the circuit, to get a better understanding of how the vias affect the performance of the circuit [3].

2.3 S-parameters

S-parameters are used to determine the reflective and transmissive behavior of electromagnetic waves traveling to a high-frequency device, regarding amplitude and phase [21].

The simplest definition of S-parameters stems from looking at a device with two connection points. Two different quantities can be determined by looking at the first connection point. The voltage waves going into the device at point 1 are referred to as $a1$, and the voltage waves coming out of the device at point 1 are referred to as $b1$. Similarly are $a2$ and $b2$ defined for access point 2 [21]. S-parameters are then defined as

$$\begin{aligned} b1 &= S_{11}a1 + S_{12}a2 \\ b2 &= S_{21}a1 + S_{22}a2 \end{aligned} \tag{2.16}$$

where S_{11} and S_{22} are the reflection coefficients, and S_{12} and S_{21} are the transmission coefficients [21].

If the characteristic impedance of the transmission line is matched to the reference impedance of the source generator, the reflection coefficients of the transmission line would ideally be zero, since no reflection would occur on the line [21]. Moreover, the transmission coefficients would reflect the propagation characteristic of the transmission line [21].

S-parameters depend on the characteristic impedance of the measurement equipment, since the reflection is measured in the transition between the measurement equipment and the test point [21]. Moreover, the S-parameters are functions of frequency since the reflective and transmissive behavior depend on the impedance, which is dependent on the parasitics of the circuit [21].

2.3.1 Vector network analyzer

A vector network analyzer (VNA) is commonly used to determine the S-parameters at high frequencies [21]. The VNA is a generator that sends signals with a single frequency at a constant amplitude. By measuring the reflected and transmitted waves at different frequencies, the S-parameters can be defined over a frequency span [21].

Calibrations are done before any measurement is taken, to account for losses in cables and non-ideal defects inside the VNA [21]. A simple form of calibration is short, open, load and thru calibration. A kit with calibration connectors is commonly provided by the manufacturer to allow the VNA to be calibrated against known sources, so the S-parameters can be corrected for different errors [21].

The characteristic impedance of a transmission line can be calculated according to

$$Z_c = \sqrt{Z_{sc}Z_{oc}} \tag{2.17}$$

where Z_c [Ω] is the characteristic impedance, Z_{sc} [Ω] is the short circuit impedance

and Z_{oc} [Ω] is the open circuit impedance [21]. The short circuit impedance is measured when the trace is terminated with a short circuit at one end and the port is located at the other end. The open circuit impedance is measured when the short circuit is removed, leaving the end open [21].

A different method used to measure the low impedance of PDNs is the Shunt-Thru measurement. The Shunt-Thru method uses two ports to measure the impedance of the PDN [22]. The two ports are connected to the PDN, where one port sends the generated signal, while the other is used to measure how much of the signal passes the PDN. The measured impedance is calculated as

$$Z_c = 25\frac{S_{21}}{1 - S_{21}} \tag{2.18}$$

where S_{21} is the transmission coefficient from port 1 to port 2, assuming the impedance of the measurement equipment is $50\,\Omega$ [22].

2.4 PDN target impedance

It is common to use the target impedance method to improve the power delivery from the voltage regulators to the load devices [3]. The target impedance method determines the maximum allowed impedance over a frequency spectrum, and then the PDN is optimized using decoupling capacitors to reach the target [3]. The target impedance is determined as

$$Z_{tar} = \frac{V_{dd}Ripple}{I_{trans}} \tag{2.19}$$

where Z_{tar} [Ω] is the target impedance, V_{dd} [V] is the positive supply voltage for the load, *Ripple* [%] is the maximum allowed voltage ripple to the load and I_{trans} [A] is the maximum transient current [3]. I_{trans} is assumed to be constant in (2.19), but a more detailed analysis would include I_{trans} as a function of frequency, thus Z_{tar} would also be a function of frequency [4].

The VRM, viewed from the load side, in the PDN could be modeled with inductors and resistors [23]. Modeling the VRM allows the impedance seen at the load side to be estimated using different simulation tools. Once the impedance is simulated, could different decoupling capacitors be evaluated to analyze the impact they have on the overall impedance.

Two main reasons exist for including decoupling capacitors in a PDN[4]. The first reason is to provide energy for the switching integrated circuit (IC), to ensure that there is no voltage drop locally at the IC when it draws current [4]. If the capacitors are not sized correctly or the inductance is too high between the capacitors and the IC, could it lead to signal integrity issues and potentially loss of function for the IC [4].

The other reason is to filter away any high-frequency disturbance present in the PDN from reaching the IC [3]. A low impedance between power and ground allows

high-frequency disturbances to be effectively filtered away through the ground before reaching the IC.

The decoupling capacitors used to reach the target impedance have parasitics, including series inductance and resistance with the capacitance [3]. At higher frequencies, the inductance of the capacitor starts to dominate, and its impedance increases. The frequency at which the impedance is lowest is called the self-resonant frequency and can be calculated as

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{2.20}$$

where L [H] is the series inductance, C [F] is the capacitance from the capacitor and f_{res} [Hz] is the resonant frequency [3].

As shown in (2.20), the self-resonance frequency increases if either the capacitance or the inductance is decreased. The package size influences the inductance of the capacitor. Choosing a smaller package lowers the lead inductance, pushing the self-resonance frequency higher [3, 24].

A common guideline is to use capacitors from 0.01 µF up to 1 µF for decoupling [4, 24]. Using lower capacitance values gives a higher self-resonant frequency, according to (2.20). However, they also introduce resonant peaks between the different valued capacitors. Since the peaks pose more problems than the gained dips from the increased self-resonant frequency, they are not recommended [24].

The old guideline also based its assumption on that there would be a difference in inductance between the capacitors of value 0.01 to 1 µF, which was true 50 years ago [24]. Today, that is not true for surface-mounted capacitors [24]. Focus should be on introducing high capacitance to improve the low frequency performance and low inductance for the high frequency performance [24]. Choosing the highest capacitance value for the given package is an optimal approach if the inductance does not significantly vary with capacitance for the given package [4, 24].

Higher capacitance values typically require bigger packages, increasing the inductance [3]. Thus, the bigger packages are important for lower frequencies and the smaller packages for higher frequencies. Using a combination of different packages is usually the best approach [3].

How close the capacitors are placed to the IC is another important concern. A common approach is to place the capacitors as close as possible to the IC [3, 4]. Close placement allows the trace between the capacitor and the IC to be kept short, reducing the inductance [3].

However, the board space around the IC might be limited, not allowing the placement of decoupling capacitors close to the IC [25]. Placing the capacitors further away from the IC might still be effective [25]. The inductance gained by placing the capacitors further away is determined by the distance to the power planes as well as how the capacitor and IC are connected to the planes [25]. A shorter distance from the planes reduces the inductance, since the length the current needs to

travel through the via is reduced. Placing the capacitor further away could allow for better connection to the planes by allowing the placement of more parallel vias. Furthermore, the number of capacitors could be increased if placed further away, which might have a greater impact on the impedance than placing a single capacitor close by [25].

Decoupling capacitors have minimal impact on the impedance at high frequencies, in the range of 100 MHz and above [4]. Instead, the via inductance starts to limit the impedance of the capacitor [4, 25]. The plane capacitance (Section 2.1.3) starts to dictate the impedance at frequencies above 100 MHz [25]. A shorter distance between the planes improves the capacitance according to (2.1), significantly improving the impedance for higher frequencies [4].

3

Case set-up

The layout of a traction inverter for an electric vehicle is a complex structure that has hundreds of signals all packaged together on a single board. The signals contained on the board can be classified into different categories, where each category has different requirements it needs to fulfill to allow the board to function within specifications. Three categories were chosen for this study, where layout plays a significant role in deciding the final performance of the signal on the PCB. The three identified key performance areas were steady state current capability of main power traces, impedance of PDNs over a frequency range, and SI of high frequency signals concerning impedance matching as well as crosstalk between traces.

A test board was designed for each performance area, thus lowering the overall complexity by clearly separating the different topics and only focusing on changes related to the specific area on each board. Designing test boards compared to measuring on the actual inverter has the benefit of enabling easy connections to the points of interest using available test equipment. The test boards should help serve to answer the questions specified in Section 1.3.

3.1 PCB set-up

The three different test boards were designed using Altium Designer, where each board was limited to investigating different options related to the area of focus. The first board, named DC IR, was used to simulate and measure the steady-state condition of current flowing through traces of the board. The two parameters of interest were the voltage drop and the temperature increase of the trace, since both are limiting factors used when designing high-current traces of a PCB.

The other two boards were designed to measure the impedance of traces for different frequencies. The PDN test board had different trace widths and layer placements for power delivery traces. Different configurations of decoupling capacitors could be connected to the trace to evaluate the impact that decoupling capacitors have on the impedance profile. The SI test board also utilizes different trace widths and layers to analyze the impedance of signal traces in microstrip and stripline configurations. Having a ground line to reduce crosstalk is also explored with the SI test board.

The PCBs were produced by JLCPCB, which has the following noteworthy tolerances and characteristics seen in Table 3.1 [26, 27]. Moreover, the via dimensions

Table 3.1: JLCPCB tolerance and characteristics for PCB manufacturing

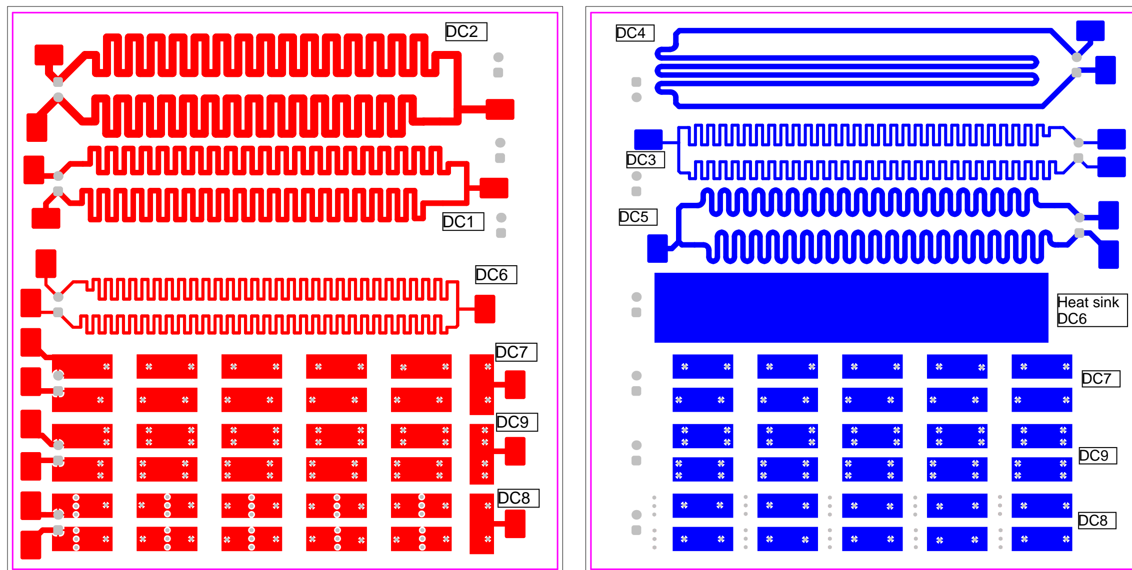
Feature	value
Board thickness tolerance (T > 1 mm)	10%
Board thickness tolerance (T < 1 mm)	±0.1 mm
Average hole plating thickness	18 µm
Minimum track width and spacing	0.10 mm
Track width tolerance	20%
Solder mask dielectric constant	3.8
Core dielectric constant	4.6
Prepreg dielectric constant	4.4

were set to be 0.3 mm hole size and 0.6 mm via diameter for all three PCBs. An overview of each PCB is presented below.

3.1.1 DC IR test board

The DC IR test board is a two-layer, 1.6 mm thick PCB. The outer copper layers are 35 µm thick and the two layers contain 9 different nets, which are used to investigate different aspects. Furthermore, are there 3 test points placed on the board for each net, to measure the voltage at the input, middle point and output of each net.

An overview of the board with traces on the top and bottom layer is displayed in Figure 3.1. Each trace net is named accordingly to DCX, where X is replaced with a number. Net DC1, DC2 and DC3 are used to investigate what effect the trace



(a) DC IR layout top view

(b) DC IR layout bottom view

Figure 3.1: DC IR layout top and bottom views

width has on the voltage drop and thermal behavior of the net. The important characteristics are summarized in Table 3.2. The impact of the corners and cornering

Table 3.2: Trace setup for net DC1, DC2 and DC3

Net name	Corner type	W_{trace} [mm]	L_{trace} [mm]
DC1	Sharp corners	0.9	500
DC2	Sharp corners	1.3	500
DC3	Sharp corners	0.5	500

type is investigated by comparing net DC1, DC4 and DC5. DC4 has fewer corners compared to DC1, and DC5 has rounded corners. All three nets have the same length and width as presented for net DC1 in Table 3.2.

The option of adding a filled copper region under the trace to act as a heat sink is explored using DC6 which compares to DC3. DC6 has the same dimensions as DC3, with the difference that there is a filled copper region on the second layer, which has no direct connection to the traces above. By not directly connecting the plane to the trace, using a thermal via, enables the thermal conductivity of the dielectric material to be assessed.

Vias' effect on thermal performance and voltage drop is investigated using nets DC7, DC8 and DC9. Each net consists of polygons with a width of 10 mm and the total length between input and output is approximately 146 mm. DC7 uses a single via to connect the different layers. In total, there are 20 via transitions in the net. DC9 uses two vias in parallel, instead of a single via to transition between the layers, making a total of 40 vias.

Vias could also obstruct the fill of different copper regions in a design. To test this scenario were three vias added in a row across the copper fill at ten different locations, evenly spaced out within the net of DC8. Everything else was the same as for DC7.

The test board aims to investigate the following questions:

- How big of an impact does trace width have?
- How much do trace bends and sharp corners impact?
- Could unconnected copper on an adjacent layer serve as a heat sink?
- What is the difference between using a single via vs two vias?
- How much impact does via cutout of a polygon have?
- How well does the thermal simulation compare to the actual board?
- How well does the voltage simulation compare to the actual board?

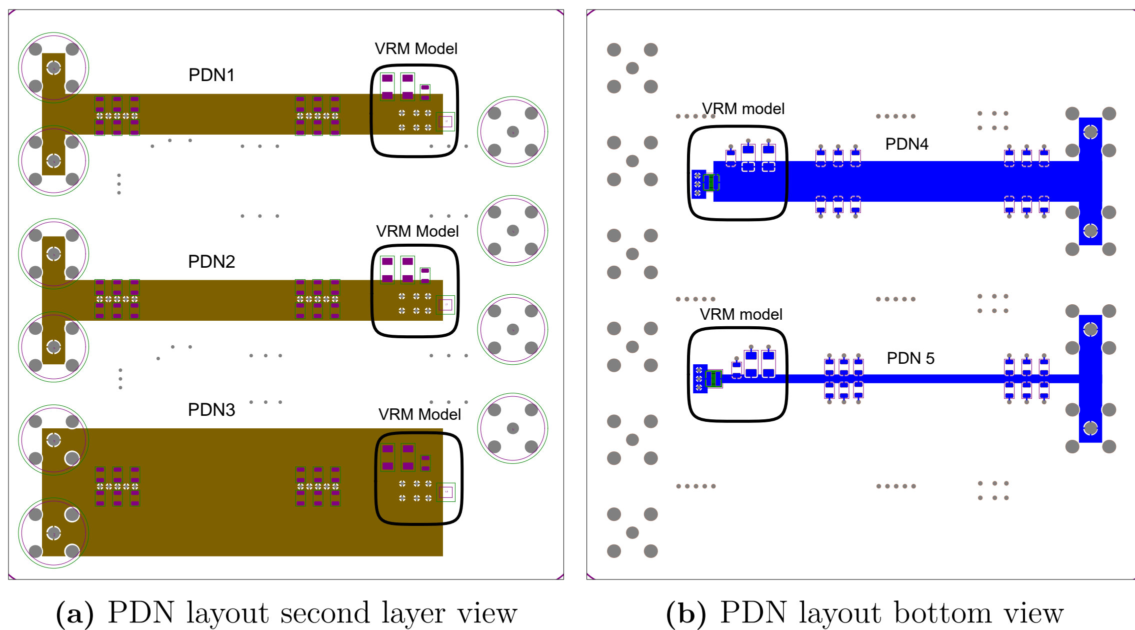
3.1.2 PDN test board

The PDN test board is a four-layer 0.8 mm thick PCB, with a stackup according to Figure 3.2. The top layer is the GND plane of the PCB, the second layer is used

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01524mm	3.8	
1	Top Layer		Signal	1oz	0.035mm		
	Dielectric 2	PP-006	Prepreg		0.2104mm	4.4	0.02
2	Pwr	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 1	FR-4	Core		0.25mm	4.6	0.02
3	Empty	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 3	PP-006	Prepreg		0.2104mm	4.4	0.02
4	Bottom Layer		Signal	1oz	0.035mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01524mm	3.8	
	Bottom Overlay		Overlay				

Figure 3.2: The stackup of the PDN test board extracted from Altium Designer

to route 3 different PDNs, the third layer is unused with no copper and lastly, the fourth layer has two PDNs. An overview of the trace routing in the second layer and fourth layer is displayed in Figure 3.3. The traces are named accordingly to



(a) PDN layout second layer view

(b) PDN layout bottom view

Figure 3.3: PDN traces second and bottom layer

PDNX, where X is a number from one to five. Each PDN has an inductor at each end with three capacitors in parallel to model the behavior of a VRM. The inductor has a value of 100 nH, while two capacitors have a value of 10 µF and the third has a value of 100 nF.

Both near the VRM and closer to the connector are a group of six capacitors placed for each PDN. Three of the twelve capacitors will be populated for each test, to test in total four different capacitor combinations and placement for each trace. The

four different capacitor scenarios are summarized in Table 3.3. The characteristics

Table 3.3: PDN capacitors combinations

Capacitor group	Values [µF]	Placement
Design guideline	1, 0.1, 0.01	Close
Design guideline	1, 0.1, 0.01	Far
10 µF	10, 10, 10	Close
10 µF	10, 10, 10	Far

of each PDN are summarized in Table 3.4. Due to a design mistake, is PDN1 identical to PDN2. The original concept had high via inductance in PDN2 so that it could be more directly compared to PDN4. PDN1 is excluded from the results since there would be no significant difference compared to PDN2.

Table 3.4: PDN characteristics

Trace	Width [mm]	Layer	Via inductance	Plane capacitance
PDN1	7	2	Low	Medium
PDN2	7	2	Low	Medium
PDN3	22	2	Low	High
PDN4	7	4	High	Low
PDN5	1.5	4	High	Lowest

The test board aims to investigate the following questions:

- How much impact does the trace width have?
- How does the far placement of decoupling capacitors compare to close placement?
- How much can the impedance be improved by optimizing the decoupling capacitors compared to usual design guidelines?
- How well does impedance simulation compare to the actual board?

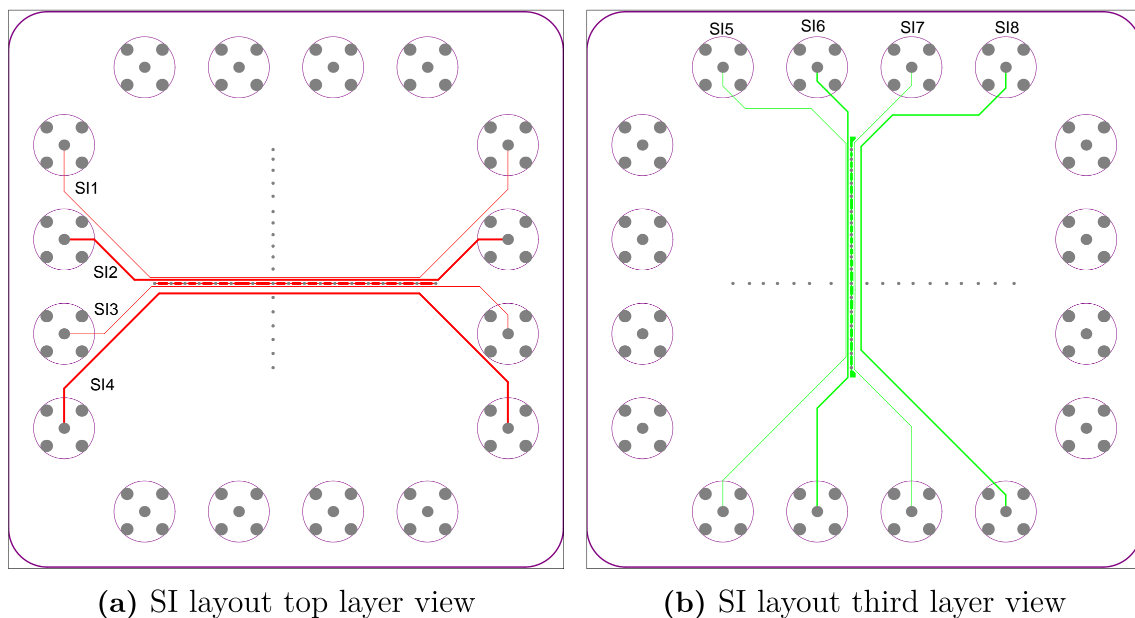
3.1.3 SI test board

The SI test board is a four-layer 1.6 mm thick PCB, with a stackup according to Figure 3.4. The top layer is used to route traces as microstrips, the second layer

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01524mm	3.8	
1	Top Microstrip		Signal	1oz	0.035mm		
	Dielectric 2	PP-006	Prepreg		0.2104mm	4.4	0.02
2	GND	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 1	FR-4	Core		1.065mm	4.6	0.02
3	Stripline	CF-004	Signal	1/2oz	0.0152mm		
	Dielectric 3	PP-006	Prepreg		0.2104mm	4.4	0.02
4	Bottom GND		Signal	1oz	0.035mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01524mm	3.8	
	Bottom Overlay		Overlay				

Figure 3.4: The stackup of the SI test board extracted from Altium Designer

is a ground plane, the third layer is used to route traces as striplines, and the last layer is a ground layer. An overview of the trace routing in the first layer and third layer is displayed in Figure 3.5. The traces are named accordingly to SIX, where



(a) SI layout top layer view

(b) SI layout third layer view

Figure 3.5: SI traces top and third layer

X is a number from one to eight. The first four traces are located on the top layer and are routed as microstrips, while the other four are routed on the third layer as striplines. The important characteristic of each trace is summarized in Table 3.5. The minimum trace width (Table 3.1) was chosen for half of the traces to get as high impedance as possible, while the other traces were designed for an impedance of 50 Ω. The target impedance was calculated using Ansys SIwave, more on that in Section 3.2.3.

Table 3.5: SI trace width and target impedance

Trace	Width [mm]	Target impedance [Ω]
SI1	0.1	84
SI2	0.36	50
SI3	0.1	84
SI4	0.36	50
SI5	0.1	74
SI6	0.27	50
SI7	0.1	74
SI8	0.27	50

The traces were placed close to each other to enhance the effect of crosstalk between traces. The distance between the traces is presented in Table 3.6. Traces on layer 1

Table 3.6: SI distance between traces

Trace	Neighbor 1 [mm]	Neighbor 2 [mm]
SI1	X	SI2 0.15
SI2	SI1 0.15	SI3 1
SI3	SI2 1	SI4 1
SI4	SI3 1	X
SI5	X	SI6 0.15
SI6	SI5 0.15	SI7 1
SI7	SI6 1	SI8 1
SI8	SI7 1	X

are mirrored on layer 3, where for example both SI1 and SI5 have the same distance to their neighbor. Furthermore, has a ground trace been placed both between trace SI2 and SI3, as well as between SI6 and SI7. The ground traces are used as shields for crosstalk, reducing the coupling between the traces. The average coupled distance for the microstrip traces is 50 mm, while for the stripline traces the distance is 40 mm.

The test board aims to investigate the following questions:

- How much effect does the ground trace have in minimizing crosstalk?
- What is the difference in crosstalk between microstrip and striplines?
- How is the crosstalk affected when traces have different terminations?
- How well does the impedance simulation compare to the actual board?
- How well does the crosstalk simulation compare to the actual board?

3.2 Simulation set-up

Ansys SIwave was the simulation software used to simulate the performance of the three different test boards. The complete PCB was exported from Altium Designer to be imported into SIwave, where PI, SI and electro-thermal performance were evaluated. An overview of the simulation set-up is presented below.

3.2.1 DC IR simulation

SIwave divides the trace into mesh elements to calculate the current density and voltage drop of each element. The total voltage drop as well as the power dissipation of the whole trace could be extracted by combining the contributions of each element.

The power dissipation is fed into Ansys Icepack, which uses the information to calculate the temperature of the board, based on the overall PCB layout. The temperature information is fed back into SIwave to update the resistivity of copper and rerun the simulation. The loop is continued between SIwave and Icepack until the temperature has reached a convergence, where the change is less than 1%.

All simulations were done in 20 °C, with the first test being to load each trace with 2 A. The traces were simulated independently, one at a time, so that the power dissipation of one trace would not affect the others.

Net DC1 was further simulated to include uncertainties in the thickness and width of the trace. The trace width tolerance is given from Table 3.1 as 20% and the tolerance for the copper is 10% for the foil and 50% for the plating, resulting in overall copper thickness having 30% tolerance, assuming that the plating and copper foil have the same thickness, see Section 2.1.2. Two end cases were considered, one where the thickness and trace width were at their minimum, and the other where both were at their maximum.

Net DC7 and DC9 were also loaded with 3 A to see if the vias would get significantly hotter than the traces.

3.2.2 PDN simulation

A port to measure the impedance was placed at one of the two connectors for each PDN. Each PDN was simulated first without decoupling capacitors, only with the capacitors and inductance used to model the VRM. A frequency sweep was done to extract the impedance seen from the port for each PDN.

The different decoupling capacitor configurations were simulated after, where only three decoupling capacitors were active for each sweep according to Table 3.3. The decoupling capacitors, as well as the capacitors and inductance of the VRM, were simulated to include the parasitics of each component.

3.2.3 SI simulation

SIwave could use the information from the PCB stackup to estimate the width needed for different transmission lines to achieve a certain impedance. The capacitance and inductance of each trace are calculated from the stackup, which is used to determine the impedance. This feature was used to determine the required width of the traces to achieve a target impedance of 50 Ω, see Table 3.5. Furthermore, could the impedance of already designed traces be estimated from the given width and layer placement of the traces. This was used to determine the impedance of the 0.1 mm wide traces, see Table 3.5.

A frequency sweep was done to get the average characteristic impedance value for each trace. A port was placed at one of the connectors to each SI trace, while the other connector was terminated with either a short circuit or an open circuit. The frequency sweep was done first with the short circuit termination and then with the open circuit termination. Using the information from each frequency sweep, the characteristic impedance of each trace could be calculated accordingly to (2.17).

The crosstalk between traces was also simulated. An aggressor, in the form of a pulse generator, was placed at the aggressor trace that was either terminated by 50 or 75 Ω in the other end. The rise time and pulse voltage level of the pulse generator were set to be 30 ps and 1.5 V in the simulation, which affects the crosstalk. The voltage levels on the nearby victim traces were measured to determine the peak voltage, both for the near-end and far-end crosstalk for each trace. The victim traces were also terminated by either 50 or 75 Ω. Changing the termination impedance of the aggressor and victim's lines allows the effect of impedance mismatch to be studied.

3.3 Hardware measurements

The manufactured test boards were tested to compare the simulation results to the actual values. How each test board was set up for hardware measurements is presented below.

3.3.1 DC IR measurements

An overview of the test setup is presented in Figure 3.6. Two multimeters were used for each test to measure the voltage drop of the trace. One measured the total voltage drop, and the other measured the voltage drop at the halfway point. Both multimeters used the first test point as a reference, thus discarding the voltage drop of the wires connecting to the trace.

Two thermocouples were placed on the PCB, where the first one was placed directly above the trace that was measured. The other was placed directly below the first thermocouple on the other layer to measure how well the heat spread between the layers. A DC supply was connected to the trace, with a multimeter in series to measure the applied current more precisely. Furthermore, a thermal camera was used to capture the temperature of the PCB.

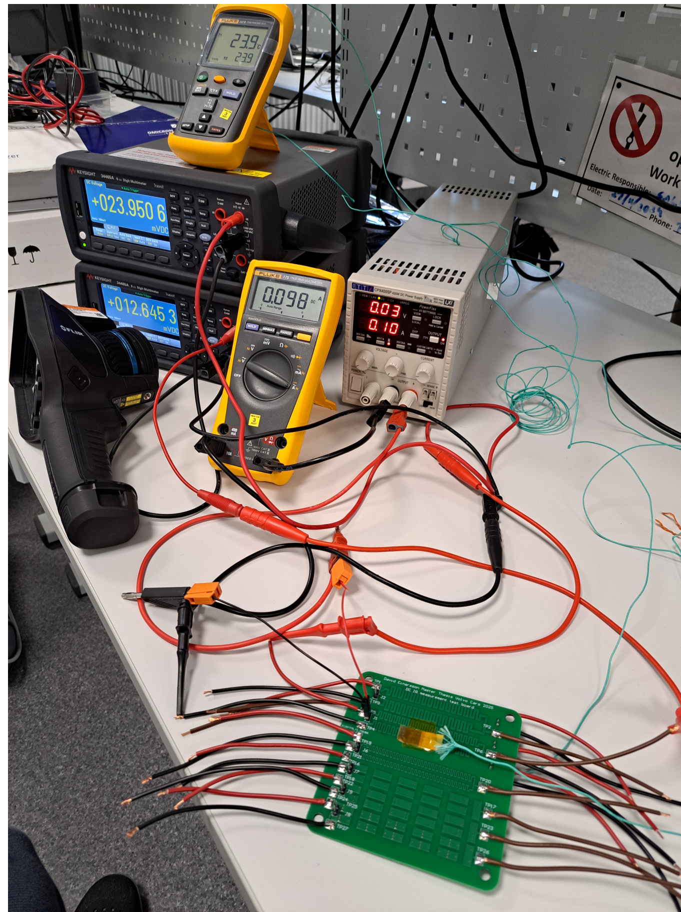


Figure 3.6: Overview of the hardware test setup for the DC IR PCB

A complete list of the measurement equipment used for the tests is presented in Table 3.7. A first test was done to establish a reference resistance, which would

Table 3.7: Equipment list for DC IR measurements

Equipment	Usage
Keysight 34465A 6.5 Digit Multimeter	Voltage drop
Fluke 52 II Dual Probe Digital Thermometer	Temperature
FLIR E96 Thermal Camera	Temperature
Aim-TTi CPX400SP DC Power Supply	DC power
Fluke 175 Digital Multimeter	Current measurement

allow the temperature increase to be calculated according to (2.6). The trace was loaded with 0.1 A, where both the temperature of the trace and the voltage drop were noted.

The current was then increased to 2 A, where the voltage drops and thermocouple temperatures were noted down every minute for 10 minutes. The final values were noted down for voltage and temperature, after five more minutes had passed and the temperature had stabilized. A thermal image of the PCB was captured using

the thermal camera, which had internal settings for finding the hottest spot on the PCB. Finally, the average trace temperature was calculated according to (2.6).

The test procedure was repeated for each trace, where only one trace was tested each time. Two other tests were also carried out on the PCBs. The variations between the produced test PCBs were tested with trace DC1. DC1 was loaded with 2 A for all five boards and the total voltage drop as well as the thermocouple temperatures were noted. DC7 and DC9 were loaded with 3 A for the main test PCB, to see if the vias would get significantly hotter. The same procedure was applied as for the 2 A test, where the voltage, temperatures and thermal image were collected after the temperature had stabilized.

3.3.2 PDN measurements

The Bode 500 from OMICRON Lab was used to measure the impedance of each PDN. An overview of the test setup is presented in Figure 3.7. The Bode 500

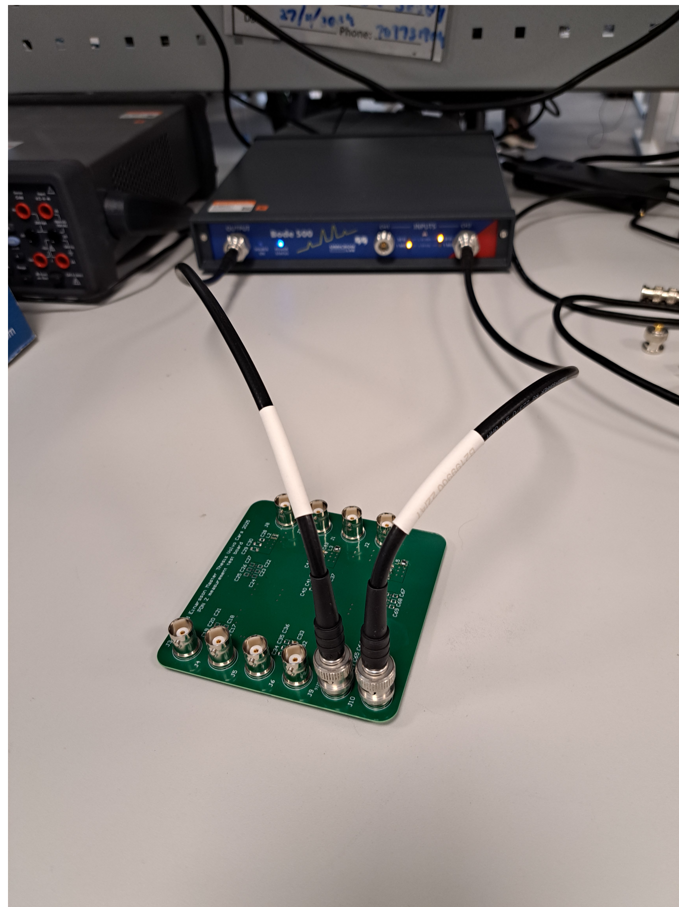


Figure 3.7: Overview of the hardware test setup for the PDN PCB

was calibrated before any measurements were taken to disregard losses in the cable and connection points. The instrument was connected to both ports of PDN1, in a so-called Shunt-Thru measurement setup, see Section 2.3.1. PDN1 had no components soldered on it, acting as an open circuit. This allowed the whole wave

to be transferred from port 1 to port 2. Any losses between the two ports are from the cables and connection points, which would allow the Bode 500 to subtract those losses from the measurements later on.

The impedance measurements of the PDNs began after the calibration was done. First, the impedance with no decoupling capacitors was measured for each PDN. Then, one of the four different decoupling configurations was soldered to the board and a new measurement was taken. The process was repeated by desoldering the soldered decoupling capacitors and soldering on a new configuration to take measurements with. The four different decoupling configurations were tested for each PDN.

3.3.3 SI measurement

The Bode 500 was also utilized for measurements of the SI PCB. A one-port measurement setup was used, compared to the Shunt-Thru setup used for the PDN PCB. The one-port setup only needs one cable connection between the Bode 500 and the PCB. Calibrations were also done before measurements on the PCB were taken. The cable was terminated with a short, open circuit and 50 Ω impedance, where calibrations were done for each termination to disregard the losses of the cable connection. Once the calibration was done, the average characteristic impedance of each trace could be determined, according to (2.17), by measuring the open circuit impedance and short circuit impedance.

The crosstalk of the PCB was also measured, where the LBE-1322 pulse generator from Leo Bodnar Electronics was used as the aggressor. The rise time of the LBE-1322 is 30 ps and the pulse voltage change was set to be 1.5 V, matching the simulation setup. The other end of the aggressor trace was terminated with either 50 or 75 Ω. The victim lines were analyzed using Keysight's DSO6054A oscilloscope.

The input impedance to the oscilloscope was set to be 50 Ω while the other end of the victim line was terminated with either 50 or 75 Ω. Which end of the victim line the oscilloscope was connected to was alternated during the test, allowing both near-end and far-end crosstalk to be measured.

4

DC IR

4.1 Simulation results

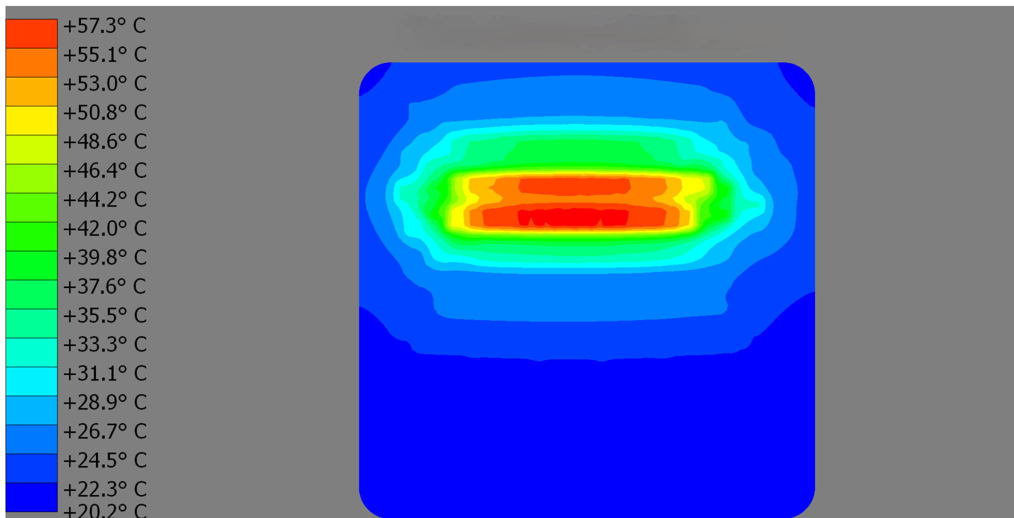
The test board was simulated and the voltage measurements as well as the temperature measurements were extracted. The results for DC1 are displayed in Figure 4.1, where temperature measurement is displayed in Figure 4.1a and voltage measurement in Figure 4.1b. As shown in Figure 4.1a, the temperature of the PCB is concentrated around the active trace and then gradually lowers as the distance from the trace increases. The voltage drop seen in Figure 4.1b drops evenly throughout the trace as expected.

The simulation results for the other nets follow the same trends as presented in Figure 4.1. The figures for the other nets are appended in Appendix A, while the data extracted from each figure is summarized in Table 4.1. As expected, DC2 has

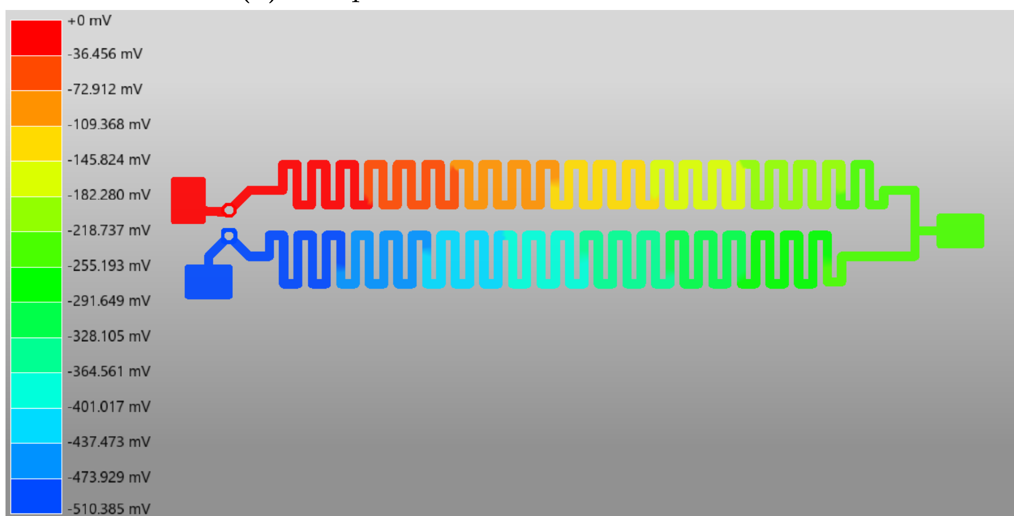
Table 4.1: Temperature and voltage simulations for the different nets

Net	Feature	Peak temp. [°C]	Voltage drop [mV]
DC1	Medium trace width	57	510
DC2	Large trace width	43	340
DC3	Small trace width	86	920
DC4	Medium trace width, less corners	53	450
DC5	Medium trace width, rounded corners	55	480
DC6	Small trace width, layer 2 heat sink	81	860
DC7	fill, single via	30	130
DC8	fill, single via, via obstruction	31	140
DC9	fill, double via	26	80

the lowest voltage drop and thus the lowest temperature. The opposite is true for DC3, which has the highest voltage drop and temperature.



(a) Temperature of DC1 loaded with 2A



(b) Voltage drop at 2A for DC1

Figure 4.1: Simulation results for DC1

The influence of corners seems to have a minimal impact on the overall trace performance, where the trend is reduced losses and resistance for smoother and fewer corners. However, the difference is minimal, which could be caused by other variations between the traces. A similar trend can be spotted for DC3 and DC6. The heat sink seems to lower the temperature by 5 °C, but there might be other factors that also impact the temperature difference.

The vias in DC7, DC8 and DC9 are the biggest contributors to the voltage drop of the nets. Assuming the via resistance is halved between DC7 and DC9, then the vias contribute with 100 mV of the total voltage drop for DC7, leaving only 30 mV for the rest of the trace. Introducing via obstruction in the fill for DC8 increases the fill resistance by roughly 25%, assuming a fill voltage drop of 30 mV in DC7.

The effect tolerances have on the trace width as well as copper thickness for DC1 is

presented in Table 4.2. The resistance, and thus the voltage drop following Ohm's

Table 4.2: Simulated tolerances effect on parameters for DC1

Feature	Avg	Worst	Best
Copper area [%]	100	56	156
Resistance at 20 °C [mΩ]	227	423	143
Peak temp. [°C]	57	86	42
Voltage drop [mV]	510	950	320

law, relates to the area of the trace according to (2.2). The temperature increase of the trace seems to have a linear dependency on the voltage drop, where an increase of 100 mV results in a temperature increase of about 7 °C.

The result from loading DC7 and DC9 with 3 A, to test the current capability of vias, is summarized in Table 4.3. SIwave suggests that the current limit for each

Table 4.3: DC7 and DC9 simulated with 3 A

Net	Peak temp. [°C]	Voltage drop [mV]
DC7	41	200
DC9	34	130

via is around 1.22 A, which both nets exceed with DC7 having 3 A in via current and DC9 having 1.5 A. The temperature peak is still low, indicating that the via current limit depends on the thermal properties of the nearby environment on the PCB instead of the current, as indicated by Section 2.2.4.

4.2 Hardware results

The result from the 0.1 A reference resistance test is summarized in Table 4.4. The

Table 4.4: Results from the 0.1 A measurement to determine reference resistance

Net	Current [mA]	Temp. [°C]	Voltage [mV]	Resistance [mΩ]
DC1	98	23.9	23.9	244
DC2	110	25.2	17.1	155
DC3	103	25.7	42.0	408
DC4	106	25.9	21.6	204
DC5	100	26.0	22.2	222
DC6	110	24.2	44.3	403
DC7	102	26.2	5.4	53
DC8	102	25.5	5.5	54
DC9	102	23.4	3.5	34

current varied between the traces, since the current tuning of the DC supply was not precise and was handled by turning a knob. The measured current was used in

the resistance calculation, so the current variation should have no greater effect on the results.

The reference temperature also varied between the traces, which stems from that the heat from the previous test was not fully dissipated before the measurement was done. However, time was given for the PCB to cool between tests, so the reference temperature spread is only a couple of degrees.

The thermocouple temperatures, as well as the thermal camera max temperature, are summarized for the different traces in Table 4.5. The measurements are taken from the 2 A tests for each trace. The initial comparison between simulated results

Table 4.5: Temperature measurements for the different nets at 2 A

Net	Couple top [°C]	Couple bottom [°C]	Camera peak [°C]
DC1	51.3	43.9	55.4
DC2	40.5	37.2	44.4
DC3	70.5	57.9	77.5
DC4	48.3	42.6	52.5
DC5	49.4	43.6	53.2
DC6	76.0	62.4	80.6
DC7	29.8	29.5	31.6
DC8	29.8	29.5	32.0
DC9	26.9	26.6	29.7

in Table 4.1 and the measured results in Table 4.5 looks promising. The max temperature in Table 4.1 is comparable to the max temperature picked up by the thermal camera. Excluding DC3 from the list would give an average deviation between the simulated and measured temperature of 1.5 °C. For DC4 and DC6 were the measured temperatures the same as the simulated, if the measurement is allowed to be rounded up to the closest integer.

Table 4.6 gives an overview of the comparison between the simulated and measured values. DC3 was the biggest outlier, with a difference of 8.5 °C. The result of

Table 4.6: Comparison between measured and simulated temperature values

Net	Simulated [°C]	Measured [°C]	Difference [°C]
DC1	57	55.4	1.6 (2.9 %)
DC2	43	44.4	-1.4 (3.2 %)
DC3	86	77.5	8.5 (11.0 %)
DC4	53	52.5	0.5 (1.0 %)
DC5	55	53.2	1.8 (3.4 %)
DC6	81	80.6	0.4 (0.5 %)
DC7	30	31.6	-1.6 (5.1 %)
DC8	31	32.0	-1.0 (3.1 %)
DC9	26	29.7	-3.7 (12.5 %)

DC3 is interesting, since DC6, which has the same width, was accurately predicted. One would also assume that the temperature of DC6 would be lower than DC3, considering the additional heat sink of DC6. However, the neighboring traces of DC3 might act as heat sinks, effectively spreading the heat over a wider area, which would allow the convection through air to be greater. It could also be a change of the airflow in the lab or tolerances in the production of the trace, which could be possible causes for the difference.

The voltage drop was also measured during the 2 A tests and the results, along with the calculated resistance and average temperature of each trace, are summarized in Table 4.7.

Table 4.7: Voltage measurements for the different nets, with trace resistance and temperature at 2 A

Net	Voltage [mV]	Resistance [mΩ]	Trace temp [°C]
DC1	537.1	267.2	47.7
DC2	339.5	168.9	47.6
DC3	954.5	477.3	68.2
DC4	439.8	219.9	45.4
DC5	482.5	241.3	47.7
DC6	1032.9	513.9	93.0
DC7	105.9	53.0	26.2
DC8	111.3	55.7	33.4
DC9	68.9	34.4	26.3

The average trace temperature (Table 4.7) is lower than the max value captured by the thermal camera (Table 4.5), except for traces DC2, DC6, and DC8. DC2 and DC8 average temperatures are a couple of degrees higher than the maximum captured by the thermal camera. For DC6, the difference is greater. The simulation and measurements (Table 4.6) give a maximum temperature of 81 °C, while the average trace temperature gives 93 °C. The estimated high average temperature stems from the high measured voltage drop of DC6. Excluding DC6 gives a good comparison of the simulated voltage drop (Table 4.1) versus the measured voltage drop.

The comparison between the simulated voltage (Table 4.1) and measured voltage (Table 4.7) is given in Table 4.8. The measured values are within 35 mV of the simulated values, excluding DC6. However, the biggest outlier in percentage is DC8. DC7, DC8, and DC9 all have low resistance, causing a small difference in absolute voltage drop to have a significant percentage difference.

DC1 was measured on each of the five produced test boards to evaluate the magnitude of the variation between the boards. The tests are summarized in Table 4.9. As expected, there is some variation between the boards. Most notable is the voltage, which varies by almost 80 mV from the lowest value to the highest value. Assuming an average voltage of 500 mV gives a variation of 8 %.

Table 4.8: Comparison between measured and simulated voltage drop

Net	Simulated [mV]	Measured [mV]	Difference [mV]
DC1	510	537.1	-27.1 (5.0 %)
DC2	340	339.5	0.5 (0.1 %)
DC3	920	954.5	-34.5 (3.6 %)
DC4	450	439.8	10.2 (2.3 %)
DC5	480	482.5	-2.5 (0.5 %)
DC6	860	1032.9	-172.9 (16.7 %)
DC7	130	105.9	24.1 (22.8 %)
DC8	140	111.3	28.7 (25.8 %)
DC9	80	68.9	11.1 (13.9 %)

Table 4.9: Measured effect of tolerances on DC1 at 2 A

Board	Couple top [°C]	Camera peak [°C]	Voltage [mV]
1	51.3	55.4	537.1
2	46.4	49.2	460.7
3	47.4	50.4	463.2
4	47.5	50.1	461.5
5	51.3	53.1	537.1

The temperature has a similar percentage variation but a bit lower in the range of 5 to 7 %. This indicates that the average tolerance might be captured from the 10 % range rather than the 30 % range used in Table 4.2. If the 10 % range is included for all the simulations, to account for margins in the manufacturing process and the material characteristic, would it allow for better predictions of the expected results.

Finally, DC7 and DC9 were loaded with 3 A to test if the vias would get significantly hotter than the rest of the trace. The results are summarized in Table 4.10. The

Table 4.10: DC7 and DC9 loaded with 3 A

Net	Peak temp. [°C]	Voltage drop [mV]
DC7	38.4	163.6
DC9	32.9	105.0

voltage drop increased almost linearly with the current, increasing by roughly 50 % compared to the 2 A test (Tables 4.5, 4.7). The temperature increased similarly, with no significant hotspots created by the vias. This would indicate that the via current limit, given by the simulation, does not need to be followed if it is connected to a sufficiently large trace to cool it.

The results suggest that layout designers could design with smaller vias to carry high DC current, thus saving important board space by not overpopulating the board with vias. In addition, the placement of vias in other signals' copper fills has minimal thermal effect, allowing the designer greater freedom in the placement of vias overall.

The result could be put into further context by comparing the current densities between the three different widths. Table 4.11 highlights important values for the three trace widths.

Table 4.11: Current densities, voltage drops and temperature increases for the three different trace widths

	Small trace	Medium trace	Large trace
Trace Width [mm]	0.5	0.9	1.3
Current density [A/mm^2]	114 (100%)	63.5 (56%)	44 (39%)
Temperature increase [°C]	57.5 (100%)	35.4 (62%)	24.4 (42%)
Voltage drop [mV]	954.5 (100%)	537.1 (56%)	339.5 (36%)

Table 4.11 highlights the observed linearity between current density and voltage drop as well as temperature increase. Showcasing that the voltage drop and temperature could be effectively controlled by changing the width of the trace. However, care should be taken when designing a complete PCB, since multiple traces and components emit losses, which could disrupt the observed linearity between trace width and temperature.

Volvo Cars uses 40 A/mm^2 as a max limit when designing traces, to keep the losses of traces minimal and the overall temperature of the PCB within limitations. The 40 A/mm^2 limit could potentially be increased if simulations are utilized, analyzing each case to decide if the trace could operate with higher current densities, thus allowing a more efficient design to be made.

5

PDNs

5.1 Simulation results

The impedance for the different PDNs with only the VRM model's components and no decoupling capacitors is presented in Figure 5.1. As expected, the impedance of

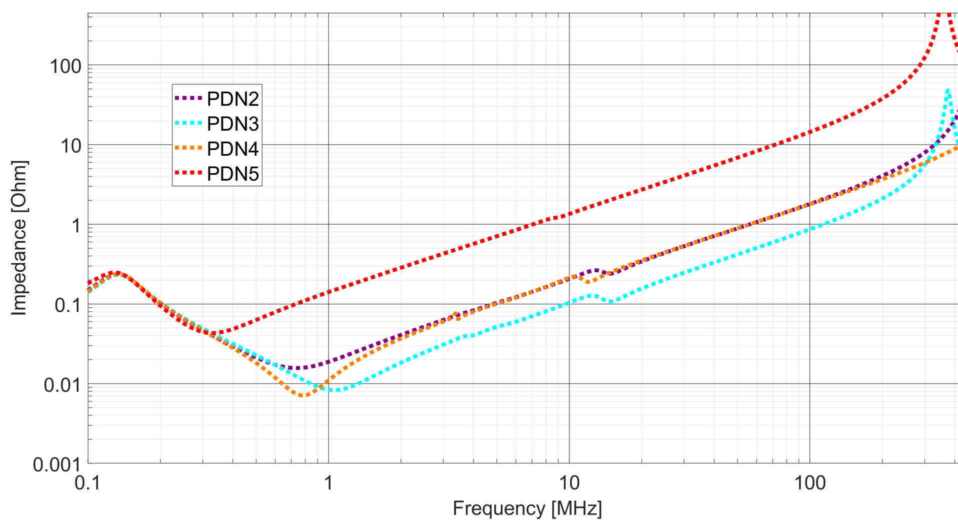


Figure 5.1: Simulated impedance for the different PDNs without decoupling capacitors

PDN5 is the highest among the PDNs, since it has the smallest width. The small width contributes to higher inductance, resulting in higher impedance at higher frequencies.

The opposite seems also true with PDN3, which has the largest width. However, the impedance of PDN4 is lower than PDN3 for frequencies around 0.8 MHz, which is a surprise. The effect might be explained by the difference in how the components for the VRM model are mounted for the different layers. PDN4 moves towards PDN2 after the dip at 0.8 MHz, which is reasonable considering they both have the same width.

PDN2 was simulated with the different decoupling capacitor configurations and

the results are presented in Figure 5.2. The 10 µF decoupling capacitors improve

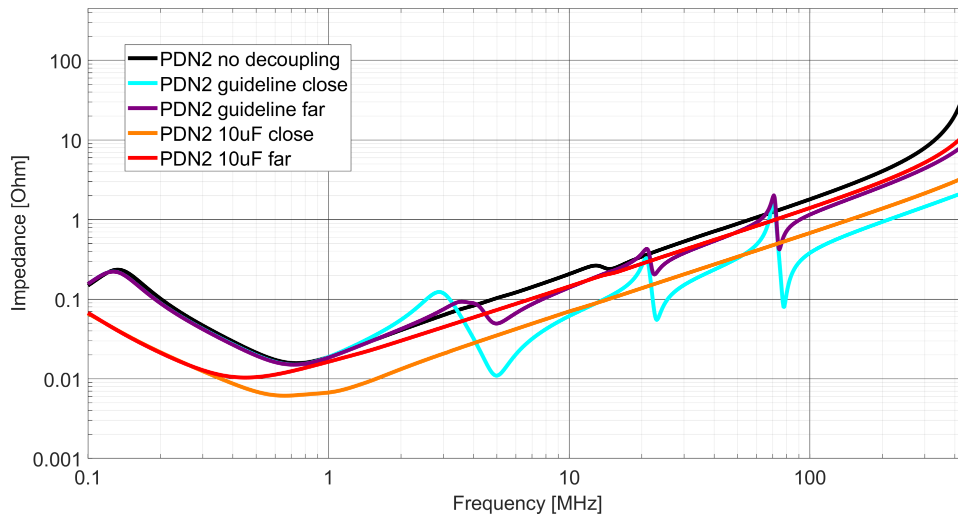


Figure 5.2: Simulated impedance for PDN2 with different decoupling capacitors

the impedance for lower frequencies significantly compared to both the guideline decoupling as well as no decoupling. The guideline decoupling starts to be effective around 4 MHz.

The main difference between the 10 µF and guideline selection of decoupling capacitors is that the 10 µF has a "smoother" impedance, while the guideline has both peaks and troughs. The far placement of decoupling capacitors provides a small improvement compared to no decoupling at higher frequencies.

Similarly, PDN3 was simulated with different decoupling capacitor configurations and the results are presented in Figure 5.3. The main difference between Figures 5.3 and 5.2, is that the impedance is lower in PDN3 and the difference between far placement and close placement of decoupling capacitors is smaller for PDN3 compared to PDN2. PDN3 has a bigger width, which lowers the inductance created from the additional length of placing the decoupling capacitors further away, thus lowering the difference.

PDN4 was also simulated with different decoupling capacitor configurations, with the result presented in Figure 5.4. An interesting observation is that the far 10 µF decoupling capacitor configuration is better compared to the close 10 µF decoupling capacitors around 0.8 MHz. This has not been the case in Figures 5.2 and 5.3.

Lastly, PDN5 was also simulated with different decoupling capacitor configurations. The results are presented in Figure 5.5. PDN5 has the biggest difference between the far and close placement of decoupling capacitors. Table 5.1 summarizes the impedance at 1 and 10 MHz for each PDN, with and without decoupling capacitors.

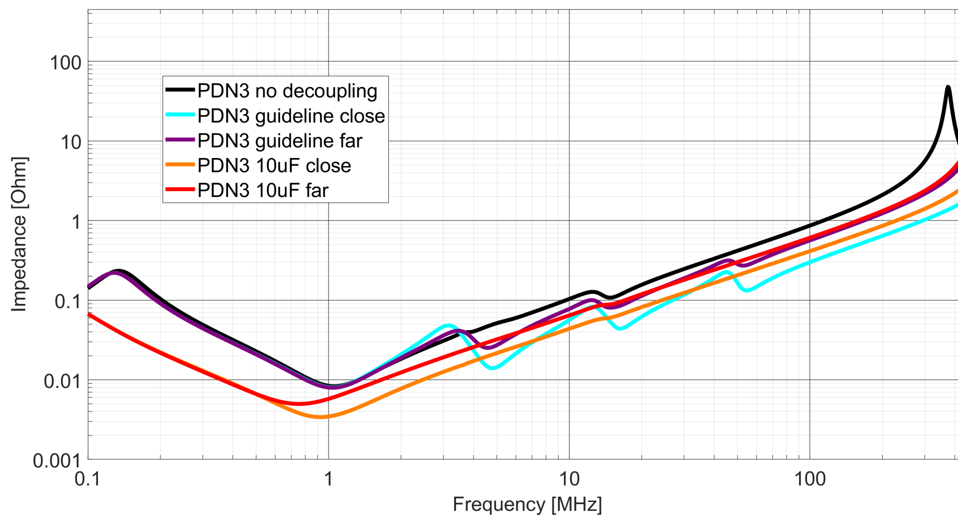


Figure 5.3: Simulated impedance for PDN3 with different decoupling capacitors

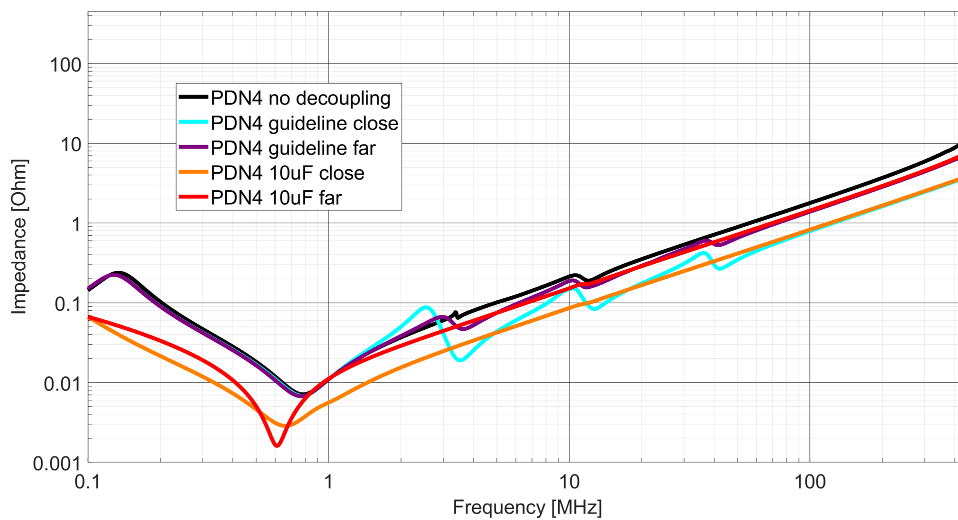


Figure 5.4: Simulated impedance for PDN4 with different decoupling capacitors

How much of the no decoupling impedance that is left after adding 10 µF decoupling capacitors is displayed in Table 5.2. A trend spotted in Table 5.2, is that the difference between far and close placement of decoupling capacitors is greatest for PDN5 and smallest for PDN3. This is expected, since PDN3 has the lowest inductance and PDN5 has the highest inductance. The increase in impedance comes from the inductance gained from the extra length between the close and far placement.

Furthermore, it could be noted that the connection of the capacitor to the PDN and ground net plays a role in determining the impedance. This is highlighted by comparing PDN2 to PDN4, since both have the same width. PDN2 is closer to ground and has more vias connecting the capacitors between the PDN and ground plane compared to PDN4. This reduces the impedance at 10 MHz by a few percent.

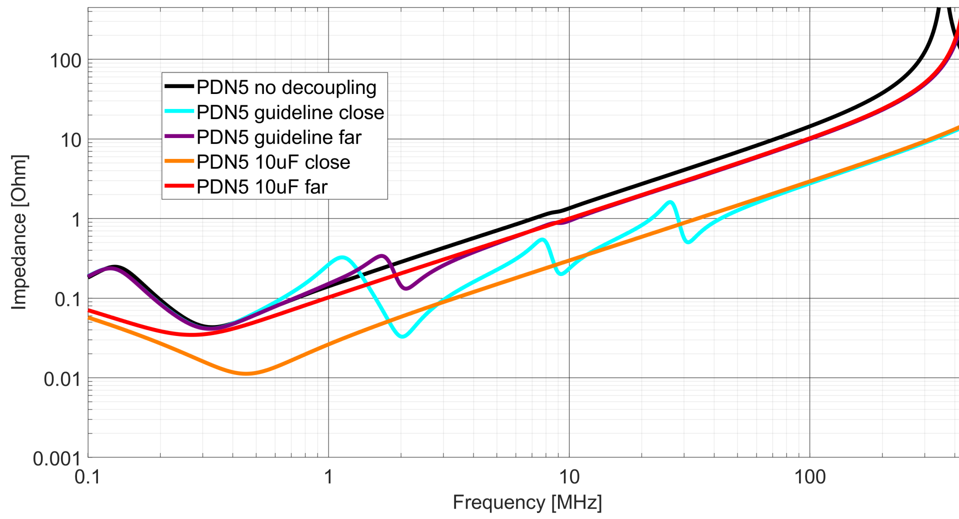


Figure 5.5: Simulated impedance for PDN5 with different decoupling capacitors

Table 5.1: Simulated impedance for the PDNs extracted from the figures

Parameter	PDN2	PDN3	PDN4	PDN5
Impedance at 1 MHz, no decoupling [mΩ]	18.8	8.4	11.0	141
Impedance at 1 MHz, 10 µF far [mΩ]	16.4	5.8	11.0	102
Impedance at 1 MHz, 10 µF close [mΩ]	6.7	3.5	5.6	26.3
Impedance at 10 MHz, no decoupling [mΩ]	207	104	214	1348
Impedance at 10 MHz, 10 µF far [mΩ]	145	64	152	1000
Impedance at 10 MHz, 10 µF close [mΩ]	70	44	86	298

Table 5.2: Improvement of adding decoupling compared to no decoupling

Parameter	PDN2	PDN3	PDN4	PDN5
Impedance left at 1 MHz, 10 µF far [%]	87	69	100	72
Impedance left at 1 MHz, 10 µF close [%]	36	42	51	19
Impedance left at 10 MHz, 10 µF far [%]	70	62	71	74
Impedance left at 10 MHz, 10 µF close [%]	34	42	40	22

5.2 Hardware results

The measured impedance for each PDN, as well as the simulated impedance, with only the soldered components that model the VRM is presented in Figure 5.6.

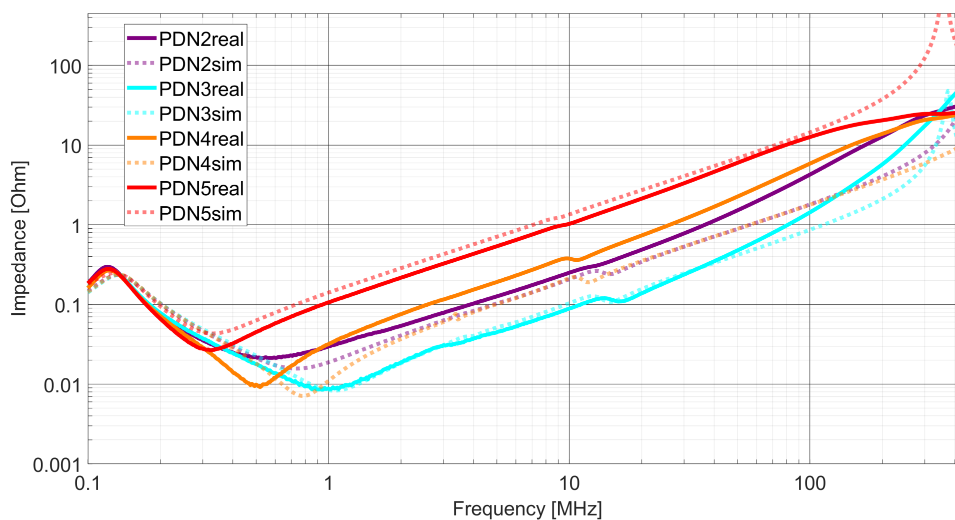


Figure 5.6: Measured and simulated impedance for the different PDNs without decoupling capacitors

The measured results generally match the simulated results. The main difference is the behavior after 100 MHz for each PDN, where the impedance starts to reach a common plateau instead of spiking as in the simulation.

PDN2 and PDN4 have higher impedance when measured compared to the simulated values. There is also a bigger difference in impedance between PDN2 and PDN4 compared to the simulation, where the measured values of PDN4 have higher impedance than PDN2 in the range of 1 to 100 MHz. Moreover, the impedance dips of PDN4 are shifted a bit in frequency, where they appear earlier when measured compared to when simulated.

The different decoupling configurations were measured for PDN2 and are presented in Figure 5.7 along with simulated values. The first difference between the simulated and measured result (Figure 5.7) is the resonance peaks of the guideline decoupling. The simulated results indicate that the peaks should be sharper with faster transitions and higher values, however they are much "smoother" in the measurement.

Another noticeable difference is that the close decoupling placement has lower impedance in the measurements compared to the simulation. This causes the gap between no decoupling and close decoupling to be wider in impedance.

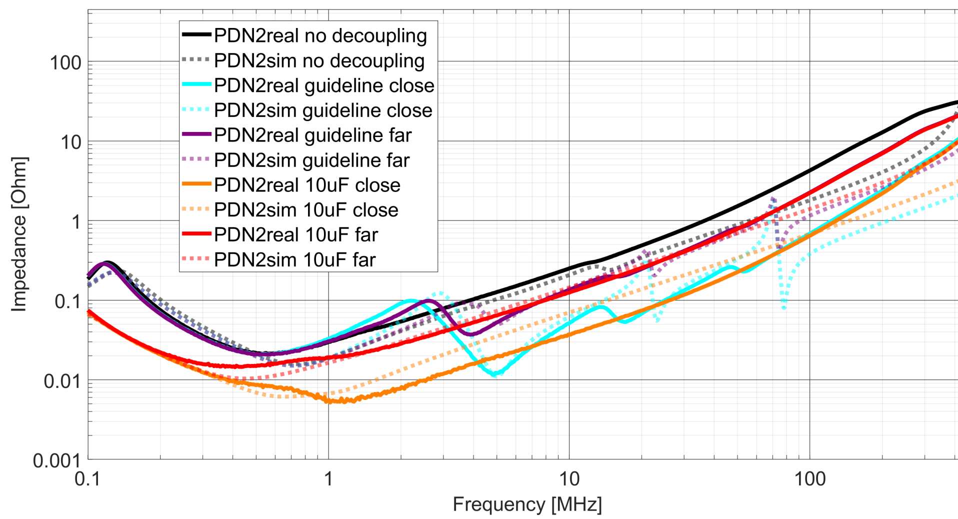


Figure 5.7: Measured and simulated impedance for PDN2 with different decoupling capacitors

PDN3 was also evaluated with different decoupling configurations and the result is presented in Figure 5.8. The simulation follows the measured result well, where the difference is that the decoupling configurations have less impedance in the measurements, especially the close placement. However, the simulated shape follows the measured shape, even though it is offset in impedance at some places.

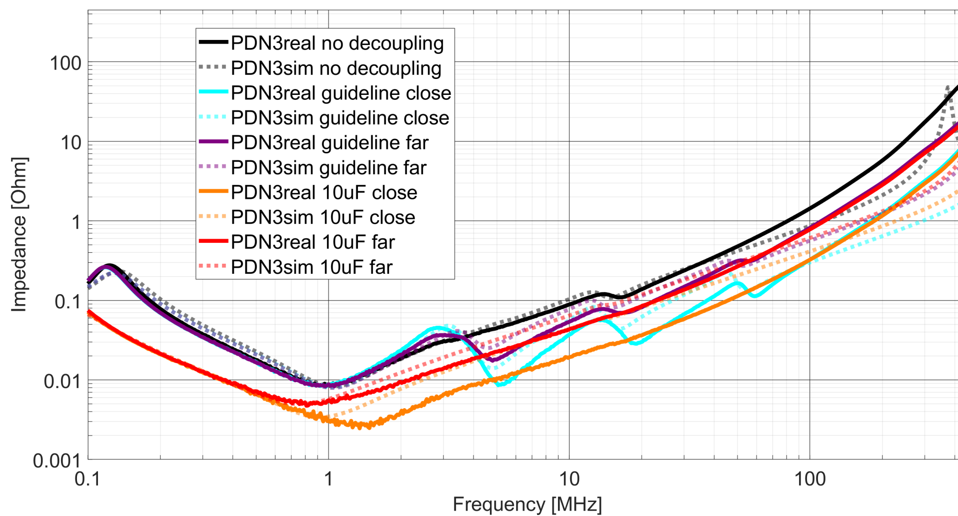


Figure 5.8: Measured and simulated impedance for PDN3 with different decoupling capacitors

The result for PDN4 with different decoupling configurations is presented in Figure 5.9. The 10 µF far configuration does not dip at 0.6 MHz compared to the simulation, instead the close 10 µF decoupling goes up. Here for PDN4, the resonance effect of

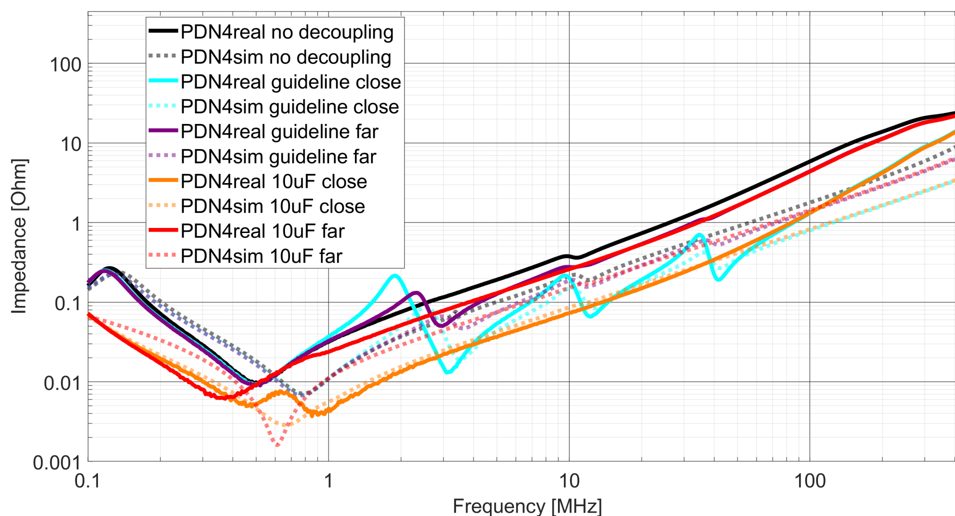


Figure 5.9: Measured and simulated impedance for PDN4 with different decoupling capacitors

the close decoupling is opposite to that of PDN2 (Figure 5.7), where the resonance is greater for the guideline decoupling when measured, compared to when simulated.

The main difference between the simulated and measured results is that both the far and no decoupling configurations have more impedance in the measurement. The measured impedance starts lower than the simulated, but the inductive characteristics start to dominate earlier in frequency when measured, causing the impedance to be above the simulated for the majority of the frequency span.

Lastly, the result for PDN5 with different decoupling configurations is presented in Figure 5.10. The main difference between the measured and simulated values is that most of the impedance values are slightly lower when measured. The impedance values for the different PDNs at 1 and 10 MHz, both with and without 10 µF decoupling, is summarized in Table 5.3. The values within the parentheses are the simulated, retrieved from Table 5.1.

There is some spread between the measured and simulated values. However, both the measured and simulated values follow the same trend with decoupling, lowering the impedance with the introduction of decoupling. In some cases, the simulated values are above the measured and in others the simulated values are below the measured.

Another interesting observation is that proper decoupling could improve the impedance of a narrower trace to be lower than the impedance of a wider trace. This would allow the design engineer to increase the interconnect density by utilizing narrower traces, while still keeping the impedance low with properly designed decoupling.

Low impedance is important in ensuring power is delivered to the IC, so that the IC signals can be kept at a high voltage level when needed. If the IC needs to send

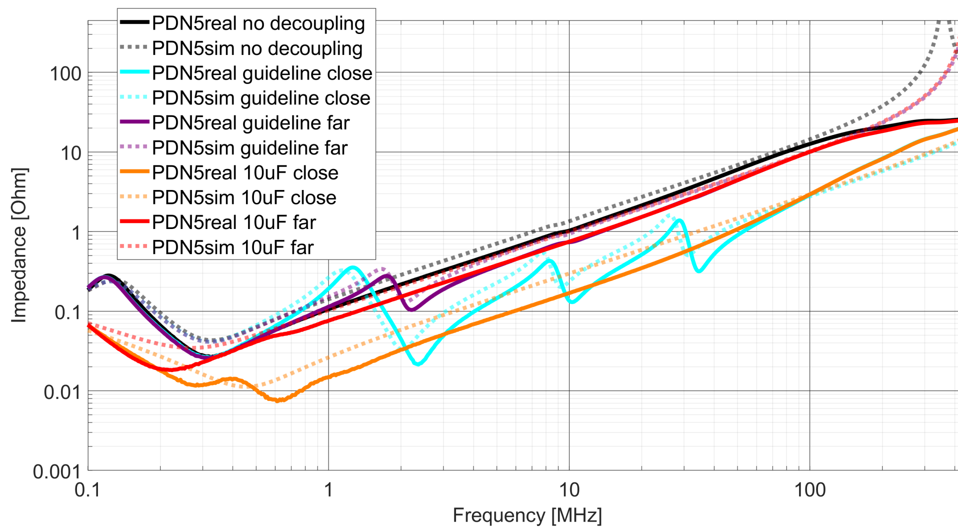


Figure 5.10: Measured and simulated impedance for PDN5 with different decoupling capacitors

Table 5.3: Measured values compared to (simulated values) for the PDNs

Parameter	PDN2	PDN3	PDN4	PDN5
Impedance at 1 MHz, no decoupling [mΩ]	30.5 (18.8)	8.8 (8.4)	32.7 (11.0)	106 (141)
Impedance at 1 MHz, 10 µF far [mΩ]	19.2 (16.4)	5.6 (5.8)	23.8 (11.0)	76.3 (102)
Impedance at 1 MHz, 10 µF close [mΩ]	5.6 (6.7)	3.1 (3.5)	4.6 (5.6)	14.9 (26.3)
Impedance at 10 MHz, no decoupling [mΩ]	251 (207)	89 (104)	376 (214)	1031 (1348)
Impedance at 10 MHz, 10 µF far [mΩ]	125 (145)	43.5 (64)	261 (152)	750 (1000)
Impedance at 10 MHz, 10 µF close [mΩ]	37.0 (70)	19.5 (44)	73.3 (86)	170 (298)

a square wave with a fundamental frequency of 1 MHz, then the voltage drop at the IC is determined primarily by the impedance at 1 MHz. The impedance can be directly translated to voltage drop, utilizing the current drawn. If the current drawn is 1 A, the voltage drop for PDN5 (Table 5.3) will be 106 mV with no decoupling or 14.9 mV with close decoupling, a 86% decrease. Highlighting the potential of proper decoupling.

The square wave also consists of multiple frequencies above the harmonic frequency, which in turn will impact the voltage drop by the impedance at their frequency. This makes the impedance at frequencies above the fundamental frequency important to analyze and keep low. That is why the peaks, caused by resonance between capacitors, are detrimental to the performance. If a harmonic of the fundamental

frequency exists at the peak, the voltage drop at the specific harmonic could cause the signal to be too low to be interpreted correctly at the receiver of the IC signal.

Comparing PDN2 with PDN4 (Table 5.3), which has the same width, highlights the importance of layer placement and connection with vias of the capacitor to the ground plane. PDN2 is placed closer to the ground plane and the capacitors have more vias connecting them compared to PDN4. This allows the impedance for PDN2 to be lower than PDN4 at 10 MHz.

The relationship between the measured and simulated values is further highlighted in Table 5.4. The percentage values are derived from dividing the simulated values by the measured values. A trend that can be spotted from Table 5.4 is that the

Table 5.4: Simulated impedance as a percentage of the measured impedance

Parameter	PDN2	PDN3	PDN4	PDN5
Impedance at 1 MHz, no decoupling [mΩ]	62%	95%	34%	133%
Impedance at 1 MHz, 10 µF far [mΩ]	85%	104%	46%	134%
Impedance at 1 MHz, 10 µF close [mΩ]	120%	113%	122%	177%
Impedance at 10 MHz, no decoupling [mΩ]	82%	117%	57%	131%
Impedance at 10 MHz, 10 µF far [mΩ]	116%	147%	58%	133%
Impedance at 10 MHz, 10 µF close [mΩ]	189%	226%	117%	175%

impedances of the close placement of 10 µF capacitors are overestimated by the simulation in all cases. However, the close 10 µF configuration has the least amount of deviation between the measured and simulated values for PDN4. This stems from that the simulated no decoupling impedance of PDN4 is low compared to the measured, thus the overestimation of the close decoupling boosts the impedance closer to the measured value.

The no decoupling impedance is best predicted by the simulation for PDN3, which has the biggest width. PDNs are commonly designed as planes, which could hint that the simulation tool is better at simulating wider traces and planes to determine the impedance.

Overall, the simulation shows promise in predicting the impedance of PDNs. The shape of the simulated options tends to follow the measurements, which allows the design engineer to compare decoupling alternatives as well as trace widths without the need to order a prototype. The simulations could help to ensure that the final product is within the target impedance if a proper margin is applied to the simulated values.

6

SI

6.1 Simulation results

The frequency sweep was done for each trace, where both the short and open circuit impedance were simulated. The combined results, using (2.17) to calculate the average characteristic impedance, are presented in Figures 6.1 and 6.2. Figure 6.1 presents the impedance for the microstrip traces.

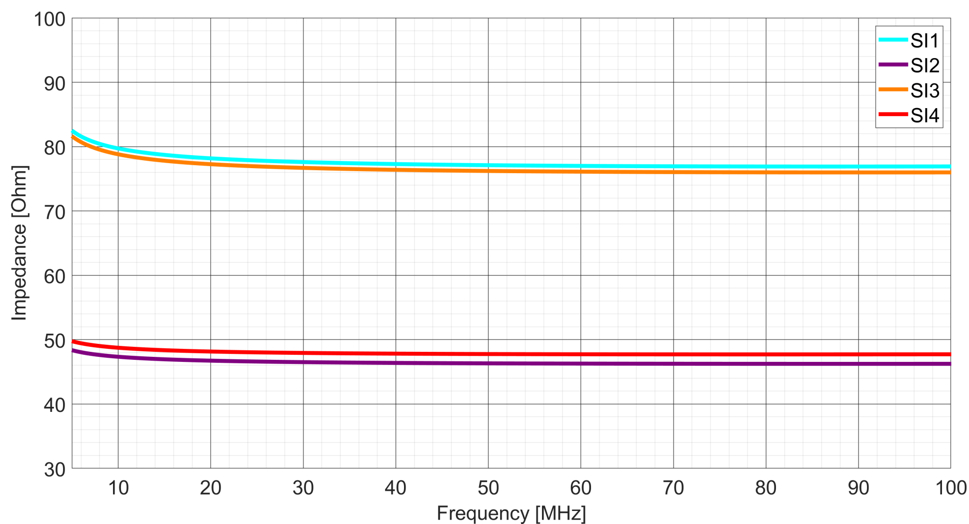


Figure 6.1: Simulated average characteristic impedance for microstrip traces

The characteristic impedances of the microstrip traces are quite stable in the region of 5 to 100 MHz, where the impedance slowly declines as the frequency is increased. How well the simulated values compare to the designed reference values, given by Table 3.5, is summarized in Table 6.1.

Noticeable is that the impedance at 5 MHz is closer to the reference than the impedance at 50 MHz. Which could be explained by the frequency SIwave uses to calculate the characteristic impedance. The characteristic impedance is usually described as a constant, independent of frequency. However, the impedance is affected by the parasitics of the circuit and the frequency dependency of the board

Table 6.1: Simulated microstrip impedance at 5 and 50 MHz

Net	SI1	SI2	SI3	SI4
Impedance at 5 MHz [Ω]	82.5	48.4	81.6	49.8
Impedance at 50 MHz [Ω]	77.1	46.3	76.2	47.8
Reference impedance [Ω]	84	50	84	50

material used. If SIwave calculated the characteristic impedance at a value closer to 5 MHz, would it explain why the reference value is closer to the measured at 5 MHz.

The reduction in impedance from 5 to 50 MHz seems to be the same for traces with the same width, which is plausible since the parasitics of the traces depend on their shape and position. Furthermore, SI2 and SI3 are both placed close to the ground trace, which seems to lower the impedance by increasing the capacitance to ground. SI4 is closest to the reference impedance, which could be explained by the fact that it is placed further away from any neighboring trace, including the ground trace.

The average characteristic impedances for the stripline traces are displayed in Figure 6.2. The decline in impedance of the stripline traces is more noticeable in the 5 MHz

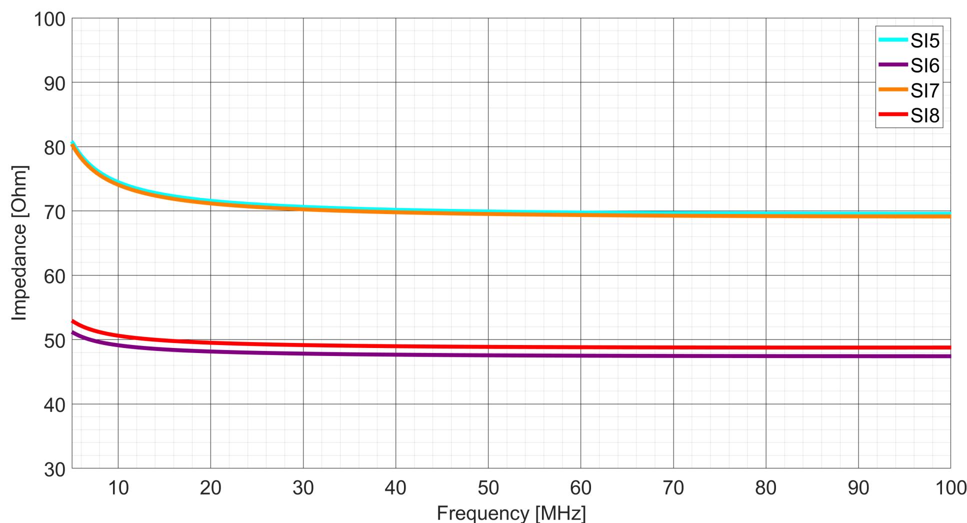


Figure 6.2: Simulated average characteristic impedance for stripline traces

region compared to the microstrip traces, see Figure 6.1. Otherwise, the shape of Figure 6.2 is comparable to Figure 6.1.

The impedance values for the stripline traces at 5 and 50 MHz, as well as the reference (Table 3.5), are summarized in Table 6.2. The stripline impedances are above the reference values at 5 MHz. However, the impedance drops as the frequency increases, eventually passing the reference values and dipping below them, resulting in a lower impedance than the reference at 50 MHz. The same trends identified in Table 6.1 are applicable here, where the group of the same trace width lowers equally in impedance from 5 to 50 MHz. SI6 and SI7, comparable to SI2 and SI3, both have

Table 6.2: Simulated stripline impedance at 5 and 50 MHz

Net	SI5	SI6	SI7	SI8
Impedance at 5 MHz [Ω]	80.8	51.2	80.3	52.9
Impedance at 50 MHz [Ω]	69.9	47.6	69.5	48.9
Reference impedance [Ω]	74	50	74	50

lower impedance, which the vicinity of the ground trace could cause. Finally, SI8, which is comparable to SI4, has the closest impedance to the reference impedance at 50 MHz.

The crosstalk between traces on the same layer was also simulated. The termination of the aggressor and victim alternated between 50 and 75 Ω. An overview of the crosstalk between the microstrip traces is displayed in Table 6.3. The results in the

Table 6.3: Simulated microstrip crosstalk with different terminations

Aggressor Victim	50/50 [Ω]	50/75 [Ω]	75/75 [Ω]	75/50 [Ω]
Near-end [mV]				
SI1 SI2	103	125	125	103
SI2 SI1	102	130	130	102
SI2 SI3	5	6	6	5
SI3 SI2	5	6	6	5
SI3 SI4	8.5	10	10	8.5
SI4 SI3	8.5	11	11	8.5
Far-end [mV]				
SI1 SI2	73	89	89	73
SI2 SI1	74	93	93	74
SI2 SI3	9	11	11	9
SI3 SI2	9	11	11	9
SI3 SI4	23	29	29	23
SI4 SI3	26	33	33	26

second row are from when both the aggressor and victim traces were terminated with 50 Ω, indicated by 50/50. In the third row, the termination of the victim trace increased to 75 Ω, indicated by 50/75.

An interesting result is that the simulated crosstalk does not change when the aggressor termination changes. This could be caused by a limitation within the program or in the implementation of the circuit within the program.

However, the crosstalk changes with different victim terminations. Increasing the termination to 75 Ω increases the crosstalk in all cases. A possible cause for the increased crosstalk is that the current might be similar for the different terminations, causing a higher ohm termination to lead to a bigger voltage drop, thus causing the crosstalk to increase.

A first assumption would be that the crosstalk would get lowered if the traces' characteristic impedance is better matched to the termination. For instance, SI1 has a reference impedance of 84 Ω, and if it was terminated with 75 Ω, one would believe that the reflection would decrease at the end, thanks to the better impedance matching, thus lowering the crosstalk voltage. But that does not seem to be the case, indicated by the simulation results.

SI1 and SI2 suffer from the greatest crosstalk, which is plausible since the traces are close to each other. Another observation is that the guard trace seems to lower the crosstalk. SI3 is placed between SI2 and SI4, where the distance between the traces is equal. However, a guard trace has been added between SI2 and SI3, which lowers the crosstalk.

The stripline crosstalk was also simulated and is summarized in Table 6.4. Table 6.4

Table 6.4: Simulated stripline crosstalk with different terminations

Aggressor Victim	50/50 [Ω]	50/75 [Ω]	75/75 [Ω]	75/50 [Ω]
Near-end [mV]				
SI5 SI6	83	100	100	83
SI6 SI5	84	105	105	84
SI6 SI7	4	4.5	4.5	4
SI7 SI6	4	4.5	4.5	4
SI7 SI8	8	9.5	9.5	8
SI8 SI7	8	10	10	8
Far-end [mV]				
SI5 SI6	29	31	31	29
SI6 SI5	29	29	29	29
SI6 SI7	1	1	1	1
SI7 SI6	1	1.5	1.5	1
SI7 SI8	2	1.5	1.5	2
SI8 SI7	2.5	1.5	1.5	2.5

follows the same structure as Table 6.3. The main difference between the crosstalk tables is that the far-end crosstalk for the striplines traces is significantly lower compared to the microstrip traces. Otherwise, Table 6.4 follows mostly the same trends discussed for Table 6.3. One small deviation is that the crosstalk is lowered for the last far-end values when changing victim termination to 75 Ω. The difference is only 0.5 to 1 mV, which is low.

6.2 Hardware results

The average characteristic impedance of the traces was measured and the result for the microstrip traces, along with the simulated values, is displayed in Figure 6.3. The main difference between the measured and simulated values is the impedance levels. The impedance values obtained from measurements are lowered by approximately 20% compared to the simulated values. Another difference between measured

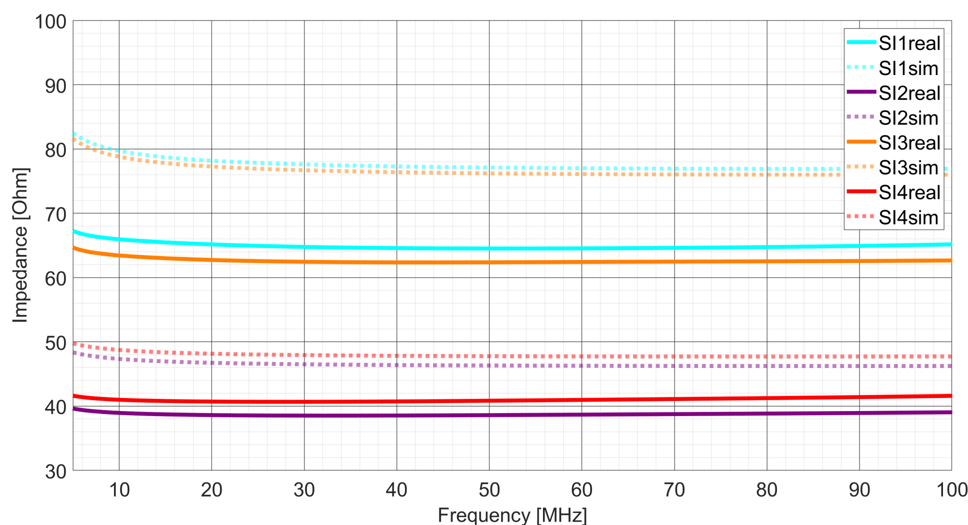


Figure 6.3: Measured and simulated average characteristic impedance for microstrip traces

and simulated values is that the difference in impedance for traces with the same width is greater, which could be caused by the vicinity of the ground trace, increasing the capacitance to ground further on the produced board than what the simulation estimated. Overall, the capacitive coupling seems to be underestimated in the simulation, causing the increased capacitance to lower the impedance when measured.

Table 6.5 highlights the important values from the measured and simulated values. The simulated values are placed within parentheses, below the measured values. What differs between the simulated and measured values, visualized by Table 6.5, is

Table 6.5: Measured and (simulated) microstrip impedance at 5 and 50 MHz

Net	SI1	SI2	SI3	SI4
Impedance at 5 MHz [Ω]	67.2 (82.5)	39.6 (48.4)	64.6 (81.6)	41.6 (49.8)
Impedance at 50 MHz [Ω]	64.5 (77.1)	38.6 (46.3)	62.4 (76.2)	40.8 (47.8)
Reference impedance [Ω]	84	50	84	50

that the frequency stability of the impedance is greater when measured. The drop in impedance from 5 to 50 MHz is roughly halved from the measured values compared to the simulated (Table 6.1).

The average characteristic impedance for the stripline traces was also measured and the result, along with the simulated values, is displayed in Figure 6.4. The measured stripline values are more closely aligned with the simulated values, compared to those of the microstrip. The decrease in impedance from the simulated to the measured values is roughly 10%, compared to the 20% for microstrip traces. This indicates

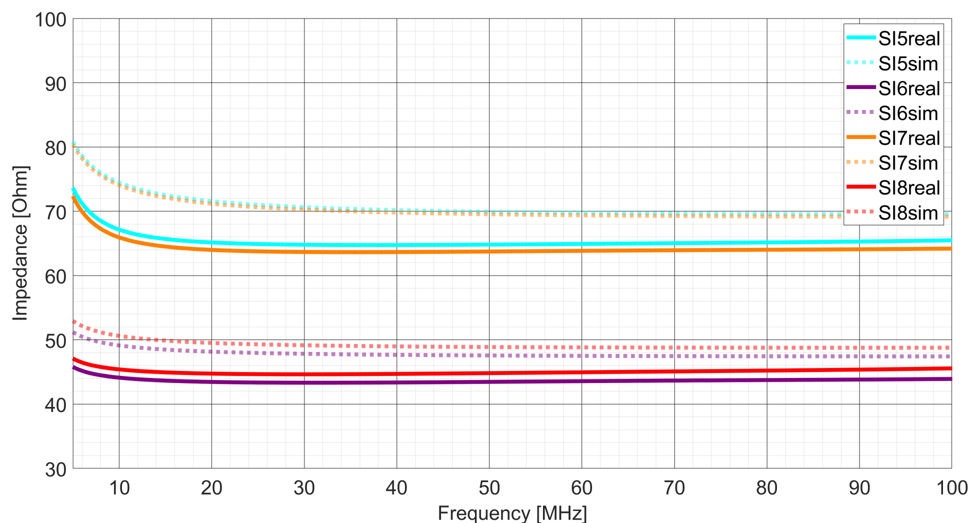


Figure 6.4: Measured and simulated average characteristic impedance for stripline traces

that the capacitive coupling is better estimated by the simulation for striplines compared to microstrip. A possible theory for the deviation is that the interface between copper, solder mask and air, for microstrip, is not properly defined within the simulation, causing the capacitive parasitic to be wrongly estimated.

Table 6.6 presents the measured and simulated stripline impedance values at 5 and 50 MHz. Two conclusions could be drawn comparing the striplines (Table 6.6) to

Table 6.6: Measured and simulated stripline impedance at 5 and 50 MHz

Net	SI5	SI6	SI7	SI8
Impedance at 5 MHz [Ω]	73.4 (80.8)	45.7 (51.2)	72.1 (80.3)	47.0 (52.9)
Impedance at 50 MHz [Ω]	64.8 (69.9)	43.5 (47.6)	63.7 (69.5)	44.8 (48.9)
Reference impedance [Ω]	74	50	74	50

those of the microstrips (Table 6.5). First, is that the stripline values match more closely those of the reference values and thus also the simulated values. Secondly, is that the impedance value for the 0.1 mm wide traces almost has the same impedance at 50 MHz, regardless of whether it is a microstrip or stripline. If it is a coincidence that the impedance value aligns for the 0.1 mm wide traces, or if the difference between microstrip and stripline configurations diminishes at 50 MHz, needs to be further studied.

The measured crosstalk, along with the simulated within the parentheses, for the microstrip traces are presented in Table 6.7. The measured near-end crosstalk roughly follows the simulated near-end crosstalk. The simulated crosstalk for a 75 Ω victim trace termination matches the measured near-end crosstalk closely. A possible

Table 6.7: Measured and (simulated) microstrip crosstalk with different terminations

Aggressor Victim	50/50 [Ω]	50/75 [Ω]	75/75 [Ω]	75/50 [Ω]
Near-end [mV]				
SI1 SI2	117 (103)	131 (125)	129 (125)	129 (103)
SI2 SI1	131 (102)	133 (130)	131 (130)	131 (102)
SI2 SI3	6.5 (5)	6.5 (6)	6.5 (6)	6.5 (5)
SI3 SI2	6.5 (5)	6.5 (6)	6.5 (6)	6.5 (5)
SI3 SI4	10 (8.5)	10 (10)	10 (10)	10 (8.5)
SI4 SI3	10 (8.5)	10 (11)	11 (11)	10 (8.5)
Far-end [mV]				
SI1 SI2	26 (73)	34 (89)	44 (89)	36 (73)
SI2 SI1	19 (74)	32 (93)	53 (93)	38 (74)
SI2 SI3	6 (9)	6 (11)	5 (11)	5 (9)
SI3 SI2	5 (9)	6 (11)	5 (11)	5 (9)
SI3 SI4	10 (23)	9 (29)	9 (29)	9 (23)
SI4 SI3	10 (26)	10 (33)	10 (33)	10 (26)

cause why the 75 Ω termination simulation better matches all the measured near-end crosstalk is that the capacitive coupling was underestimated in the simulation, as discussed above. This effect is counteracted by the increase caused by the 75 Ω termination, which levels the crosstalk to match the measured.

However, an interesting observation from the measured near-end crosstalk is that it is quite independent of both aggressor and victim trace termination. The observation could be explained by that the near-end crosstalk is not dependent on coupled length, which would indicate that it is not affected by how the rest of the trace looks, including the termination. If the following argument is valid, the simulation variation between the different terminations becomes more peculiar.

The far-end crosstalk has a greater discrepancy between measured and simulated values. The simulated values are generally twice or three times the value of the measured value. The difference could be caused by limitations with the measurement setup.

The oscilloscope's sample rate was slow in comparison to the rise time of the pulse generator. The oscilloscope had a sampling rate of 4 Gsamples/s, resulting in 250 ps between each sample. This could affect the measured result in that the peak of the crosstalk was between the captured samples, making the measured crosstalk appear lower than the actual value.

The shape of the pulse was captured by the oscilloscope and is showcased in Figure 6.5. The pulse has a specified rise time of 30 ps, which is much faster than the measured rise time of roughly 600 ps. The increased rise time could be an effect of the slower sample rate, but might also be affected by the parasitic effects of the cable and oscilloscope, which would delay the signal.

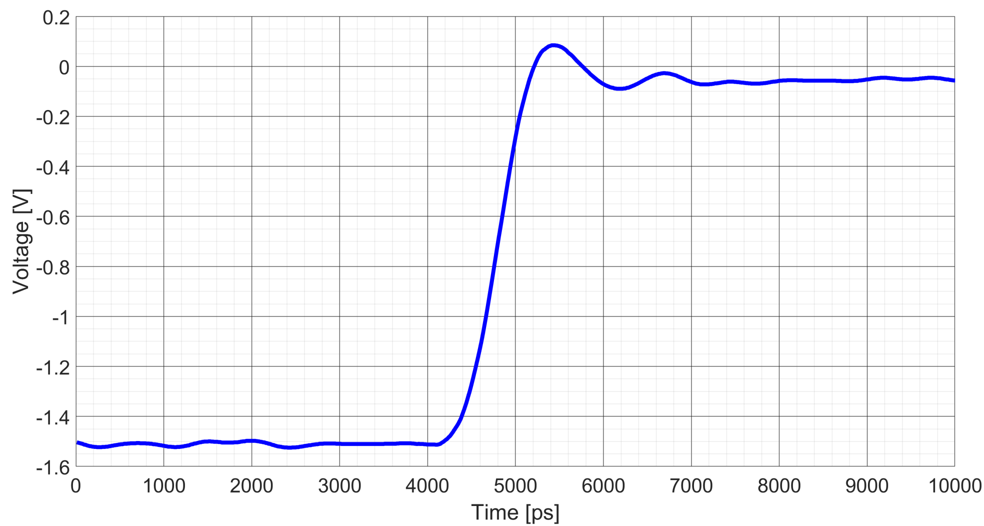


Figure 6.5: Measured pulse waveform using the oscilloscope

The far-end crosstalk between SI1 and SI2 has greater variation between the different trace termination combinations. The observed trend is that the crosstalk increases as the termination changes from 50 Ω to 75 Ω, both for aggressor and victim, and is not dependent on matching the trace impedance to the termination, as initially thought.

Another drawback with the measurement setup was that a pulse was sent, which was allowed to settle before the next pulse was sent. The oscillations, caused by the impedance mismatch, might have had a greater impact on the crosstalk if the frequency of the pulse generator were to be increased.

Lastly, the measured crosstalk, along with the simulated within parentheses, for the striplines is presented in Table 6.8. The measured near-end crosstalk follows closely the simulated and does not change significantly in the measured voltage as the termination is changed, following the same trend as for Table 6.7.

The major difference in the near-end crosstalk between microstrip (Table 6.7) and stripline (Table 6.8), is that the simulated 50 Ω termination is a better prediction for "low" crosstalk voltages in striplines compared to microstrip, where the 75 Ω termination better matched the simulated values. However, the 75 Ω termination simulation is best in predicting the measured voltage for the "high" crosstalk voltages in both cases.

The far-end crosstalk has a similar discrepancy for "high" crosstalk, as noted for microstrip (Table 6.7), where the simulated value is twice the measured. However, the simulated value is lower and sometimes half the measured value for "low" crosstalk, opposite to that of the "high" crosstalk situation, see Table 6.8.

An interesting observation is that the crosstalk of SI6 SI5 is constant with different terminations, which the simulation accurately predicted would happen, even though

Table 6.8: Measured and (simulated) stripline crosstalk with different terminations

Aggressor Victim	50/50 [Ω]	50/75 [Ω]	75/75 [Ω]	75/50 [Ω]
Near-end [mV]				
SI5 SI6	90 (83)	97 (100)	98 (100)	99 (83)
SI6 SI5	100 (84)	100 (105)	100 (105)	98 (84)
SI6 SI7	3 (4)	3 (4.5)	3 (4.5)	3 (4)
SI7 SI6	3 (4)	3.5 (4.5)	3 (4.5)	3 (4)
SI7 SI8	7 (8)	7 (9.5)	7 (9.5)	7 (8)
SI8 SI7	7 (8)	7.5 (10)	7 (10)	7 (8)
Far-end [mV]				
SI5 SI6	14 (29)	22(31)	27 (31)	11 (29)
SI6 SI5	15 (29)	15 (29)	15 (29)	15 (29)
SI6 SI7	2.5 (1)	2.5 (1)	2.5 (1)	2.5 (1)
SI7 SI6	2 (1)	2 (1.5)	2 (1.5)	2 (1)
SI7 SI8	2 (2)	2 (1.5)	2.5 (1.5)	2 (2)
SI8 SI7	2 (2.5)	2.5 (1.5)	2.5 (1.5)	2 (2.5)

the simulated value is off.

Finally, comparing microstrip (Table 6.7) to stripline (Table 6.8), there is one major difference and that is that stripline has lower crosstalk. The difference is most prominent for the far-end crosstalk, where the striplines' crosstalk is generally half or less of the microstrip's crosstalk. Furthermore, the simulated values align quite well with the near-end crosstalk values for both microstrip and stripline. However, the far-end crosstalk differs, where the striplines are a much better fit to the simulated values than the microstrip.

The advantage of designing striplines over microstrip is that the far-end crosstalk is reduced and the simulations agree better with the measured result. However, microstrip needs fewer resources from a layout perspective, requiring only one ground plane, which would allow for more efficient design. Furthermore, the simulation of microstrip could potentially be improved by better understanding and describing the interface from copper to solder mask to air.

In the end, both microstrip and stripline configurations might be needed to design the optimal board. In each case, simulations could be used to get an overview of the potential crosstalk and reduce it early, by separating the lines further or introducing ground traces. The reduced impedance gained from the introduction of a ground trace could be counteracted by adjusting the width to get a characteristic impedance that matches the circuit.

7

Conclusion

7.1 Results from present work

The DC IR simulations show promising results in capturing the performance of manufactured PCBs. Including the tolerances of the produced PCB in the simulations improves the results, resulting in a majority of the traces being very similar to the simulated values. Furthermore, the DC IR measurements support the idea that heat effectively travels between the layers and that vias could handle higher currents if they are connected to sufficiently large copper areas. Lastly, the temperature of each trace could be effectively managed by varying the trace width and controlling the current density.

The impedance simulations, both for PDN and SI, gave a good understanding of the characteristics of the different options. The shape of the simulations shows good agreement with the measurements, allowing the designer to evaluate the significant differences between the available options. However, the exact values of the measurements are harder to match for the simulation, particularly for the PDNs, where the simulated value could be half or double that of the measured value.

Improving the decoupling strategy by increasing the capacitance of the given package to its maximum value gives two benefits compared to the older guideline. The impedance at low frequencies is improved, thanks to the added capacitance. Furthermore, the high-frequency performance is improved by removing the resonance created by the different valued capacitors, thus removing the peaks of impedance at higher frequencies. Implementing optimized decoupling could reduce the impedance for narrower traces to be lower than wider traces, giving the design engineer greater margins by utilizing narrower traces.

Far placement of decoupling capacitors could be a viable option if the board space is constrained around the IC. The far placement is best in situations where the PDN has a high width, thus lowering the gain in inductance from placing it further away.

Stripline shows better performance than that of the microstrip. The simulated and reference values of the trace impedance are both closer to the measured value of the striplines compared to the microstrips. Furthermore, the crosstalk is lower for the striplines compared to the microstrip, where the simulated values are also in greater

agreement with the measured values for the stripline.

The far-end crosstalk had great deviation between the measured and simulated values for both microstrip and striplines. The resulting difference could be caused by limitations with the measurement equipment, as it was not fast enough to detect the true peak of the crosstalk.

The simulation also had limitations in including the effect that different trace terminations had on crosstalk. Only victim termination affected the result of the crosstalk in the simulations, while both the victim and aggressor terminations had an impact on the measured result. The near-end crosstalk appeared independent of the different terminations, while the far-end crosstalk changed more with different terminations.

To conclude, layout plays a big role in deciding the final performance of thermal, PI and SI of the PCB. By changing the design of copper interconnects, including traces, planes, and vias, could the final performance of the product be adjusted to be within the specified limits.

Modifying the size, placement, number, and distance to neighboring interconnects allows the thermal, PI and SI properties to be effectively changed and improved. Simulations allow the comparison between different options to be easily visualized, allowing the best option to be picked out for the specific application.

However, care should be taken when the absolute values of a design option are required, compared to just relative values between different options. Tolerances in the manufacturing process, as well as error margins within the material characteristics, needs to be included in the simulation to produce a more accurate span of where the final results might end up.

Introducing simulations in the design phase of the PCB would improve the process, reducing the need to produce more prototype PCBs. This would reduce the time to market of new products while still reducing the cost and environmental impact associated with the design work of a new product.

7.2 Future work

Future work is required to understand the capabilities and limitations of the simulation tools in more detail. Tolerances and material error margins need to be better defined to get a better understanding of the error margin related to that of the simulation tool.

Thermal simulations could be expanded to make a thorough investigation of the difference between external and internal layers of the PCB, simulating how effective the heat spread is within the PCB. The effect copper planes have as heat sinks could also be examined in greater detail. The measurements could be done over a wider span of test PCBs, in a controlled environment, to limit the effect of variation

between boards and external factors.

The decoupling capacitor optimization could expand to include different package sizes, allowing both bigger and smaller packages to be combined to evaluate the performance. The different options could be analyzed using cost, area, and the number of different capacitors needed. Furthermore, could a more realistic scenario be implemented where a single capacitor with a single via connection close to the IC is compared to multiple capacitors with multiple via connections placed further away.

Lastly, could the analysis of crosstalk between traces be improved by utilizing an oscilloscope with a higher sampling rate, which would allow faster changes to be captured more precisely. The frequency of the pulse generator could also be increased to see if the trace termination plays a bigger role when there is less time allowed for the crosstalk to settle between pulses.

Bibliography

[1] R. S. Khandpur, *Printed circuit boards: design, fabrication, assembly and testing ; [high density interconnects ; CAD/CAM techniques ; laminates ; soldering]* (McGraw-Hill electronic engineering), eng. New York, NY: McGraw-Hill, 2006, ISBN: 9780071464208.

[2] S. Solanki and R. Kumaraswamy, "Signal integrity check by simulation to improve PCB performance," in *8th International Conference on Electromagnetic Interference and Compatibility*, Chennai, India: IEEE, 2003, pp. 69–76, ISBN: 9788190065214. DOI: `10.1109/ICEMIC.2003.237840`. [Online]. Available: `https://ieeexplore.ieee.org/document/1287764` (visited on 03/28/2025).

[3] T. T. Tran, *High-Speed System and Analog Input/Output Design*, eng, 2nd ed. 2023. Cham: Springer International Publishing, 2023, ISBN: 9783031049545.

[4] B. R. Archambeault, *PCB Design for Real-World EMI Control.* Boston, MA: Springer US, 2002, ISBN: 9781475736427 9781475736403. DOI: `10.1007/978-1-4757-3640-3`. [Online]. Available: `http://link.springer.com/10.1007/978-1-4757-3640-3` (visited on 03/13/2025).

[5] D. Brooks and J. Adam, *PCB design guide to via and trace currents and temperatures*, eng. Boston: Artech House, 2021, ISBN: 9781630818609 9781630818616.

[6] Y. Liu *et al.*, "A Simulation-based strategy used in electrical design for reliability," in *2009 10th International Symposium on Quality Electronic Design*, ISSN: 1948-3295, Mar. 2009, pp. 208–212. DOI: `10.1109/ISQED.2009.4810295`. [Online]. Available: `https://ieeexplore.ieee.org/document/4810295` (visited on 04/02/2025).

[7] R. Kamali-Sarvestani, E. Nielson, and P. Weber, "Sustainability in printed circuit board manufacturing decreasing waste using additive technology," in *2015 IEEE Conference on Technologies for Sustainability (SusTech)*, Ogden, UT, USA: IEEE, Jul. 2015, pp. 67–72, ISBN: 9781479918027. DOI: `10.1109/SusTech.2015.7314324`. [Online]. Available: `http://ieeexplore.ieee.org/document/7314324/` (visited on 04/02/2025).

[8] K. Grant, S. Zhang, and J. Kettle, "Improving the sustainability of printed circuit boards through additive printing," in *2023 IEEE Conference on Technologies for Sustainability (SusTech)*, Portland, OR, USA: IEEE, Apr. 2023, pp. 86–90, ISBN: 9798350345483. DOI: `10.1109/SusTech57309.2023.10129587`.

[Online]. Available: https://ieeexplore.ieee.org/document/10129587/ (visited on 04/02/2025).

[9] G. K. Kantak, N. Sharma, and S. Mp, “Circular Design for Electronic Waste Reduction,” in *2023 International Conference on Power Energy, Environment & Intelligent Control (PEEIC)*, Greater Noida, India: IEEE, Dec. 2023, pp. 1338–1343, ISBN: 9798350357769. DOI: 10.1109/PEEIC59336.2023.10451549. [Online]. Available: https://ieeexplore.ieee.org/document/10451549/ (visited on 04/02/2025).

[10] M. Chakraborty, J. Kettle, and R. Dahiya, “Electronic Waste Reduction Through Devices and Printed Circuit Boards Designed for Circularity,” *IEEE Journal on Flexible Electronics*, vol. 1, no. 1, pp. 4–23, Jan. 2022, ISSN: 2768-167X. DOI: 10.1109/JFLEX.2022.3159258. [Online]. Available: https://ieeexplore.ieee.org/document/9733886/ (visited on 04/02/2025).

[11] F. Ling, K. Cai, and B. Sen, “Fast Full Board Crosstalk Scan for Signal Integrity Sign-Off for High Speed PCB Designs,” in *2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI & PI)*, Long Beach, CA: IEEE, Jul. 2018, pp. 122–125, ISBN: 9781538666210. DOI: 10.1109/EMCSI.2018.8495173. [Online]. Available: https://ieeexplore.ieee.org/document/8495173/ (visited on 04/02/2025).

[12] A.-M. Silaghi, C. Pescari, C. Bleoju, and A. De Sabata, “Solving Automotive Signal Integrity Issues by EMC Simulation,” in *2021 IEEE 27th International Symposium for Design and Technology in Electronic Packaging (SIITME)*, Timisoara, Romania: IEEE, Oct. 2021, pp. 33–36, ISBN: 9781665421102. DOI: 10.1109/SIITME53254.2021.9663717. [Online]. Available: https://ieeexplore.ieee.org/document/9663717/ (visited on 04/02/2025).

[13] S. Liang *et al.*, “Decoupling Capacitor Optimization to Achieve Target Impedance in PCB PDN Design,” in *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, Raleigh, NC, USA: IEEE, Jul. 2021, pp. 967–972, ISBN: 9781665448888. DOI: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559159. [Online]. Available: https://ieeexplore.ieee.org/document/9559159/ (visited on 04/02/2025).

[14] S. Wei, L. Ye, Z. Shaokun, and S. Qibiao, “Optimal Design of PCB Layout Based on Thermal Analysis Using Taguchi Method,” in *2021 3rd Asia Energy and Electrical Engineering Symposium (AEEES)*, Chengdu, China: IEEE, Mar. 2021, pp. 198–202, ISBN: 9781665425513. DOI: 10.1109/AEEES51875.2021.9403195. [Online]. Available: https://ieeexplore.ieee.org/document/9403195/ (visited on 04/02/2025).

[15] D. Hou, Y. Zhang, and Y. Zhou, “A Novel Heat Dissipation Optimization Design Scheme of Printed Circuit Board,” in *2024 3rd International Conference on Energy, Power and Electrical Technology (ICEPET)*, Chengdu, China: IEEE, May 2024, pp. 1635–1641, ISBN: 9798350352658. DOI: 10.1109/ICEPET61938.2024.10627435. [Online]. Available: https://ieeexplore.ieee.org/document/10627435/ (visited on 04/02/2025).

[16] Jayasekar Micheal, "PCB Stackup Design for Modern Electronics," Oct. 2023. DOI: 10.5281/ZENODO.8397973. [Online]. Available: https://zenodo.org/record/8397973 (visited on 03/12/2025).

[17] P. R. Wilson, *The Circuit designer's companion*, eng, Fourth edition. Oxford: Newnes, 2017, ISBN: 9780081017647 9780081017654.

[18] M. I. Montrose, *EMC and the printed circuit board: design, theory, and layout made simple* (IEEE Press series on electronics technology), eng. Piscataway, NJ: IEEE Press, 1999, ISBN: 9780471660903.

[19] E. Bogatin, *Bogatin's practical guide to transmission line design and characterization for signal integrity applications*, eng. Norwood, MA: Artech House, 2020, ISBN: 9781630816926.

[20] *Why is There a Transmission Line Critical Length?* en, Nov. 2019. [Online]. Available: https://resources.altium.com/p/why-there-transmission-line-critical-length (visited on 03/11/2025).

[21] F. Ndagijimana, *Signal Integrity: From High-Speed to Radiofrequency Applications*, en, 1st ed. Wiley, May 2014, ISBN: 9781848215504 9781118649183. DOI: 10.1002/9781118649183. [Online]. Available: https://onlinelibrary.wiley.com/doi/book/10.1002/9781118649183 (visited on 03/14/2025).

[22] T. Schuster and F. Hämmerle, *Impedance Measurements using the Bode 100*, 2020. [Online]. Available: https://www.omicron-lab.com/fileadmin/assets/Bode_100/ApplicationNotes/Impedance_Measurement_methods_using_the_Bode_100/2020-10-21_Bode_Appnote_Impedance_Measurements_V1_0.pdf (visited on 03/28/2025).

[23] J. Xu *et al.*, "A Novel System-Level Power Integrity Transient Analysis Methodology using Simplified CPM Model, Physics-based Equivalent Circuit PDN Model and Small Signal VRM Model," in *2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI)*, New Orleans, LA, USA: IEEE, Jul. 2019, pp. 205–210, ISBN: 9781538691991. DOI: 10.1109/ISEMC.2019.8825256. [Online]. Available: https://ieeexplore.ieee.org/document/8825256/ (visited on 04/03/2025).

[24] E. Bogatin, *Bogatin's practical guide to prototype breadboard and PCB design*, eng. Norwood, MA: Artech House, 2021, ISBN: 9781630818487.

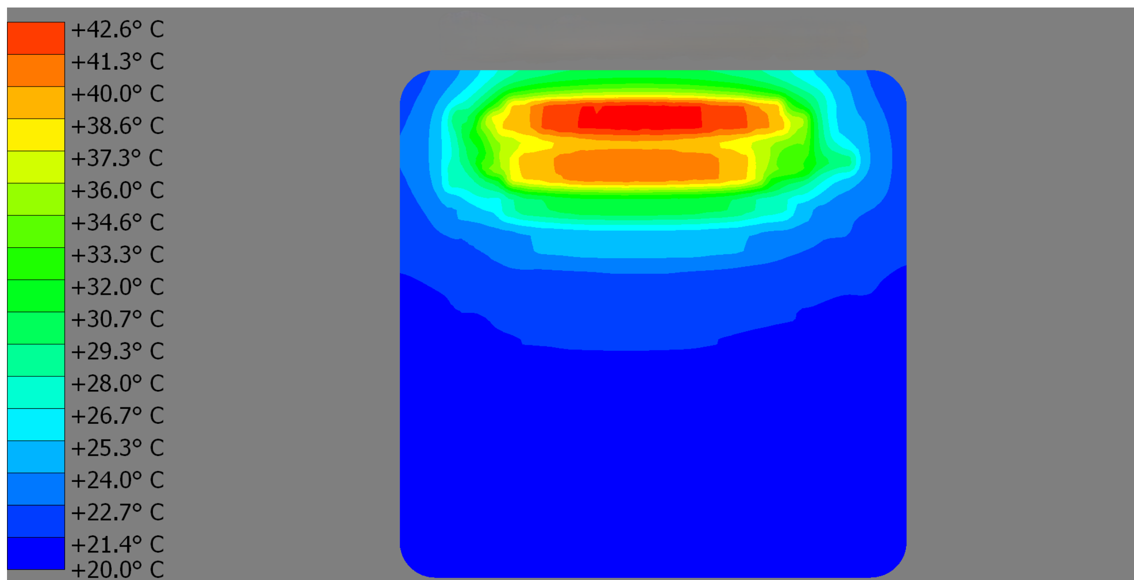
[25] J. Fan, J. Knighten, A. Orlandi, N. Smith, and J. Drewniak, "Quantifying decoupling capacitor location," in *IEEE International Symposium on Electromagnetic Compatibility. Symposium Record (Cat. No.00CH37016)*, vol. 2, Aug. 2000, 761–766 vol.2. DOI: 10.1109/ISEMC.2000.874717. [Online]. Available: https://ieeexplore.ieee.org/document/874717/citations#citations (visited on 03/14/2025).

[26] *Controlled Impedance PCB Layer Stackup- JLCPCB*, en. [Online]. Available: https://jlcpcb.com/impedance (visited on 03/20/2025).

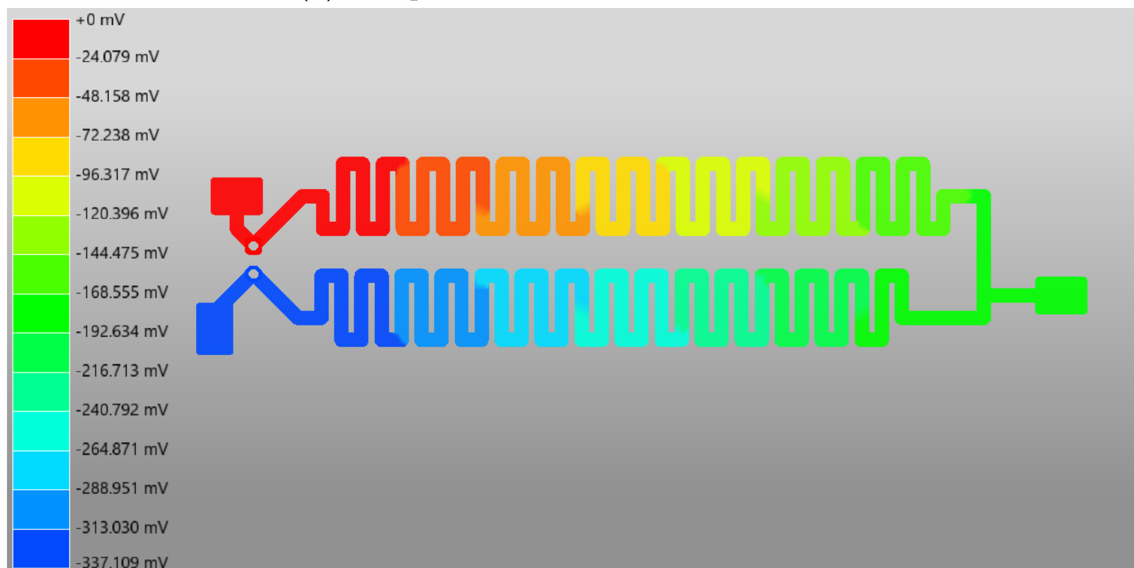
[27] *PCB Manufacturing & Assembly Capabilities - JLCPCB*, en. [Online]. Available: https://jlcpcb.com/capabilities/pcb-capabilities (visited on 03/20/2025).

A

DC IR simulation figures

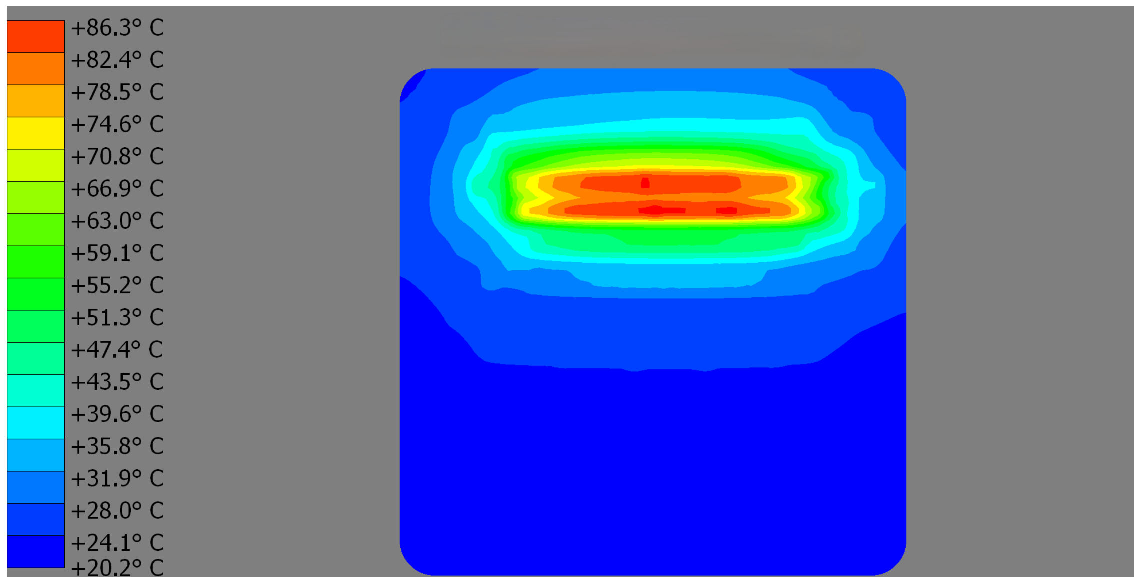


(a) Temperature of DC2 loaded with 2A

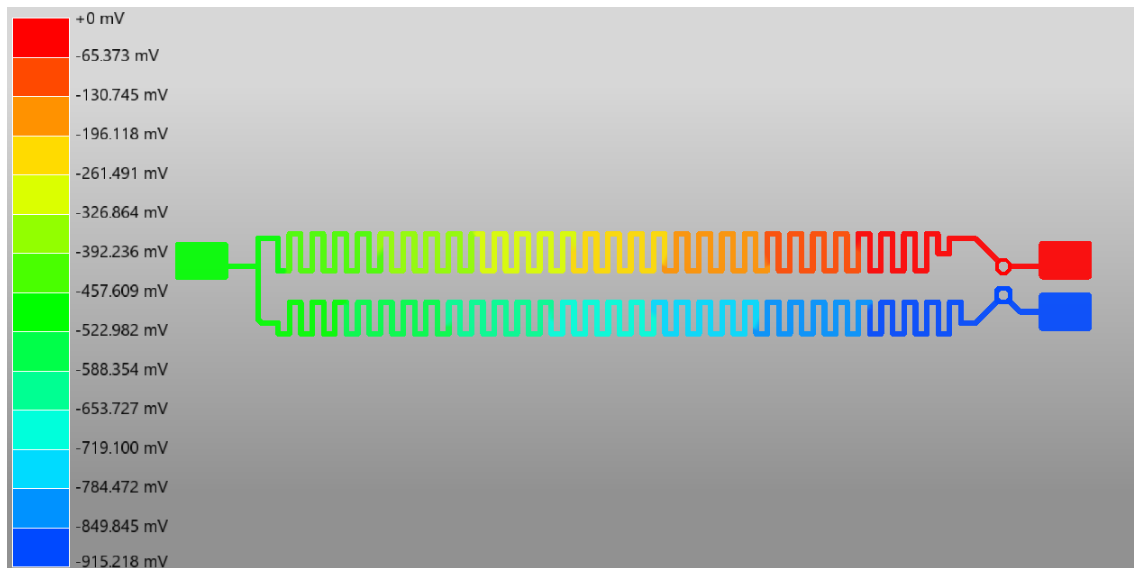


(b) Voltage drop at 2A for DC2

Figure A.1: Simulation results for DC2 which has the Large trace width

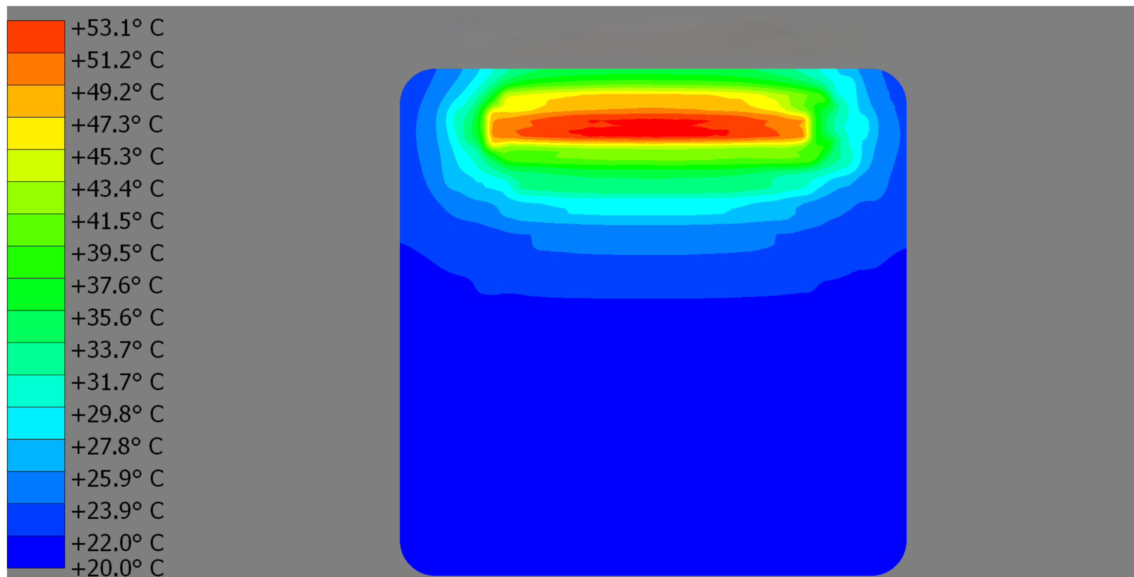


(a) Temperature of DC3 loaded with 2A

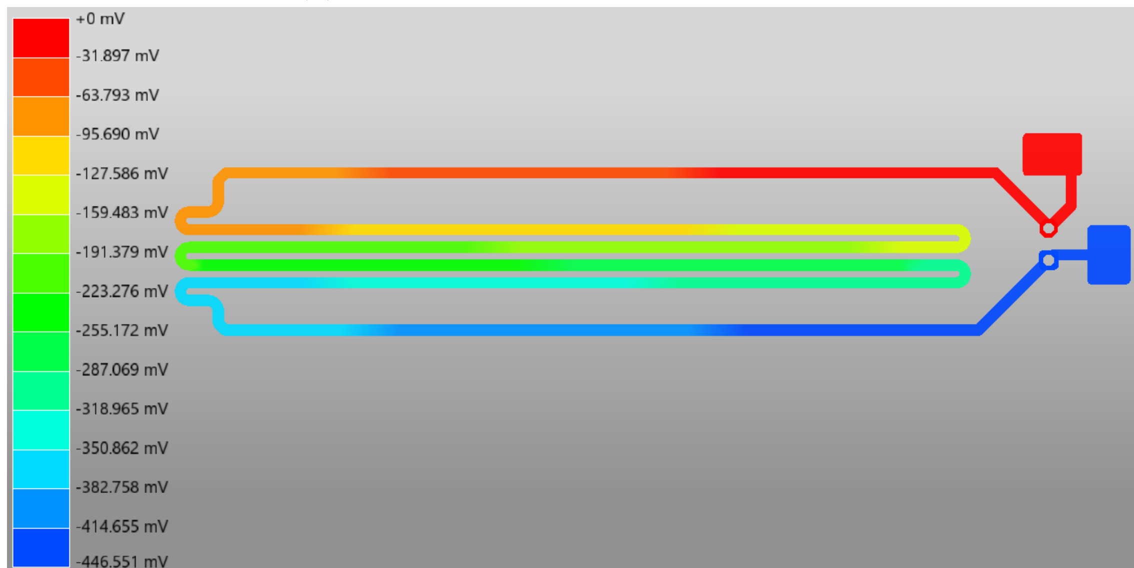


(b) Voltage drop at 2A for DC3

Figure A.2: Simulation results for DC3 which has the small trace width

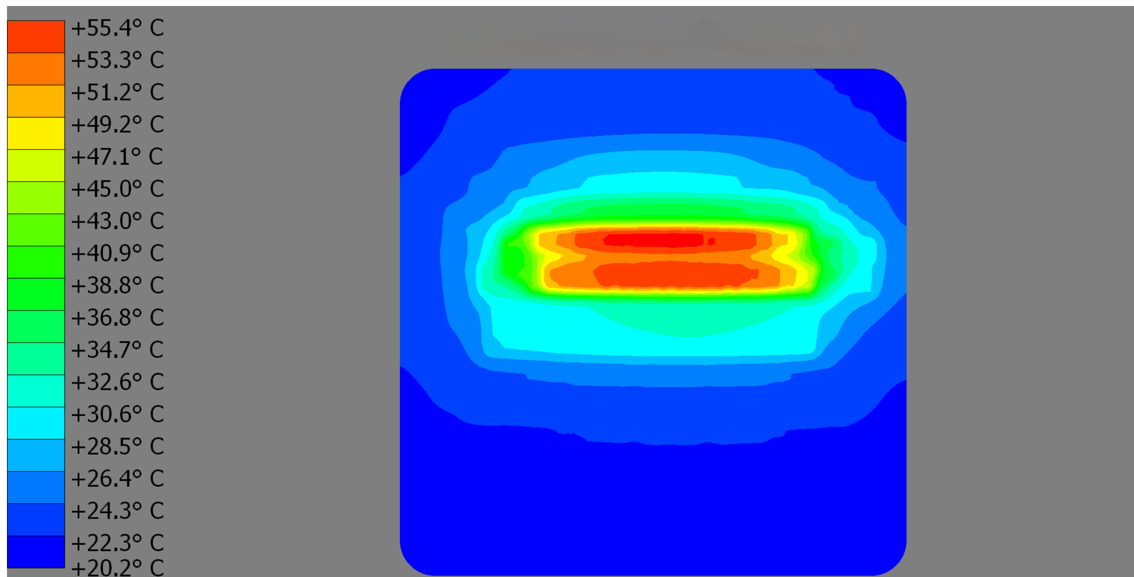


(a) Temperature of DC4 loaded with 2A

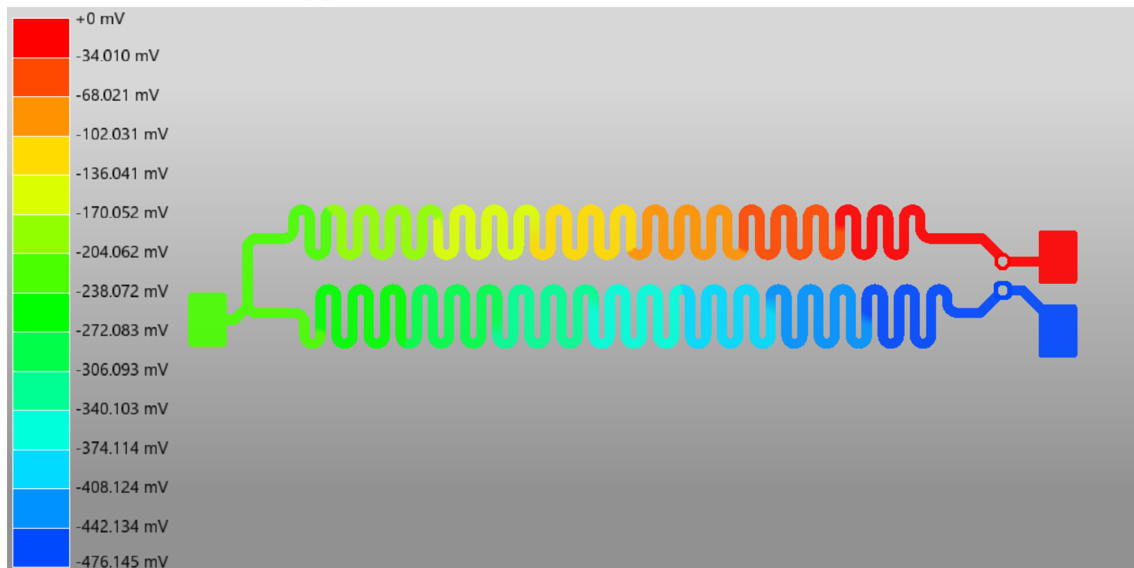


(b) Voltage drop at 2A for DC4

Figure A.3: Simulation results for DC4 which has the medium trace width, less corners

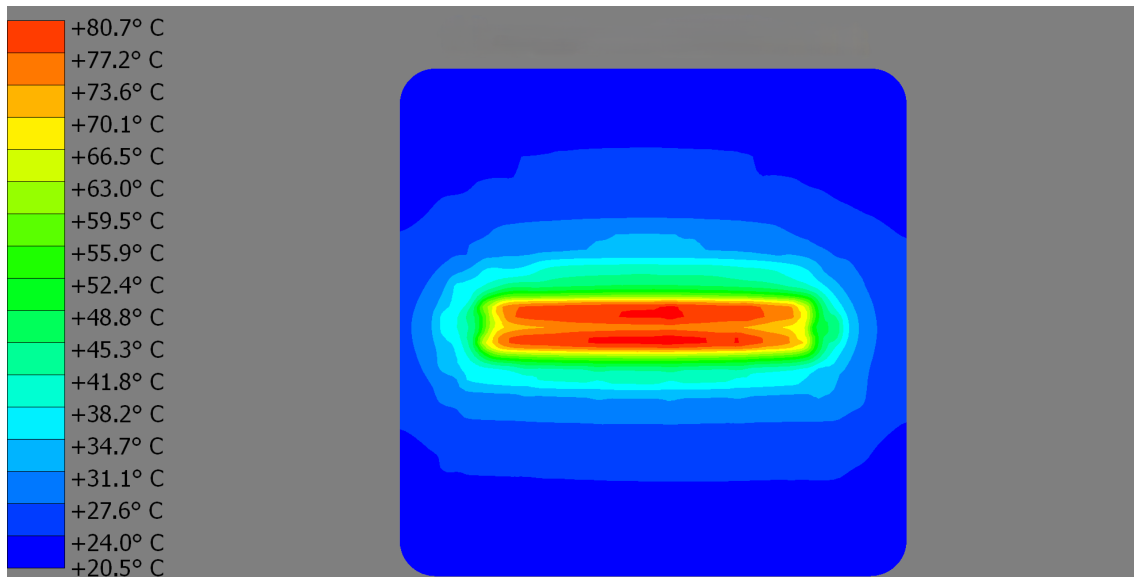


(a) Temperature of DC5 loaded with 2A

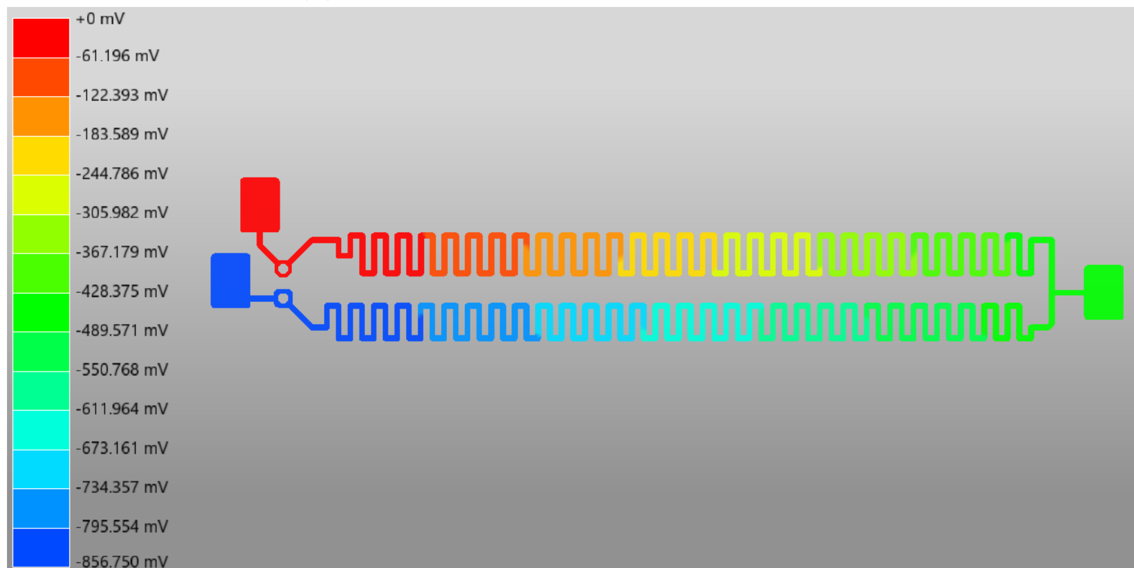


(b) Voltage drop at 2A for DC5

Figure A.4: Simulation results for DC5 which has the medium trace width, rounded corners

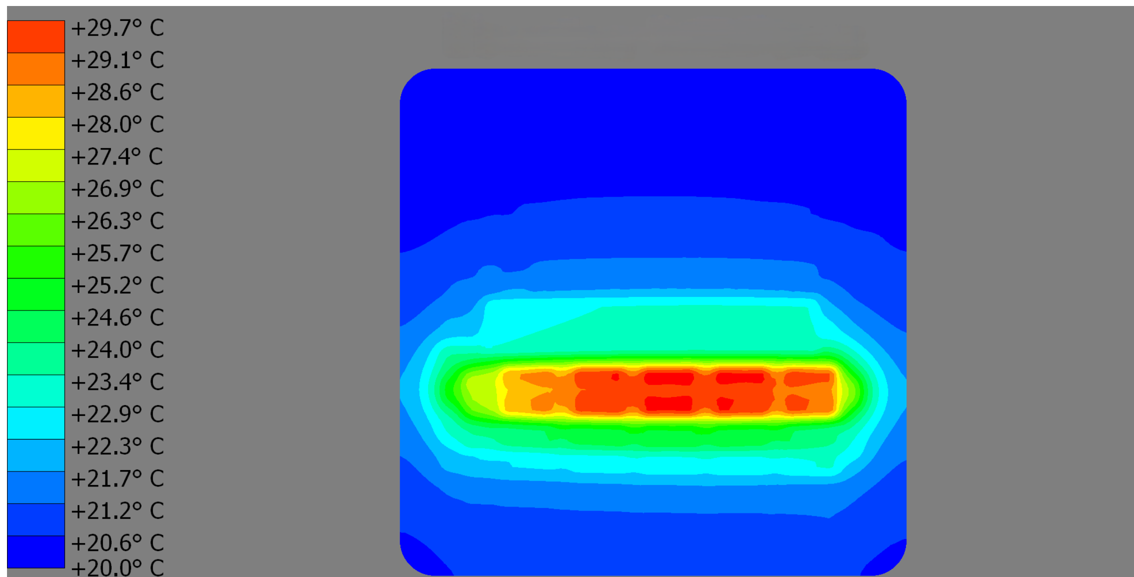


(a) Temperature of DC6 loaded with 2A

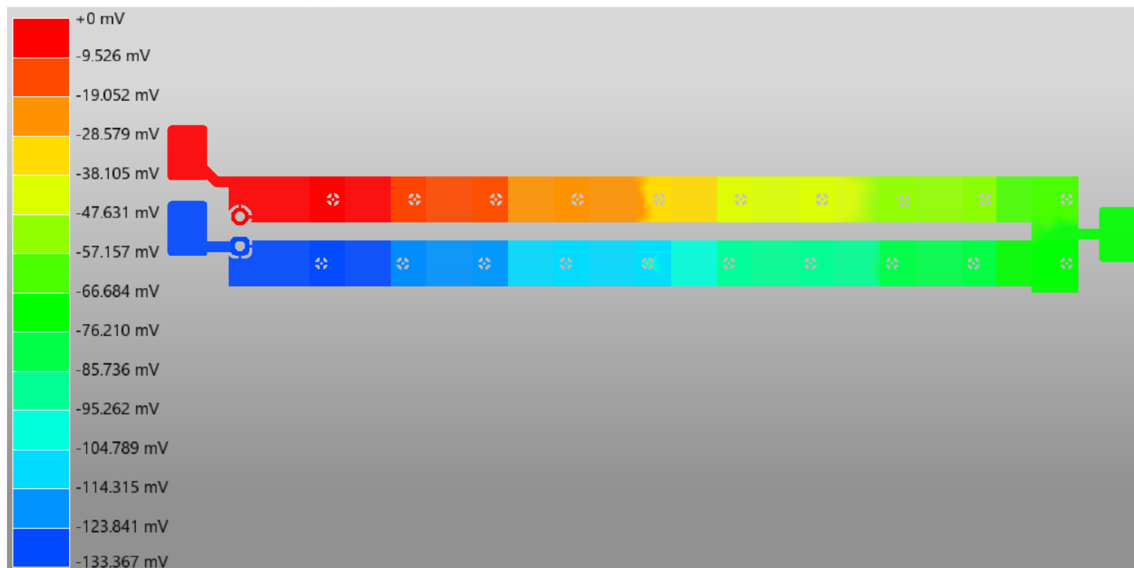


(b) Voltage drop at 2A for DC6

Figure A.5: Simulation results for DC6 which has the small trace width and heatsink

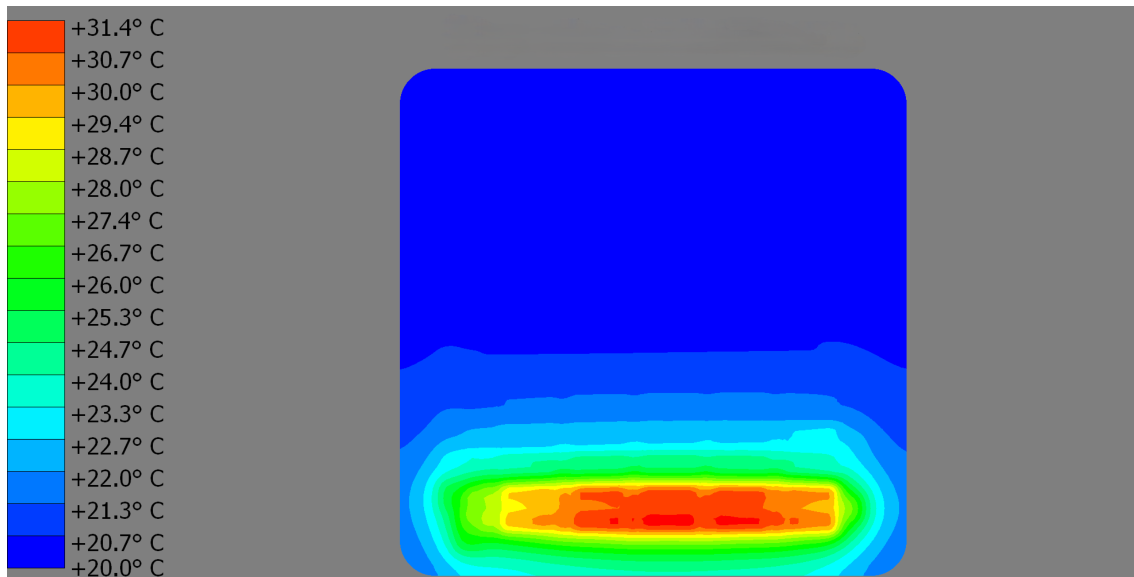


(a) Temperature of DC7 loaded with 2A

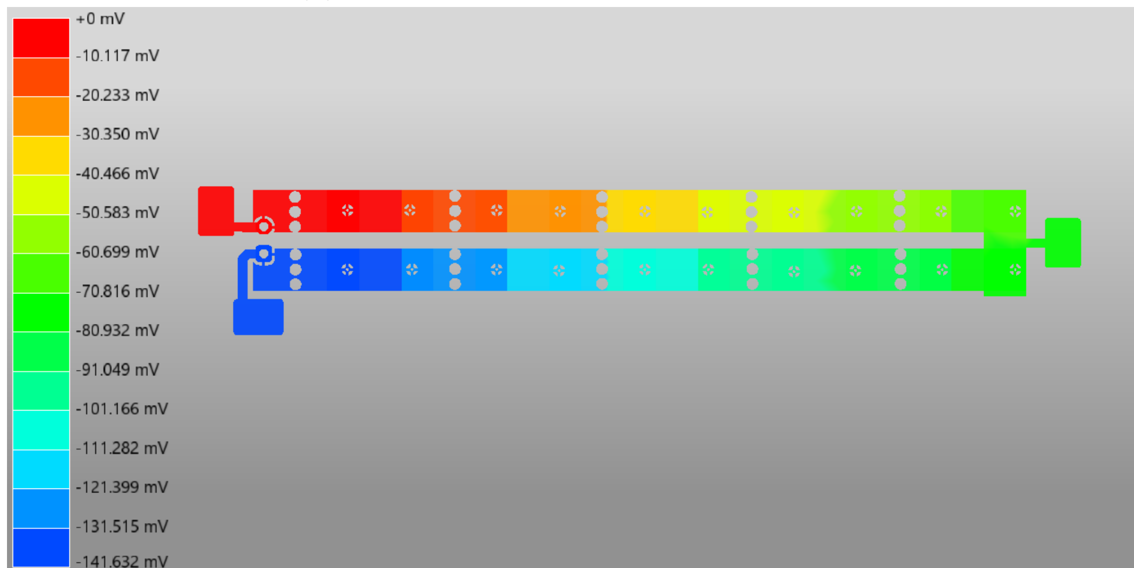


(b) Voltage drop at 2A for DC7

Figure A.6: Simulation results for DC7 which has single via

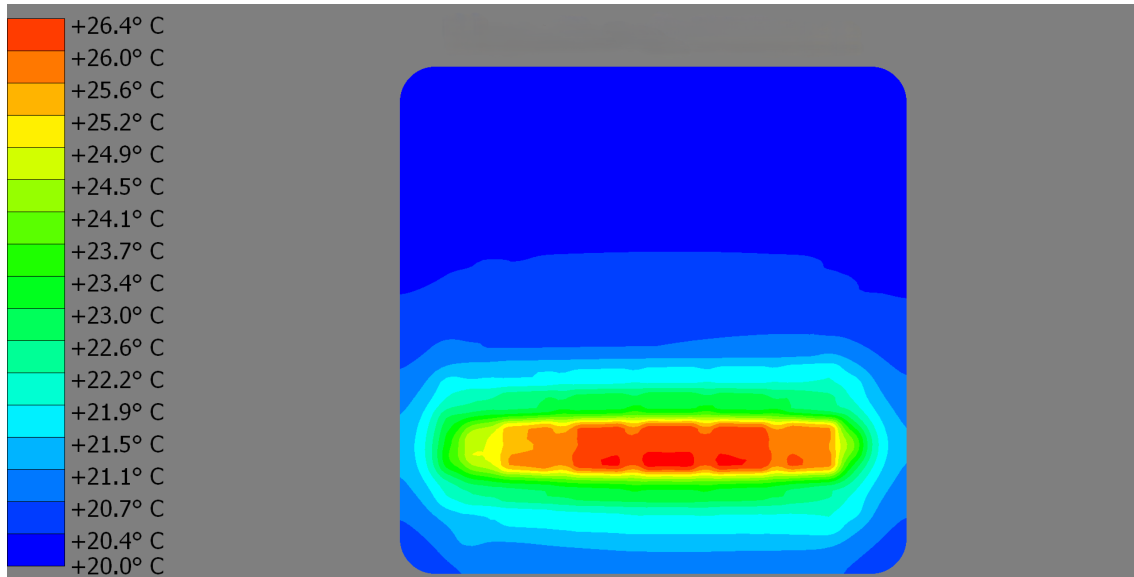


(a) Temperature of DC8 loaded with 2A

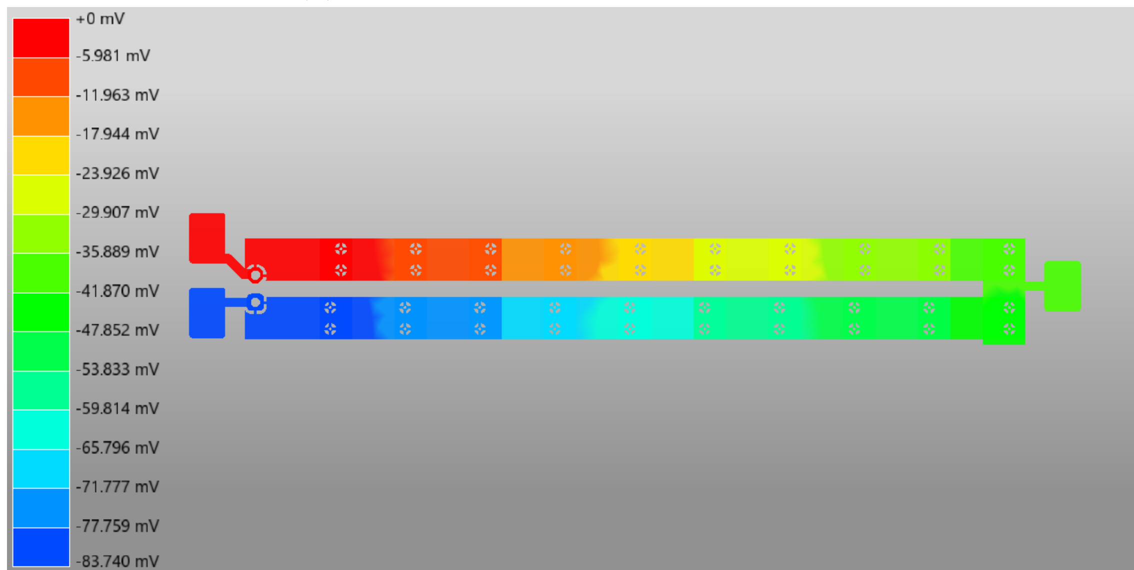


(b) Voltage drop at 2A for DC8

Figure A.7: Simulation results for DC8 which has single via and polygon obstruction



(a) Temperature of DC9 loaded with 2A



(b) Voltage drop at 2A for DC9

Figure A.8: Simulation results for DC9 which has two vias

Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden
www.chalmers.se

CHALMERS
UNIVERSITY OF TECHNOLOGY