Abstract

Vertical-cavity surface-emitting lasers (VCSELs) have been considered as one of the promising candidates for today's high speed communication systems. Small size, high data transmission rates, capability of achieving high production yields out of 2D array-based structures and wavelength tunability are some of the outstanding features of the VCSELs. Currently, there is a great deal of research on tunable VCSELs and these devices are believed to become the key components of the future optical networks. Microelectromechanical systems (MEMS) are one of the most successful technologies being utilized to obtain wide wavelength tuning ranges with the tunable VCSELs.

In this master thesis a wavelength tunable MEMS-VCSEL operating at the central wavelength of 850 nm has been designed and fabricated for applications in wavelength division multiplexed (WDM) reconfigurable optical interconnects. The fabrication technology followed a hybrid integration of curved micro-mirrors on GaAs-based half-VCSEL chips in a one-chip approach. The gain medium of the laser consisted of five GaAs quantum wells and the bottom $Al_xGa_{1-x}As/Al_yGa_{1-x}As$ DBR was grown epitaxially. Six highly p-doped current spreading layers were grown on top of the active region to enhance the current flow. Spherical photoresist structures were utilized as the sacrificial layer and titanium oxide (TiO_2) / silicon oxide (SiO_2) pure dielectric materials were deposited by DC and RF sputtering techniques to compose the MEMS distributed Bragg reflector (DBR). After surface micromachining and critical point drying (CPD) steps suspended MEMS mirrors were realized. From MATLAB simulations the reflectivity of the top 7.5-pair DBR was found to be around 99.9% with a full-width at half-maximum (FWHM) bandwidth of 320 nm.

The final device had a foot print of 230 μm × 370 μm and consisted of a curved micro-mirror supported by four suspension beams, placed carefully on the 15-μm current aperture of the half-VCSEL chip. A transverse multi-mode behavior was observed in the MEMS-VCSEL device and the laser showed a threshold current around 6 mA with the maximum output power of 1.7 mW. The wavelength of the laser was tuned by sourcing electric current through a Ni actuation network, patterned on top of the micro-mirrors. The maximum obtained tuning range was around 12 nm with MEMS current of 18 mA.

Keywords: VCSEL, MEMS-tunable VCSEL, DBR, single mode emission, wavelength tuning, longitudinal and transverse modes.

Acknowledgment

Before all else, I would like to express my gratitude to Prof. Anders Larson for kindly accepting me in the Photonics Laboratory and giving me this unique opportunity to work in the field of optoelectronics. My exceptional appreciation goes to my supervisor Dr. Benjamin Kögel for his inspiring ideas, never-ending help and encouragement, support and motivation in my work and for considering me as a friend. I am grateful to all the people in the Photonics Laboratory for the peaceful and nice atmosphere and for being warmly accepted as a member during my thesis work. To Göran Adolfsson for the very nice SEM images. To Erik Haglund for his fruitful comments on my thesis report. To Jeanette Träff for always being kind and helpful. I also wish to thank my former examiner and supervisor Dr. Hassan Rasooli at the University of Tabriz for introducing me to the interesting field of photonics.

The main part of this work has been carried out in the Nanofabrication Laboratory at the Department of Microtechnology and Nanoscience at Chalmers University of Technology, so I would like to highly acknowledge all the help and support that I have got from the cleanroom staff especially from Henrik Frederiksen for his continuous guidance and assistance with thin film deposition at the FHR tool. Thanks to Christian Grasse at the Walter Schottky Institute at Technische Universität München (TUM) for helping me with the DBR measurements.

The last but the most important, I am willing to express my gratefulness to my friends and family. To Amir and Hadi for all the fun time we have had together. To Omid whose unique sense of humor turned some boring cleanroom processings into fun and helpful discussions. To Saleh for always being there for me and to Kaveh for being a truly supportive friend. I would like to express my deepest gratitude to my mother, may rest in peace, for all her unconditional love, faith and motherhood without whom I could never have reached where I am today. You will be in my heart forever. To my father for always believing in me and to my lovely sister for her care and sympathy. Finally I must thank my dearest uncle for all his endless support and encouragements during my master studies.

This work was financially supported by the project “SUBTUNE” within the 7th Framework Programme of the European Commission.

Amin Abbaszadeh
Göteborg, March 2011

List of Abbreviations and Symbols

AR-C	Anti-Reflection-Coating
BCB	Benzo-Cyclo-Butene
CD	Compact Disk
CW	Continuous Wave
CPD	Critical Point Drying
DBR	Distribute Bragg Reflector
DC	Direct Current
DIW	De-Ionized Water
DVD	Digital Video Disc
FSR	Free Spectral Range
FWHM	Full-Width at Half-Maximum
HMDS	Hexamethyldisilazane
ICP	Inductively Coupled Plasma
LASER	Light Amplification by Stimulated Emission of Radiation
MASER	Microwave Amplification by Stimulated Emission of Radiation
MEMS	Micro-Electro-Mechanical-Systems
OSA	Optical Spectrum Analyzer
PAC	Photo Active Compound
PVD	Physical Vapor Deposition
RF	Radio frequency
RIE	Reactive Ion Etch
SEM	Scanning Electron Microscope
SiN	Silicon Nitride
SiO_2	Silicon Oxide
TEM	Transverse Electro-Magnetic
TiO_2	Titanium Oxide
UV	Ultraviolet
VCSEL	Vertical Cavity Surface Emitting Laser
WDM	Wavelength Division Multiplexing

Symbols

A	area
C	polymer concentration
E_{Fc}	quasi Fermi level (conduction ba
E_{Fv}	quasi Fermi level (valence band)
g	optical gain
h	Plank constant
I	clectric current
L	cavity length
l	length
n	refractive index
$\bar{n}$	effective refractive index
P	optical output power
q	longitudinal mode number
RoC	radius of curvature
r	reflection coefficient
T	Transmission matrix, photoresist thickness
T_{ij}	Transmission matrix element
t	transmission coefficient
V	voltage
w	radius of the laser beam
w_0	radius of the laser beam waist
z	propagation direction
z_0	Rayleigh distance

Greek symbols

α	amorphous, material absorption loss
α_m	mirror losses
β	propagation constant
η	photoresist viscosity
λ	wavelength
ν	frequency
ρ	specific resistance
ω	angular velocity

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1 Introduction

When the idea of "Optical MASERs[1]" was first presented by Charles Hard Townes and Arthur Leonard Schawlow in 1957 [1] it was hardly anticipated that these devices would have such an enormous effect on human life that in almost 50 years they become a major part of our everyday life. Nowadays different kinds of "LASERs", the abbreviation which stands for Light Amplification by Stimulated Emission of Radiation, are being used over a broad range of applications from ordinary CD and DVD players to complicated medical instruments and high-speed communication systems. Internet with its tremendous influence on almost all aspects of human society would never have reached its capacity of today without the help of propagating optical signals carrying huge amounts of data at the speed of light. Over the past few decades the very dramatically growing trends towards higher data capacities and faster information transfer have led to the sustained development of communication technologies including the delivery of novel transmitters (semiconductor lasers), propagation mediums (optical fibers) and receiving hardware (optical detectors).

Vertical-Cavity Surface-Emitting Laser (VCSEL) is one of the most favorable light emitting sources which has satisfied some major demands of today's industry: Very small physical dimensions, high information transport capacity and low production costs. In addition to extensive use in optical communications, specifically in short-haul optical interconnects, VCSELs are being used in a vast range of other applications such as absorption spectroscopy, data storage, optical mice and optical displays [2]. As the name indicates, this type of laser employs a vertically oriented optical cavity to emit photons perpendicular to the top surface. Circular beam shape with low divergence which favors an easy and excellent coupling to optical fibers, low power consumption and high efficiency at low output powers (in mW range) as well as capability of wafer-level fabrication and testing make VCSELs a very promising candidate for today's integrated optics and high-speed communications [3]. Furthermore, wavelength tunability is another unique feature of the VCSEL that has attracted lots of interest because of its numerous applications in wavelength-division multiplexing (WDM) optical communication systems [4], gas detection [5] and fiber Bragg-grating sensors [6]. One of the major technologies that has been developed to realize widely-tunable VCSELs is the fabrication of microelectromechanical system (MEMS)-VCSEL [7]. The MEMS-VCSEL can provide a wide wavelength tuning range, in the order of tens of nanometers, by employing a movable MEMS membrane as its top mirror.

[1] MASER: Microwave Amplification by Stimulated Emission of Radiation.

One common fabrication technology is a two-chip approach [8] which consists of the assembly of separately fabricated 'half-VCSEL' chips, which possess a similar structure to the ordinary fixed-wavelength VCSELs but with the top distributed Bragg reflector (DBR) removed, and micromachined MEMS devices. The wavelength of the laser is then tuned by electrostatic [9] or electro-thermal [10] actuation of the membrane which changes the length of the laser cavity and shifts the wavelength of emission. MEMS-tunable VCSELs can be used in different wavelength ranges for different applications. For instance, 850-nm tunable MEMS-VCSEL, which is studied in this master thesis as a part of the European project "SUBTUNE", are typically used in short distance data communication networks, while tunable lasers with wavelength ranges of 1.52-1.58 μm and 1.95-2.01μm are being exploited in gas spectroscopy [11].

This thesis work represents a convenient and versatile fabrication technology for GaAs-based tunable MEMS-VCSELs contemplated for WDM reconfigurable optical interconnects. The devices are designed to operate at the wavelength of 850 nm, but the technology can also be transferred to any other wavelength of demand. Opposed to the two-chip assembly techniques, which require challenging wafer bonding [12] and manual assembly [10] methods, this approach suggests a single-chip hybrid integration technology where MEMS micro-mirrors are fabricated directly on the half-VCSEL chips (cf. Figure 1.1). Some technologies have been represented up to date towards the realization of single-chip wavelength-tunable MEMS-VCSELs by (Chang-Hasnain et.al) using epitaxial material [9] and (Cole et.al) using amorphous Germanium (α-Ge) [13] as the sacrificial layer. The technology developed in this project at Chalmers University of Technology, employs photoresist as the sacrificial layer and utilizes pure dielectric materials (TiO_2 and SiO_2) for DBR composition. Design aspects for the planar-concave cavity structure of the MEMS-VCSEL are studied and the data extracted from the calculations and simulation results is applied to shape the MEMS-mirrors. Final structures are released after the removal of the sacrificial layer. Attempts aim at realizing the single mode tunable devices with low-threshold conditions and a wide tuning range.

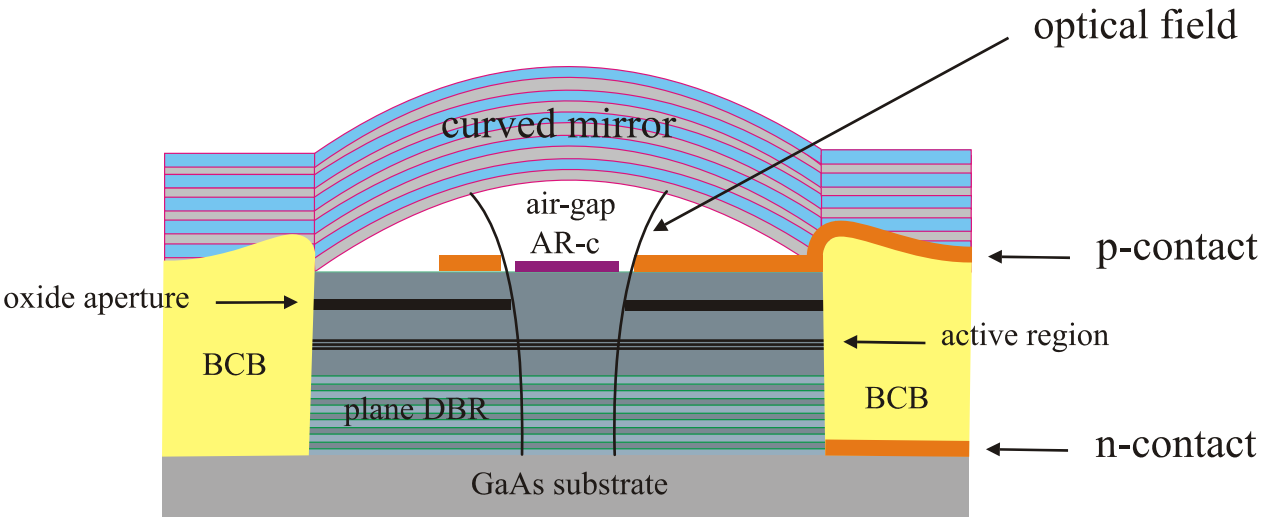


Figure 1.1. Schematic of a single-chip MEMS-tunable VCSEL.

The basic principles of the VCSEL and theory needed for understanding the MEMS-tunable VCSEL design, longitudinal and transverse mode selection, single-mode emission and the DBR structure are provided in chapters 2 and 3. Chapter 4 describes the fabrication procedure and different processing technologies. The optical characteristics of the final devices are discussed in chapter 5 and the measurement results are presented. Finally, chapter 6 shows some future directions and the outlook for this work.

2 Semiconductor Lasers

Semiconductor lasers are light emitting sources which utilize a semiconductor material as their gain medium and emit photons by stimulated emission. In laser diodes, a very common type of semiconductor lasers, injecting electric current through the active area establishes the population inversion and provides the lasing condition. Laser diodes in their simplest structure employ a p-n junction as an optical gain medium and two cleaved facets of the wafer to form the laser resonator. A very compact and small size, low cost, higher efficiency compared to other types of lasers and long lifespan are some of the major advantages of diode lasers, which has made them become the most common type of lasers in use. This chapter will briefly discuss the basic principles and characteristics of semiconductor lasers with an emphasis on vertical-cavity surface-emitting lasers (VCSELs).

2.1 VCSEL Structure

VCSELs in their simplest structure, as it is shown in figure 2.1, consist of an active gain medium located between two distributed Bragg reflectors which form the laser cavity and establish the optical feedback. Considering a GaAs-based VCSEL the active region is made up of one or multiple GaAs quantum wells [14]. The upper and lower DBRs are p-doped and n-doped respectively and an electric current is injected through the metallic contacts to bias the laser. Different VCSEL structures have been designed to achieve efficient current and light confinement, higher output power, lower differential resistance and smaller threshold current. Etched-mesa [15], buried heterostructure [16], proton-implanted [17] and oxide-confined [18, 19] structures are four common VCSEL designs all with trade-offs in the above-mentioned characteristics. In an oxide-confined VCSEL for instance, which provides both carrier and optical confinement, an AlGaAs layer with very high Al concentration is placed just on top of the active region and is selectively oxidized to form a current aperture. Excess electrons and holes injected to the active region are guided through this current aperture and thus contribute to the light generation. Furthermore, optical guided modes are confined to the core due to the lateral index guiding and experience net optical gain. This is the technique to attain fundamental transverse mode operation, where mode selection relies on the size of the oxide aperture and the effective index step.

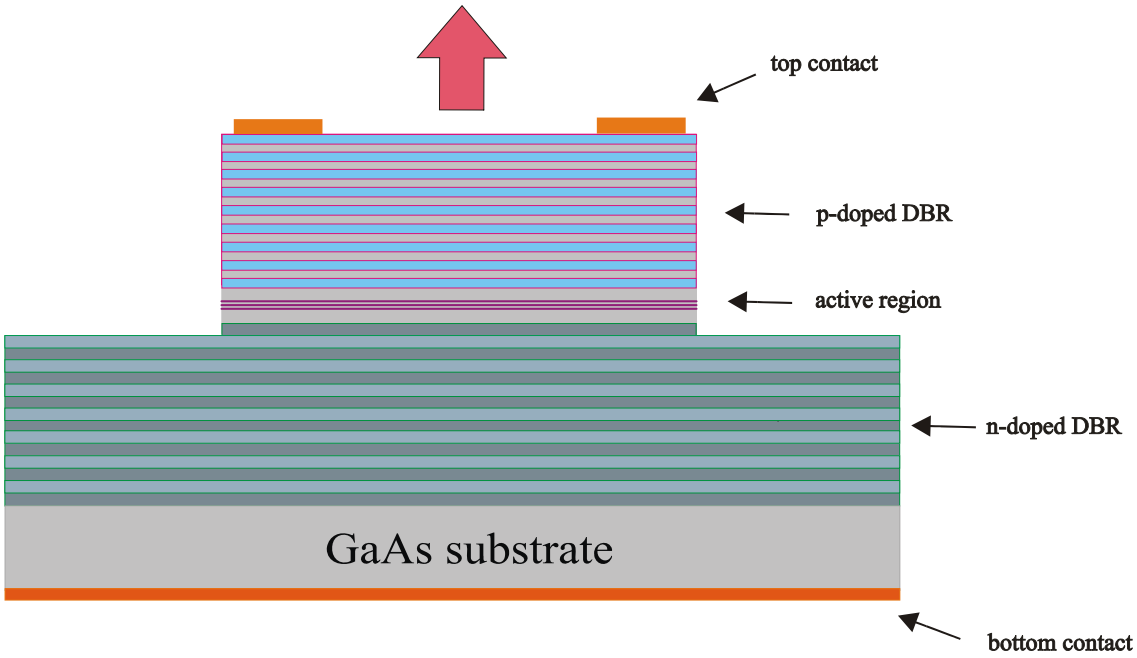


Figure 2.1. Basic structure of a fixed-wavelength VCSEL with the active region sandwiched between n- and p-doped DBRs.

As the device size is in the order of micrometers and the gain medium is very thin, it is important to have a low-loss resonator which compensates for the short length of the active region and provides sufficient optical gain for the laser. Therefore, DBRs have a very high reflectivity around 99% typically achieved by epitaxial growth of layers with alternating refractive indices such as $Al_xGa_{1-x}As/Al_yGa_{1-y}As$ layers with different x and y Al concentrations or deposition of dielectric materials with higher refractive index contrasts.

2.2 Theory

Semiconductor lasers require two main conditions to start radiation: Optical gain and optical feedback. Optical gain is provided by the active region of the laser and stimulated emission occurs through population inversion created by electrons and holes injected to the gain medium. Stimulated photons are then trapped in a semiconductor cavity that gives rise to the optical feedback and makes photons to oscillate inside the optical resonator. [20]

2.2.1 Semiconductor band structures and band-to-band transitions

To find out the basics of optical gain in semiconductors one first needs to look at some inherent characteristics like crystalline structure, band gap energy and energy band structures which explain the optical properties and behavior of these materials. The whole concept of light-matter interaction or more precisely electron-photon interactions as a basis for any kind of lasing depends on the specific electronic states of different materials and the energy exchange between the incident photons and traveling electrons during fundamental band-to-band transitions in the semiconductor lattice.

In direct band gap semiconductors like GaAs, there are three main types of radiative electronic transitions between the conduction and valence bands [20]: Stimulated absorption, spontaneous emission and stimulated emission [20]. These three processes contribute to the field energy inside the cavity by affecting the population of energy states with stimulated emission being the most important for the coherent emission of photons. Stimulated emission produces photons with same polarization, same phase, same direction and same frequency to incident photons which initiate the process by interacting with electrons in the conduction band, stimulating them to make a downwards transition and adding their excess energy to the propagating electromagnetic field. [21]

2.2.2 Population inversion and optical gain

Under non-equilibrium conditions where the charge population of energy states is reversed and the conduction band is more occupied than the valance band downwards transitions are more probable and amplification of light by stimulated emission is initiated. The basic condition for stimulated emission to occur is called Bernard-Duraffourg condition [22]:

$$E_{Fc} - E_{Fv} > h\nu \tag{2.1}$$

This happens when the population inversion is established and quasi-Fermi levels are separated far enough and go beyond the band-gap energy. The more quasi-Fermi levels penetrate into the band structures the broader becomes the gain curve.

E_{Fc} and E_{Fv} are the quasi-Fermi levels [22] for conduction and valence bands respectively, h is the Plank's constant and υ is the photon frequency. To provide the required net optical gain electrons and holes are injected to the gain medium and by increasing the input current the carrier concentration in the conduction band increases. At a certain current density, called threshold current, active medium provides net optical gain which balances the mirror out-coupling and intra-cavity losses. By further increasing the input current the laser output power increases rapidly and almost all carriers contribute to stimulated emission process. At threshold, the gain in the active region and the excess carrier population are clamped at a certain level known as the threshold gain and the threshold carrier density respectively [22].

2.2.3 Optical resonator characteristics for MEMS-VCSELs

Field components of propagating electromagnetic fields inside the waveguide are perpendicular to the direction of propagation [21]. Hence, these optical modes are called transverse electric and magnetic (TEM). For almost every kind of fundamental mode laser where TEM_{00} is the desired operation mode, optical beam intensity obeys the characteristics of a Gaussian. From Gaussian beam theory [23] two important factors are introduced which characterize the fundamental Gaussian beam: the beam diameter or the spot size (2w) of the laser beam at distance z from the origin:

$$w^2(z) = {w_0}^2 \left[1 + \left(\frac{z}{z_0}\right)^2\right] \tag{2.2}$$

and the wave front radius of curvature:

$$R(z) = z\left[1 + \left(\frac{z_0}{z}\right)^2\right]. \tag{2.3}$$

z is the propagation direction, w_0 is the radius of the Gaussian beam at the waist and $z_0 = \frac{\pi \bar{n} {w_0}^2}{\lambda_0}$ is the Rayleigh distance which defines the opening of the Gaussian beam [21]. λ_0 is the wavelength of the electromagnetic wave and $\bar{n}$ is the effective refractive index in the medium.

It is important to note that these parameters are in a direct relation with the characteristics of the optical cavity and thus can be tailored by adjusting geometrical parameters of the resonator. For instance, as depicted in figure 2.2, in a planar-concave resonator of MEMS-tunable VCSEL the beam waist with minimum spot size can be set to the plane bottom DBR and the curvature of the phase front matches itself to the radius of curvature (*RoC*) of the top DBR.

The minimum spot size of the beam inside the planar-concave VCSEL resonator with cavity length of L and radius of curvature of RoC can be calculated from equation (2.3):

$$2w_0 = 2\sqrt{\frac{\lambda_0}{\bar{n}\pi}\sqrt{L(RoC - L)}} \tag{2.4}$$

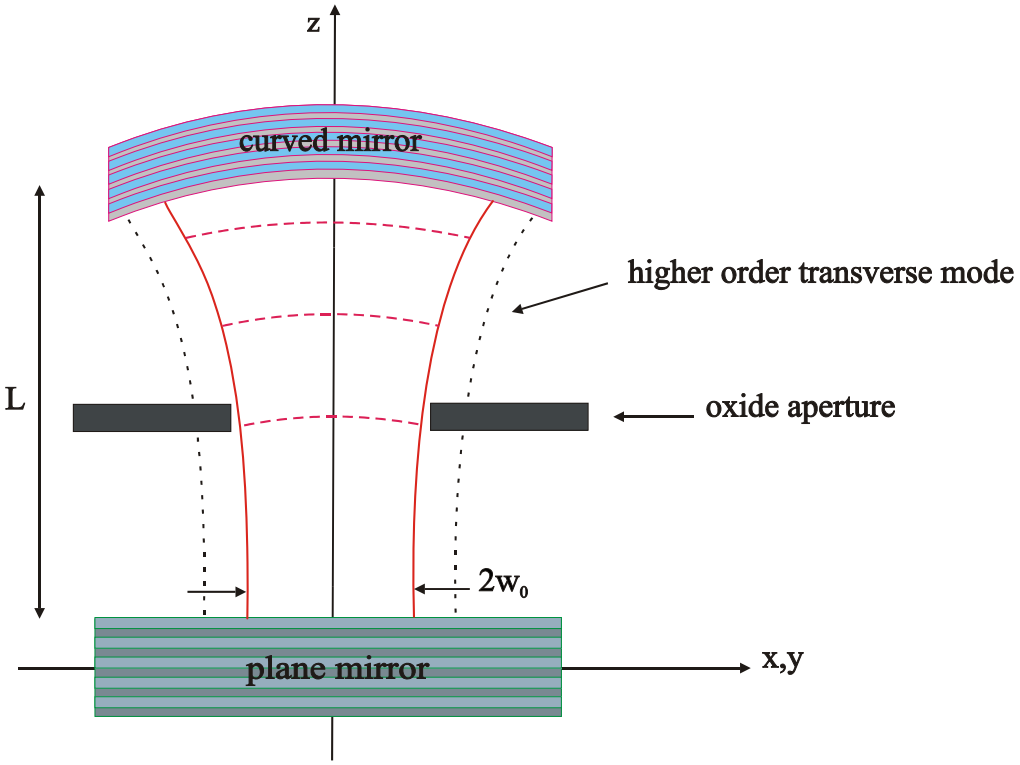


Figure 2.2. Planar-concave cavity structure of the MEMS-VCSEL. The fundamental Gaussian beam (solid line) has its waist ($2w_0$) on the flat mirror and the phase front radius of curvature matches to the ROC of the curved MEMS-mirror. Higher order transverse modes are attenuated and suppressed from oscillating inside the cavity by the oxide aperture.

For the planar-concave resonator it is also found from the resonator stability conditions [21] that RoC of the curved mirror has to be a lot larger than the cavity length ($RoC \gg L$). Furthermore, looking at the resonant standing electromagnetic field inside the laser cavity denotes that the phase shift of the field after one round-trip inside the cavity is a multiple of 2π [21]:

$$Roundtrip\ phase\ shift = 2\beta L = q2\pi\ , \tag{2.5}$$

where β is the propagation constant ($\beta = \frac{2\pi\bar{n}}{\lambda}$) and q is an integer called the mode number. From the phase condition it can be shown that each standing wave inside the cavity has a wavelength of:

$$\lambda_q = \frac{2\bar{n}L}{q} \tag{2.6}$$

These standing modes inside the laser cavity as illustrated in figure 2.3 are called longitudinal modes of the resonator and separation between longitudinal modes which is called free spectral range (FSR) can be calculated from:

$$\Delta\lambda_q = \frac{{\lambda_q}^2}{2\bar{n}L} \tag{2.7}$$

In a VCSEL the cavity length is very small and consequently separation between longitudinal modes is very large in comparison to the width of the gain spectrum. So there is only one longitudinal mode within the gain spectrum of the active region providing the single longitudinal mode operation. This also favors the tunable VCSELs by avoiding any longitudinal mode jumping during the wavelength tuning [24].

Besides, transverse side-modes in a tunable VCSEL are controlled by the design of the top curved DBR. By matching the size of the current aperture to the beam waist of the fundamental transverse mode and the wave front radius of curvature to the *RoC* of the top DBR, higher order modes with a wider beam waist e.g. $2w_{01} = 2\sqrt{2}w_0$ for the next higher order mode [25], experience less overlap with the gain profile and are no longer amplified (cf. figure 2.2). More details can be found in section 3.3.

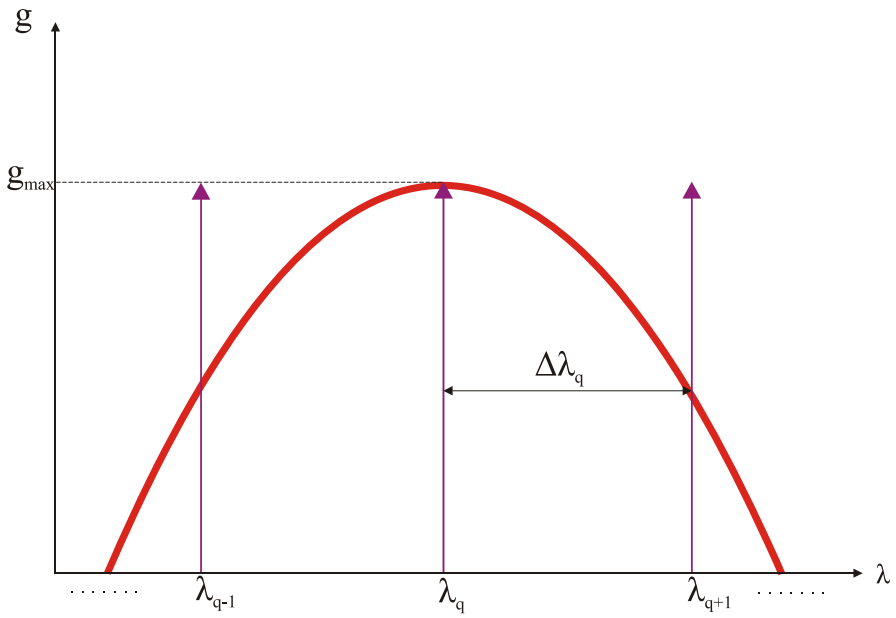


Figure 2.3. Longitudinal modes of the cavity and their overlap with the gain spectrum. The separation of the modes is $\Delta\lambda_q = \frac{\lambda_q{}^2}{2\bar{n}L}$ and only the modes within the gain curve experience lasing.

2.2.4 Wavelength tuning in MEMS-VCSELs

Wavelength tuning in VCSELs with suspended mirrors is basically realized by physical displacement of the curved membrane which changes the length of the air-gap and ultimately results in wavelength shifting [13]. As it is previously indicated, location of the longitudinal modes inside the laser cavity is defined by equation (2.6), thus by changing the cavity length wavelength of these modes will also change. For lasing to occur it is necessary that net cavity losses equal the net propagation gain at the desired wavelength [24]. Therefore, during the wavelength tuning only wavelengths that fall within the gain spectrum and have mirror losses lower than the maximum achievable optical gain experience lasing (c.f. figure 2.4). For a short cavity length there will be only one longitudinal mode inside the cavity and thus a single mode tuning condition is satisfied. Limitation of the tuning range is defined by the spectral width of the gain and mirror loss curves as well as the FSR, where larger FSRs prevent any mode-hop during the tuning process.

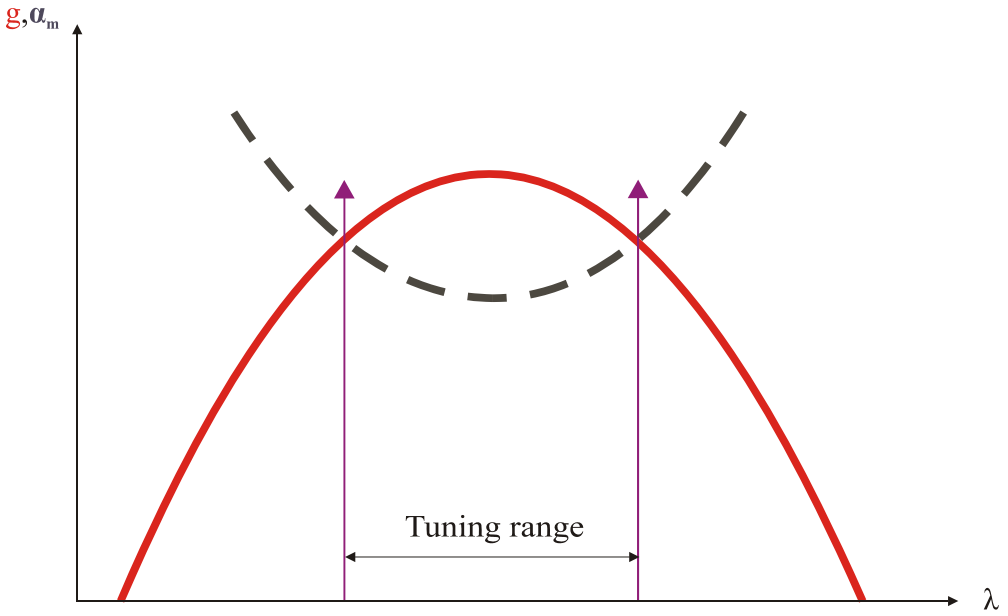


Figure 2.4. Tuning range of the MEMS-VCSEL with the longitudinal mode wavelength shifting inside the gain curve. The bold curve indicates the net optical gain (g) and the dashed curve is the mirror losses (α_m). Lasing happens for wavelengths which have mirror losses lower than the maximum net gain.

2.2.5 Scattering and transfer matrix method

Basically scattering happens when propagating electromagnetic waves are perturbed by an obstacle in their traveling path. The result of such collisions is creation of reflected and transmitted powers from and through the barrier. To analyze the properties of these interacting electromagnetic waves a matrix formalism is built up to relate the inputs and outputs at scattering junctions [24]. As a related matter of interest, the problem is solved for incident optical electromagnetic waves (photons) at the interfaces of consecutive dielectric materials with alternating indices of refraction. Considering a structure made of two separate dielectric materials as shown in figure 2.5 and assigning A, B, C and D as the wave amplitudes for the interface at $x=x_1$ the linear relation between amplitudes of right and left hands of the interface can be represented as:

$$A = T_{11}C + T_{12}D \tag{2.8}$$

$$B = T_{21}C + T_{22}D$$

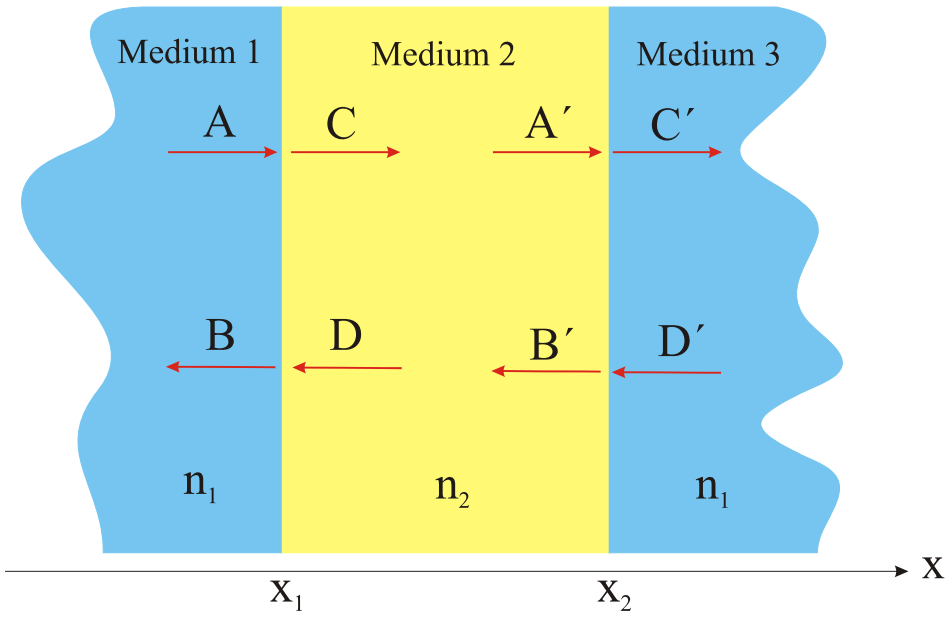


Figure 2.5. A dielectric sequence with alternating refractive indices (n_1 and n_2). Incident, transmitted and reflected waves have amplitude factors of A, B, C, D at $x=x_1$ and A',B',C', D' at $x=x_2$.

T_{ij} coefficients are the transmission matrix components and thus the matrix form of the above equations will be:

$$\begin{bmatrix} A \\ B \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} C \\ D \end{bmatrix} = T_1 \begin{bmatrix} C \\ D \end{bmatrix}. \tag{2.9}$$

Following the same approach will result in transmission matrices of mediums 2 and 3 and the overall T-matrix for the combination is obtained by ordinary multiplication of individual matrices:

$$\begin{bmatrix} A \\ B \end{bmatrix} = T_1 T_2 T_3 \begin{bmatrix} C' \\ D' \end{bmatrix}. \tag{2.10}$$

For the second interface at $x=x_2$ field distributions are simply modified by interchanging the wave numbers and assigning A',B',C' and D' as the amplitude factors [24].

Assuming no incident wave from the right hand ($D'=0$), the transmission probability of the whole structure is defined by the ratio of transmitted and incident waves and is expressed as:

$$T = \left|\frac{1}{T^*_{11}}\right|^2. \tag{2.11}$$

Overall power reflection is also calculated from the below equation:

$$R = \left|\frac{T^*_{21}}{T^*_{11}}\right|^2. \tag{2.12}$$

Where, T^*_{11} and T^*_{21} are the components of overall transmission matrix. By developing T-matrix method for sequential structures with several dielectric layers it is possible to acquire the reflectivity and transmittance of such complicated combinations as well.

2.2.6 Distributed Bragg Reflectors

Distributed Bragg reflectors (DBRs) are one of the most important structures employed by surface-emitting diode lasers to provide very high reflectivity and form the laser resonator. Layers with optical thickness of quarter-wavelength ($\lambda_0/4n$) from two different materials with alternating refractive indices (n_1 and n_2) are stacked to form highly reflective structures serving as the mirrors of the laser cavity. Constructive reflections add up in phase at the emission wavelength and provide a high total reflectivity. Maximum reflectivity of the Bragg reflectors increases with the number of grown pairs and a higher refractive index contrast of layers results in a broader reflectivity bandwidth [24]. Transfer matrices can be cascaded as indicated in section 2.2.5 to achieve the total T-matrix of the structure from where the total reflectivity is calculated. T-matrix parameters for a DBR layer, including one interface, for instance at $x=x_1$ (c.f. figure 2.5), can be expressed as:

$$T_{11} = \frac{1}{t_{12}}.\, e^{i\beta_2(x_2-x_1)} \tag{2.13}$$

$$T_{12} = \frac{r_{12}}{t_{12}}.\, e^{-i\beta_2(x_2-x_1)} \tag{2.14}$$

$$T_{21} = \frac{r_{12}}{t_{12}} . e^{i\beta_2(x_2 - x_1)} \quad (2.15)$$

$$T_{22} = \frac{1}{t_{12}} . e^{-i\beta_2(x_2 - x_1)} \quad (2.16)$$

x_2-x_1 is the thickness and β_2 is the propagation constant in medium 2. t_{12} and r_{12} are the transmission and reflection coefficients respectively. Assuming air ($n \approx 1$) as the input and output medium, from equation (2.12) the total reflectivity for an m-pair plane DBR at the central emission wavelength is:

$$R = \left[\frac{1 - \left(\frac{n_1}{n_2}\right)^{2m}}{1 + \left(\frac{n_1}{n_2}\right)^{2m}} \right]^2 . \quad (2.17)$$

3 Design of Tunable MEMS-VCSEL

The basic structure of the complete integrated MEMS-VCSEL device consists of a curved dielectric membrane supported by four suspension beams, placed carefully on the current aperture of the half-VCSEL chip (cf. figure 1.1). These beams are fixed on the substrate by means of circular adhesion posts at the end, which provide micro-mirrors with stable support after the structures are released. Suspended MEMS mirrors are electro-thermally actuated using a Ni actuation network and the wavelength of emission is tuned. The spherical shape of the micro-mirrors is achieved by forming photoresist pillars during a photolithography process and then turning these cylindrical structures to sacrificial photoresist half-spheres during a reflow step. Two photomask sets are designed and fabricated; one preliminary mask set for experiments on the plane GaAs surfaces and one final set for integration with half-VCSEL chips. The layout of the final mask set has been modified slightly due to process requirements. Experiments with different parameters and methods are accomplished to find out the suitable fabrication technique. Details of the fabrication procedure are provided in chapter 4.

3.1 Half-VCSEL Structure

Basically, the half-VCSEL structure employed in this project is the same as the conventional VCSEL structure [26] aside from the top flat DBR being omitted. From the bottom-up view, fabrication technology on the pure GaAs substrate consists of epitaxially grown n-doped $Al_{0.9}Ga_{0.1}As/Al_{0.15}Ga_{0.85}As$ bottom DBR with 36.5 pairs designed for the reflectivity ~100% followed by 5 GaAs quantum wells serving as the gain medium. The active region is designed to be located at a maximum of the longitudinal field to provide maximum optical gain [24]. An $Al_{0.98}Ga_{0.02}As$ layer with high Al concentration (0.98) is located over the gain medium and is selectively oxidized to favor lateral carrier confinement. This oxide aperture or so-called the current aperture is placed at a node of the longitudinal cavity mode for minimum optical confinement [27], because contrary to conventional oxide-confined VCSELs where this current aperture provides both current and optical confinement, in the MEMS-VCSEL structure transverse mode selection is accomplished by the top curved micro-mirror as described in section 3.3.

6 highly p-doped layers are grown on top of the oxide layer to realize the current spreading through the oxide aperture [28] and an anti-reflection SiN (n=1.85) coating with the optical thickness of λ/4 is added to the semiconductor-air interface which significantly enhances the effective reflectivity of the interface and reduces the threshold gain by factor of ~2 [27]. Detailed information of epi-layers of the half-VCSEL and the fabrication procedure can be found in [27] and [29], respectively. Some process parameters such as mesa size, thickness of the contact ring, etc. are modified due to the integrated MEMS technology and process requirements. An optical-microscope picture of a half-VCSEL with a 120-μm mesa is shown in figure 3.1.

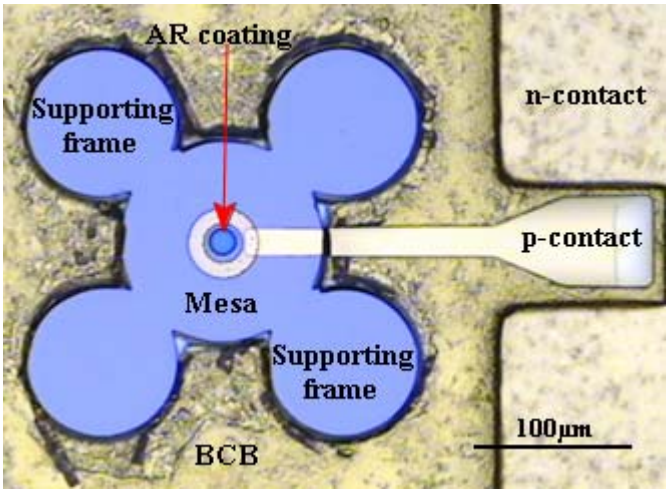


Figure 3.1. Optical-microscope picture of a half-VCSEL with mesa diameter of 120 μm.

3.2 Photomask sets for MEMS Devices

MEMS patterns are adjusted for different resist cylinder diameters and two, straight-line and zigzag, patterns are designed for the actuation layer. Figure 3.2 shows the photomask patterns for two similar arrays of devices with different actuation structures. Adhesion posts and micro-mirrors have a diameter of 200 μm and suspension beams are 90 μm long and 50 μm wide. MEMS devices have a dimension of 600 μm × 600 μm with resist cylinder diameters of 200, 250, 300, and 330 μm.

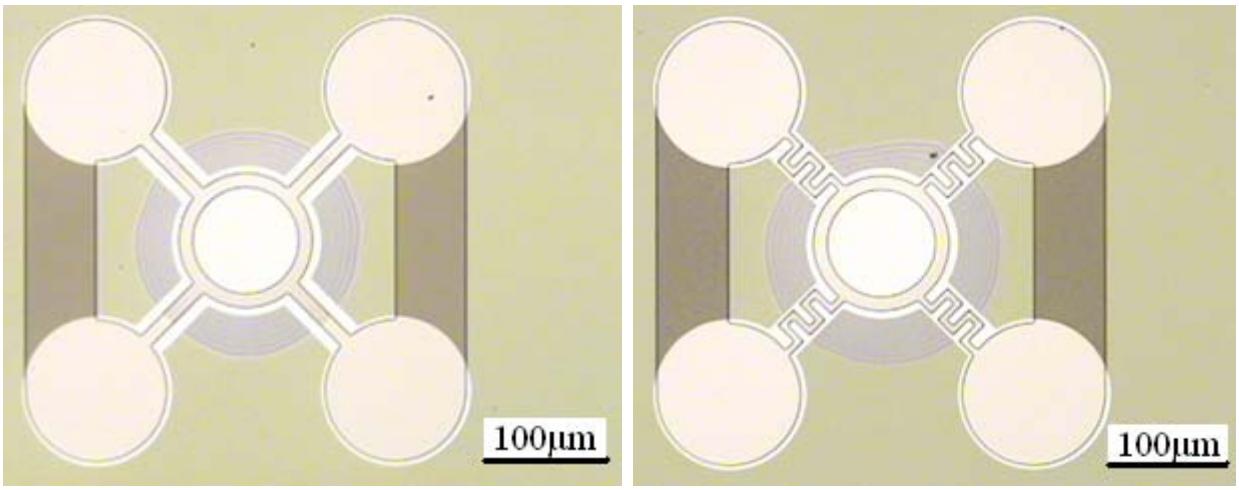


Figure 3.2. Straight line (left) and zigzag (right) actuation patterns.

MEMS photomasks are adapted slightly after the final design for the half-VCSEL chips is decided. Three different mesa sizes with diameters of 120, 150 and 200 µm are chosen to serve as the platform for MEMS membranes. The size of the photoresist cylinders is adjusted to cover the area of the mesas by taking the broadening ratios of reflow process into account. Therefore, three experimental broadening ratios of 1.2, 1.4 and 1.6 are selected and resist volume before reflow is defined by dividing the mesa diameter by the broadening ratios. Mesa diameter of 120 µm and broadening ratio of 1.4 are used for the first devices. MEMS mirrors have a diameter of 80 µm and supporting beams are designed in two different dimensions with widths of 30 µm and 20 µm and lengths of 23 µm and 20 µm respectively. Final devices have a footprint of 230 µm× 370 µm.

3.3 Design Aspects of Curved Micro-Mirrors

Spherical MEMS mirror technology employs an underlying spherical photoresist structure which serves as a sacrificial layer for the final devices. These photoresist half-spheres play a significant role in the MEMS technology because they form the final shape and define the *RoC* for the curved micro-mirrors. According to Gaussian beam theory [24], the *RoC* of the mirrors defines the transverse modes in the resonant cavity. For the stable planar-concave resonator to support the fundamental transverse Gaussian mode, the wave front curvature should match the mirror curvature. The beam waist is placed at the flat mirror with infinite radius of curvature.

The desired beam radius of the fundamental mode at the plane DBR is initially set to be $\omega_0 = 6\,\mu m$ and thus for a cavity length of L=3.7 μm (height of reflowed spheres on 120-μm mesas) radius of curvature for the curved micro-mirrors should be ~ 4.7 mm. To provide optical gain for the resonant mode the current aperture of the half-VCSEL is set to be ~15 μm, somewhat larger than the mode diameter in the flat mirror [27]. This cavity design approach will also prevent higher order transverse modes from resonating inside the micro-cavity thus they experience higher diffraction losses and are suppressed by the oxide aperture. Suppression of higher order side modes along with very small size of the optical cavity will satisfy both longitudinal and transverse single mode emission conditions.

For the top distributed Bragg reflector TiO_2 and SiO_2 are chosen as the dielectric materials and reflectivity is calculated for a 6.5-pair TiO_2/SiO_2 DBR with refractive indices of 2.36 and 1.45 by using a MATLAB code developed based on the transfer matrix method for multilayer structures. Some simulations have been done to investigate the effect of the material absorption on the maximum reflectivity showing a decrease of only 0.21% for a relatively high absorption loss of α=30 cm^{-1} for both dielectric materials. Therefore, the material absorption has been neglected in the DBR simulations. Maximum reflectivity is 99.8% at the central wavelength of 850 nm and the reflector has a bandwidth of ~330 nm. Simulated DBR spectrum is illustrated in figure 3.3.

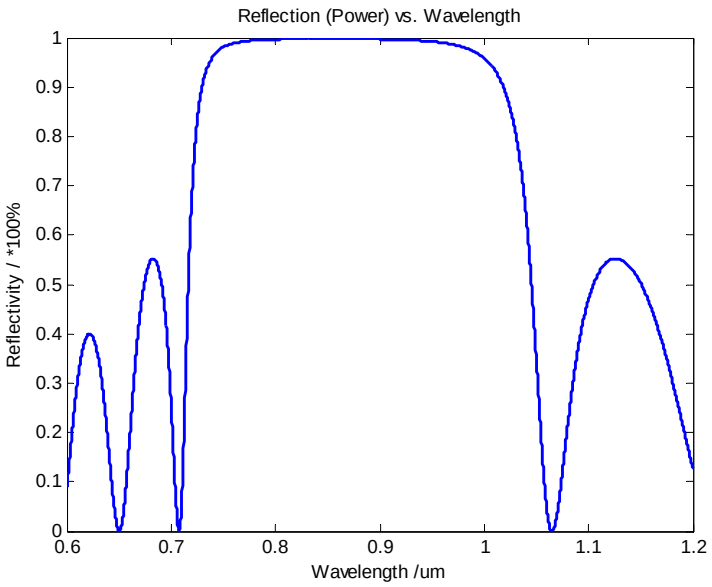


Figure 3.3. Simulated reflectivity spectrum for a 6.5-pair TiO_2/SiO_2 DBR with maximum reflectivity of 99.8% at λ=850 nm and the FWHM bandwidth of 330 nm.

4 Fabrication of Hybrid Integrated MEMS-VCSEL

The fabrication technology employs GaAs as the substrate material which is provided in 2" wafers and being cleaved to smaller chips of desired dimensions. GaAs wafers are cut into pieces along the "cleavage plane", (110) plane, where the bonding forces of the material are frail and thus the wafer can simply be cleaved. It is very important to have clean and contamination-free samples before starting the fabrication procedure, as in micro regime, device-sized contaminants can completely "kill" the device. Cleaved samples are first moved into a beaker of acetone, heated up to 50°C, and then are transferred to a sonic bath. By adjusting appropriate timing and ultrasound power, adhered contaminants are cleaned from the substrate. After the ultrasonic cleaner, cleaning process continues by passing the samples into methanol- and IPA-filled beakers respectively. After a short time around two minutes in each solvent, samples are taken out and air-dried by a nitrogen gun. Due to a huge amount of experimental data generated during the device fabrication procedure and to avoid repetitions and misunderstandings the only data presented in this report is from the final integrated device. However, some information, pictures and curves are also provided from different fabrication experiments to enhance the better understanding.

4.1 Photolithography

Undoubtedly, photoresist is the most substantial part of photolithography. Three main constituents of these chemicals are: the base material, which is a polymer, the light-sensitive component called photoactive compound (PAC) and a solvent which controls the mechanical properties of the resist. The photoactive component of the photoresist is sensitive to ultraviolet (UV) light and will react when it is exposed, which ultimately changes the solubility of the resist in the developer. Depending on the photoresist type this change can be an increase or a decrease of solubility in exposed areas. Positive photoresists become more soluble in the exposed areas, so these parts will be washed away when put in the developer. The pattern on the sample would be exactly the same as on the mask. On the other hand, negative resist will react contrariwise, i.e. the developer will solve non-exposed areas.

Substrate coating with photoresist is another important issue which has to be considered during lithography process. A nice, uniform and well adhered resist with an expectable thickness is desired on top of the coated wafer. Typically spinning is used to achieve a close-to-uniform thickness on the wafers. In specific cases, for instance a Si wafer, when a thin layer of oxide is formed on the surface, an adhesion promoter such as hexamethyldisilazane (HMDS) is applied beforehand to increase the resist adhesion to the substrate. Thickness of the resist depends on some parameters like resist viscosity (η), polymer concentration (C) and the angular velocity of the spinner (ω). An experimental relation between these factors can be expressed as:

$$T = \frac{KC^{\beta}\eta^{\gamma}}{\omega^{\alpha}}$$

where K, α=1/2, β=1 and γ=1 are experimental constants and T is the thickness of the resist [30].

Table 4.1 shows some data of thickness vs. spin-speed for AZ5214E image reversal photoresist, provided by the manufacturer[2] [32].

Spin speed (rpm)	2000	3000	4000	5000	6000
Resist thickness (μm)	1.98	1.62	1.4	1.25	1.14

Table 4.1. Thickness vs. spin-speed for AZ5214E image reversal photoresist.

MEMS fabrication process begins with preparing 1cm by 1cm GaAs chips for photolithography and coating them with AZ5214E. After spinning for 60 seconds at 1500^{rpm} speed which provides a resist thickness of 2.5 μm, excess resist drops at the sample edges are removed by using a Teflon rod. Samples are then soft baked at 100°C for 60 seconds to remove the remaining solvent after spinning and also increase the adhesion of the resist to the substrate. A KS MJB3-UV 400 mask aligner is used which utilizes a mercury-xenon vapor lamp to provide UV light for the lithography process. The mask set is of the common binary chromium type which is a translucent glass plate with chromium patterns. First, a frame mask is used to do a frame exposure before writing the main pattern on the sample. This is to avoid the effect of rough and bumpy surface of the resist at the edges which has the maximum height after spinning and will become in contact with the pattern mask at first if not removed. After the mask is set up and tightened in place, sample is mounted on an appropriate chuck and placed under the mask. A vacuum condition is applied through vacuum holes on the chuck to keep the chip fixed during the process.

[2] AZ5214E image reversal photoresist from MicroChemicals GmbH.

Frame exposure is being performed at *soft contact* mode for 80 seconds with the exposure intensity of 6 mW/cm^2. Sample is then transferred to AZ351B[3] developer, which is diluted by de-ionized water (DIW) with the dilution ratio of (1:4 / 20 ml:80 ml). Developing time for this lithography process is 45 seconds and the chip is rinsed in DIW for another 45 seconds and N_2-dried afterwards. The process is continued by mounting the sample in the mask aligner again and setting the pattern mask up to transfer the final pattern on the resist. Pattern exposure takes place in *contact* mode for 15 seconds.

Developing procedure and parameters are the same as they were for frame exposure and as a positive photoresist has been used we will get a positive image of the patterns. After final development is finished, an Oxygen plasma cleaning step is applied to remove unwanted residual photoresist from the surface. 2D surface topography of the resist cylinders is being scanned by means of a stylus surface profilometer. Measured surface profile of a photoresist cylinder is shown in figure 4.1.

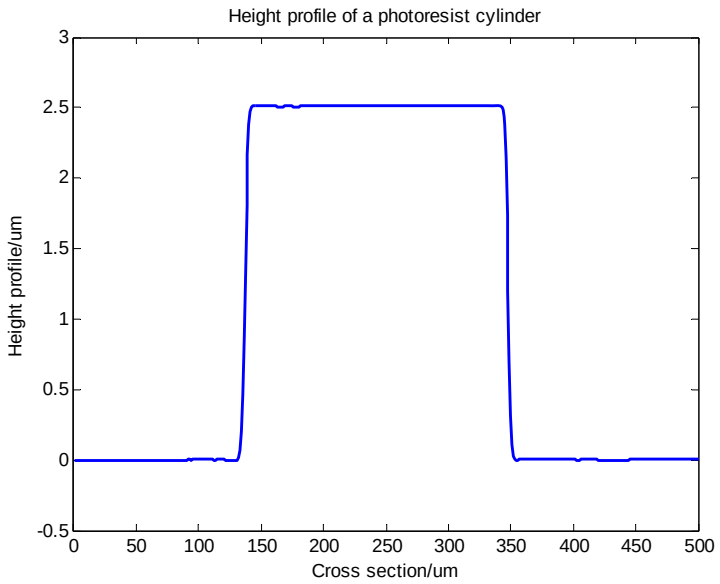


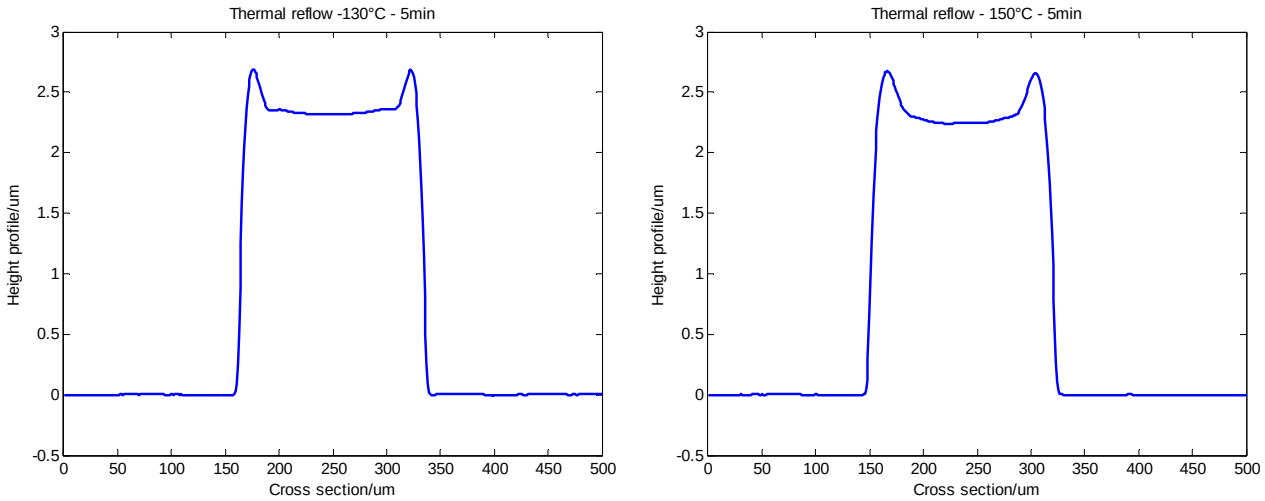
Figure 4.1. Height profile of a photoresist cylinder with the diameter of 200 μm and height of 2.5 μm.

One of the most significant concerns in MEMS fabrication is mask alignment. As MEMS fabrication is a layer-by-layer process and requires several lithography steps, it is of a great importance to have different layers placed exactly on top of each other. This matter is simply handled by introducing a set of similar alignment marks like cross-shaped features on all designed photomasks for different process steps. However, one of the most outstanding aspects of the MEMS technology introduced in this project is the self-alignment characteristic of the resist cylinders after reflow process on the half-VCSEL chips which subsides the restrictions of an accurate mask alignment.

[3] AZ351B developer from MicroChemicals GmbH.

4.2 Spherical Resist Structures

Cylindrical resist pillars formed on the GaAs substrate are made to ultimately serve as the sacrificial layer for the spherical micro-mirrors. There are some common techniques to create spherical resist structures out of these resist cylinders. Resist melting and reflow techniques are the two most important and practical ways being used for this purpose. During the melting or reflow process there is a surface profile transfer from cylindrical structures to curved spherical shapes which is referred to as the nominal surface being created due to the physical effects of surface tension. The static boundary conditions upon which the formation of such minimal surfaces depends are photoresist footmark, surface contact angle, resist volume and resist gravitation [31]. Thermal reflow or melting the photoresist by means of heating is one of the techniques being tried to get smooth spherical resist structures. Resist cylinders with the width of ~ 200 μm and height of 2.5 μm are processed to find the best experimental parameters. Baking temperature and time are two process parameters that have to be controlled carefully. As a starting point the sample is treated on a regular hot plate at 130°C for 5 min and then is left to cool down to the room temperature. The measured surface profile of the resist structure is shown in figure 4.2(a). As the final shape is not satisfactory, the process is continued by keeping the process temperature and increasing the baking time to 10 min. There is no significant change in the surface topography and therefore another change in parameters is necessary. A second sample is being processed at 150°C for 5 min and at the end no major improvements can be seen in figure 4.2(b). There is a limit in choosing the melting temperature as some other changes happen in chemical compounds at higher temperatures. Polymerization or polymer cross-linking is a phenomenon during which adjacent polymer chains are linked to each other by chemical reactions creating huge polymer molecules. Heat, radiation, pressure and change of the PH value are some initiators for such chemical reactions to occur. Cross-linked photoresist becomes more physically and chemically stable, resulting in hardened and more adhesive materials which makes the reflow process more difficult and may cause distortion and deformation of the desired spherical profiles. This along with unacceptable thermal reflow results at relatively high temperatures makes this technique be of no more interest.



(a) (b)

Figure 4.2. Thermal reflow with two different process parameters. a) 130°C for 5 min, b) 150°C for 5 min.

Reflow process by exposing photoresist to the vapor of specific solvents is another way of forming spherical structures. Acetone and Microposit remover 1165 are the two different solvents that have been tried. As a first experiment, samples are exposed to the acetone vapor in a closed container at room temperature (~20°C) for 30 min. The final shape is shown in figure 4.3.

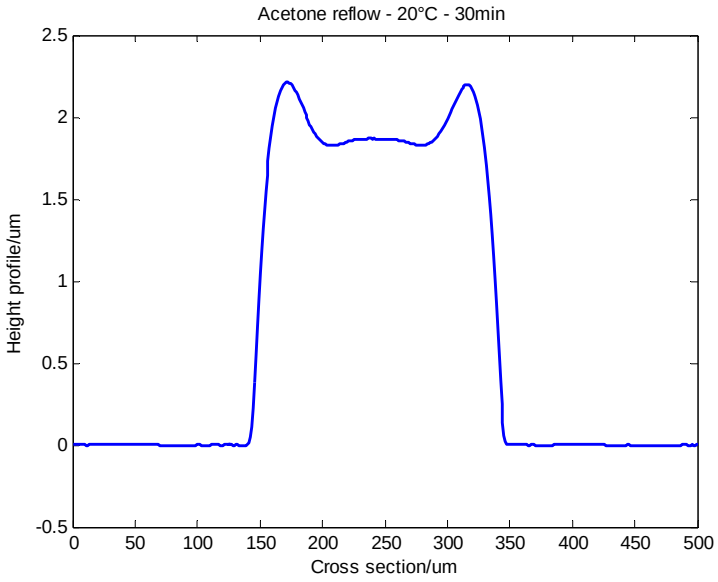


Figure 4.3. Surface profile of a reflowed photoresist pillar in acetone container for 30 min at room temperature.

In order to improve the results, heat is also introduced as a process factor which increases the vapor concentration inside the receptacle and reduces the reflow time. Acetone is heated up to 50°C under controlled process conditions for approximately 3 min and samples are blown gently with nitrogen afterwards to remove remaining solvent vapor form the surface. The final result is promising; nice and smooth spherical structures are formed. The height profile and the broadening ratios of a reflowed resist cylinder are shown in figure 4.4 left. From the spherical fitting, the *RoC* of the structure is found to be ~ 3.5 mm over a 100-µm fitting area, see figure 4.4 right.

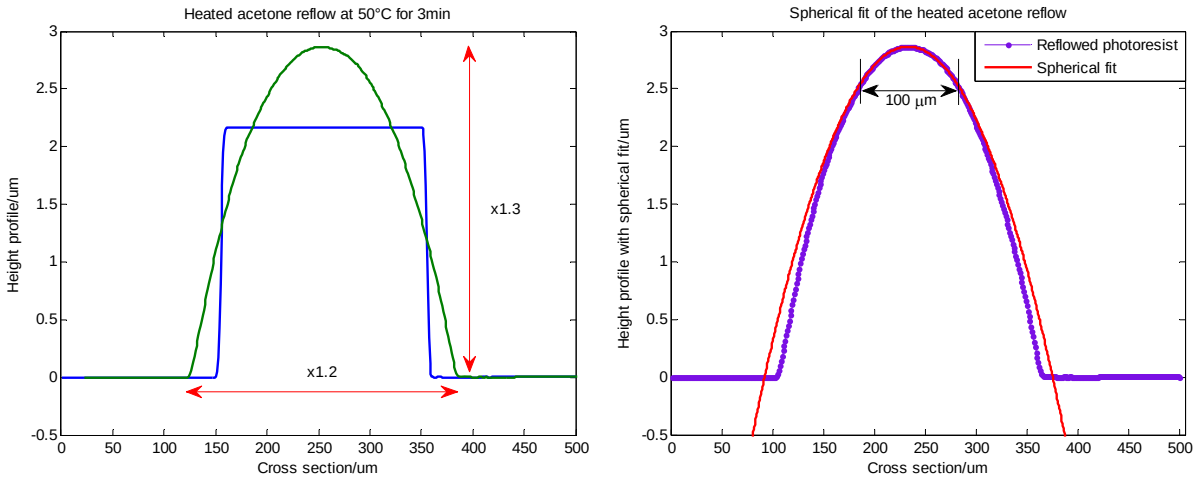


Figure 4.4. Surface profile (left) and the spherical fitting (right) of a resist cylinder reflowed in 50°C heated acetone for 3 min.

Microposit remover 1165[4] is the other solvent which is used in the reflow process. All the process parameters are alike to the acetone reflow, but the time is increased to 20 min. The surface profile of the reflowed resist is shown in figure 4.5 left. Compared to the heated acetone method, the surface at the peak of the structures is flatter and by fitting the surface profile (cf. figure 4.5 right), it is seen that a larger *RoC* around 8 mm can be obtained over a relatively small fitting area (~ 100 µm). However, because of the surface roughness problem in this method, the heated acetone reflow process is finally chosen to shape the photoresist half-spheres.

[4] Microposit remover 1165 from Rohm and Haas electronic materials.

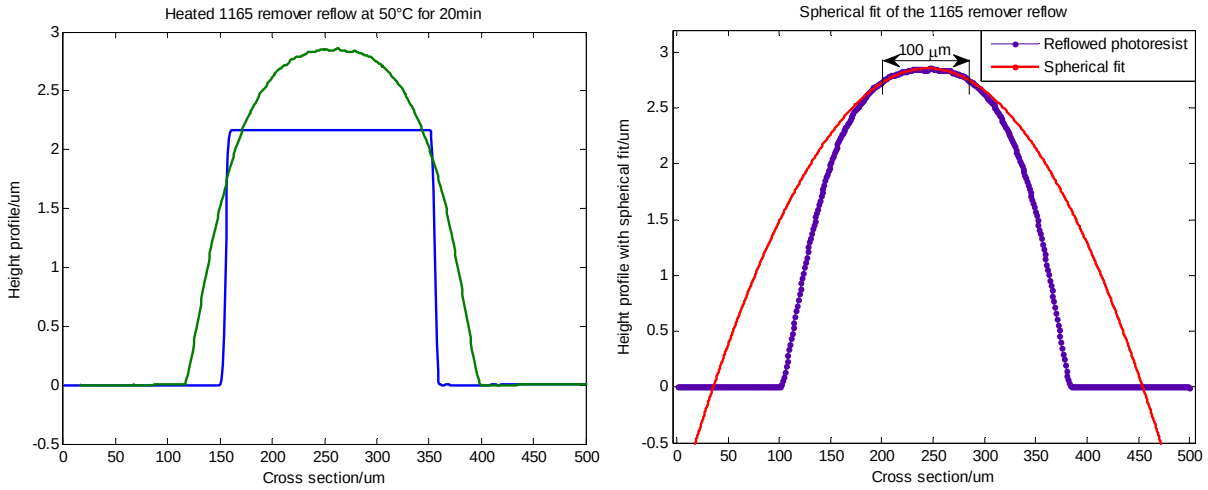


Figure 4.5. Surface profile of a spherical resist structure reflowed in 50°C heated 1165 remover for 20 min (left). Spherical fit of the resist structure with *RoC* ~ 8 mm over the fitting area of ~ 100 µm (right).

4.3 Dielectric Deposition

From what that has been described so far, the most important part of the work in this project is to fabricate a layered microstructure with specific characteristics operating under exactly pre-defined conditions. After the auxiliary spherical structures are formed, it comes to the fabrication of the micro-mirrors on top of these layers. The design and fabrication approach of the external movable mirror is to use pure dielectric materials with different refractive indices assembled together in a layered structure with layer thicknesses of the quarter of the emission wavelength. (cf. sec 2.2.6).

When photoresist is meant to be used as a sacrificial layer for subsequent processing steps in MEMS fabrication it undergoes some post-exposure treatments known as hard baking. This post-bake procedure increases the stability of the resist both chemically and physically and makes it adequately strong to endure the following process steps like electroplating, material deposition and etching. Different post-bake recipes can be applied based on the type of the resist and the process requirements. One important thing to be taken into account is the flow or melting temperature of the photoresist. Heating the resist above this softening point will result in the deformation of the spherical structures thus demanding the use of more thermally stable photoresists like AZ5214E which has a quite high softening point around 130°C [32].

A lot of experiments have been done to find out the best hard baking recipe which will guarantee the survival of the photoresist during thin film sputtering. Finally a post-bake process employing UV irradiation and heating is established which fulfills the desired demands of heating and plasma resistance needed for the deposition procedure.

4.3.1 Sputtering

Sputtering is one of the physical vapor deposition (PVD) techniques widely used in material deposition by condensation of the vapor of specific solid materials on the substrate. Ejecting the atoms from the surface of the target material and forming a very thin layer of atoms on the substrate under specific vacuum conditions is simply what happens during PVD. The low pressure or vacuum environment inside the deposition chamber, also called vacuum chamber, is to prevent the vaporized atoms from atomic collisions with other gas atoms and ions during the deposition process. Moreover, it conserves the deposited thin film from the probable contaminants. In sputtering argon is usually used to create high energy plasma to bombard the source material with positively charged ions. Two very common methods of sputtering are DC (direct current) and RF (radio frequency) sputtering, where the former only allows the deposition of electrically conductive materials while the latter provides the possibility to sputter non-conductive materials too. Nitrogen and Oxygen are also two reactive gases used in the sputtering process. One of the major disadvantages of the sputtering techniques is their low sputtering yield which means the main part of the input energy is converted to heat instead of contribution to deposition itself, resulting in quite low deposition rates.

DC sputtering

In DC sputtering, the source material which has to be electrically conductive acts as the cathode with negative charge in the system configuration and grasps positive argon ions which are generated by means of a high DC voltage. The walls of the vacuum chamber are used as the anode. As high-energy positive ions of the argon plasma strike the material target, atoms are released from the material and travel towards the substrate where they bond to the surface atoms and form the thin top layer. TiO_2 is sputtered with this technique using a titanium target and Oxygen as the reactive gas.

RF sputtering

Radio frequency sputtering relinquishes the requirement of the coating material to be conductive. Insulators cannot be formed through DC sputtering because the positive charge will accumulate on the target surface and the process will stop. Instead an RF electric field is applied to the anode and similar to the DC sputtering the target material serves as the cathode with negative charge. Argon is highly ionized by the RF current and the collision of argon atoms with electrons in the plasma accelerates positive ions towards the source material ejecting the surface atoms under a well controlled vacuum condition. These released atoms are then deposited on the substrate and form the thin insulator film.

Dielectric TiO_2/SiO_2 DBRs with 7.5 pairs are fabricated to achieve > 99.9% reflectivity at the central wavelength of 850 nm. To carefully control the thickness and stress of the layers a 3" silicon wafer is processed in parallel with the main samples and ellipsometer and stress tests are being done after the deposition of each layer. To obtain the exactly desired layer thickness and refractive index, sputtering is stopped approximately 1 min before the whole sputtering time for each layer. Ellipsometer tests are done and the process continues with new parameters from the provided data. Table 4.2 gives the ellipsometer information for the final integrated device with 7.5 pairs and total thickness of 1.76 μm. The stress of individual dielectric layers is also measured and recorded by stylus-Tencor P15 profiler system. Stress measurements show a tensile (~ +450 MPa) and a compressive stress (~ -100 MPa) for single TiO_2 and SiO_2 layers respectively. For a single DBR pair this stress is measured to be around +80 MPa tensile which points out a stress compensation in TiO_2/SiO_2 dielectric pairs. The mean stress of the full 7.5-pair DBR is around +36 MPa tensile (cf. figure 4.6).

Dielectric Layer	Layer Thickness	Refractive index @ λ=850 nm
TiO_2	93.2 nm	2.37
SiO_2	147.3 nm	1.45
TiO_2	92.490 nm	2.35
SiO_2	147.030 nm	1.45
TiO_2	88.938 nm	2.39
SiO_2	145.831 nm	1.45
TiO_2	92.405 nm	2.35
SiO_2	146.877 nm	1.45
TiO_2	87.556 nm	2.37
SiO_2	146.591 nm	1.45
TiO_2	90.8 nm	2.34
SiO_2	143.899 nm	1.45
TiO_2	89.6 nm	2.37
SiO_2	147 nm	1.45
TiO_2	101.430 nm	2.33
SiO_2 (Thin oxide layer)	1 nm	-
Si (Wafer)	1 mm	-

Table 4.2. Layer thickness and refractive indices of subsequent dielectric pairs at λ=850 nm measured by ellipsometry.

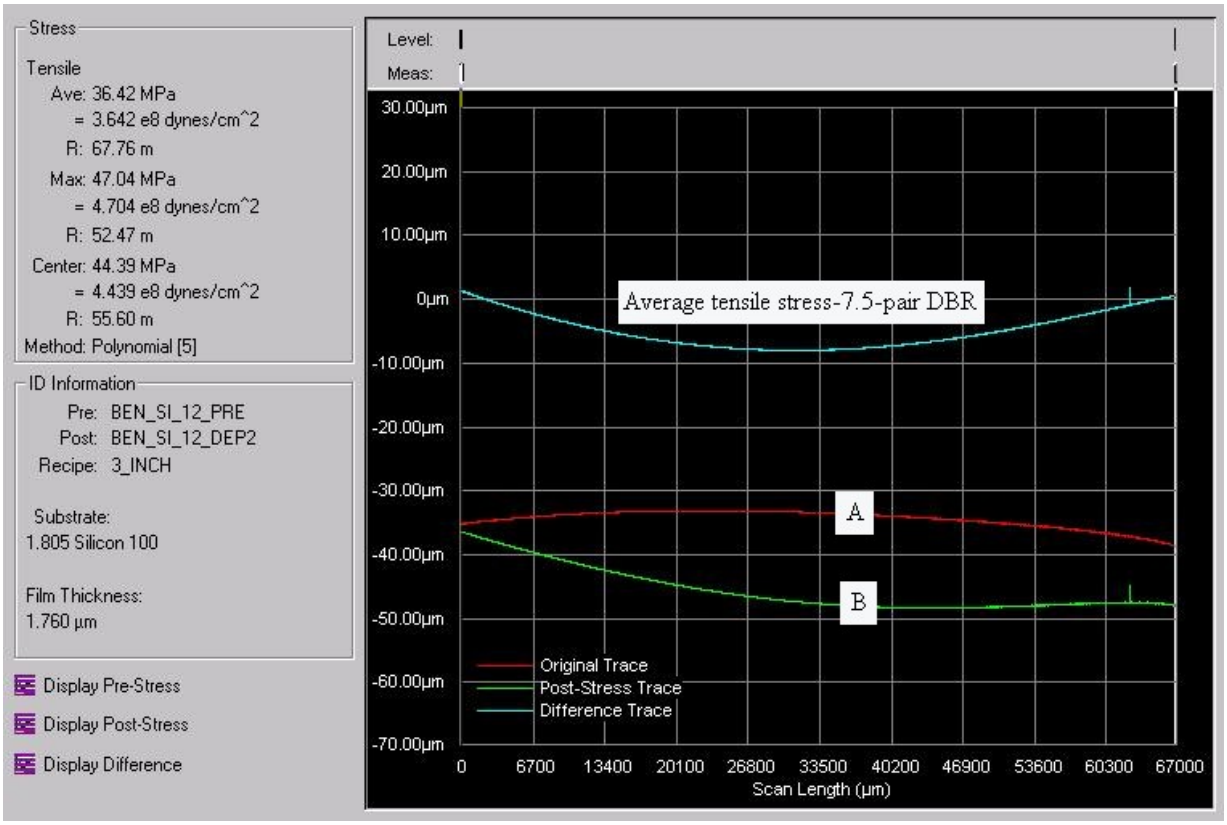


Figure 4.6. Average tensile stress of ~ +36 MPa for the 7.5-pair TiO_2/SiO_2 DBR. A- and B-labeled curves are the profiles of a 3" Si wafer before and after DBR deposition.

As an unchanging rule of science, with no exceptions for the current subjects of concern, the nature of each experiment is always mingled with unexpected challenges. The realization of this 7.5-pair DBR has not been as easy as it was described as well. Neglecting process delays due to technical problems of the FHR tool[5], the major challenge has been the film corrosion during dielectric sputtering. Excessive heat generated during the process along with surface ion bombardment of the photoresist half-spheres leads to a "disaster". The resist film burns severely and the structures swell. Optical Microscope pictures of some damaged structures are shown in figure 4.7.

[5] Sputtering tool from FHR Anlagenbau GmbH.

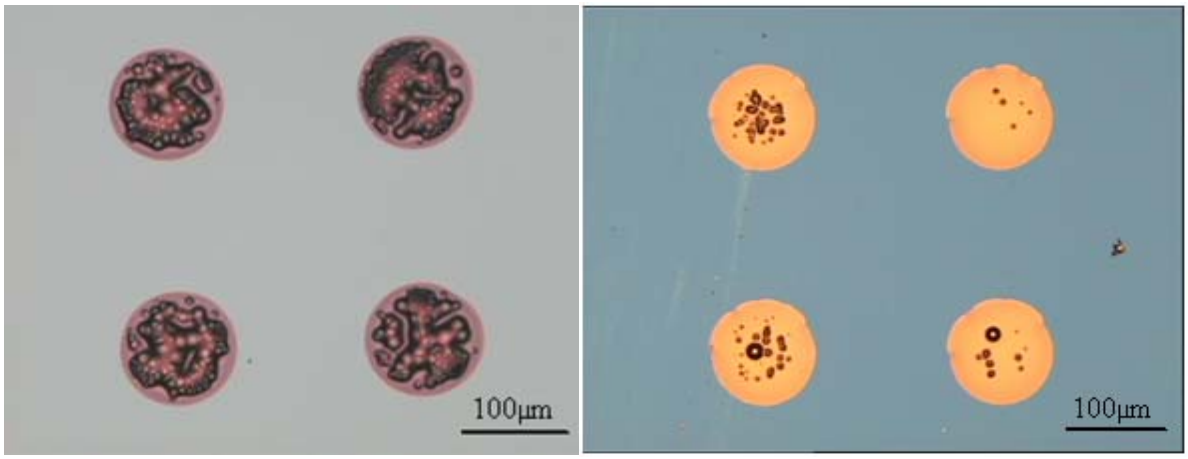


Figure 4.7. Microscope picture of photoresist film corrosion during dielectric sputtering.

Many efforts have been made in order to overcome this obstacle. Several hard baking recipes have been tested, sputtering time for each layer has been divided into shorter intervals with long pauses in between, and cooled substrate position of the FHR tool has been used to apply water cooling underneath the sample carrier. The carrier is unloaded after each deposition interval; the temperature of the carrier is monitored and microscope pictures are taken.

As indicated before, the most reliable post-bake recipe is a combination of UV irradiation for 2 min followed by closed cover hard bake at 100°C for 20 min. It is also important to note that the first deposition cycles are critical in the process and thus the sputtering time of these layers has been more conservative. A microscope picture of a successful dielectric deposition on photoresist half-spheres is shown in figure 4.8.

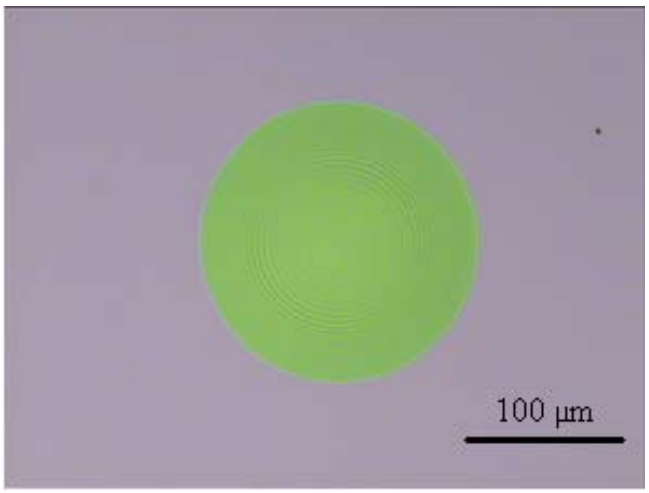


Figure 4.8. Microscope picture of a successful DBR deposition. Fringes denote the spherical shape of the structure.

DC and RF sputtering parameters and intervals for both TiO_2 and SiO_2 are depicted in tables 4.3 and 4.4 respectively.

TiO_2 DC Sputtering	DC Power	1 kW
	Ar Flow	40 sccm
	O_2 Flow	O_2=12 sccm (pre-cond.) O_2= 4 sccm (process)
	Pre-time	60 s
	Pressure	5e-3 mbar
	Sputter Time (intervals)	First layer: 60 s Successive layers: 2 min Total time per layer: ~ 7 min
	Pause Time	7 min

Table 4.3. DC sputtering parameters for TiO_2 layers.

SiO_2 RF Sputtering	RF Power	1 kW
	Ar Flow	40 sccm
	O_2 Flow	O_2= 15 sccm
	Pre-time	60 s
	Pressure	1.3e-2 mbar
	Sputter Time (intervals)	60 s Total time per layer: ~ 10 min
	Pause Time	3:30 min

Table 4.4. RF sputtering parameters for SiO_2 layers.

4.4 Nickel Evaporation

After the deposition of dielectric DBR mirrors, a thin metallic layer is evaporated on the surface of the structures which will serve as an etch mask and also the actuation network in subsequent MEMS processing steps. Nickel has been chosen as the metallic mask layer due to the proper adhesion between the Ni thin film and dielectric materials, high resistance to corrosion and oxidation, very good strength and durability at high temperatures and finally its low thermal and electrical conductivity which provides adequate resistance needed for the membrane actuation.

A Ni thickness of ~50 nm is evaporated under specific vacuum conditions using Lesker UHV e-beam evaporator tool. This Ni layer is evaporated at two different deposition rates of 2 Å/s and 1 Å/s and the sheet stress is measured afterwards. Stress tests reveal that evaporation at lower rates results in notably lower layer stress as well. Deposition at 1 Å/s rate shows a +362 MPa tensile layer stress which is almost less than one-half of the stress for 2 Å/s case (+757 MPa, tensile).

4.5 Surface Micromachining

Building layered mechanical structures on top of a substrate, such as a Si or GaAs wafer, utilizing a thin film material deposition process and removing unwanted parts during chemical etching is simply called surface micromachining. In contrast to bulk micromachining, there is no material removing of the underlying substrate, but the surface coating materials are patterned and engineered by lithography and etching techniques. Sacrificial or auxiliary layers are formed on the surface, giving support to the main structural material films and being etched away afterwards to bring about the final patterns. Wet and Dry chemical etch techniques are being used based on the requirements of different processing steps. Isotropic wet etching provides a high level of selectivity but a shortcoming is mask undercutting. Dry etch however is much more precise than wet etching but it requires complicated tools and parameter controlling procedures; besides the selectivity is worse. Two processing approaches are discussed in this section and the results are presented.

4.5.1 Actuation network and Inductively Coupled Plasma (ICP) etch

The evaporated Ni layer is shaped with MEMS-mirror and actuation patterns before the dry etching step. Two different processing approaches are examined which will be discussed in details in sections 4.5.2 and 4.5.3. The processing steps of the two methods are summarized below:

First Scheme (cf. figure 4.9):

- MEMS pattern is developed on the Ni layer.
- Samples undergo the wet etch and the Ni etch mask for MEMS dry etching is created.
- Actuation network is patterned on the processed Ni mask.
- Dielectric layer is dry-etched.
- Samples undergo the second wet etch step to form the actuation layer.
- Sacrificial layer and the photoresist on top of the actuation network are removed in the appropriate solvent and MEMS structures are released.

Second Scheme (cf. figure 4.10):

- Actuation pattern is developed on the Ni layer.
- Samples undergo the wet etch and the Ni actuation network is created.
- Samples are coated with a 6-µm-thick Megaposit™ SPR™220-3.0[6] positive photoresist and patterned with the MEMS mask.
- Dielectric layer is dry-etched.
- Sacrificial layer and the photoresist on top of the actuation network are removed in the appropriate solvent and MEMS structures are released.

4.5.2 First scheme

Samples are coated with HMDS and SPR™220-3.0 both at 3000^{rpm} for 30 sec and then are soft-baked at 115°C for 90 sec. Conventionally there has to be a frame exposure prior to pattern transfer, but in this case this step is skipped in the lithography process in order to protect spherical DBRs from contacting the photomask which will cause structure damages. After a pattern exposure for 17 sec in *soft contact* mode samples are developed in MF-24A[7] developer which is optimized for the highest resolutions and needs no dilution. Development time is 45 sec and samples are rinsed in water for another 45 sec afterwards.

[6] Megaposit™ SPR™220-3.0 from Rohm and Haas electronic materials.
[7] MF™-24A developer from Rohm and Haas electronic materials.

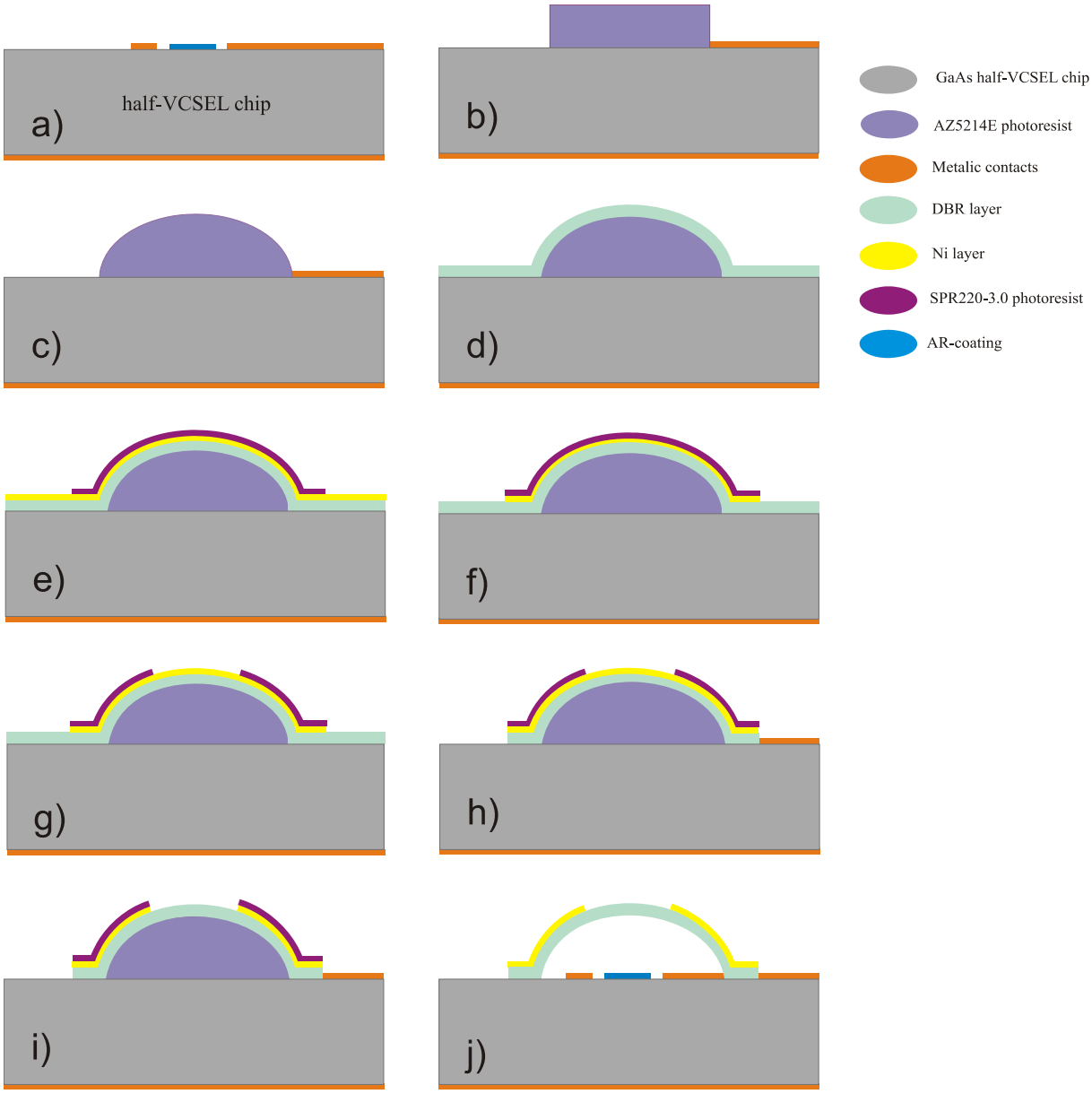


Figure 4.9 MEMS processing flow , first scheme. a) half-VCSEL chip b) photolithography to definr resist cylinders c) reflow d)dielectric deposition e)Ni evaporation and MEMS patterning f)Ni etch g) actuation network patterning h) dielectric dry etch i) Ni etch j) photoresist remove and critical point drying (CPD).

Wet etch

A Ni wet chemical etching step is applied to the samples after pattern development is finished. During the wet etching a series of chemical reactions occurs between the material on the surface and the chemical solutions, simply called etchants, which the samples are exposed to. The etch rate of the etchants differs from one material to another which is referred to as etching selectivity. In selective etching, etchants remove the target layer in a multilayer structure without damaging the other parts, meaning that unwanted parts of the surface Ni coating are being "eaten" by etchants and the resist mask and the parts underneath are left behind.

A nitric acid (HNO_3) and water (H_2O) solution is prepared with the ratio of (1:30 / 5 ml:150 ml) at 50°C and the samples are etched for ~ 2 min which indicates an etch rate of ~ 25 nm/min. As the etching solution is acidic the etch process is isotropic, which means the surface materials are struck from all directions and the etch rate is constant. A 1 min DIW rinsing is done afterwards to remove any remaining solutions from the substrate.

To create the actuation network afterwards, the etched sample has to be patterned again with the actuation mask. The patterned Ni-layer is next used as an etch mask in a dry etching process to form the MEMS structures.

Inductively Coupled Plasma (ICP) etch

In dry etching, chemicals are applied to the wafers in the form of ionized gas plasma. Similar to sputtering, the surface bombardment with high-energy ions ejects the atoms from the surface material and etches the pattern. Reactive gases are used together with a noble gas, typically argon, to create ionized plasma. Plasma dry etching is a combination of chemical and physical etching which removes the surface material in anisotropic (accelerated plasma ions hitting the wafer surface) and isotropic (reactive radicals striking the surface) processes providing sharp sidewalls without mask undercutting and with high aspect ratios. In plasma etching high etch rates can be provided due to high reactive ion densities ($\sim 10^{12}$ Cm^{-3}) generated inside the process chamber [30]. To generate the plasma two separate RF sources, at the frequency of 13.56 MHz, are introduced to the bottom electrode and the upper ceramic part of the chamber. The upper electromagnetic field is applied to the plasma from a coil surrounding the ceramic chamber and couples to the plasma inductively. The magnetic confinement of the plasma by the coil results in more electron-ion collisions thus producing dense ionized plasma in the chamber. Using two separate RF power generators provides a good control over plasma density and the ion bombardment of the substrate at the same time which ultimately leads to a good control over the etch rate and selectivity. The ICP/RIE plasmalab system 100 tool from Oxford Instruments is used.

The tool is mainly dedicated for etching III-V semiconductors and dielectrics and has two process chambers and a load lock for sample transfer. Samples are loaded on a sapphire plate and transferred to the process chamber 2 which is used for fluoride-based processes. Tool specifications and the recipe with which the samples are etched can be found in tables 4.5 and 4.6 respectively.

Tool Specifications	Electrode RF power	0-500 W
	ICP RF power	Ch1:0-2000 W Ch2:0-3000 W
	Dc bias	0-1000 V
	Base pressure	$3x10^{-7}$ Torr
	Process pressure	1-99 mTorr
	Gases Chamber1	Cl_2, $SiCl_4$, CH_4, H_2, Ar, O_2
	Gases Chamber2	NF_3, CF_4, CHF_3, O_2, H_2, Ar, N_2O, N_2, SiH_4
	Wafer Size	100 mm

Table 4.5. ICP/RIE plasmalab system 100 tool specifications.

Process Parameters	Argon	50 sccm
	NF3	80 sccm
	RF power	25 W
	Etch time – 6.5-pair DBR	66 min
	Etch time – 7.5-pair DBR	78 min

Table 4.6. Dry etch process parameters.

MEMS fabrication process continues with another Ni wet etch step to wash the Ni mask away, leaving only the actuation pattern unetched. Etchants and process parameters are the same as previous wet etch process. Exposing the samples to the etchants shows an unexpected and strange behavior of the surface material. Those areas of the Ni mask which were not covered by the resist have become completely resistant to etchants and could not be removed even with relatively long etch times (8 min in three steps), whereas, the actuation network is lifted up and washed away in the solution.

During the quite long DBR etch process photoresist is burned and the resist mask is not capable of protecting the underlying actuation pattern any longer. This might be the explanation for the actuation pattern lift off, but the reason for the uncovered parts becoming etch-resistant could be described later when some ICP etch tests were done on dummies. An identical Ni layer was evaporated on dummy samples and an ICP etch with the same recipe and for 30 min was introduced. The Ni layer behaved the same and could not be etched in the acid/water solution. As a first guess this was interpreted as the effect of the NF_3 reactive gas on the Ni during the long ICP etch, forming a stubborn fluoride layer (NiF_2) on the top which resisted the etchants. To solve this problem, an argon plasma cleaning step was initiated with different power, gas flow and time parameters. Process parameters and the results of the experiments can be seen in table 4.7. By adding this Ar plasma cleaning step to ICP etch the problem of wet etching is solved, but as it is obvious in table 4.7 there is a significant change in the etching time which is because the Ni layer itself is also being physically etched in the argon plasma. This thickness decrease, however, will cause the actuation Ni pattern to be totally damaged and washed away when samples are exposed to photoresist removers to remove the underlying sacrificial layer. Consequently, this problem results in setting this approach aside.

Reactive Etch Time for all Samples : 30 min	RF Power	Ar Flow	Cleaning Time	Wet Etch Time
Sample 1	100 W	20 sccm	5 min	35 s
Sample 2	100 W	20 sccm	2 min	40 s
Sample 3	25 W	20 sccm	1 min	Could not be etched
Sample 4	100 W	20 sccm	1 min	1:15 min

Table 4.7. Process parameters of the experiment with Ni wet etch rate.

4.5.3 Second scheme

In the second approach identical processing steps are employed to accomplish standing-MEMS micro-mirrors. The only difference is in the formation of protective masks for the ICP etch, see figure 4.10. Samples are spin-coated with HMDS and SPR™220-3.0 at 3000^{rpm} for 30 sec and then are soft-baked at 115°C for 90 sec. The actuation structure is patterned and developed on the Ni layer with the same process parameters as explained earlier. The distinctive part of this method is to use a thick photoresist layer on top, as an etch mask, during the dry etching. After removing the actuation photoresist pattern in acetone, samples

are coated with HMDS promoter and SPR™220-3.0 at 1600^{rpm} for 30 sec. The approximate thickness of the resist at this speed is ~ 6 µm which provides a safe margin to selectively etch the 7.5-pair, 1.76-µm-thick dielectric DBRs.

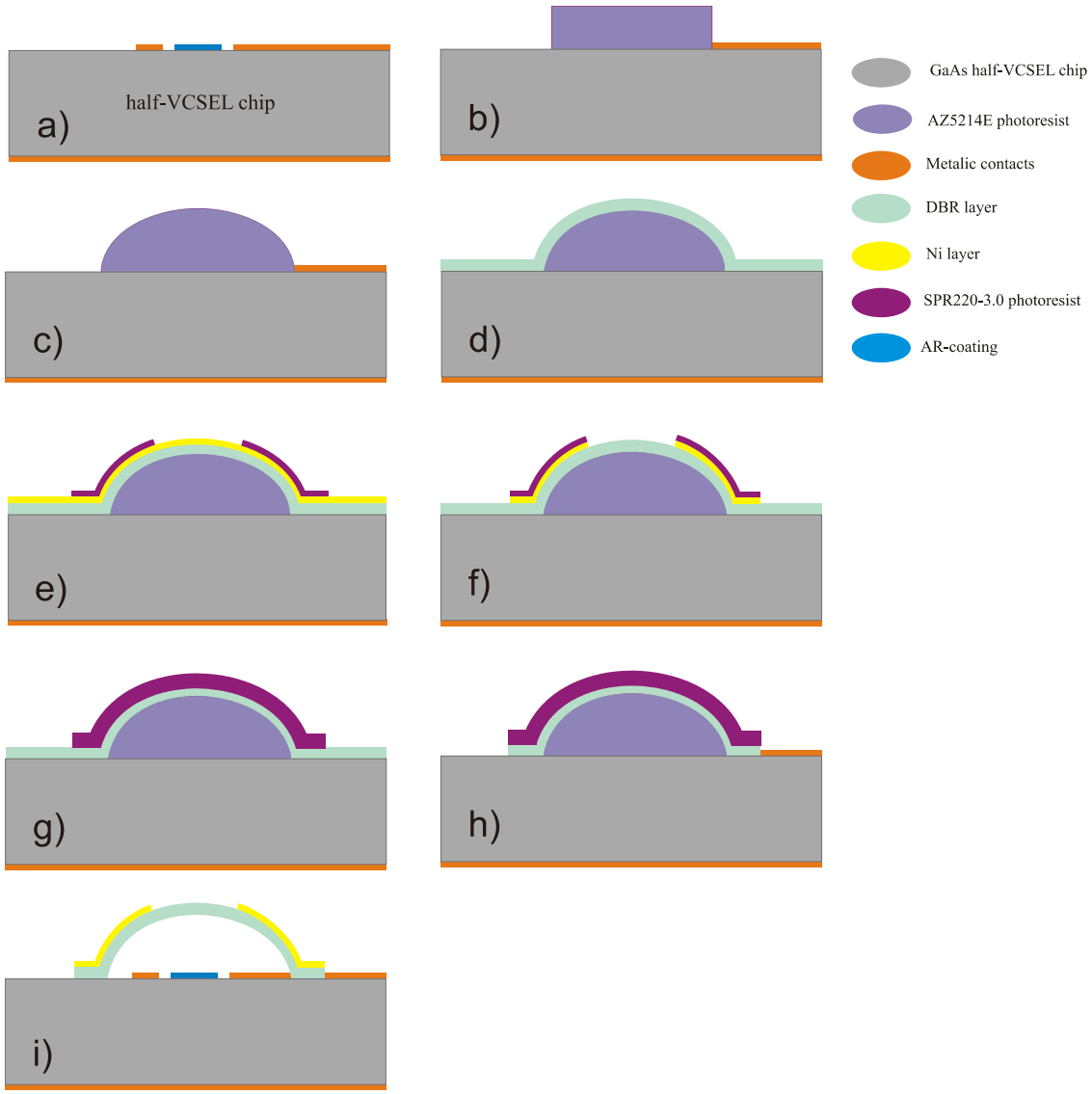


Figure 4.10. MEMS processing flow, second scheme. a) half-VCSEL chip b) photolithography to define resist cylinders c) reflow d) dielectric deposition e) Ni evaporation and actuation network patterning f) Ni etch g) 6 µm-thick photoresist etch mask h) dielectric dry etch i) photoresist remove and critical point drying (CPD).

After curing the resist film at 115°C for 90 sec an accurate mask alignment is done and the MEMS pattern is written on the thick resist film in *soft contact* mode with exposure and development times of 25 and 60 sec respectively. A closed-cover hard bake at 115°C for 5 min is applied afterwards to increase the resist durability in plasma etching. Samples are then etched with the same recipe and the total etch time is divided into shorter steps to control the photoresist mask and preserve it from burning. Initially, a 35 min ICP etch is applied and samples are unloaded and checked afterwards. As the resist mask is still in a good shape to protect the structures, etching process continues. The same procedure is repeated for even shorter etching times and after 25 min the resist mask becomes too vulnerable and cannot function properly anymore. Samples are taken out and the burned resist is removed in heated acetone. Another lithography step is applied with the parameters of the first mask and process continues for 18 min until the DBRs are fully etched.

4.6 Critical Point Drying (CPD)

After the dielectric DBRs are etched and the desired structures are formed, the underlying sacrificial layer is to be removed to release the MEMS membranes. Chemical removers are used for this purpose which will remove both the top burned resist and the sacrificial photoresist layer. One of the main challenges in this step is to remove the photoresist underneath the structures. During the long MEMS fabrication process photoresist half-spheres go through a lot of different fabrication steps. Especially during the quite long sputtering process the resist spheres become more adhesive and sticky to the substrate. In the subsequent DBR etching, photoresist is severely burned because of the excessive heat generated in the chamber and becomes difficult to remove. A photoresist removing step is applied using a powerful Posistrip[8] positive photoresist remover. Samples are kept in 70°C heated Posistrip for 10 min and are then transferred to an acetone container which will be kept in for at least 24 hrs. One of the most destructive problems in MEMS fabrication is stiction. Stiction occurs when the released structure turns into a very close proximity with the other surface. In such a case, the structure becomes totally or partially pulled into the substrate, making the devices completely damaged and useless. Removing the underlying sacrificial layer, typically by means of etchants or solvents, is the crucial point for stiction to happen. When the structures are N_2-dried after removing the sacrificial layer, interfacial capillary forces arise mainly due to the surface tension. These adhesion forces between the stripping liquid and the surface of the structures can result in stiction. Efforts have been dedicated to find techniques which will overcome the challenge. Supercritical CO_2 drying or critical point drying (CPD) is one the most successful methods to relieve this surface tension and therefore help such detached devices to survive the process [33].

[8] EKC830™ Posistrip from EKC technology.

Using liquid CO_2 is very handy and safe, besides it has a relatively low critical temperature and pressure and no toxic material is used in the process. As depicted in figure 4.11 it is necessary to pass the boundary of liquid and gas phase when the material vaporizes which brings about the surface tension and makes the structures to collapse and break apart. A way to avoid this boundary crossing is moving along the liquid-gas interface by increasing the temperature and pressure of the liquid to a certain point which is called the critical point and passing the supercritical region instead. For CO_2 this critical point can be reached at 31°C and 73 bars.

After the sacrificial layer removing in Posistrip and acetone, structures are transferred into the chamber of the CPD tool which is filled with acetone. Liquid CO_2 is then mixed with the solvent at ~ 10°C during a dilution step (figure 4.11, point A). After CO_2 replaces the solvent inside the chamber, it is heated up to reach its critical temperature and pressure point. In this supercritical region the liquid and gaseous phases are not distinguishable anymore (figure 4.11, point B). The temperature inside the chamber is increased even beyond the critical point which helps to the evacuation of gaseous CO_2 (figure 4.11, point C). Samples are then taken out fully released and completely dried with no stiction to the substrate.

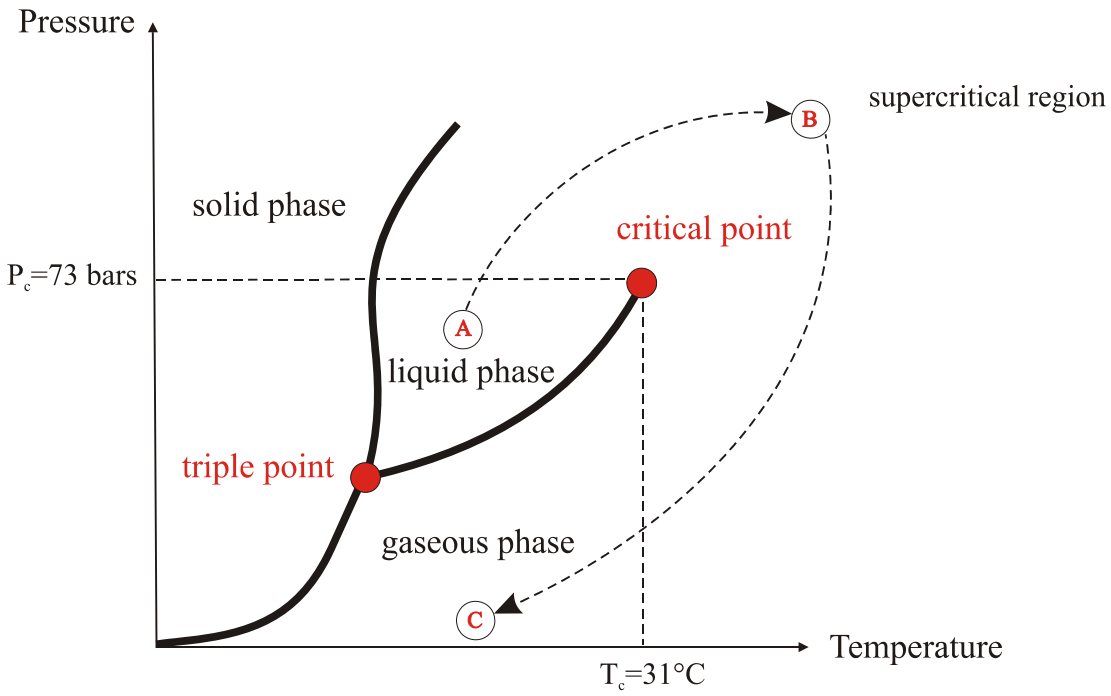


Figure 4.11. Pressure-temperature phase diagram and the critical point of liquid CO_2. A, B and C indicate the different CPD process steps.

4.7 Integration on Half-VCSEL

The final step in fabrication of tunable MEMS-VCSELs is to join the fabricated half-VCSEL chips with suspended micro-mirrors. It has been described in the introduction section that instead of two-chip fabrication approaches, this project suggests a hybrid integration technology, which eliminates the requirement of manual assembly or wafer bonding techniques.

4.7.1 Reflow on uneven surfaces

Integrated one-chip technology requires direct fabrication of micro-mirrors on the processed half-VCSEL chip. Therefore, both lithography and reflow process are done on processed chips with an uneven topography. Smoothness of reflowed resist should not be affected though, as any surface roughness will result in non-spherical MEMS mirrors and prevent appropriate device performance. To avoid such problems photoresist pillars have to mask the underlying pattern of the contact rings and the AR coating of the half-VCSEL. Experiments on dummies show that mesa diameter and height of the contact rings are two most important aspects of half-VCSEL chips to be considered in having smooth and uniform mirror surfaces. As mentioned earlier the self-alignment feature of the reflow process on the mesas makes it become well-controlled and perfectly centered over the oxide aperture. Reflow stops at the edges of the mesa and prevents the resist structure from expanding more than desired ratios and thus satisfies both height and width requirements. Moreover, considering the height of the underlying contact rings, it will result in a smooth and perfectly curved structure. An optical-microscope image of reflow on 150-nm-thick contact rings is shown in figure 4.12.

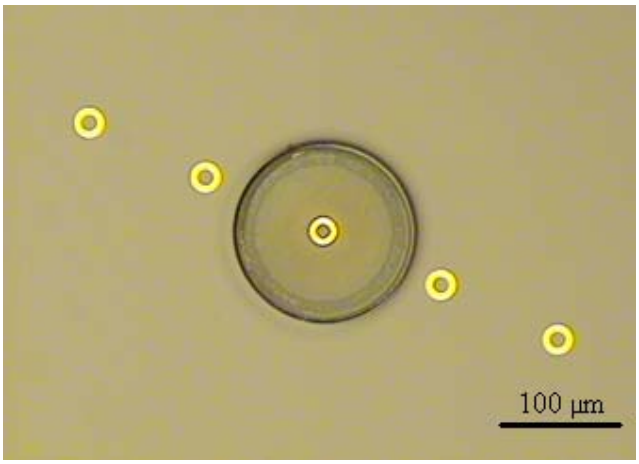


Figure 4.12. Optical-microscope picture of reflowed photoresist on 150-nm-thick contact rings. Resist spheres have a smooth surface and the pattern underneath is completely masked (cf. figure 4.13d).

Figure 4.13 also shows the height profile of some structures with different parameters for the mesa size and the thickness of contact rings. Reduced height of the contact rings from 300 nm to 150 nm and reflow stop at the borders of mesas are the key to form desired preliminary shapes for the MEMS mirrors.

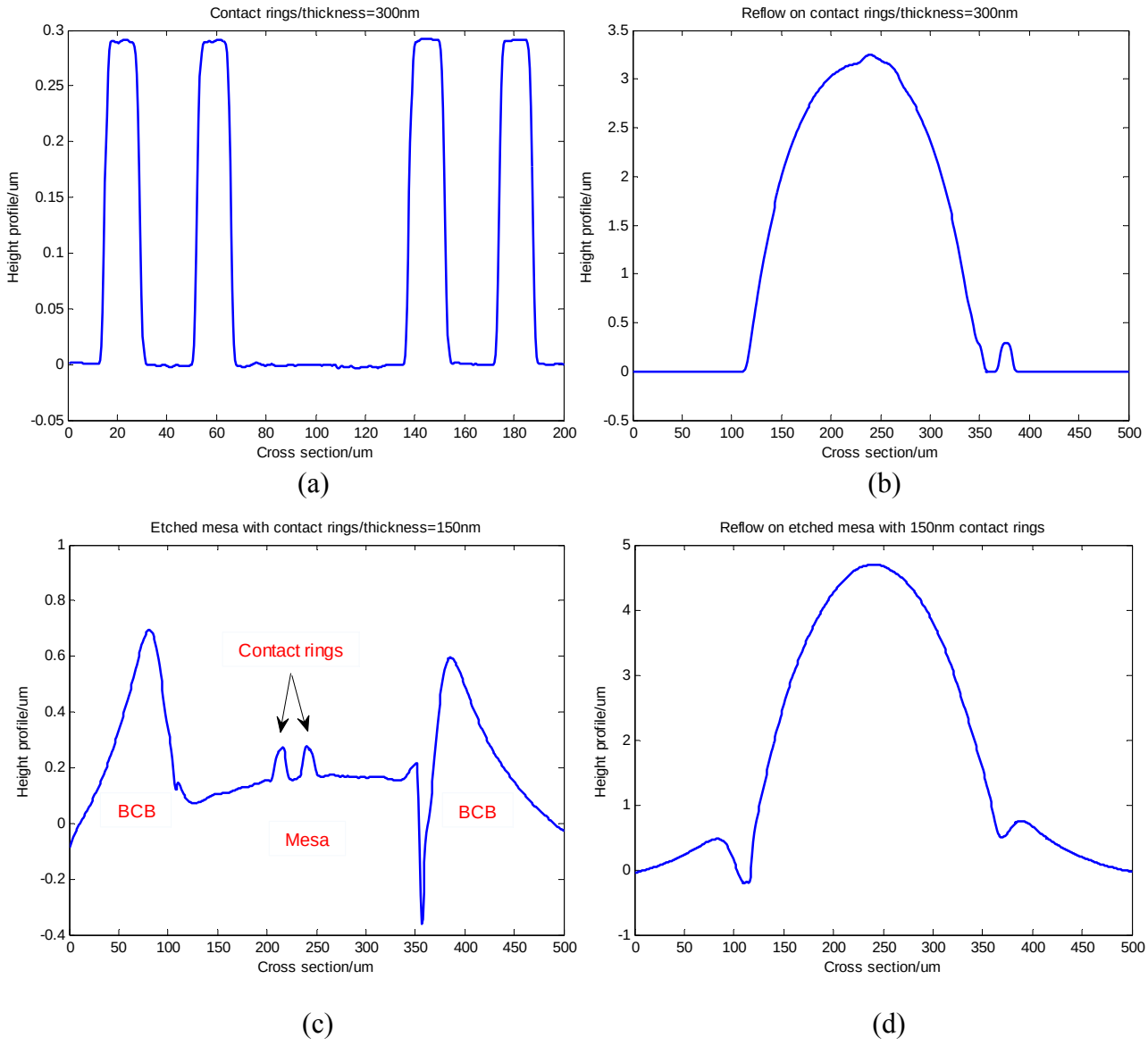


Figure 4.13. Surface topography of a) test contact rings (thickness=300 nm), b) heated acetone reflow on 300-nm thick contact rings, c) etched-mesa structure with 150-nm thick contact rings prepared for the half-VCSEL integration, d) heated acetone reflow on the etched-mesa structure with the resist masking the underlying topography and stopped at the mesa edges.

4.7.2 Final devices

The second MEMS process method from Sec 3.3.5 is applied and the final structures are created. Samples are left in heated acetone for ~24 hrs to dissolve the sacrificial layer and then processed in critical point dryer. Light-microscope and SEM pictures of a complete device are shown in figure 4.14.

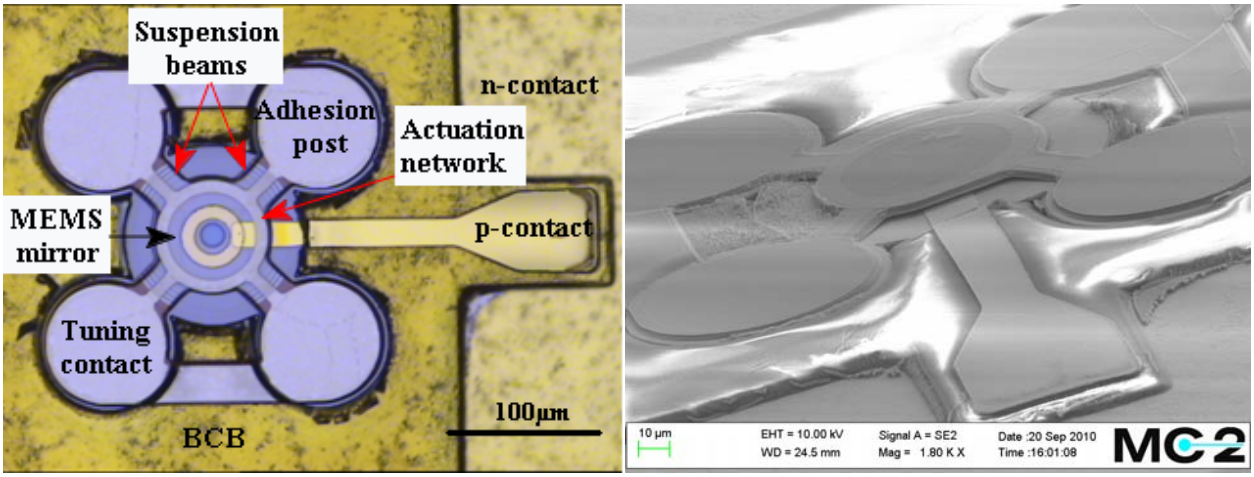


Figure 4.14. Microscope image (left) and SEM (right) picture of the hybrid MEMS-VCSEL with 120-µm mesa and a footprint of 230 µm× 370 µm.

5 Characterization of Final Devices

5.1 Spherical Mirrors

The height profile of the reflowed resist on a 120-µm mesa with fitting is shown in figure 5.1. *RoC* of the structures is obtained from spherical fitting to be ~ 420 µm which is different from the calculations of sec.3.3 assuming the beam diameter of 12 µm. From equation (2.4) the beam radius of the fundamental Gaussian mode is calculated $w_0 = 3.25$ µm which gives a diameter of 6.5 µm. Considering a 15 µm oxide aperture, this mismatch between the mode size and the aperture also allows for the higher order transverse modes to oscillate inside the laser cavity. (cf. figure 5.8).

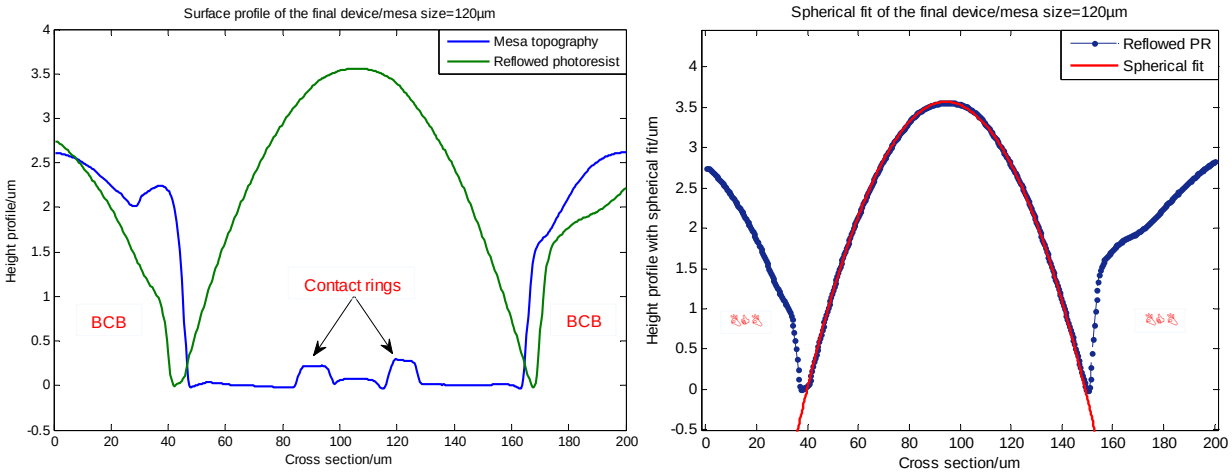


Figure 5.1. Height profile of the final integrated MEMS-VCSEL device with mesa size of 120 µm (left) and spherical- fit (right) with *RoC*=420 µm.

5.2 I-V Characteristics of Actuation Network

Current-voltage (I-V) characteristics of the actuation network is found by using a parameter analyzer which injects a known direct current through the tuning contacts and extracts the resistance of the actuation layer. Basis of the measurement is the Ohm's law ($R = \frac{V}{I}$) and resistance is computed by dividing the voltage drop by the injected current. Keithley 4200-SCS is the parameter analyzer tool used for such purpose. The tool has four Source Measure Units and is connected to a KarlSuss PM5 probe station with six probe heads. Two probes are brought into contact with the tuning pattern and the resistance of the thin Ni layer is measured. Straight line and zigzag patterns from the test samples are both examined at the sourced current of 10 mA and the results are depicted in figure 5.2. The resistance of the zigzag pattern (~175 Ω) is higher than the straight line (~133 Ω). From the DC resistance equation ($R = \rho \frac{l}{A}$), with l, A and ρ being the length, cross-sectional area and the specific resistance of nickel (ρ_{Ni}=0.069 μΩ-m) respectively, the resistance values for both straight line and zigzag patterns are calculated. R~100 Ω for the straight line and R~180 Ω for the zigzag network are in a fair agreement with the measurements. 30 mA is the upper limit for the injected current before the actuation layer is damaged. The layout of the final MEMS-VCSEL device is slightly different from the initial test samples and only the straight line pattern is employed. See figure 4.14.

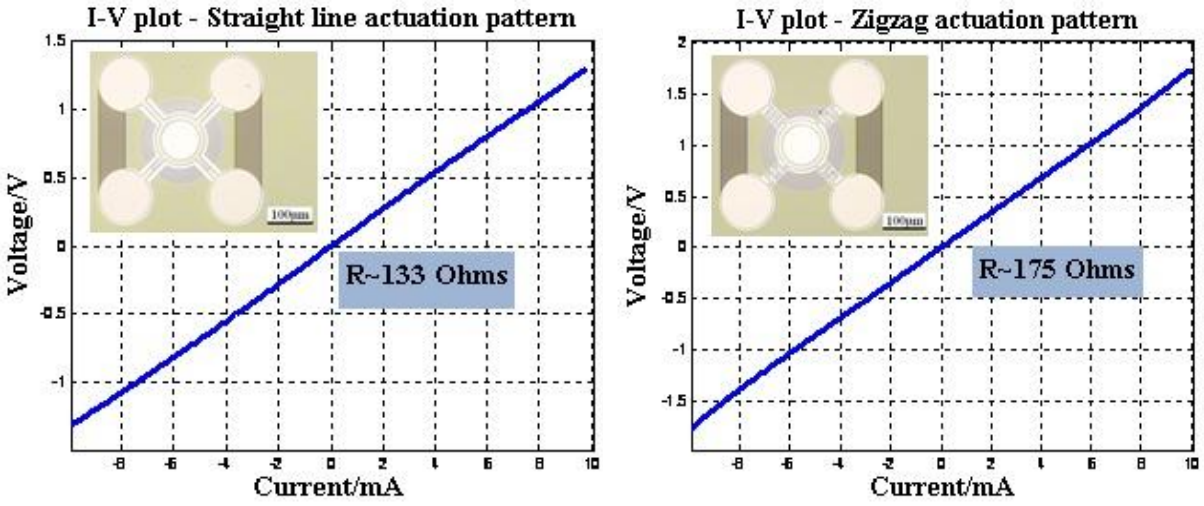


Figure 5.2. Resistance of the actuation network (test devices) for the straight line pattern (left) with R=133 Ω and zigzag pattern (right) with R=175 Ω. Insets are microscope pictures of the two actuation patterns (cf. figure 3.2).

5.3 DBR Characterization

A plane TiO_2/SiO_2 DBR mirror with 6.5 pairs deposited on a glass substrate and serving as the top mirror of pre-fabricated half-VCSEL chips is used to examine the optical characteristics of micro-mirrors. This plane mirror is processed together with integrated curved microstructures so all the fabrication parameters and process conditions are the same. MATLAB simulation results from sec.3.3 together with measured[9] reflectivity spectrum of the plane mirror are shown in figure 5.3. Measured spectrum shows the maximum reflectivity at $\lambda = 850\,nm$ with a full width at half-maximum (FWHM) bandwidth of ~320 nm confirming a close agreement with simulation results.

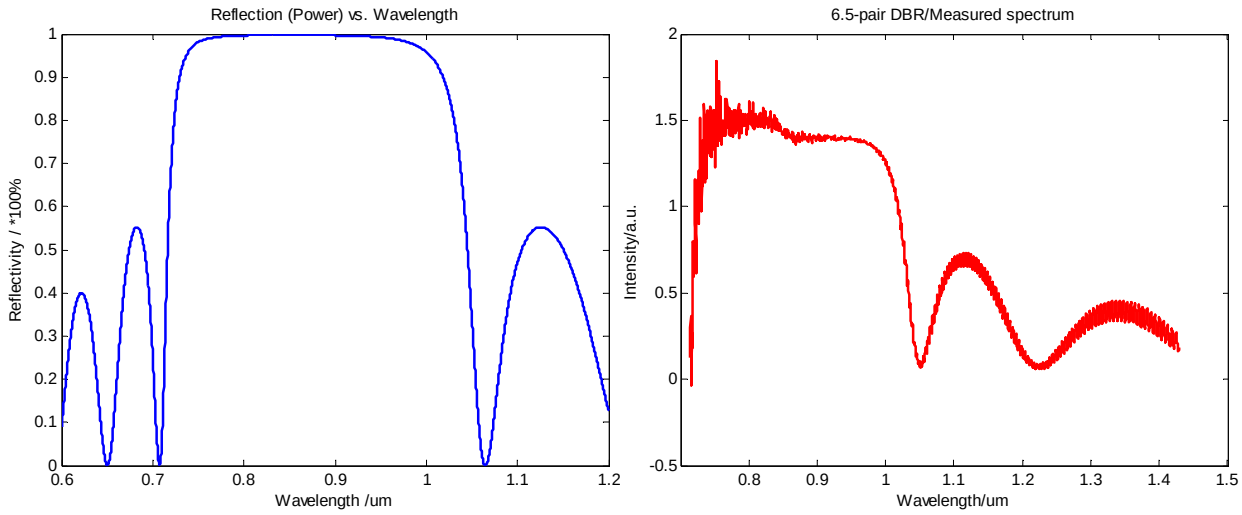


Figure 5.3. Simulated (left) vs. measured (right) spectrum of the 6.5-pair TiO_2/SiO_2 DBR with reflectivity of 99.8% at λ=850 nm and bandwidth of ~320 nm.

[9] Measurments done by Christian Grasse at the Walter Schottky institute of the Technische Universität München (TUM).

The flat mirror is manually mounted and fixed with adjusting-needles on a half-VCSEL chip fabricated with process parameters found in [27]. The laser diode is biased at room temperature and the output beam is coupled to a multimode optical fiber. After mirror adjustments lasing starts and the output spectrum is recorded in optical spectrum analyzer (OSA). OSA trace of the device (cf. figure 5.4) shows lasing at central wavelength around 852 nm.

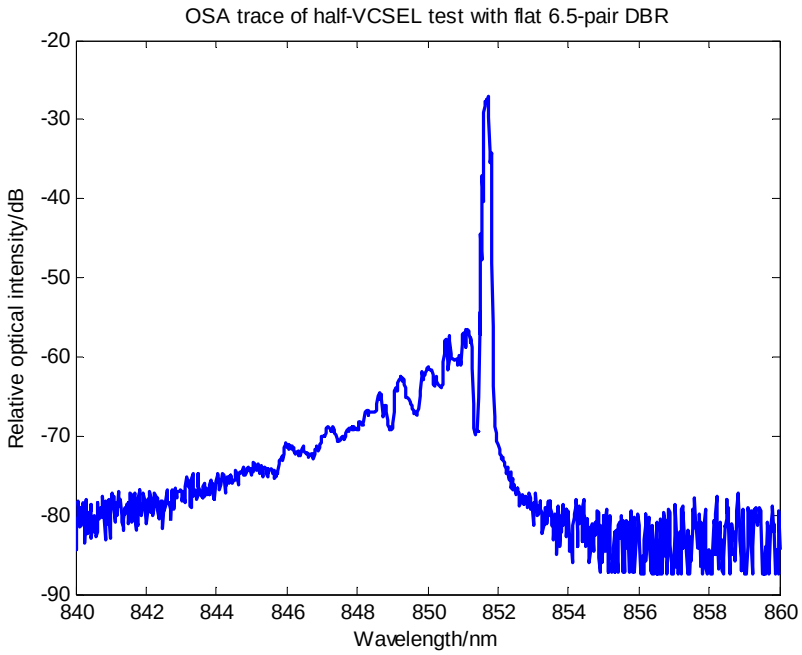


Figure 5.4. OSA trace of the half-VCSEL with the flat top DBR (6.5 pairs).

Although the flat 6.5-pair DBR test is successful, another dielectric pair is added to the DBR reflector to achieve a lower threshold gain in the final integrated device. Simulated spectrum of this 7.5-pair reflector is depicted in figure 5.5 showing a very high reflectivity of 99.9% with a bandwidth of 320 nm. An SEM image of the dielectric micro-mirror with 7.5 TiO_2/SiO_2 pairs is also illustrated in figure 5.6.

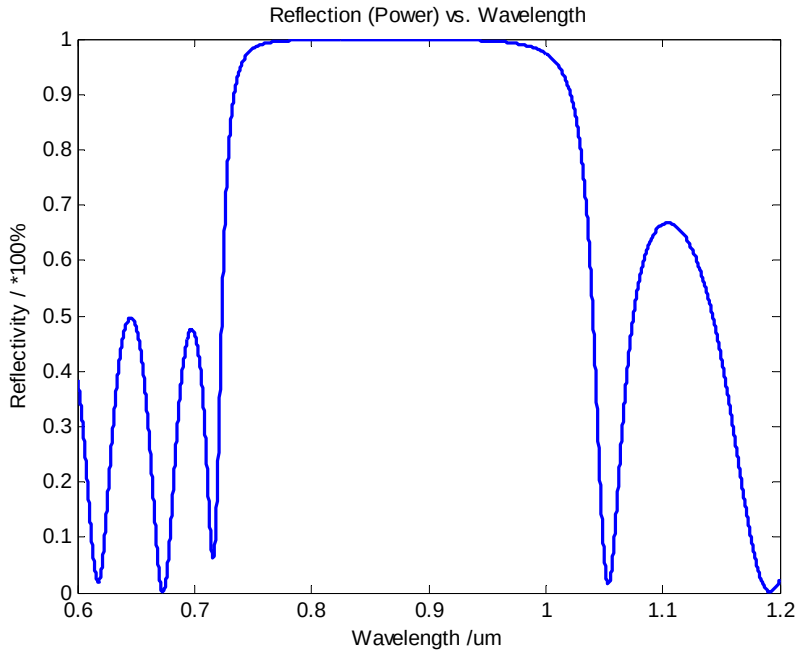


Figure 5.5. Simulated reflectivity spectrum for the 7.5-pair TiO_2/SiO_2 DBR with characteristics from table 4.2. DBRs have the maximum reflectivity of 99.9% at λ=850 nm and the FWHM bandwidth of 320 nm.

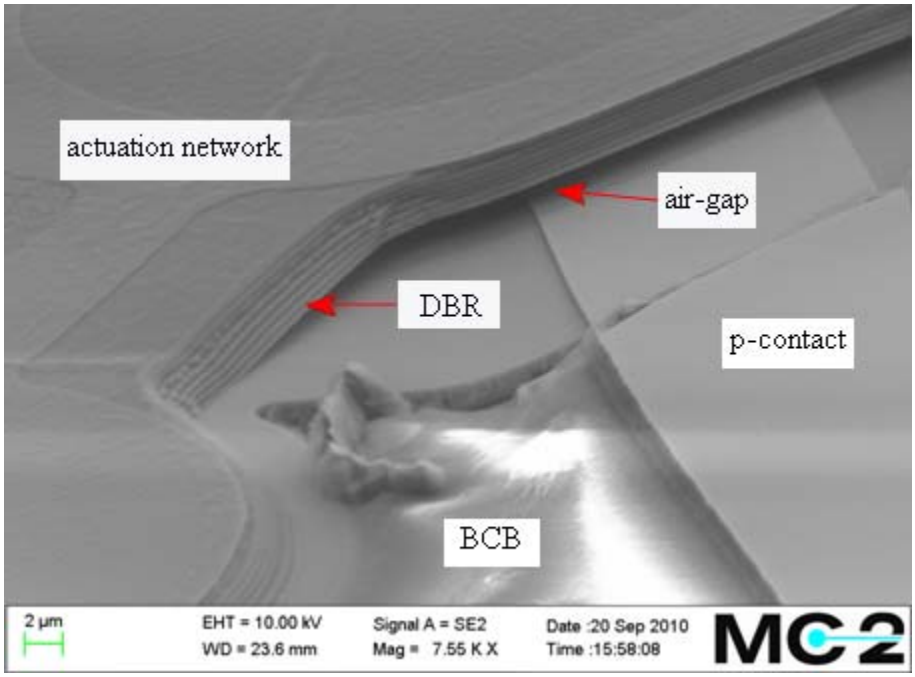


Figure 5.6. SEM image of the 7.5-pair TiO_2/SiO_2 DBR.

5.4 LIV Characteristics and Emission Spectra of MEMS-VCSELs

An electric drive circuit is set up to inject both driving and actuation currents to the devices. The sample is placed on a chuck for test and a multi-mode optical fiber is fixed over the sample in order to capture lasing from the surface. Devices are tested in continuous wave (CW) mode of operation at room temperature. The laser is biased by connecting the current probe to the transmission line of the device. Current is increased gradually and the fiber-coupled output power is monitored. A relatively high threshold current ~6 mA is observed which can be interpreted with the high absorption losses in 6 current spreading layers and the active region with 5 quantum wells. Figure 5.7 shows the optical output power and the voltage drop vs. input current (*L-I-V* curve). The emission spectra of the tunable VCSEL for the laser current of (I_L=10 mA) and tuning current of ($0 \leq I_{MEMS} \leq 18\,mA$) can be seen in figure 5.8. A voltage drop of 2.7 V corresponds to a current of 20 mA with maximum emitted output power of 1.7 mW. The device has a tuning range of ~12 nm with I_{MEMS}=18 mA. The laser shows a low differential resistance ~50 Ω. From the small signal analysis the parasitic capacitance of the 120-µm-wide mesa is found to be around10 pF which results in a 3dB cut-off frequency ~400 MHz.

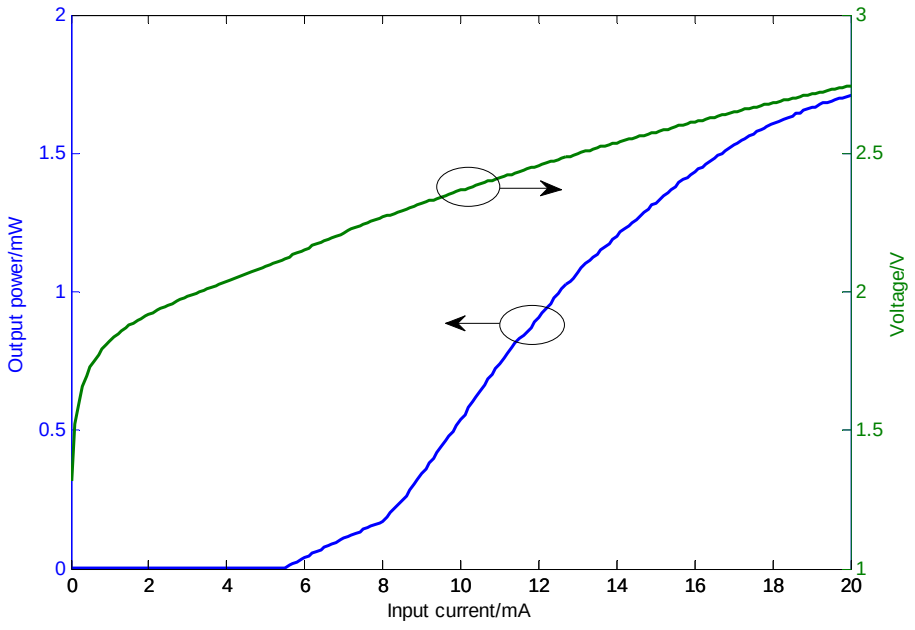


Figure 5.7. Light-current-voltage (*LIV*) graph of the MEMS-VCSEL with I_{th}=6 mA and maximum optical output power of *P*=1.7 mW.

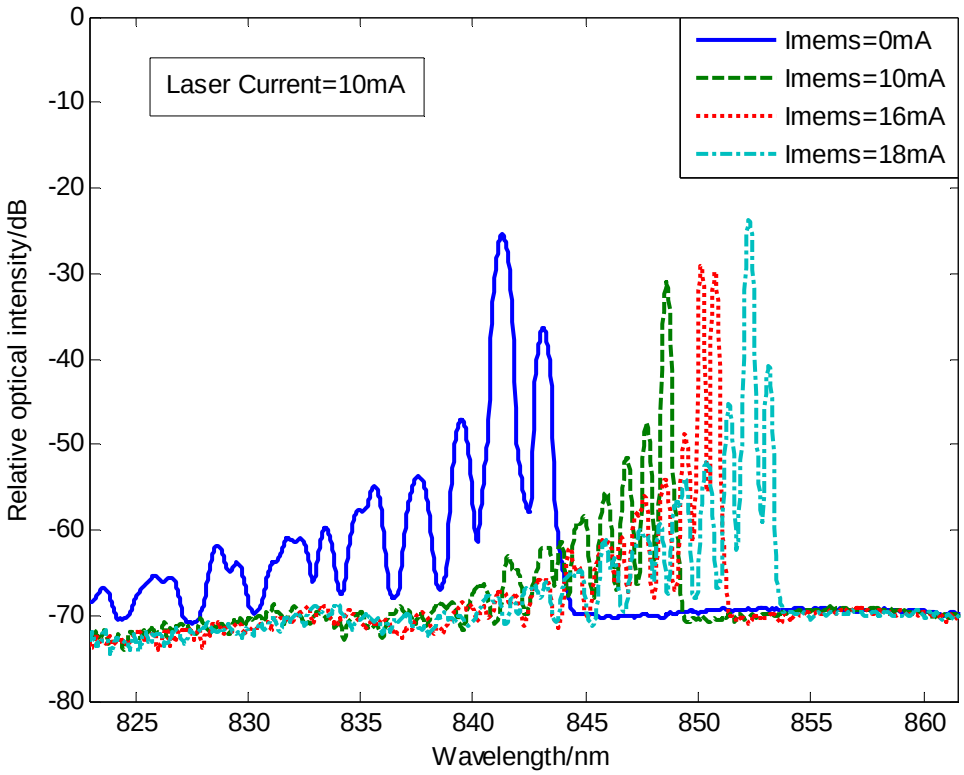


Figure 5.8. Emission spectra of the laser with I_L=10 mA and different MEMS tuning currents ($0 \leq I_{MEMS} \leq 18\,mA$).

6 Conclusions and Outlook

A simple and straightforward method for fabrication of single-chip tunable MEMS-VCSELs devoted for reconfigurable optical interconnects was represented in this thesis work. The MEMS technology was developed on a GaAs substrate and the devices were designed to operate in the near-infrared regime. The fabrication procedure is nevertheless independent of the gain material and could be transferred to any wavelength of interest. The project suggested a hybrid integration of electro-thermally actuated spherical micro-mirrors with half-VCSEL chips in a one-chip concept. AZ5214E photoresist sacrificial layer was used to define the spherical shape of the mirrors and TiO_2/SiO_2 pairs were deposited to form the DBR structure. The final device had a footprint of 230 μm × 370 μm and consisted of a 7.5-pair TiO_2/SiO_2 DBR, integrated on a half-VCSEL chip with the mesa size of 120 μm. The self-alignment feature of the photoresist pillars during the reflow process was an asset which relieved the very-accurate lithography requirements. The post backing process of the photoresist before thin film deposition was found to be one of the most important and critical steps of the fabrication process. Curing the reflowed structures with UV light for 2 min followed by a closed-cover hard bake at 100°C for 20 min turned out to be the best recipe to increase the durability of the photoresist film during the dielectric sputtering. Moreover, short sputtering steps and relatively long pauses were applied to minimize the risk of film corrosion. Critical point drying (CPD) was also a significant step to remove the sacrificial layer and release the freely-standing structures which worked successfully.

Spectral measurements of the DBR with 6.5 pairs corresponding to a reflectivity of 99.8% showed a central emission wavelength of 850 nm with a FWHM bandwidth of 320 nm which is in a good agreement with the simulation results. 7.5-pair DBRs had a reflectivity around 99.9%. Final MEMS-VCSELs showed a relatively high threshold current of 6 mA and were transverse multi-mode. The *RoC* of the micro-mirrors found to be ~420 μm which with a 15-μm-wide oxide aperture allowed for up to 5 side modes to oscillate inside the laser cavity. Also the maximum tuning range of the devices was ~12 nm with I_{MEMS}=18 mA and I_{Laser}=10 mA. A relatively low 3dB cut-off frequency of 400 MHz was observed due to a 10pF parasitic capacitance of the mesa platform limiting the VCSEL's high-speed operation at high modulation rates.

It is believed that single mode operation can be achieved by matching the size of the oxide aperture to the fundamental mode diameter or by repeating the reflow process on larger diameter mesas which results in spherical shapes with larger *RoC* and ensures single mode lasing. However, the larger diameter of the mesa platform will result in devices with even bigger parasitics. Therefore, it is required to investigate some new ideas to enhance the modulation response of the tunable VCSELs while maintaining the single mode operation.

One suggestion could be the reconsideration of 1165 remover reflow process on smaller mesa diameters which can provide a larger radius of curvature due to the flat surface of the reflowed resist structures (cf. figure 4.5).

In the fabrication process of DBR structures, amorphous silicon (α-Si) and silicon dioxide (SiO_2) dielectric materials have also been considered. Si/SiO_2 pairs are interesting alternatives due to the higher refractive index contrast which gives rise to the DBR structure of the same reflectivity but with less number of dielectric pairs (3.5 pairs). This is a noticeable improvement for the time-consuming DBR sputtering process which can save a lot of time and effort. Due to the time limitations, just a few numbers of experiments with Si/SiO_2 pairs have been done indicating the requirement of looking into adjusted post-bake and sputtering parameters.

Wavelength tuning process of the MEMS device is also another area for further improvements. Going through a more flexible design with longer suspension beams, employing the zigzag pattern instead of the straight line for the actuation network and studying electrostatic actuation could be some potential thoughts to get wider wavelength tuning ranges.

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Appendix A

MEMS Process Plan (integration on half-VCSEL)

1. Photolithography: defining photoresist cylinders

Tool: Mask aligner KS MJB3-UV 400
Photoresist: AZ5214E
Spin rate: 60 s at 1500 rpm (thickness ~2.5 μm)
-Remove edge resist droplets with Teflon stick
Soft bake: hot plate-60 s at 100 °C
Frame exposure: 80 s at soft contact mode
Develop: AZ351B:H_2O (1:4): 45 s, rinse in DIW: 45 s
Pattern exposure: 15 s at contact mode (mask: Reflow)
Develop: AZ351B:H_2O (1:4): 45 s, rinse in DIW: 45 s
Ash tool: Plasma strip – Tepla 300PC, recipe No.4

2. Reflow: forming photoresist half-spheres

-Heated acetone (50°C), 3 min, closed container
-Blow gently with Nitrogen

3. Post bake:

UV flood exposure: 2 min at soft contact mode
Hard bake: 20 min at 100 °C, closed cover

4. DBR deposition:

Tool: Sputter - FHR MS150

TiO_2 Progr.: Auto 3 (cooled position):TiO2_noPDC.AUT
Ar = 40 sccm, O_2 = 12 sccm (pre-cond.), O_2 = 4 sccm (process)
DC = 1 kW
Pressure = 5E-3 mbar
Pre-time = 60 s
Sputter time = 60 s, 120 s, 120 s, 120 s
Pause time (manual): 7 min
Check the sample after each deposition run

SiO_2 Progr.: Auto 3 (cooled position): rfsputter3_with_pause_source6_ reactive_O2_noPDC_main.AUT (test folder)
Pre-time = 60 s
Ar = 40 sccm, O_2 = 15 sccm
RF = 1 kW
Pressure = 1.3E-2 mbar (DC bias = 127 V)
Sputter time: 60 s
Pause time: 3:30 min
Cycles: 10
Check the sample after each 5 deposition cycles

5. Ni vaporization:

Tool: E-beam evaporator - Lesker Spectros
Deposition rate: 1 Å/s
Thickness: 50 nm

6. Photolithography: defining actuation pattern

Tool: Mask aligner KS MJB3-UV 400
Adhesion promoter: HMDS, 3000 rpm, 30 sec
Photoresist: SPR 220-3.0, 3000 rpm, 30 sec (thickness ~2.6 µm)
-Remove edge resist droplets with Teflon stick
Soft bake: hot plate-90 s at 115 °C
No frame exposure!
Pattern exposure: 17 s at soft contact mode (mask: actuation)
Develop: MF24A developer: 45 s, rinse in DIW: 45 s

7. Ni wet etching:

Etchant: HNO_3:H_2O (1:30), rinse in DIW: 60 s
Time: 2 min

8. Photolithography: defining MEMS pattern

Preparing samples for plasma dry etch

Tool: Mask aligner KS MJB3-UV 400
Adhesion promoter: HMDS, 1600 rpm, 30 sec
Photoresist: SPR 220-3.0, 1600 rpm, 30 sec (thickness ~6 μm)
-Remove edge resist droplets with Teflon stick
Soft bake: hot plate-90 s at 115 °C
No frame exposure!
Pattern exposure: 25 s at soft contact mode (mask: MEMS)
Develop: MF24A developer: 60 s, rinse in DIW: 60 s
Hard bake: 5 min at 115 °C

9. Dielectric plasma etch

Tool: Plasma etch-RIE/CVD - Oxford Plasmalab System 100
NF3: 80 sccm
Ar: 50 sccm
RF power: 25 W
ICP power: 0 W
Time: 78 min

10. Photoresist removal

-Heated acetone (50°C), 24 hours

11. Critical Point Dryer (CPD)

CO_2 supercritical drying

Tool:
-Put the sample inside the specimen.
-Place the specimen in the chamber.
-Fill the chamber with solvent (acetone or IPA).
-Start cooling: at 10°C open CO_2 valve and dilute with liquid CO_2 (6-8 times).
-Start heating: Increase temperature to 31°C (pressure: 73 bar)→critical point.
-Open the valve and let the gaseous CO_2 out.
-Open the chamber, take out the sample.