CHALMERS

Digital filters

Computable efficient recursive filters

Master of Science Thesis in Signal Processing

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ABSTRACT

In signal processing, the most widely used digital filter type is the Finite Impulse Response (FIR), mainly for its guaranteed stability. However, these filters requiring a higher order for the same specification compared with its recursive correspondence, the Infinite Impulse Response (IIR) filter. The order can be seen as required number of adders, multipliers and memory for the filter. In Application Specific Integrated Circuits (ASIC) and Field Programmable Gate Arrays (FPGA) applications, especially number of multipliers is desirable to keep low due the extensive logic. Hence, signal processing with FIR filters will result in a large amount of silicon or gates used. This thesis proposes two recursive filters, the Cascaded Integrator Comb- (CIC) filter and the Wave Digital Filter (WDF), where the former is used mainly for interpolation- or decimation. The CIC is a recursive moving average filter which is multiplier free, consisting only of two building blocks and has a linear phase. The WDFs simulates an analog lossless network, such as the ladder- or the lattice structure by using the bilinear transform and voltage waves as signal parameters. For fair comparison of the filters, methods for estimating the hardware cost are developed. A FIR halfband filter is also included and may be seen as a reference in both hardware cost and performance. For comparing performance Error Vector Magnitude (EVM) and Adjacent Channel Leakage Ratio is used, according the method described in 3GPP (3rd Generation Partnership Project). Moreover, interpolation and decimation is handled in a mathematical way to show the importance of using good lowpass filters in multirate systems.

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TERMINOLOGY

ACLR	Adjacent Channel Leakage Ratio
CDMA	Code Division Multiple Access
CIC	Cascaded Integrated Comb
DFT	Discrete Fourier Transform
EVM	Error Vector Magnitude
FIR	Finite Impulse Response
IIR	Infinite Impulse Response
ISI	Inter Symbol Interference
LHP	Left half plane
LWDF	Lattice Wave Digital Filter
RC	Raised Cosine
RHP	Right half plane
RRC	Root-Raised Cosine
WCDMA	Wideband CDMA
WDF	Wave Digital Filter

1 Introduction

The main purpose of this thesis is to evaluate other filters than the commonly used FIR (Finite Impulse Response) filters, this to broaden the knowledge of the subject in the department. In order to do this, and narrow it down, we would like to answer a more concrete question: is there a better way of designing the down- and uplink filter chains than the solution used today.

FIR filter has the advantages that they are easy to design, easy to implement and above all, they are always stable. The main disadvantage of using these filters, are the cost of the hardware, which is the main drive to look at other filters.

In order to evaluate the filters we will use a test matrix with requirements of EVM (Error Vector Magnitude) and ACLR (Adjacent Channel Leakage Ratio) values. To do an estimation of the hardware cost we will calculate how many adders, multipliers and memory there will be a need of in every filter.

The downlink filter chain that will be evaluated consists of one RRC (Root Raised Cosine) filter and four half-pass interpolation filters. The purpose of the RRC filter is to shape the input signal and is basically an ideal low pass filter. The total interpolation factor of the chain is 32, multiples of interpolation with two. Meaning, when the input signal has a sample rate of 3.84 MHz the outgoing up-sampled rate is 122.8 MHz. The two filter types that will be evaluated are the CIC (Cascaded Integrator Comb) filter and the WDF (Wave digital filter) as illustrated in Figure 1-1.

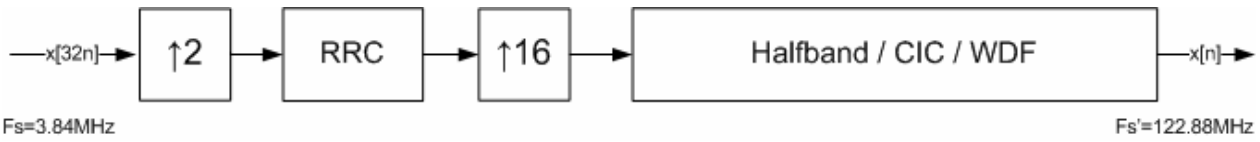

Figure 1-1: Interpolation chain

The reader of this thesis is supposed to have basic knowledge of signal processing and electronics. The thesis will start with a theoretical part about multirate filtering, CIC and WDF theory and an explanation of the evaluation tool used. After this the empirical part, i.e. the results, will follow. The report will thereafter be summarized in discussion and conclusions.

1.1 Multirate systems

A multirate system can be explained as a system with multiple sample rates. It increases or decreases the sample rate in a system. The reason to use multiple sample rates is twofold. For example, if two subsystems are running at different sampling rates and are supposed to work together, then a rate conversion is required. But the most and common reason to use multiple sample rates is the possibility to greatly increase processing efficiency, which reduces the hardware cost in the system. Hence, multirating is simply the technology of changing sampling rates. Multirate consists of three parts; interpolation, decimation and resampling.

1.1.1 Interpolation

Upsampling is the process that inserts $L-1$ zero-valued samples between the original samples which also adds undesired spectrum mirror images of the signal centered at multiples of the original signal's sample-rate. Interpolation is upsampling followed by an ideal lowpass filter to remove the mirrors, as illustrated in Figure 1-2. The filtering process is needed, otherwise the signal is distorted.

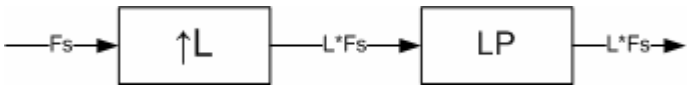

Figure 1-2: Sampling rate increase by L with interpolation.

An ideal interpolator can be described as

$$Y(\omega)=\begin{cases} X(L\omega) & if\ |\omega|<\frac{\pi}{L} \\ 0 & if\ \frac{\pi}{L}\le|\omega|\le\pi \end{cases} \tag{1-1}$$

To accomplish this digitally, consider the input signal $x(n)$ into the upsampler which give the output signal according

$$x_L(m)=\begin{cases} x\left(\frac{m}{L}\right), & m=0,\pm L,\pm 2L,... \\ 0, & otherwise \end{cases} \tag{1-2}$$

The z-transform of $x_L(m)$ is given as

$$X_L(z)=\sum_{m=-\infty}^{\infty}x_L(m)z^{-m}=\sum_{m=-\infty}^{\infty}x(m)z^{-mL}=X\left(z^L\right) \tag{1-3}$$

Evaluating $X_L(z)$ on the unit circle, $z=e^{j\omega}$, gives the Fourier transform of the input signal's spectrum as given as

$$X_L(\omega)=X(L\omega) \tag{1-4}$$

Hence, upsampling creates undesired mirror images in the spectrum which can be removed by a lowpass filter according

$$y(m) = \sum_{k=-\infty}^{\infty} h_{LP}(k) x_L(m-k) \tag{1-5}$$

which in the frequency domain will look as

$$Y_L(\omega) = X_L(\omega) H_{LP}(\omega) \tag{1-6}$$

where the frequency response for a lowpass filter is

$$H_{LP}(\omega) = \begin{cases} 1 & if\ |\omega| < \frac{\pi}{L} \\ 0 & if\ \frac{\pi}{L} \le |\omega| \le \pi \end{cases} \tag{1-7}$$

The interpolation process is shown in Figure 1-3.

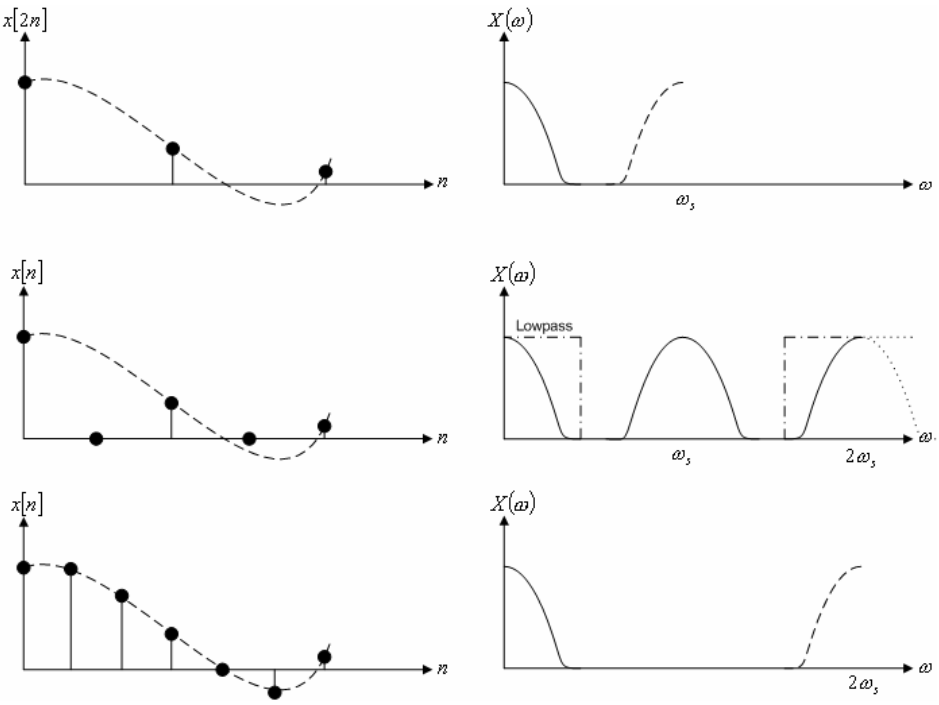

Figure 1-3: Interpolation by two.

Furthermore, an interpolation process can be done in multiple stages, which are sometimes more economical. The restriction is that the interpolation factor not is a prime **[2]**.

1.1.2 Decimation

Downsampling is the process that removes M-1 samples from the input-signal. If the input-signal has frequency components outside the low-rate Nyquist frequency, aliasing will occur. Hence, a lowpass filtering before the downsampling is needed to avoid distortion of the

output signal. A decimation process is a lowpass filtering followed by downsampling, as illustrated in Figure 1-4.

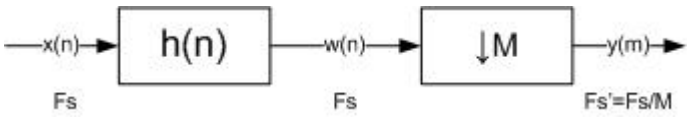

Figure 1-4: Sampling rate decrease by M with decimation

It is of interest to see the impact of using a non-ideal lowpass filter with a signal that has frequency components outside the low-rate Nyquist frequency, $F_s^{'}/2$. For a more explained derivation, refer to **[2]**.

First $w(n)$ can be written as

$$w(n) = \sum_{k=-\infty}^{\infty} h(k)x(n-k) \tag{1-8}$$

and let $w'(n)$ be defined according to

$$w'(n) = \begin{cases} w(n), & n = 0, \pm M, \pm 2M, ... \\ 0 & otherwise \end{cases} \tag{1-9}$$

Hence, for $w'(n) = w(n)$ at all sampling instances at $y(n)$, otherwise zero. An impulse-train expressed in a discrete Fourier series can be used to express $w'(n)$, given by

$$w'(n) = w(n)\left[\frac{1}{M}\sum_{k=0}^{M-1} e^{j2\pi kn/M}\right], \quad -\infty < n < \infty \tag{1-10}$$

where the term in brackets corresponding to the Fourier representation. Now it can be stated that $y(m) = w'(Mm) = w(Mm)$.

The z-transform of $y(m)$ is given by

$$Y(z) = \sum_{m=-\infty}^{\infty} y(m)z^{-m} = \sum_{m=-\infty}^{\infty} w'(Mm)z^{-m} \tag{1-11}$$

where $w'(m)$ is zero at all sampling instances, expect for multiples of M, which gives

$$\begin{aligned} Y(z) &= \sum_{m=-\infty}^{\infty} w'(Mm)z^{-m/M} = \sum_{m=-\infty}^{\infty} w(m)\left[\frac{1}{M}\sum_{k=0}^{M-1} e^{j2\pi km/M} z^{-m/M}\right] \\ &= \frac{1}{M}\sum_{k=0}^{M-1}\left[\sum_{m=-\infty}^{\infty} w(m)e^{j2\pi km/M} z^{1/M}\right] = \frac{1}{M}\sum_{k=0}^{M-1} W\left(e^{j2\pi k/M} z^{1/M}\right) \end{aligned} \tag{1-12}$$

It is clear that $W(z) = H(z)X(z)$ and $Y(z)$ can be expressed according

$$Y(z) = \frac{1}{M}\sum_{k=0}^{M-1} H\left(e^{-j2\pi k/M} z^{1/M}\right) X\left(e^{-j2\pi k/M} z^{1/M}\right) \tag{1-13}$$

This equation can be rewritten to evaluate $Y(z)$ on the unit-circle, as given by

$$Y\left(e^{j\omega'}\right) = \frac{1}{M}\sum_{k=0}^{M-1} H\left(e^{j(\omega'-2\pi k)/M}\right) X\left(e^{j(\omega'-2\pi k)/M}\right) \tag{1-14}$$

where $z = e^{j\omega'}$ and $\omega' = 2\pi f T_s^{'}$.

This expresses the output signal $y(m)$ of the aliased components of the filtered input signal $x(n)$.

It can also be expressed as given by

$$Y\left(e^{j\omega'}\right) = \frac{1}{M}\left[H\left(e^{j\omega'/M}\right) X\left(e^{j\omega'/M}\right) + H\left(e^{j(\omega'-2\pi k)/M}\right) X\left(e^{j(\omega'-2\pi k)/M}\right) + \ldots\right] \tag{1-15}$$

It is desirable that $H\left(e^{j\omega}\right)$ rejects the spectral components above the frequency $\omega = \pi/M$ since otherwise these will be folded into the information band. Hence, $H\left(e^{j\omega}\right)$ acts as an anti-aliasing filter.

If $H\left(e^{j\omega}\right)$ are ideal, then

$$Y\left(e^{j\omega'}\right) = \frac{1}{M} X\left(e^{j\omega'/M}\right), \quad |\omega'| \le \pi \tag{1-16}$$

The decimation process is shown in Figure 1-5.

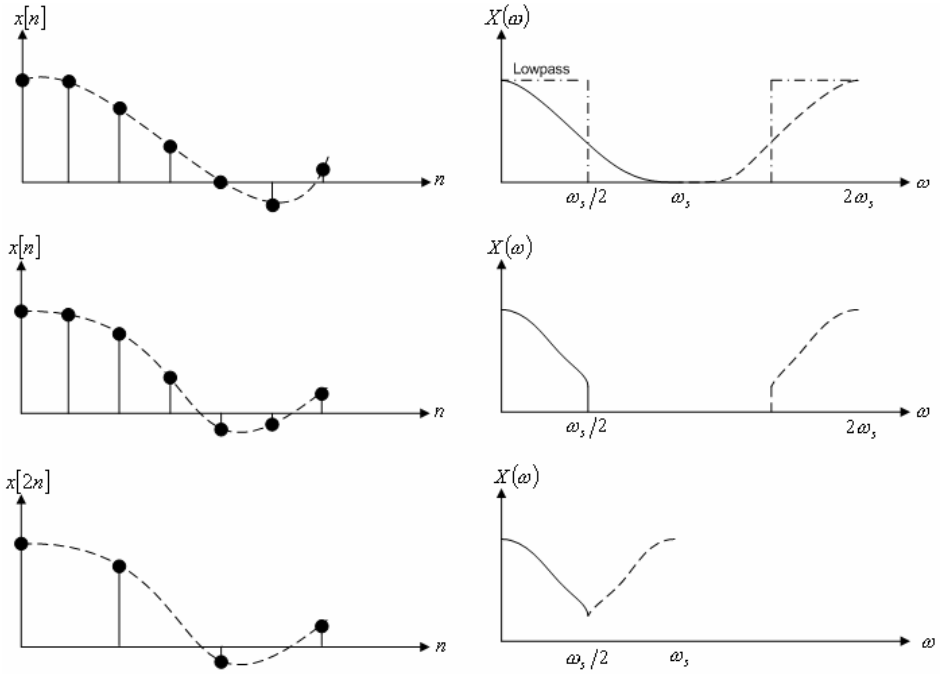

Figure 1-5: Decimation by two with an ideal lowpass filter which results in no aliasing.

1.2 Pulse shaping

Inter Symbol Interference (ISI) is present in both wired and wireless communication systems, as shown in Figure 1-6. Very shortly it can be described as when some of the energy in one symbol leaks into others which may destroy the signal.

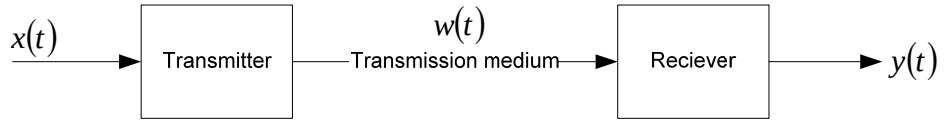

Figure 1-6: Transmission system.

Consider a signal, as illustrated in Figure 1-7, with the sequence which is generated by nearly ideal square-waves due the rise- and fall time in the hardware.

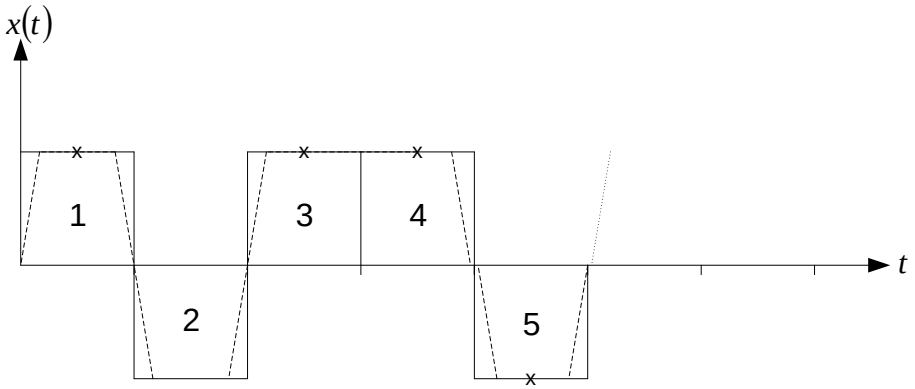

Figure 1-7: A data sequence $\{1,0,1,1,0\}$ described by the dashed line is sent.

The transmission medium will create tails of all symbols as shown in Figure 1-8. The size of tails depends on the medium.

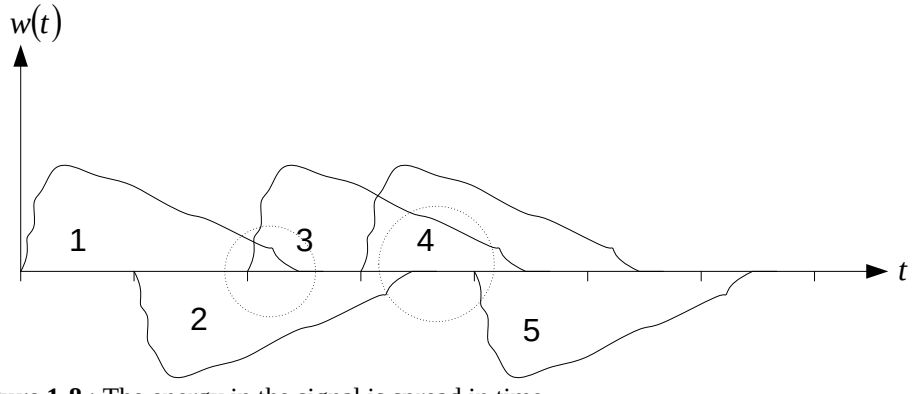

Figure 1-8 : The energy in the signal is spread in time.

At each sample the receiver will take the sum of the present and the former samples. The received signal is not what was sent, as illustrated in Figure 1-9.

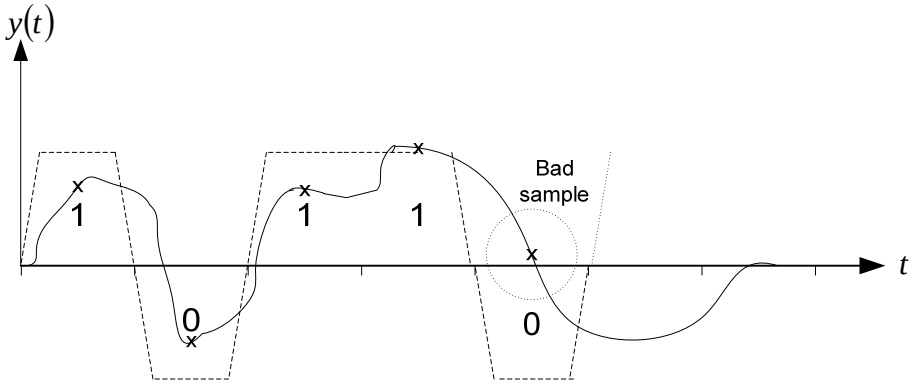

Figure 1-9: The received signal

Hence, the signal in the receiver may contain errors. Symbols which are represented by square-waves in the time-domain or equivalently sinc-waves in the frequency domain have large bandwidth and much ISI. To reduce that unwanted effects, the most straightforward way is to slow down the transmission. But slowing down the transmission is not an option these days where speed is a key to success. The solution is to pulse-shape the signal which means to find a waveform that has a small bandwidth per symbol with minimal ISI.

The optimal solution would be to sinc-shape the signal in time-domain which results in a brick-wall in the frequency-domain, with bandwidth of $1/2\,Hz$ per symbol and no ISI. But sinc-shaping a signal is impossible, due the infinite length of the filter.

Instead, Nyquist introduced realizable shapes that had the same desirable properties as the sinc-shape. One of these are the Raised Cosine (RC) filters which have zero crossings where the adjacent symbols are suppose to occur, which also is known as the Nyquist pulse criterion for zero ISI **[5]**.

Instead of using a single RC-filter on either the transmitter or the receiver side, the common way is to take the square root of the frequency response of the RC-filter and put the corresponding filter, simply named as Raising Root Cosine (RRC) filter on each side as shown in Figure 1-10.

Figure 1-10: Common solution of pulse-shaping using RRC-filters.

The most straightforward way to design a RRC-filter is to either design in the time domain by any of the known formulas, or in frequency domain by using the definition of the RRC response and then use the inverse Discrete Fourier Transform (DFT) to obtain the coefficients.

The general RRC-filter impulse response can be defined according **[7]**.

$$h(t) = \frac{4\alpha}{\pi\sqrt{T}} \left[\frac{\cos\left[(1+\alpha)\pi\frac{t}{T}\right] + \frac{\sin\left[(1+\alpha)\pi\frac{t}{T}\right]}{4\alpha t/T}}{1-(4\alpha t/T)^2} \right] \tag{1-17}$$

where t is the time index, T is how many times faster the filter is operating than the chip-rate and α is the ratio of excess bandwidth past the 3dB point of the total bandwidth of the RC-filter. The frequency response for an 20 order RRC-filter and its corresponding RC-filter are shown in Figure 1-11, where $T = 2$ and $\alpha = 0.20$.

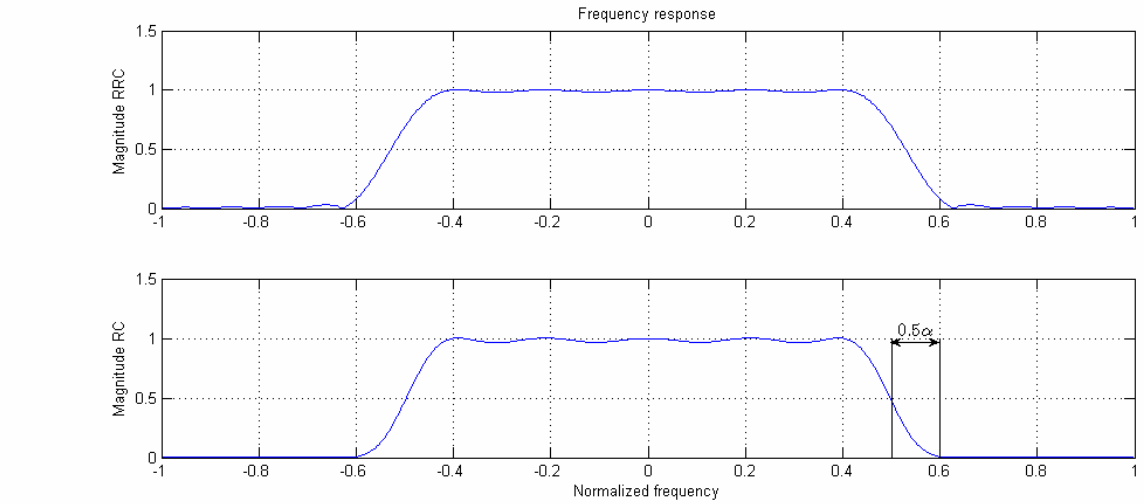

Figure 1-11: Frequency response for a RRC- and its corresponding RC-filter.

When designing the RRC-filters it is necessary to make the roll-off factor α as small as possible, due the often limited bandwidth resource. Furthermore, a high order results in a less ripple in passband and more rejection in stopband. It may also be valuable to apply a window, such as a Kaiser- or Blackman type.

1.3 The Cascaded Integrator Comb filter

The CIC-filter is a multiplier free filter and use limited storage which is very good in an economical perspective. It was introduced by Eugene B. Hogenauer for over two decades ago and is used for interpolation and decimation. Furthermore, the filter do not require any storage for the filter coefficients, can be designed with only two basic building blocks and it is possible to use the same design for different rate changes. Unfortunately, the filter has an undesired passband droop due to the boxcar characteristic which often leads to use of a conventional FIR filter for compensation. Furthermore, the designer has only three design parameters resulting in a limited desirable frequency response.

1.3.1 The relationship to the Boxcar filter

A moving average filter is a filter whose task is to reduce unwanted random white noise. It calculates the average sum of M previous samples and has difference equation according to

$$y[n] = \frac{1}{M}\sum_{k=0}^{M-1} x[n-k] \tag{1-18}$$

This filter is optimal to reduce noise (smoothing) but is poor to separate different bands in the frequency domain (i.e. lowpass filtering). Great performance in the time domain results in bad performance in the frequency domain. If the average part is removed then the equation can be written as

$$y[n] = \sum_{k=0}^{M-1} x[n-k] \tag{1-19}$$

Equation (1-19) describes a Boxcar filter, which are a filter where all coefficients are unity, i.e. 1.0. These kinds of filters do not involve any multipliers and is therefore very computable efficient filters. The frequency response of the filter, which is shown for various lengths in Figure 1-12, and is given by

$$\left|H\left(e^{j\omega}\right)\right| = \left|\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right| \tag{1-20}$$

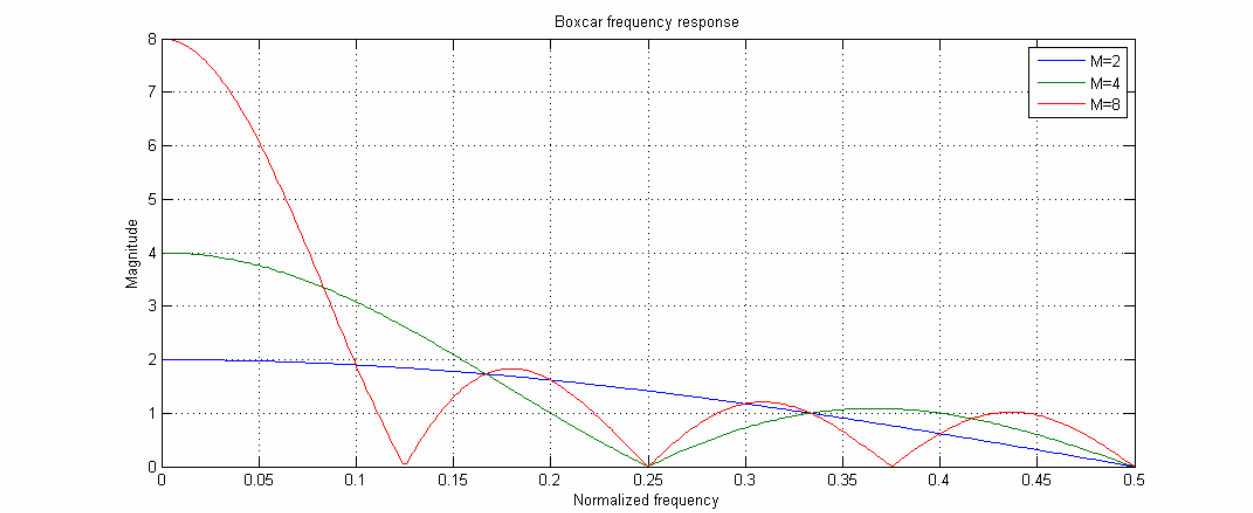

Figure 1-12: Frequency response for Boxcar filters with different lengths.

As just mention, the Boxcar filter is not a really good lowpass filter due the poor stopband rejection and its slow roll-off. However, the filter does not require any multipliers and that is a really desirable property among ASIC- and FPGA designers. Hence, it is of big interest to see if the Boxcar filter can be modified to work in a lowpass process with a more definite specification.

1.3.2 The recursive form

When considering the difference equation for the Boxcar filter the process can be stated as: A new sample, $x[n]$ arrive and the old samples $x[n-1] \rightarrow x[n-M+1]$ in the register is shifted to make room for the new one, which discarding the sample $x[n-M]$. Then the output $y[n]$ is the sum of the data in the register. This process is repeated each time a new sample arrive to the input of the filter. However, for every output there are $M-1$ required additions, which may be a big cost if M is large. It turns out that the filtering process can be made recursive according to

$$y[n] = \sum_{k=0}^{M-1} x[n-k] = x[n] - x[n-M] + \sum_{k=0}^{M-1} x[n-1-k] = x[n] - x[n-M] + y[n-1] \tag{1-21}$$

Each output sample is now requiring only two additions compared with $M-1$ in the standard form, which are a pretty good improvement. This form is also known as the CIC filter, the first "C" stands for cascaded and the integrator is the "I" and the comb is the second "C". Block diagrams of the CIC is shown in Figure 1-13 and its Boxcar equivalence as well.

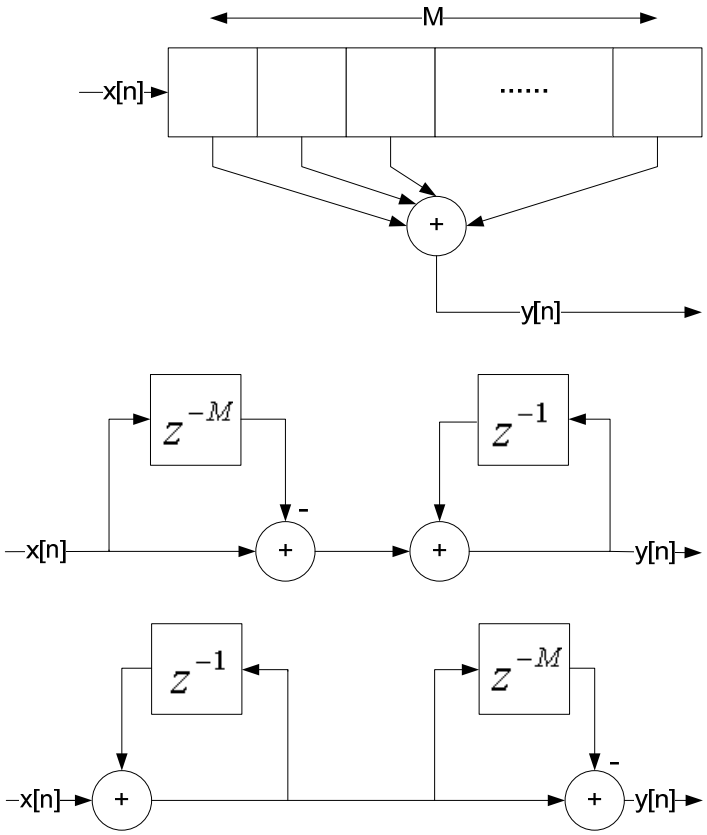

Figure 1-13: The original Boxcar structure and the two corresponding CIC structures.

The comb and integrator blocks are LTI systems and hence they commute.

The z -transform of the last term in equation (1-21) gives the transfer function according to equation (1-22) which can further be expressed to better describe the pole- and zero placements.

$$H(z) = \frac{1 - z^{-M}}{1 - z^{-1}} = \frac{1}{z^{M}} \frac{z^{M} - 1}{1 - z^{-1}} = \frac{1}{z^{M-1}} \frac{z^{M} - 1}{z - 1} \tag{1-22}$$

The last term shows that the pole at the positive real axis is cancelled by the zero at the same location which also is illustrated in Figure 1-14 for a fixed M .

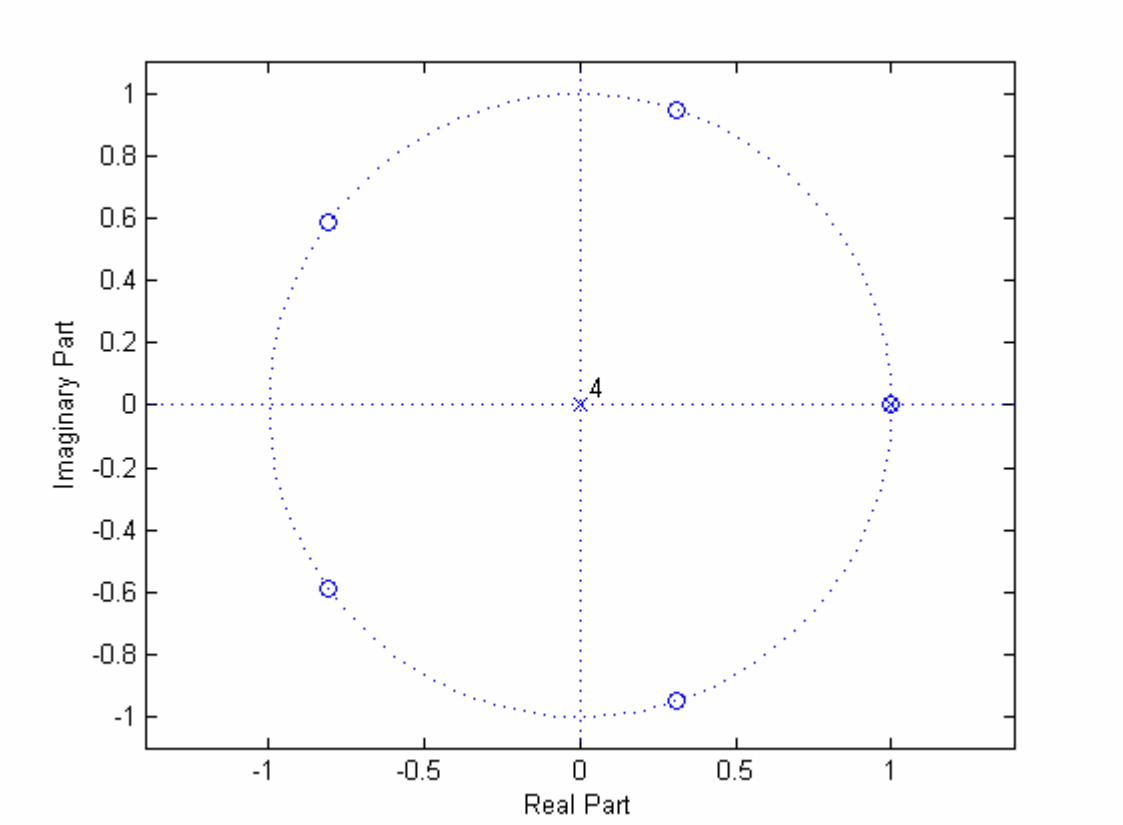

Figure 1-14: Pole and zero locations for a CIC filter where the zeros are located on the unit circle and the poles in the origin.

It may be interesting to study the cancellation and the impact when it is not applied. The first term in equation (1-22), which is the transfer function of the CIC filter, does not involve any cancellation at all. That will result in an internal state, denoted $w[n]$ in Figure 1-15, which is not present in the original Boxcar filter. Consider the case for a step response in the Boxcar filter and for a CIC filter. Both will have identically responses, also when the comb and the integrator is reordered. It looks like the CIC filter is stable but unfortunately it is not. The integrator in the latter case is on the way to infinity causing overflow.

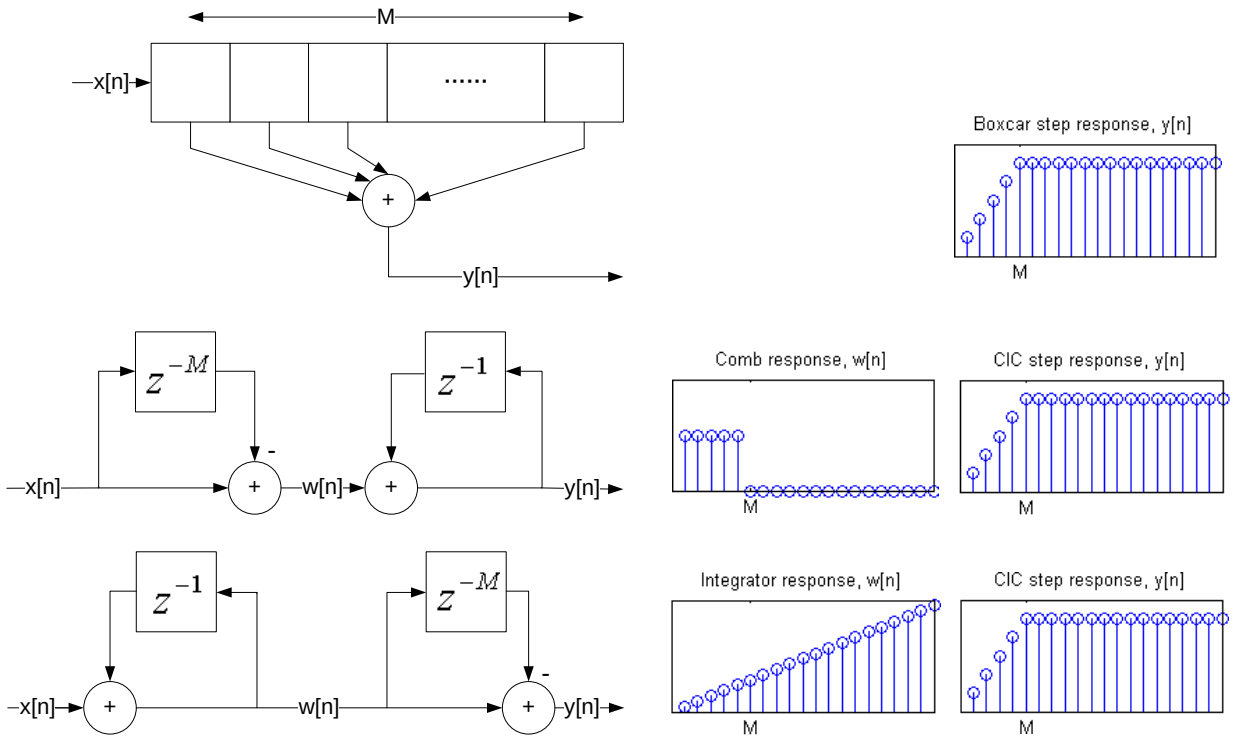

Figure 1-15: Step response for the Boxcar filter and the CIC filter with reordering of comb and integrator.

An impulse response will give similar result, the original impulse circulates in the integrator but the summation in the comb stage results in zero at the output. Hence, the CIC filter is stable from the overall perspective but not internally. Fortunately, the overflows will not cause any problem, which will be handled in section 1.3.5.

1.3.3 Interpolation and decimation with the CIC filter

As stated before, interpolation means upsampling followed by lowpass filtering. Decimation means lowpass filtering followed by downsampling. Ignoring the fact that the CIC filter is not a good lowpass filter, insert an R upsampler for interpolation before the CIC filter and put an R downsampler after the CIC filter for decimation, as shown in Figure 1-16.

It is allowed to reorder the comb and the resampler due the noble identity **[5]**. It yields two major benefits by performing that operation:

- The comb new delay is decreased to M/R, which will reduce storage requirements.
- The comb is now running at the low clock rate which will reduce power consumption.

Hence, when ordering this way the comb is always running at the low clock rate and the integrator always running at the high clock rate. That is valid both for interpolation and decimation.

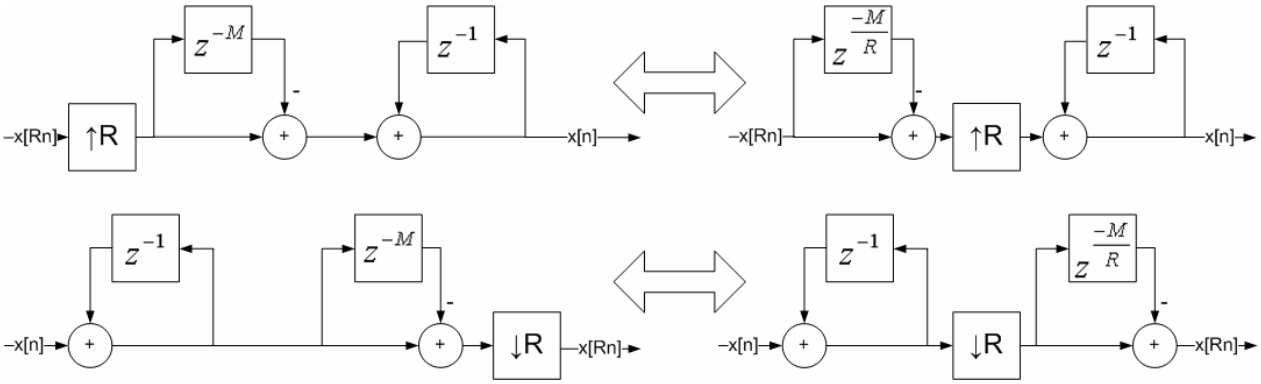

Figure 1-16: Interpolation- and decimation with the CIC filter, and its equivalence

1.3.4 Frequency characteristic and improve of stopband rejection

The frequency response of the filter is determined by evaluating its transfer function on the unit-circle at the z-plane.

The transfer function is given as

$$H(z) = \frac{1 - z^{-M}}{1 - z^{-1}} \tag{1-23}$$

By setting $z = e^{j\omega}$, yields

$$H\left(e^{j\omega}\right) = \frac{1 - e^{-j\omega M}}{1 - e^{-j\omega}} = \frac{e^{-j\omega M/2}\left(e^{j\omega M/2} - e^{-j\omega M/2}\right)}{e^{-j\omega/2}\left(e^{j\omega/2} - e^{-j\omega/2}\right)} \tag{1-24}$$

Eulers identity is defined as

$$\sin(\alpha) = \frac{e^{j\alpha} - e^{-j\alpha}}{2j} \Leftrightarrow 2j\sin(\alpha) = e^{j\alpha} - e^{-j\alpha} \tag{1-25}$$

Substitute equation (1-25) into (1-24), yields

$$H\left(e^{j\omega}\right) = \frac{e^{-j\omega M/2}}{e^{-j\omega/2}} \frac{2j\sin(\omega M/2)}{2j\sin(\omega/2)} = e^{-j\omega(M-1)/2} \frac{\sin(\omega M/2)}{\sin(\omega/2)} \tag{1-26}$$

The amplitude function of the frequency response can now be expressed as

$$\left|H\left(e^{j\omega}\right)\right| = \left|\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right| \tag{1-27}$$

where ω is relative to the high sample-rate.
It is not a coincidence that the frequency response of the CIC filter is exactly the same as for the Boxcar filter. Again, the CIC is just a recursive form of the Boxcar. It is of a great interest to see if it is possible to improve the stopband rejection. That can be accomplished by cascading a number of CIC filters, as showed in Figure 1-17.

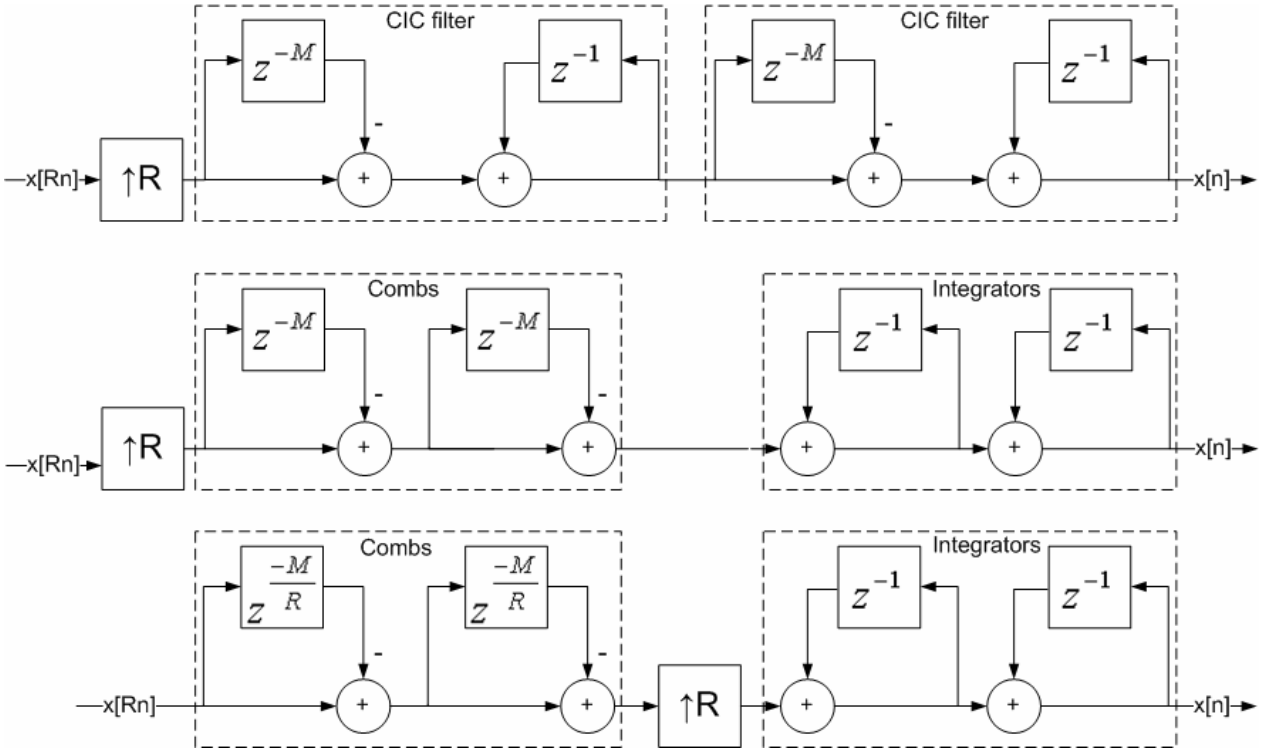

Figure 1-17: A two stage interpolator CIC filter

The frequency response for a multiple stage is then given by

$$\left|H\left(e^{j\omega}\right)\right| = \left|\frac{\sin\left(\omega M/2\right)}{\sin\left(\omega/2\right)}\right|^{N} \tag{1-28}$$

where N is number of stages and the frequency ω is relative to the high sample-rate.

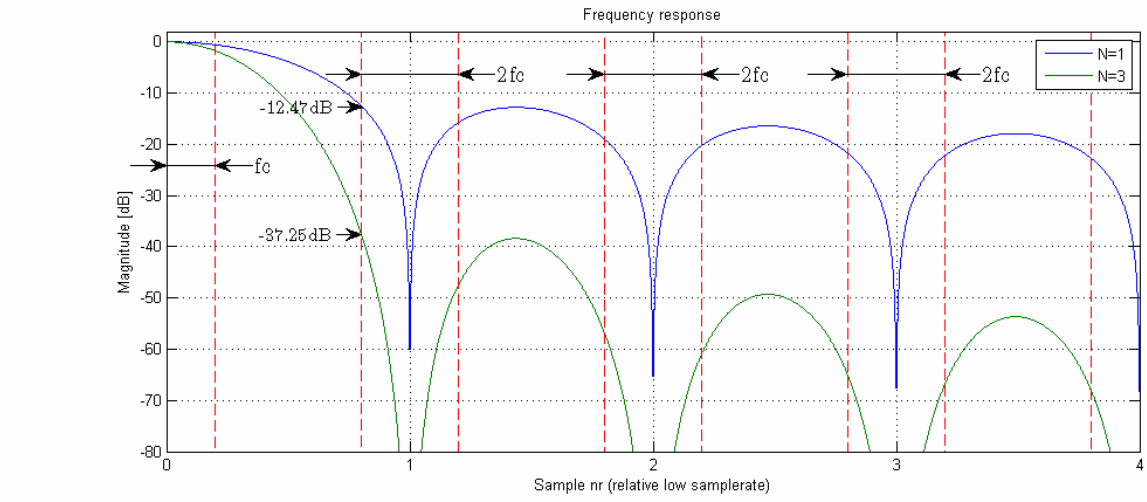

Figure 1-18: CIC with different stages and corresponding rejection of spectral components.

The imaging or aliasing occur in the regions around the nulls. More rejection in stopband results in smaller spectral images or aliasing. Furthermore, if the number of stages, N is increased it will result in an undesired increase of passband "droop" and an undesired increase of net gain which also are dependent of the delay in combs, M . Now, let $M = RD$ where R is rate change and a differential delay, D . The differential delay can be used to set the null placements but are in practice usually held to $D = 1$ or 2 **[6]**.

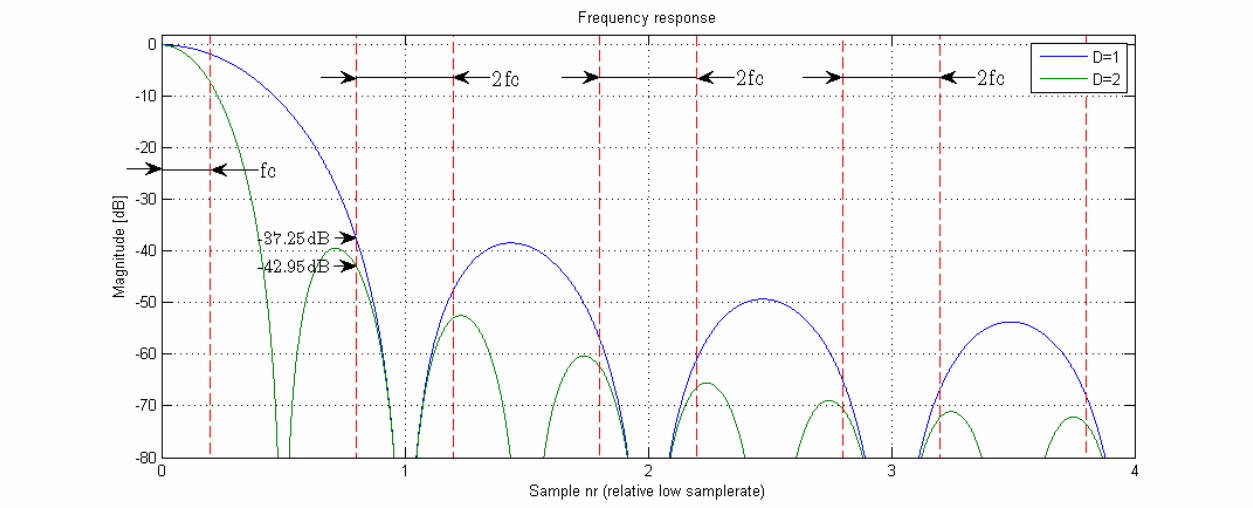

Figure 1-19:The differential delay set the placements of nulls.

An increase of differential delay will cause an even faster passband "droop" but results in a moderate increase of the stopband rejection which may not payoff. One important thing is that the relative bandwidth of the signal determines when it is profitable to use the CIC filter. Clearly, if the bandwidth is small it will result in a relative flat passband, high rejection of imaging or aliasing components. In **[6]**, values of passband attenuation and rejection of imaging or aliasing components is determined, according Table 1-1 and 1-2.

Table 1-1: Passband attenuation for large rate change factors

Relative bandwidth-Differential delay product (Df_c)	Passband Attenuation at f_c (dB) as a function of Number of stages, N					
	1	2	3	4	5	6
1/128	0.00	0.00	0.00	0.00	0.00	0.01
1/64	0.00	0.01	0.01	0.01	0.02	0.02
1/32	0.01	0.03	0.04	0.06	0.07	0.08
1/16	0.06	0.11	0.17	0.22	0.28	0.34
1/8	0.22	0.45	0.67	0.90	1.12	1.35
1/4	0.91	1.82	2.74	3.65	4.56	5.47

Table 1-2: Imaging or aliasing attenuation for large rate change factors

Differential delay (D)	Relative bandwidth (f_c)	Imaging or aliasing attenuation at $f_{IA} = f_{low} \pm f_c$ as a function of number of stages, N					
		1	2	3	4	5	6
1	1/128	42.1	84.2	126.2	168.3	210.4	252.5
1	1/64	36.0	72.0	108.0	144.0	180.0	215.9
1	1/32	29.8	59.7	89.5	119.4	149.2	179.0
1	1/16	23.6	47.2	70.2	94.3	117.9	141.5
1	1/8	17.1	34.3	51.4	68.5	85.6	102.8
1	1/4	10.5	20.9	31.4	41.8	52.3	62.7
2	1/256	48.1	96.3	144.4	192.5	240.7	288.8
2	1/128	42.1	84.2	126.2	168.3	210.4	252.5
2	1/64	36.0	72.0	108.0	144.0	180.0	216.0
2	1/32	29.9	59.8	89.6	119.5	149.4	179.3
2	1/16	23.7	47.5	71.2	95.0	118.7	142.5
2	1/8	17.8	35.6	53.4	71.3	89.1	106.9

Table 1-1 and 1-2 is derived from an approximation of the frequency response and are equal for large rate change factors, i.e. $RD \geq 10$. It may still be used for an indication of impact of the design parameters and the relative bandwidth of the signal. For example, by using Table 1-1 and 1-2 an interpolation by 10 of a signal with relative bandwidth $f_c = 1/4$ with a minimum attenuation in stopband of $60dB$ needs a six stages CIC filter, $N = 6$. Furthermore, droop in passband is then $5.47dB$. To summarize, the transfer function for a CIC filter gives by

$$H(z) = \left[\frac{1 - z^{-RD}}{1 - z^{-1}} \right]^N \tag{1-29}$$

and its frequency response is

$$\left| H\left(e^{j\omega}\right) \right| = \left| \frac{\sin(\omega RD/2)}{\sin(\omega/2)} \right|^N \tag{1-30}$$

Hence, it is three design parameters in the CIC filter, the rate change factor, R, the differential delay, D and number of stages, N.

1.3.5 Overflow and bit-growth

A block diagram of the CIC interpolation- or decimation filter with arbitrary stages is shown in Figure 1-20.

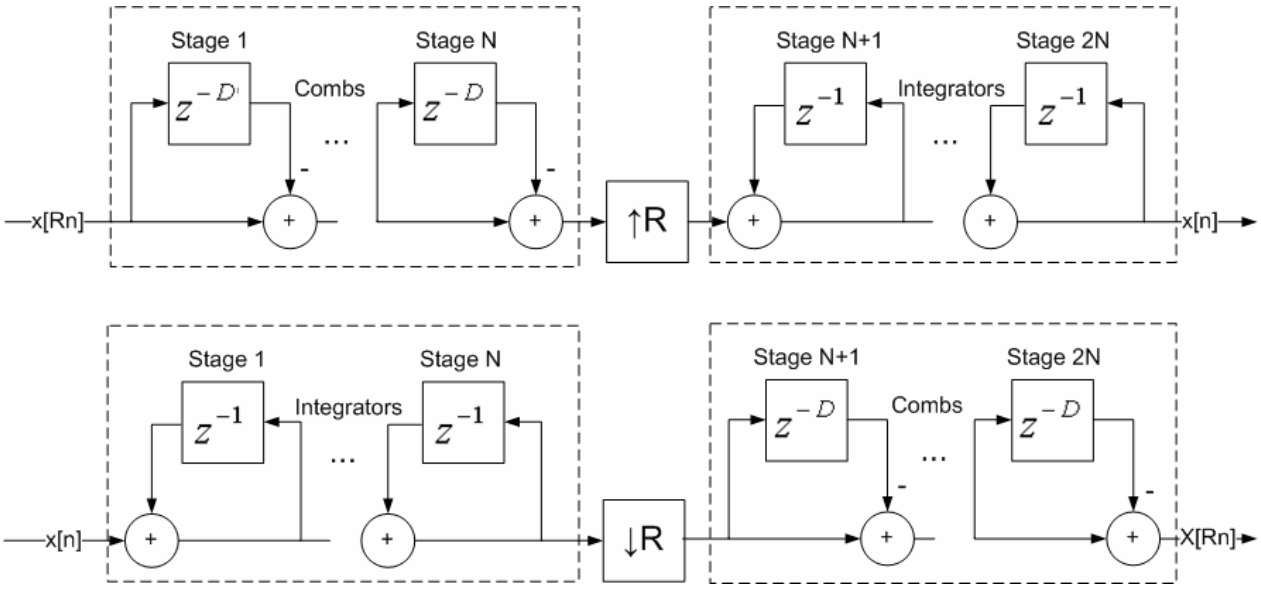

Figure 1-20: CIC interpolation- and decimation filter with arbitrary stages

The integrator in a CIC decimation filter has a unity feedback coefficient and will results in a register overflow in all integrator stages in the filter. However, it will not be a problem if two conditions are met **[6]**.

1. The filter is implemented with a number system which allows "wrap-around".
2. The maximum output value from the composite filter is less or equal than the range of the number system.

Integrators in interpolators will not be affected by overflow, due the data are preconditioned by the comb stages and resampler **[6]**. The maximum gain in a comb or an integrator is depending of its input sequence. For an interpolator, the gain with respect to a sequence which generate maximum gain at each filter stage is

$$G_i = \begin{cases} 2^i & i = 1,2,..,N \\ \dfrac{2^{2N-i}(RD)^{i-N}}{R}, & i = N+1,...,2N \end{cases} \tag{1-31}$$

which gives the required data width at the *i:*th stage according to

$$W_i = \left[B_{in} + \log_2(G_i)\right] \tag{1-32}$$

where B_{in} is the input data width.

Hence, when designing an interpolation filter, the minimum data width at each register gives by equation (1-32). If differential delay is one, then the data width of the last comb is larger than the first integrator. A special condition for the last comb can be stated as **[6]**.

$$W_N = \left[B_{in} + N\right] \quad if \quad D = 1 \tag{1-33}$$

The data width in the output stage is according

$$B_{out} = \left[B_{in} + N\log_2(RD) - \log_2(R)\right] \tag{1-34}$$

Rounding can not be applied in interpolation CIC filters, except in the last integrator, due the small errors grows without bound in the integrator stages, which result in an unstable filter **[6]**. For a decimation filter, the output gain is

$$G = (RD)^N \tag{1-35}$$

and the output data width is

$$B_{out} = \left[B_{in} + N\log_2(RD)\right] \tag{1-36}$$

To prevent data loss it is required that each integrator and comb has a bit-width of B_{out}. However, by using a pruning technique, described in **[6][5]**, it is possible to reduce the bit-width at specific stages that will lead to a more efficient implementation.

1.3.6 Compensation filter

In most applications it is required to have a flat passband, otherwise the original signal may be destroyed. Unfortunately, the CIC filter alone suffers with a passband droop, which in many cases, cannot be accepted. The big droop is due the sinc-like characteristic of the filter. Hence, it is of a great interest to get a flat passband using a compensation filter.

The compensation filter will take the form of the inverse of the CIC filter frequency response in the passband, and attenuate as much as possible in the stopband. The last statement is optional, the compensation filter may be used for further interpolate or decimate, which may be good where the relative bandwidth are too wide. If the compensation filter is also used for interpolation or decimation, then the desired frequency response is given as

$$H_{comp}\left(e^{j\omega}\right) = \begin{cases} \left|\dfrac{\sin(\pi f)}{\sin(\pi RDf)}\right|^N, & f \le f_c \\ 0 & else \end{cases} \tag{1-37}$$

An example of the resulting frequency response is illustrated in Figure 1-21.

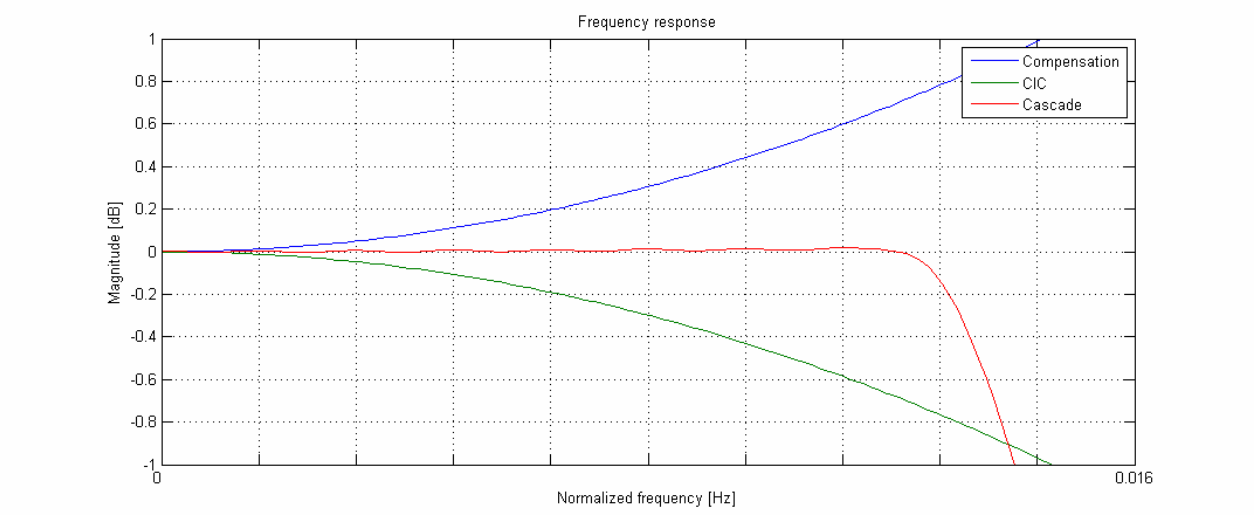

Figure 1-21: The compensation filter effectively compensates the undesired "droop" in the passband.

When number of stages or a differential delay in the CIC is increased it will cause higher demands on the compensation filter, because more correction is needed. Likewise when increasing the passband as well. The demands have a direct impact on the length of the compensation filter, which will lead to undesirable multipliers, adders and memory.

1.4 Wave Digital Filters

Infinite Impulse Response (IIR) filters are possible to implement both as analog and digital. However, it is very hard to design digital IIR filters because very few methods are available. On the other hand, for analog IIR filters, there exist a lot of design methods, techniques, approximations and software. Hence, when designing an IIR digital filter an analog counterpart is first designed (i.e. Chebyshev filter, Butterworth filter or Cauer filter). Then, a discretization technique is used such as the bilinear transformation or the impulse invariance to obtain the corresponding IIR digital filter.

Moreover, a digital IIR filter require a less order for the same specification compared with a FIR filter and will result in a cheaper hardware cost. It seems that there is no need for FIR filters when design methods and transformations for IIR filters are available. Unfortunately, there are a lot of problems associated with IIR digital filters. In the digital domain, the coefficients and data is under finite precision arithmetic which may result in overflow of the number range, parasitic oscillations, round-off errors and coefficient errors or all in all, a possible unstable filter.

However, a given transfer function can be realized in different structures. For infinite precision arithmetic all structures produces the same output for a given input. But under finite precision arithmetic different kinds of errors may occur, as mention earlier. The best structure is a trade-off between many different aspects such as stability, coefficient sensitivity and other quantization effects. Hence, the problem is how to find a good filter structure for the application.

Here is an introduction of a different way of designing digital IIR filters. The theory was first introduced by Alfred Fettweis in the seventies but has not been very used in implementations from then on. The explanation is something that will be discussed later on in the chapter. These kinds of filters are called Wave Digital Filters (WDF). The literature seems to be very limited, but for the interested reader **[3][18][11]** may be valuable.

The difference with the classical IIR filter design method is that instead of first making the bilinear transformation between the domains and thereafter trying to come up with a good filter structure, now make the structure in the analogue domain with lumped elements and then transforming the whole structure to the z-domain. By doing this it is possible to use known design methods, approximations and software that are used in analogue filter design.

The theory is however quite hard to understand. To overcome this problem, having to understand the theory before actually using the filters, **[4]** can be used, where explicit formulas for designing lattice wave digital filters are explained. It is widely known that lossless filters inserted between resistive terminations have good properties. Some of these properties that are inherited from the analogue filters when using WDFs are **[18]**:

- Guaranteed stability
- Low sensitivity in passband
- Regular and modular

The work flow when designing a wave digital filter is different to the classical approach as seen in Figure 1-22. The main difference is that the structure is designed directly when dimensioning the analogue filter. When doing this the problem come up that one can not

directly use the bilinear transformation as in the classical filter dimension approach. Instead it is necessary must use transmission lines and then map the design to the digital domain.

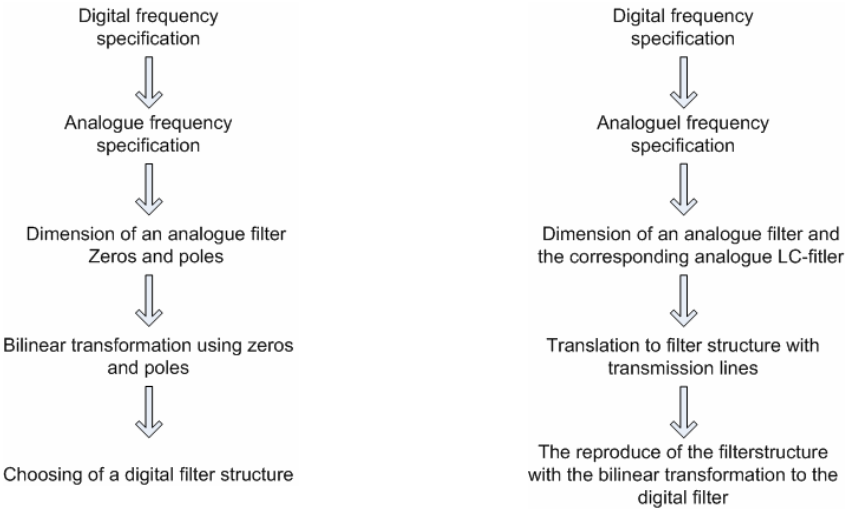

Figure 1-22: Work flows of a classical IIR filter dimension and WDF filter dimension.

A WDF is realized using a reference filter. The reference filter is typically a ladder or lattice network realized with transmission lines as shown in Figure 1-23. The transmission lines have the special property that the frequency is periodic, as with digital circuits.

Next chapters will explain the theory behind the WDF and how the workflow from going to a frequency specification to a filter structure with the desired properties as a WDF has. The building blocks of a WDF will be derived using wave theory. The end result will be a recursive filter with adders, multipliers and delays as any digital filter. It is the structure that is of interest. How to come up with the structure and the filter coefficients is the somewhat tricky part. However, there are designed structures and formulas available **[4]**.

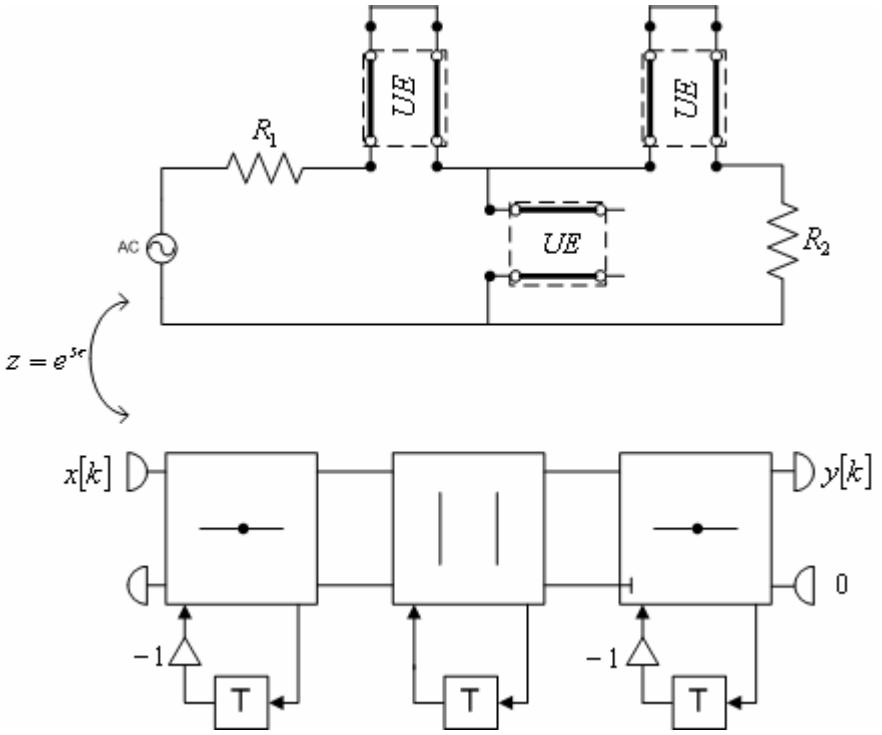

Figure 1-23: A ladder filter realized as a transmission line filter and its digital correspondence

1.4.1 Wave theory

When simulating an analog circuit, one would first think of selecting the voltages and currents as the signal parameters and then using the bilinear transform to receive the digital correspondence.

By applying the strategy of using voltages, currents and the bilinear transformation, it will in general results in unrealizable structures due delay-free loops **[3]**, i.e. feedbacks with no delay.

However, by transforming voltages and currents into voltage waves and then applying the bilinear transformation, the problem of delay-free loops will disappear.

The steady-state voltage waves for the one-port network in Figure 1-24 are defined according to

$$\begin{cases} A = V + RI \\ B = V - RI \end{cases} \tag{1-38}$$

where A is the incident wave, B is the reflected wave and R is a positive real constant which has the dimension of resistance and is called port-resistance.

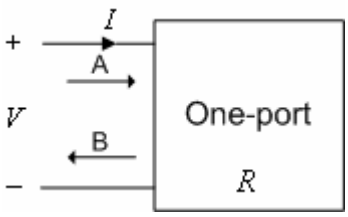

Figure 1-24: One-port network with incident- and reflected voltage waves.

A one-port network can also be described by the reflectance function which is defined as

$$S = \frac{B}{A} = \frac{V - RI}{V + RI} \tag{1-39}$$

The reflectance function can be rewritten by using the impedance $Z = V/I$ in the wave equations which yields

$$S = \frac{Z - R}{Z + R} \tag{1-40}$$

1.4.2 Transmission lines

The lumped element model is a simplified model that makes the assumption that the wires connecting elements are perfect conductors. The operating wavelength needs too be much smaller than the circuit's characteristic length for this model to work. Otherwise a more general model like the distributed element model needs to be considered. This model does not make the assumption that the wires are perfect conductors but has impedance. Lossless commensurate-length transmission lines are the most commonly used.

Furthermore, the frequency response in a commensurate length transmission line is periodic with a period of $1/\tau$ and turns out to be a significant property. A lossless commensurate-length transmission line is shown in Figure 1-25 and can be described by a two-port chain matrix according to equation (1-41) **[18]**.

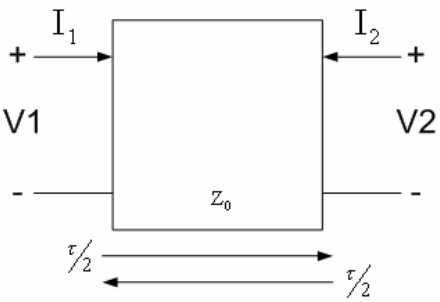

Figure 1-25: A commensurate-length lossless transmission line

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \frac{1}{\sqrt{1-\tanh^2\left(\frac{s\tau}{2}\right)}} \begin{pmatrix} 1 & Z_0 \tanh\left(\frac{s\tau}{2}\right) \\ \frac{1}{Z_0}\tanh\left(\frac{s\tau}{2}\right) & 1 \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{1-41}$$

where Z_0 is the characteristic impedance and $\tau/2$ the electrical propagation time. The port-resistance, as was shortly described in the former section, is set to be equal the characteristic impedance.

1.4.3 Richards' transformation

A new complex frequency variable is introduced according to equation (1-42), which is called Richards' variable **[18]**.

$$\psi = \Sigma + j\Omega = \tanh\left(\frac{s\tau}{2}\right) = \frac{e^{s\tau/2}-1}{e^{s\tau/2}+1} \tag{1-42}$$

The mapping between the s-domain and the ψ-domain is illustrated in Figure 1-26 and has two interesting properties. First, because $\tanh(s\tau/2 - j\pi) = \tanh(s\tau/2)$ make the ψ-plane to be mapped into infinite number of sections of $2\pi/\tau$ high in the s-plane. The second property is that the left half-plane (LHP) of the ψ-plane is mapped into LHP of the s-plane and likewise for right half-plane (RHP).

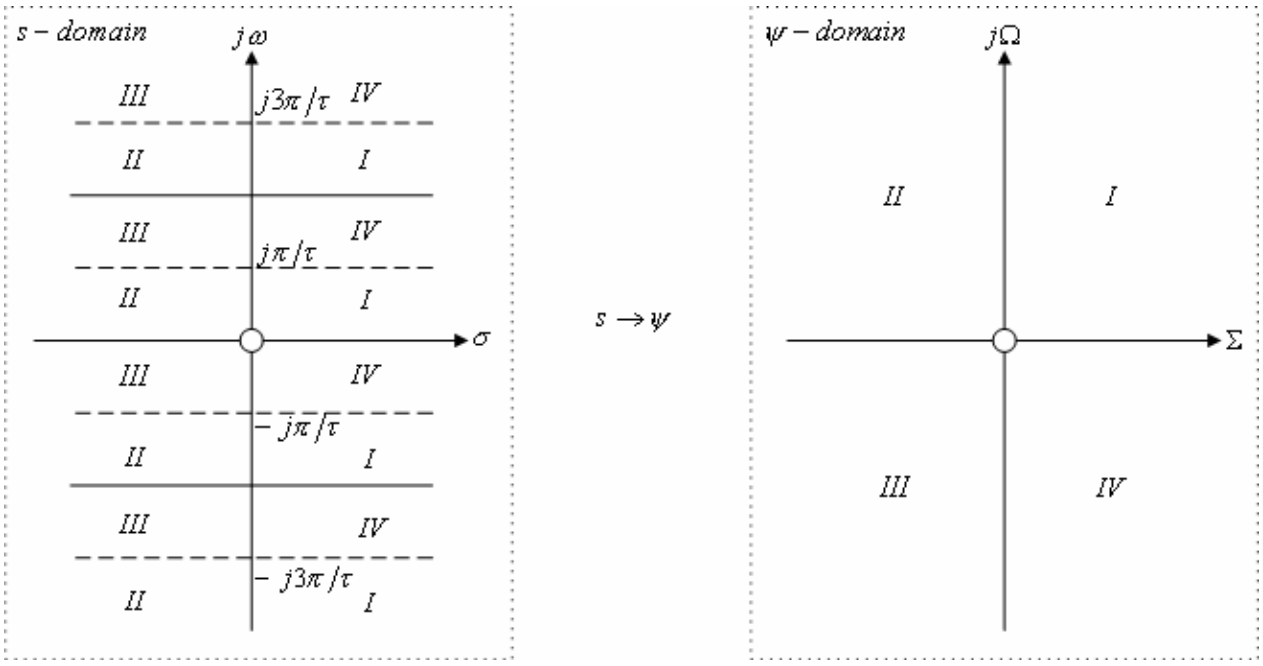

Figure 1-26: The mapping between s-domain and ψ-domain.

For $s = j\omega$, equation (1-42) can be written as

$$\psi = \Sigma + j\Omega = \tanh\left(\frac{j\omega\tau}{2}\right) = j\tan\left(\frac{\omega\tau}{2}\right) \Leftrightarrow \Omega = \tan\left(\frac{\omega\tau}{2}\right) \tag{1-43}$$

where the last term describe the periodic frequency behavior in the s-domain along the ω-axis as illustrated in Figure 1-1Figure 1-27.

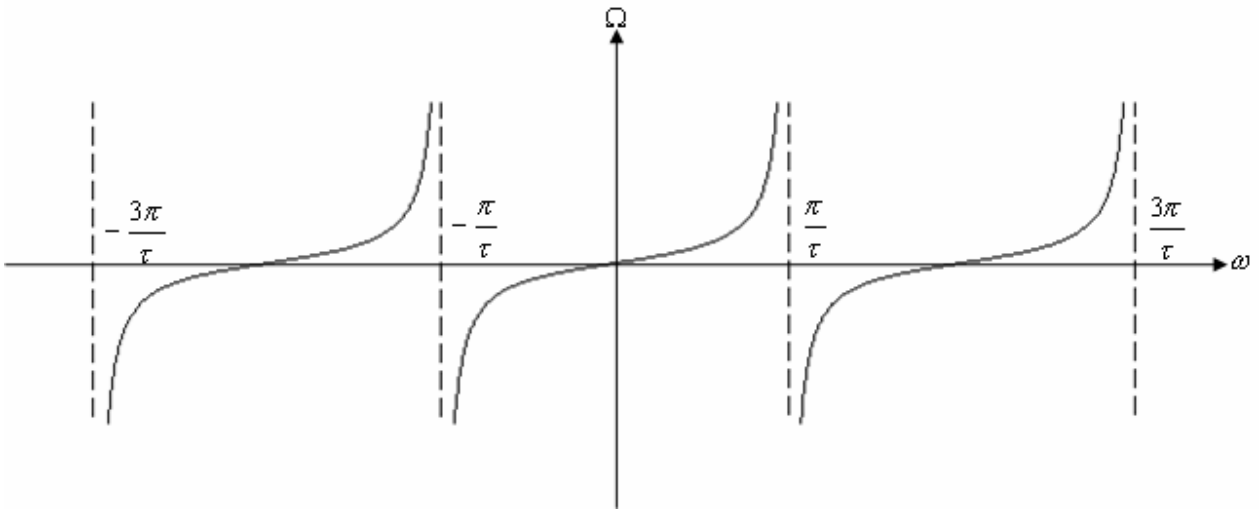

Figure 1-27: The frequency mapping between s-domain and ψ-domain

Hence, a correspondence between the s-domain and ψ-domain is now established.

1.4.4 Unit elements

Now by inserting Richards' variable into the chain matrix for a commensurate-length transmission line defined in equation (1-41) gives the new chain matrix according to

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \frac{1}{\sqrt{1-\psi^2}} \begin{pmatrix} 1 & Z_0\psi \\ \frac{1}{Z_0}\psi & 1 \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{1-44}$$

Hence, the reference filter realized by lossless commensurate-length transmission lines in the ψ-domain can be designed by starting from a lumped filter in s-domain.

In the next section it will be shown that an open-circuited lossless commensurate-length transmission line in the s-domain behaves like a capacitor in the ψ-domain, a short-circuited line behaves like an inductor and a resistance is not affected because it is frequency independent.

The lossless commensurate transmission line is also called a unit element **[18]**. Consider a unit element with characteristic impedance Z_0 and terminated by the impedance Z_2, as illustrated in Figure 1-28.

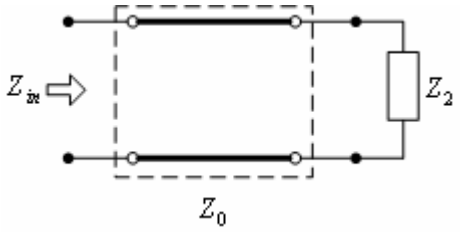

Figure 1-28: A terminated unit element

By using the chain-matrix according to equation (1-44), the input impedance can be written as

$$Z_{in}(\psi) = \frac{V_1}{I_1} = \frac{Z_2 + Z_0\psi}{Z_0 + Z_2\psi} Z_0 \tag{1-45}$$

The input impedance for a unit element with characteristic impedance $Z_0 = R$ is depending on the load impedance. It can be short-circuited, open-ended or matched terminated. Hence, it is interesting to investigate the input impedance for these three cases.

For a short-circuit unit element is $Z_2 = 0$. By using equation (1-45) gives

$$Z_{in}(\psi) = \left.\frac{Z_2 + Z_0\psi}{Z_0 + Z_2\psi} Z_0\right|_{Z_2=0} = R\Psi \tag{1-46}$$

Hence, an inductor in the s-domain corresponds to an inductor in the ψ-domain with the value R.

For an open-circuit unit element is $Z_2 = \infty$ and the input impedance is given by

$$Z_{in}(\psi) = \left.\frac{Z_2 + Z_0\psi}{Z_0 + Z_2\psi} Z_0\right|_{Z_2=\infty} = \frac{R}{\psi} \tag{1-47}$$

A capacitor in the s-domain corresponds to a capacitor in the ψ-domain with the value $1/R$.

When the unit element is matched terminated, $Z_2 = Z_0$ the input impedance is then given by

$$Z_{in}(\psi) = \left.\frac{Z_2 + Z_0\psi}{Z_0 + Z_2\psi} Z_0\right|_{Z_2=Z_0} = R \tag{1-48}$$

The reflectance function as defined in equation (1-40) is now used together with the Richards' variable to obtain the digital element. The resistors are frequency independent and are not affected by the transformation.

A short-circuit unit element where the input impedance is $Z_{in}(\psi) = R\psi$ and by using the reflectance function according to equation (1-40) then gives

$$S(\psi)=\frac{Z_{in}-R}{Z_{in}+R}=\frac{\psi-1}{\psi+1}=-e^{-s\tau}\longleftrightarrow S(z)=-z^{-1} \tag{1-49}$$

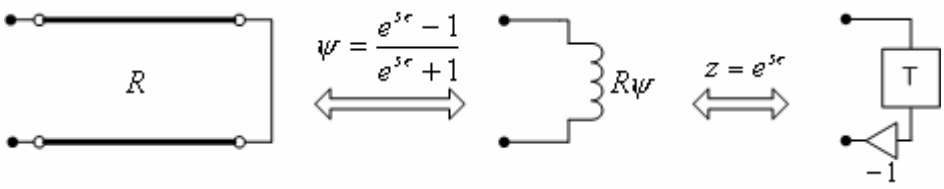

Figure 1-29: A short-circuit unit element and its correspondence in the different domains

An open-circuit unit element where the input impedance is $Z_{in}(\psi)=R/\psi$ and using the reflectance function which yields

$$S(\psi)=\frac{Z_{in}-R}{Z_{in}+R}=\frac{1-\psi}{1+\psi}=e^{-s\tau}\longleftrightarrow S(z)=z^{-1} \tag{1-50}$$

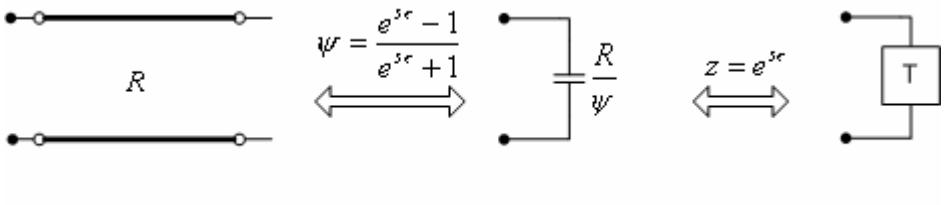

Figure 1-30: An open-circuit unit element and its correspondence in the different domains

A matched-circuit unit element where the input impedance is $Z_{in}(\psi)=R$ and using the reflectance function yields

$$S(\psi)=\frac{Z_{in}-R}{Z_{in}+R}=0\longleftrightarrow S(z)=0 \tag{1-51}$$

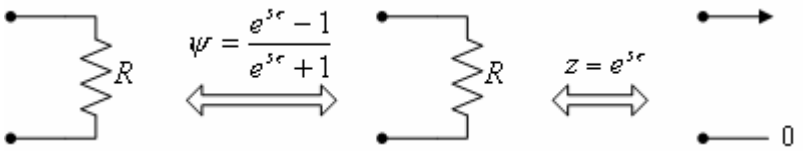

Figure 1-31: A matched-circuit unit element and its correspondence in the different domains

Hence, by using voltage waves, commensurate-length transmission lines and the bilinear transform, relationships between different domains is obtained. As just shown, an open-circuit unit element in the s-domain is represented as a capacitor in the ψ-domain and as a delay in the z-domain.

To summarize, to synthesize a lumped element filter to a wave digital filter first use a transmission filter and transform that into the ψ-domain and thereafter map this to the digital one.

1.4.5 Interconnection of elements

When interconnecting two networks with different characteristic impedance an adaptor must be used. Using the definition of voltage waves gives a wave description of the two port adaptor. A connection of two ports is shown in Figure 1-32.

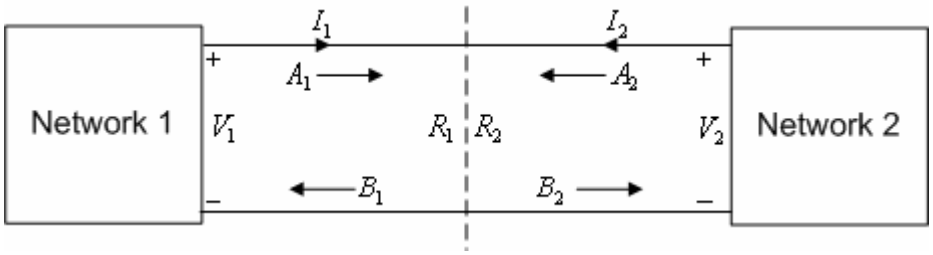

Figure 1-32: Transmission and reflection described by a two-port adaptor in s-domain

By using the definition for voltage waves, the waves at the two ports is given according to

$$\begin{cases} A_k = V_k + R_k I_k \\ B_k = V_k - R_k I_k \end{cases} \tag{1-52}$$

where $k = 1,2$.

Kirchoff´s voltages- and currents laws gives the relationships according to

$$\begin{cases} V_1 = V_2 \\ I_1 = -I_2 \end{cases} \tag{1-53}$$

Eliminating voltages and currents from equation (1-52), the relationship between the incident and reflected waves for the adaptor is

$$\begin{cases} B_1 = A_2 + \alpha(A_2 - A_1) \\ B_2 = A_1 + \alpha(A_2 - A_1) \end{cases} \tag{1-54}$$

where $\alpha = \dfrac{R_1 - R_2}{R_1 + R_2}$.

The wave-flow graph for equation (1-54) is shown in Figure 1-33 and Figure 1-34. For $R_1 = R_2$ corresponding to $\alpha = 0$, which means no reflection. For $R_2 = 0$ corresponding to $\alpha = 1$ and the incident wave at port 1 is reflected and is phase-shifted by 180^{O} and $R_2 = \infty$ corresponding to $\alpha = 1$ which means incident wave is reflected by no phase-shift. The phase-shift of 180^{O} corresponds to a multiplication by -1.

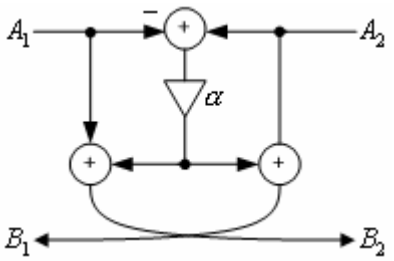

Figure 1-33: Wave-flow chart for the symmetric two-port adaptor in z-domain

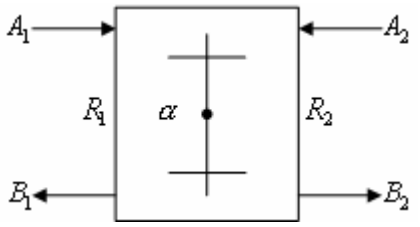

Figure 1-34: Symmetric two-port adaptor

Other adaptors are also available, but the symmetric two-port adaptor is common in the lattice structure, which is handled in this thesis.

1.4.6 The lattice WDF

An analog lattice filter illustrated in Figure 1-35 is not used in practice, other than measurements, because it has very high stopband sensitivity. However, the passband sensitivity is very low and if a digital implementation is performed, the high sensitivity in the stopband would not be a problem due the high resolution in digital circuits. For example, with 10 bits the resolution is 0.0009765625. Accuracy like that is not possible to reach with standard analog components.

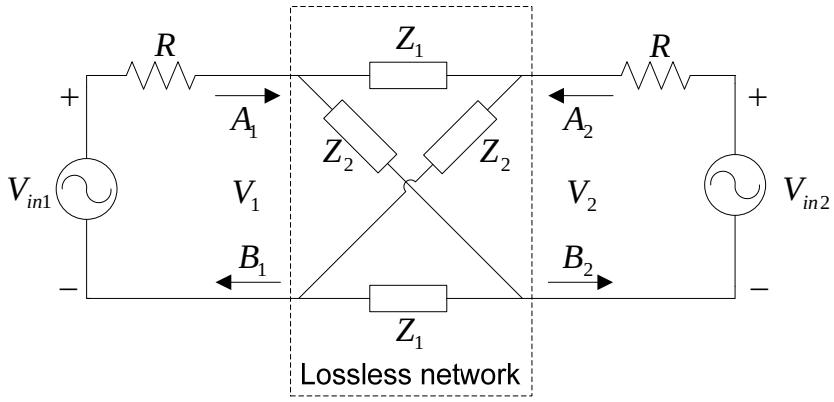

Figure 1-35: An analog lattice lossless network

The incident and reflected wave on port two in Figure 1-35 is given by

$$\begin{cases} A_2 = V_2 + RI_2 = V_{in2} \\ B_2 = V_2 - RI_2 \end{cases} \tag{1-55}$$

A scattering matrix defined in equation (1-56) can be used to describe the lossless network.

$$\begin{pmatrix} B_1 \\ B_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} = \begin{pmatrix} A_1 \\ A_2 \end{pmatrix} \tag{1-56}$$

By elimination of voltages and currents and some algebra gives

$$\begin{aligned} B_1 &= 0.5\left[S_1\left(A_1 - A_2\right) + S_2\left(A_1 + A_2\right)\right] \\ B_2 &= 0.5\left[S_1\left(A_2 - A_1\right) + S_2\left(A_1 + A_2\right)\right] \end{aligned} \tag{1-57}$$

where

$$\begin{aligned} S_{11} &= S_{22} = 0.5\left(S_2 + S_1\right) \\ S_{21} &= S_{12} = 0.5\left(S_2 - S_1\right) \end{aligned} \tag{1-58}$$

and

$$\begin{aligned} S_1 &= \left(Z_1 - R\right)/\left(Z_1 + R\right) \\ S_2 &= \left(Z_2 - R\right)/\left(Z_2 + R\right) \end{aligned} \tag{1-59}$$

If Z_1 and Z_2 are pure reactances, then S_1 and S_2 is two allpass-functions.

If the second voltage source is short-circuit and using the first one as source it will results in $A_2 = 0$ and the reflected waves is given by

$$\begin{aligned} B_1 &= 0.5\left(S_2 + S_1\right)A_1 \\ B_2 &= 0.5\left(S_2 - S_1\right)A_1 \end{aligned} \tag{1-60}$$

The transfer function H and the corresponding complementary transfer function is then

$$H = B_2/A_1 = S_{21} = S_{12} = 0.5\left(S_2 - S_1\right) \tag{1-61}$$

$$H_c = B_1/A_1 = S_{11} = S_{22} = 0.5\left(S_2 + S_1\right) \tag{1-62}$$

By using Feldtkeller's equation which states that input power is equal to output- and reflected power, the realization of the two transfer functions is given by

$$\left|H\right|^2 + \left|H_c\right|^2 = 1 \tag{1-63}$$

It can be shown that for a lowpass and highpass filter the order must be odd **[18]**.

A wave flow graph over an analog lattice filter is illustrated in Figure 1-36.

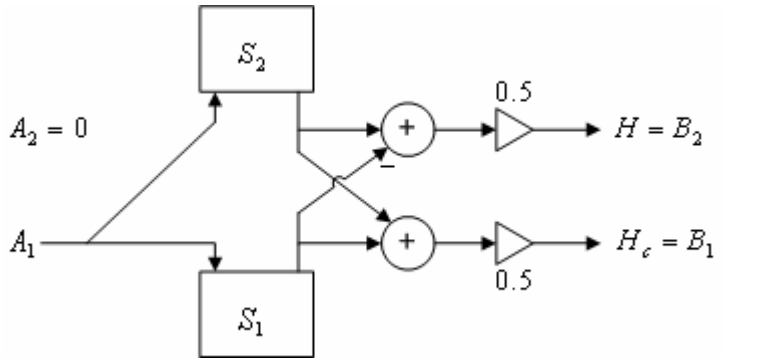

Figure 1-36: Wave flow graph

Hence, for a lowpass lattice filter, it is possible to use its complement to obtain a highpass filter. The allpass-functions S_1 and S_2 can be realized by using Richards' structures which are described in next section.

1.4.7 Richards' and circulator structures

An arbitrary reactance function can be obtained by a cascade of a number of lossless commensurate-length transmission lines as illustrated in Figure 1-37.

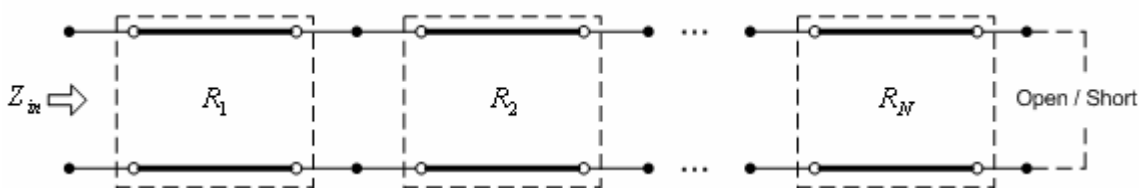

Figure 1-37: A reactive function realized in an N-order Richards' structure

It is possible to connect two or more Richards' structures with circulators, as illustrated in Figure 1-38. A circulator reflecting back incident waves at one port to next port.

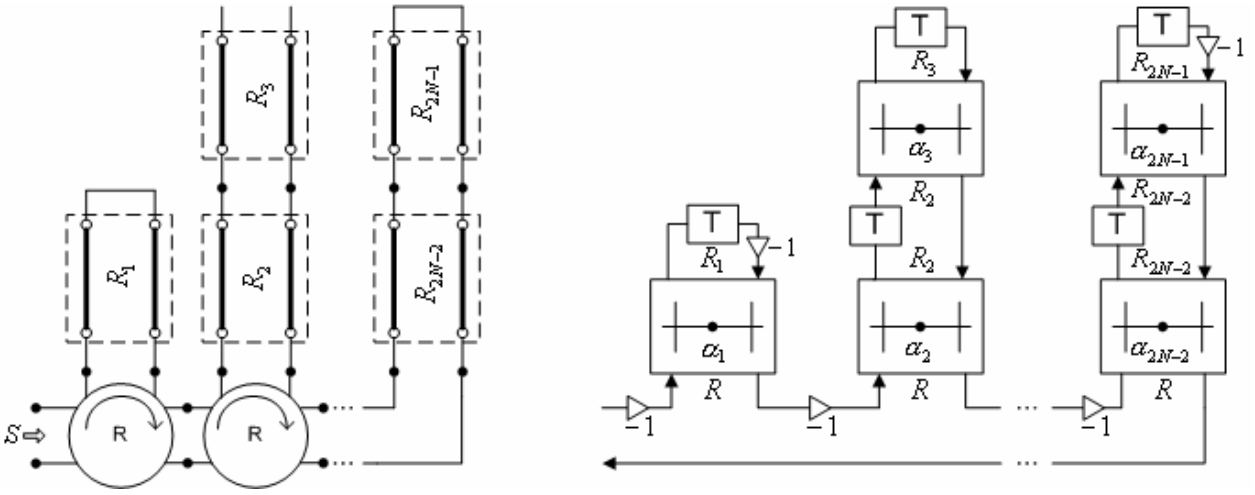

Figure 1-38: One- and two order Richards' structures in a circulator structure

A one- and two order Richards' structure can be written as allpass functions according to

$$S(z) = \frac{-\alpha_0 z + 1}{z - \alpha_0} \tag{1-64}$$

where $\alpha_0 = R - R_0 / R + R_0$ and

$$S(z) = -\frac{\alpha_1 z^2 + \alpha_2(1+\alpha_1)z + 1}{z^2 + \alpha(1+\alpha_1)z - \alpha_1} \tag{1-65}$$

where $\alpha_1 = (R - R_1)/(R + R_1)$ and $\alpha_2 = (R_1 - R_2)/(R_1 + R_2)$.

1.4.8 Bireciprocal lattice WDF

One of the most used filter is the Bireciprocal lattice Wave Digital Filter. It has the same properties as the Finitie Impulse Response halfband filter but with one disadvantage against these that it suffer of a non-linear phase, which is a problem with recursive filters. How to solve this will be explained later on.

One form of the bireciprocal lattice filter is illustrated in Figure 1-39. The upper output is a lowpass filter and the lower the complementary output, which is a highpass filter. The total transfer function is received just by adding the two branches transfer functions, according to

$$H(z) = \frac{1}{2}(H_0(z^2) + z^{-1}H_1(z^2)) \tag{1-66}$$

where H_0 and H_1 are allpass functions.

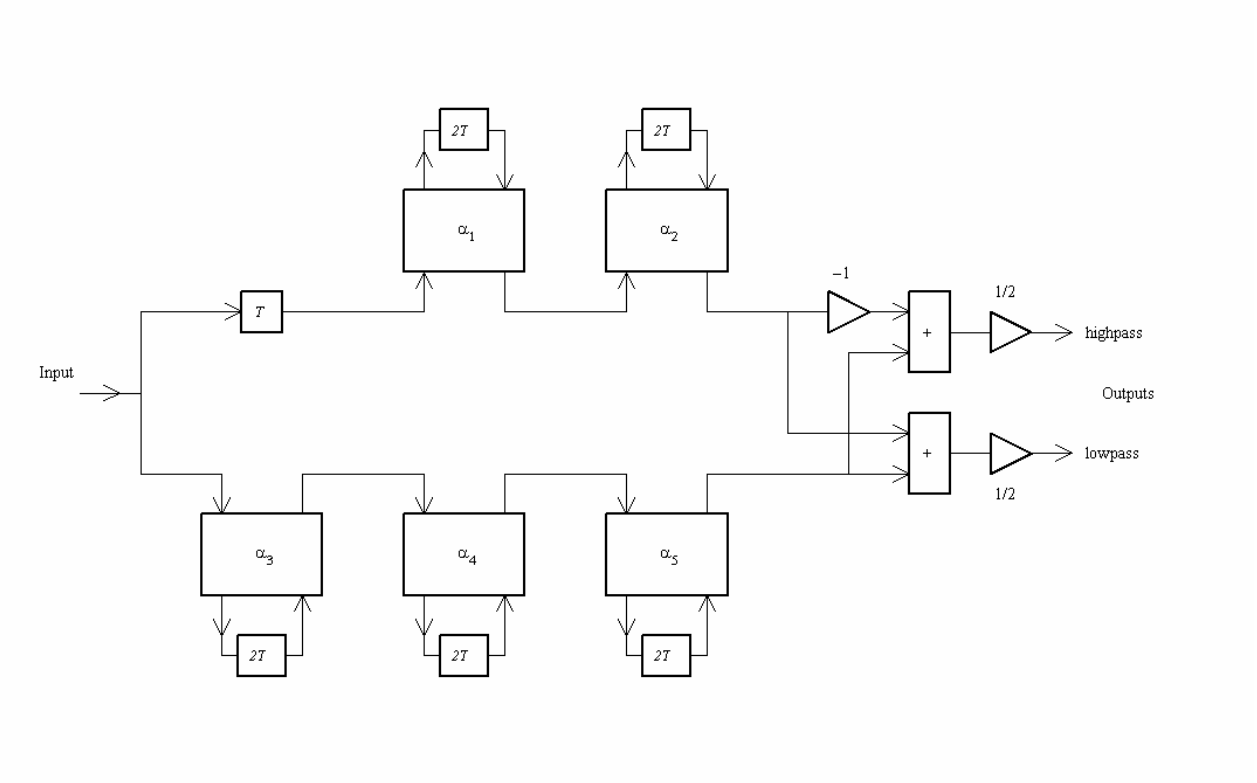

Figure 1-39: 11-order Bireciprocal Lattice Wave digital filter.

The frequency response for the filter is shown in Figure 1-40, with complementary frequency response is included.

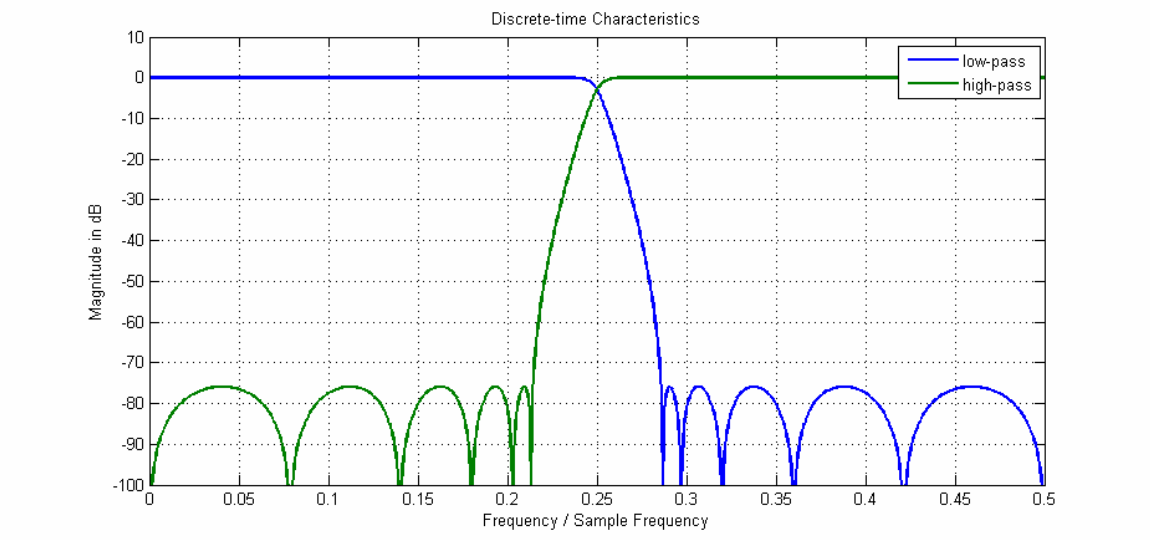

Figure 1-40: 11-order Bireciprocal Lattice Wave digital filter frequency response.

1.5 Hardware cost

In general it is difficult to estimate the cost in the hardware for a design, without consideration of the design implementation. However, by using assumptions and try to simplify, to a certain degree, it is possible to give an understanding of how much resources the implementation will require.

The most straightforward example may be a filter implementation in an FPGA. Multipliers are very expensive in FPGA architectures, due to the limited gates. Therefore, if one filter needs many multiplications, it does not mean that the filter implementation requires many multipliers. In many cases a multiplier can be a shared resource by utilizing a higher clock rate as illustrated in Figure 1-41 . That is true not only for multipliers but also for other operations.

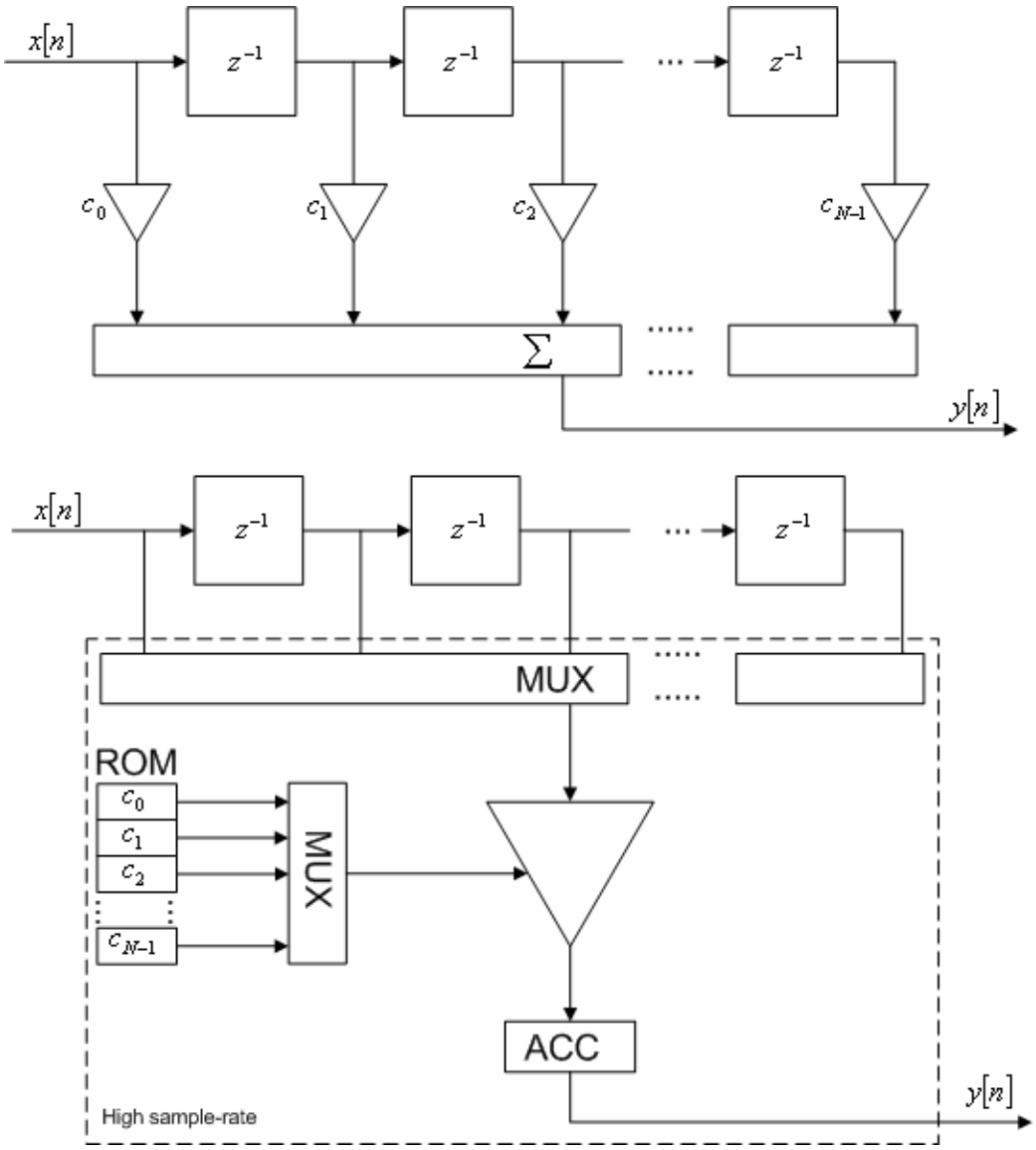

Figure 1-41: FIR filter with N-1 multipliers (upper). Same filter which utilize one multiplier running at high sample-rate.

Hence it is of greatest importance to take this into consideration when hardware costs of designs are compared. This section will explain how the hardware cost is estimated in the various filter designs, and introduce a model for a fair assessment between them.

1.5.1 FIR halfband hardware cost

There will be a need for multipliers, adders and memory for each FIR halfband filter. How many is decided by the length and placement in the chain. The closer to the highest sampling frequency the more multipliers and adders are needed. The basics are that one adder and one multiplier are required for every tap, which should make the necessary amount for instances equal to the filter length. But there are other things to take into considerations which will change this.

1. The instance works with a speed of $f_{\max}$ which makes it possible to use one instance per $f_{in} / f_{\max}$ times in every sequence.

2. Symmetry and a zero in every other tap in the filter reduce the number needed to one fourth, with reservation of the three center taps.

3. The instance shall be shared between the real and imaginary parts.

The number of instances relative high clock-rate for one part is given as

$$\#Add/Mult = \frac{f_{in}}{f_{\max}} \times \left(\frac{L-3}{4} + 2 \right) \tag{1-67}$$

Furthermore, a shift register bank is required to store the last L input values and allocating memory for the filter coefficients. Hence, the total memory for the halfband FIR filter is given according to

$$\#Bits = LW_{in} + \left(\frac{L-3}{4} + 2 \right) W_{coef} \tag{1-68}$$

where W_{in} and W_{coef} is the input- and coefficient bit width.

1.5.2 CIC hardware cost

As implies of the equations in the CIC theory section, the register width may become large for large rate factors and many sections, due the gain. The impact will be a cost in form of more required memory, mainly caused by the last stages where the gain is most affected.

To calculate the total memory required for the registers for a CIC filter, a summation of all register sizes is performed, according to

$$Mem = 2N \times B_{in} + \sum_{i=1}^{2N} W_i \tag{1-69}$$

where N is number of stages and W_i the register size of the present stage.

The adders that are running at the high clock rate are the main cost in a CIC filter. Number of required adders is given by

$$Adders = N(1+1/R) \tag{1-70}$$

where N is number of sections and R is the interpolation or decimation factor and with the condition that either the output or input sample rate is equal to $f_{\max}$.

For example, consider a CIC interpolation filter with design parameters according to

Table 1-3: **Design parameters**

Number of sections	6
Interpolation rate	8
Differential delay	1

By first calculate the gain and required register size for each stage, and furthermore calculate the number of required adders, the resulting required memory is shown in Table 1-4.

Table 1-4: **Required memory and adders for a CIC interpolation filter. Note that the number of input bits is not included here.**

	Stage number											
	1	2	3	4	5	6	7	8	9	10	11	12
Gain	2	4	8	16	32	64	32	128	512	2048	8192	32768
Size	1	2	3	4	5	5	5	7	9	11	13	15
Adders required relative high clock frequency									6.75			
Required extra dedicated memory in bits due the gain									80			
Total memory with input bits									12*[Number of input bits]+80			

A compensation filter is often involved together with the CIC filter. In normal conditions, one usually uses the CIC filter for large rate factors. The compensation filter may be a symmetric FIR filter and the hardware cost is estimated as the same way as for the halfband FIR filter with reservation for the non zero taps.

1.5.3 WDF hardware cost

The lattice WDFs that are used in the solution are build up with modular blocks. Each block looks the same, which makes it easy to calculate the hardware cost based on which filter order used.

For every block there will be a need of 1 multiplier, 3 adders and 1 delay. The number of coefficients can be done by using

$$Multipliers = \frac{M+1}{4} \tag{1-71}$$

where M is the filter order. Moreover, number of coefficient is equal to the number of adaptors used in the filter and the number of adders is

$$Adders = Multipliers \times 3 + 1 \tag{1-72}$$

2 Evaluation and results

2.1 Evaluation

To compare and evaluate the filters we will use EVM (Error Vector Magnitude) and ACLR (Adjacent Channel Leakage Ratio). This chapter will give a short explanation of the two different measurement methods.

2.1.1 EVM

EVM is used for measure vector modulated signal accuracy in a transmitter or receiver. A system that is using any vector modulation format would have all constellation points at ideal locations on the IQ plane. Unfortunately, due imperfectly filtering, noise and other error sources, there will be some deviation.

The EVM can be performed at different stages in a communication system, it is not necessary to measure the whole system. The measurement helps the designer to troubleshoot and get an insight in the quality of the received signal. It is necessary that the input signal is long enough, otherwise the measure will not converge. The EVM is used to compare different filter implementations with each other. To evaluate the suitability for a specific solution, a BER (Bit Error Ratio) test must be performed **[10]**.

EVM is the root-mean-square error between an ideal constellation point and the actual symbol in the IQ plane at an optimal clock transition. The EVM for a vector modulation can be expressed as **[8]**

$$EVM_{RMS} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\frac{|S(k)-R(k)|^2}{|R(k)|^2}} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\frac{[\mathrm{Re}(S(k))-\mathrm{Re}(R(k))]^2-[\mathrm{Im}(S(k))-\mathrm{Im}(R(k))]^2}{[\mathrm{Re}(R(k))+\mathrm{Im}(R(k))]^2}} \quad (1\text{-}73)$$

where $R(k)$ and $S(k)$ are complex numbers, representing the ideal position and the actual position on the received signal at the sampling instant k, as shown in Figure 2-1.

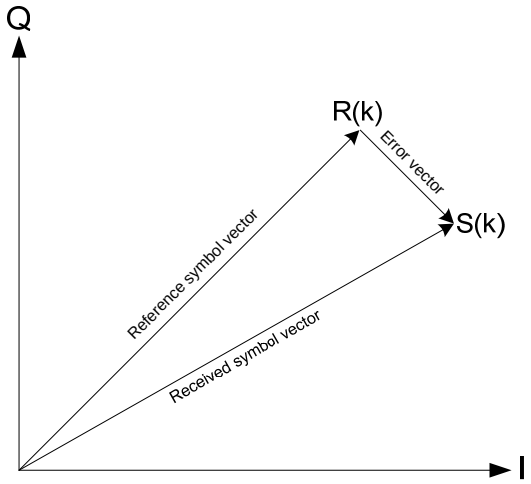

Figure 2-1: EVM in one quadrant

The definition above is just for measuring the vectors. However, other specifications of how to performing an EVM is provided from current standard authorities, for instance in **[1]** at 3GPP (3rd Generation Partnership Project), which is present in this project.

2.1.2 ACLR

The Adjacent Channel Leakage Ratio (ACLR) determines how much of the transmitted power or interference is allowed to leak into adjacent channels. The measurement is made through the ratio of integrating the power over an ideal RRC filter convolved with the current channel and an ideal RRC filter convolved with the adjacent channel. This is fully described in **[1]**.

2.1.3 EVM and ACLR demands

The demands, EVM and ACLR will be the same for every solution.

$$\begin{cases} EVM \leq 0.5\% \\ ACLR \leq -90dB \end{cases}$$

One important thing to point out is that in this evaluation, the RRC filters, that pulse shapes, are held fixed.

2.2 FIR halfband

This section will present the result for a TX-chain consisting of an RRC-filter and interpolating FIR halfband filters. This may represent the most common way to do interpolation with lower interpolation or decimation factors.

A straightforward way to design the chain is shown in Figure 2-2. The pulse-shaping RRC-filter first followed by interpolating FIR halfband filters with decreasing passband width.

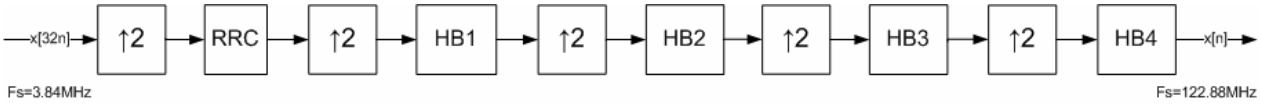

Figure 2-2: TX-chain

Table 2-1: Specification

	Passband width, ω_c [rad/s]	Stopband attenuation, $A_{\min}$ [dB]	Resulting order
HB1	0.33π	90	30
HB2	0.17π	90	14
HB3	0.08π	90	6
HB4	0.05π	90	6

It is important to consider the passband width when designing a halfband filter. A wide passband result in a high order, which will have significant impact on the hardware cost, at least for the latter filters in the TX-chain.

The frequency response is shown in Figure 2-3 and Figure 2-4, where the fourth side-lobe is attenuated with approximately $90dB$. The passband ripple present is small and that will lead to a small EVM.

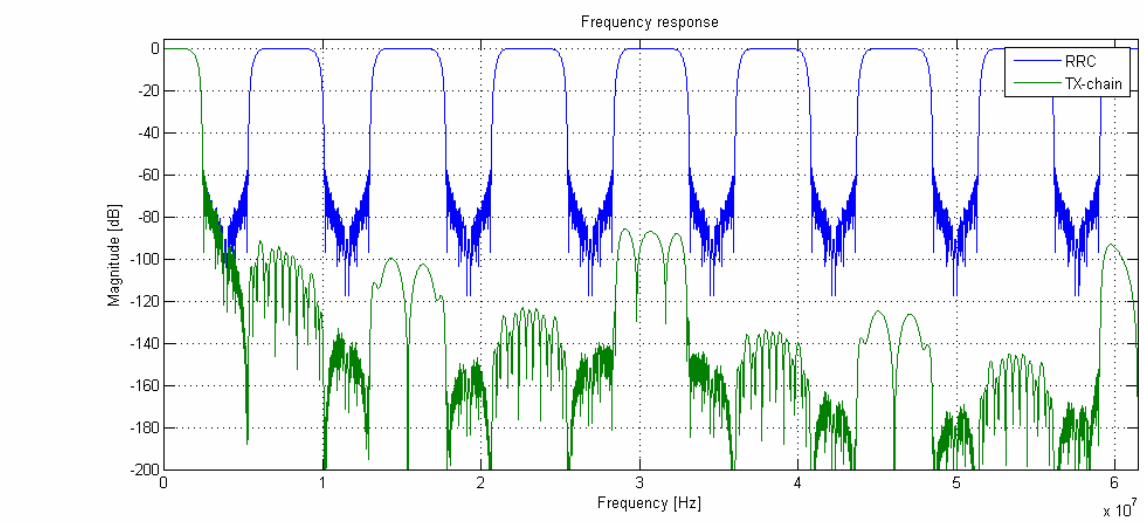

Figure 2-3: Frequency response for the TX-chain

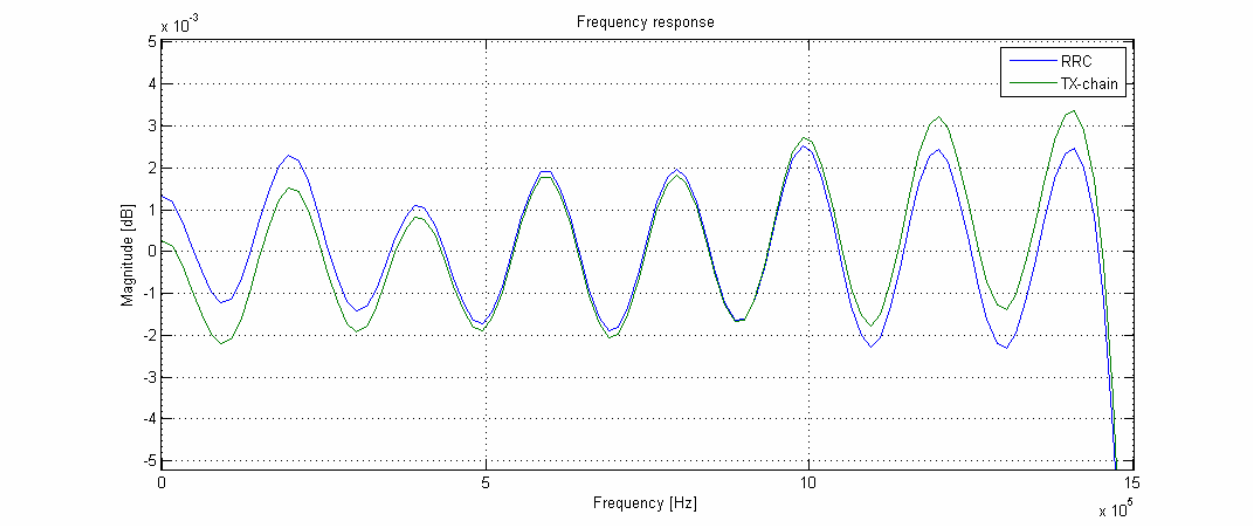

Figure 2-4: Frequency response for the TX-chain

The performance is shown in Table 2-2 and the hardware cost in Table 2-3. The hardware cost is calculated according description in section 11.5.1.

Table 2-2: Performance

EVM [%]*	0.13
Maximum ACLR [dB]*	-88.2

*(with 16 bits data width)

Table 2-3: Hardware cost

Adders relative high sample-rate	3.25
Multipliers relative high sample-rate	3.25
Memory required*	1300

*(with 16 bits data width)

To minimize hardware cost, quantization of the coefficients are performed which have a negative effect on the performance. First, same quantization is applied on all filters, except the RRC-filter.

Table 2-4: Quantization and its impact on performance

Quantization [bits]	EVM [%]	Maximum ACLR [dB]
17	0.13	-88.2
15	0.14	-88.7
13	0.14	-75.2
11	0.19	-69.6
9	0.46	-52.2
7	1.57	-42.4
5	3.47	-30.9

Both EVM and ACLR are affected of quantization which is no surprise. However, the most interesting property is when FIR half-band filters are compared with low sensitive lattice WDF filters.

It can be stated that it is possible to perform harder quantization on the latter filters in the TX-chain. A hard quantization on the first FIR halfband will destroy the signal while on the latter one does not have same impact on the performance.

To summarize, the FIR halfband filter is simple to design, hardware cost effective and has moderate coefficient sensitivity. When optimizing a chain, the latter ones in the chain should be handled first, because they are most expensive due to the high sample-rate.

2.3 CIC

This section will present various results for the CIC filter, in terms of hardware cost and performance, i.e. EVM and ACLR. A comparison between chains consisting of CIC versus halfband filters will also be presented and when it will advantageous to use the CIC filter for a WCDMA signal.

2.3.1 Design of the TX-chain – first approach

The TX-chain is supposed to pulse-shape and interpolate by 32. It is determined that the RRC filter is used for the pulse-shaping and also interpolates by 2. The first approach is to see the performance of the RRC followed by the CIC with interpolating factor by 16.

The RRC filter is running at low sample rate and should be placed before the CIC filter to minimize the hardware cost, as shown in Figure 2-5.

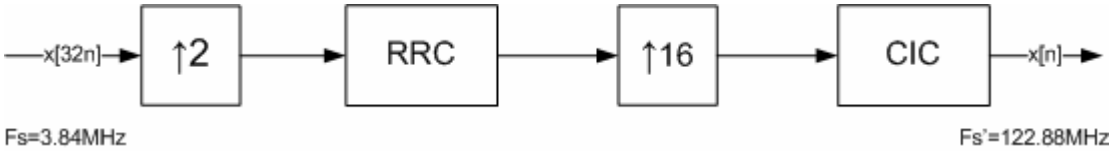

Figure 2-5: First approach of the TX-chain.

A moderate length, $N \leq 2$ of the CIC filter is chosen to not destroy the signal due to much attenuation in passband according to Table 1-1, the resulting frequency response is shown in Figure 2-6 and Figure 2-7.

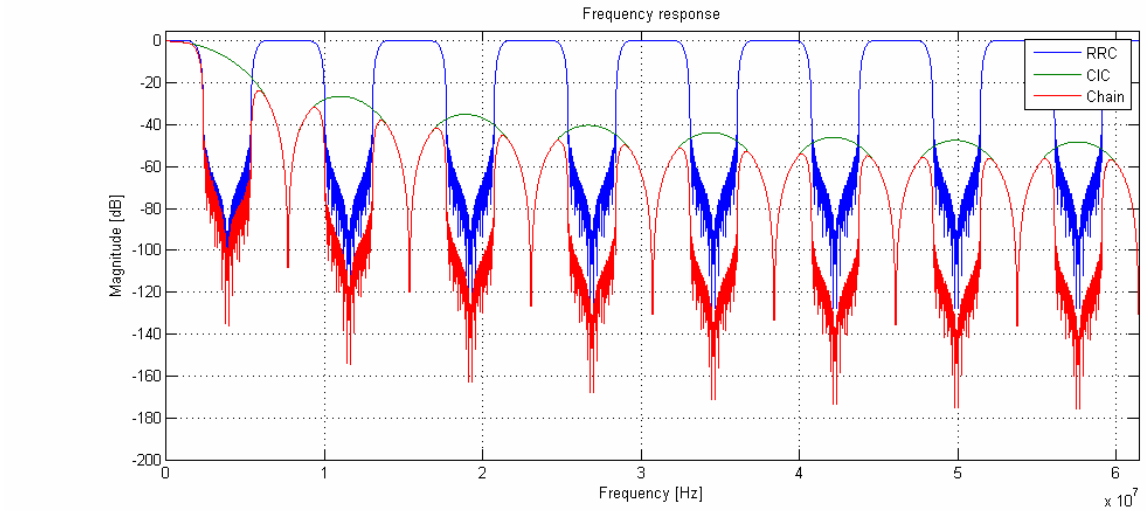

Figure 2-6: Frequency response of the first approach of the TX-chain, consisting of a RRC- and a CIC filter.

The frequency response shows that the attenuation of the images components is poor. The first component is only attenuated with approximately $25dB$. This will not be accepted due poor ACLR values, it is obvious that more stages or decreasing of relative bandwidth are required to reach an acceptable attenuation of imaging components.

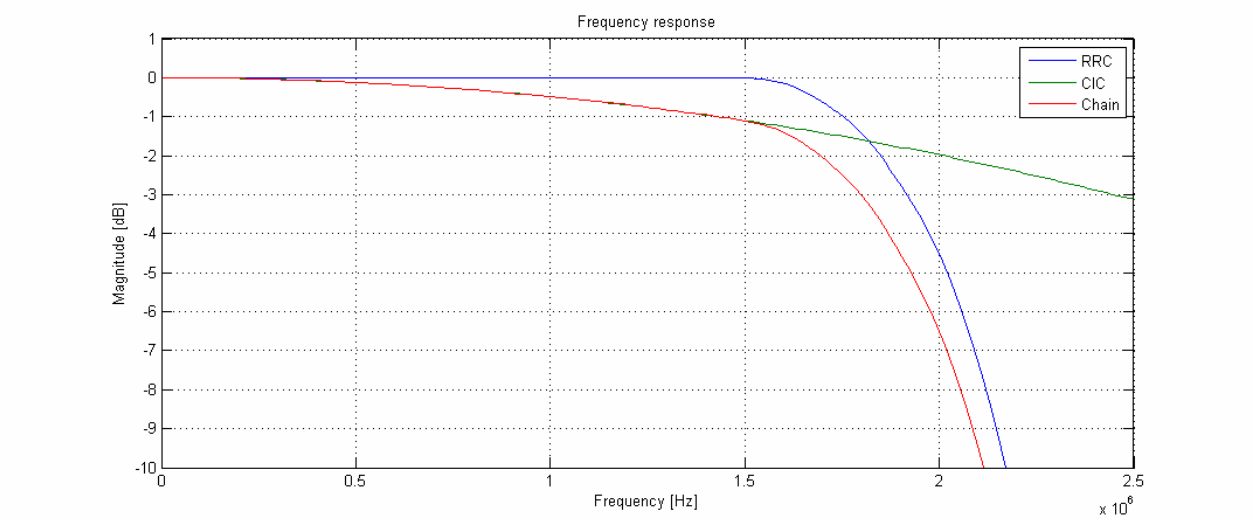

Figure 2-7: Attenuation in passband for the first approach of the TX-chain

Although the number of stages of the CIC filter only was limited by two, evident shortcomings in the passband are present. To get a flat passband, a compensating filter must be included in the chain.

These problems originate from the fact that the relative bandwidth of the signal is too wide. The bandwidth of the signal is $\beta = 2 f_c = 5MHz$. After the pulse-shaping the relative bandwidth is $f_{relative} = 2.5/7.68 \approx 1/3$, which is too wide for an practical and economical use of the CIC filter.

It may still be interesting to see the hardware cost and performance for this design.

Table 2-5: Hardware cost for the first approach of TX-chain

Adders relative high sample-rate	3.34
Multipliers relative high sample-rate	1.22
Memory required*	1965

*(with 16 bits data width of input signal)

Table 2-6: EVM and ACLR values for the first approach of TX-chain.

EVM [%]	2.09%
Maximum ACLR [dB]	$-30.16dB$

The hardware cost is calculated according description in section 1.5.2.

2.3.2 Design of the TX-chain – second approach

Design of the TX-chain – second approach
In the theory of the CIC-filter it was established that a wide relative bandwidth results in a non-flat passband and poor stopband attenuation.

Hence, at least three major improvements are possible:

- Make the relative bandwidth relative narrow, by interpolate at least by 2 before the CIC-filter.
- Increase number of stages of the CIC-filter to improve the rejection of imaging components.
- Insert a compensation filter to compensate for the attenuation in passband.

A second approach of a TX-chain result in a design is shown in Figure 2-8. By using a frequency sampling algorithm the compensation filter is designed to compensate for the passband attenuation in the CIC but also interpolates by two as well. A merger of that kind may be more cost efficient.

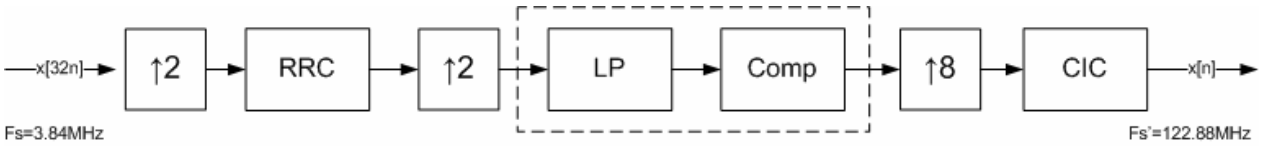

Figure 2-8: Second approach of the TX-chain

When the signal is being interpolated by 4, the relative bandwidth is $f_c = 2.5/15.36 \approx 1/6$ which will result in a better rejection of imaging components but also less attenuation in passband. The resulting frequency response for the design can be seen in Figure 2-9 and Figure 2-10.

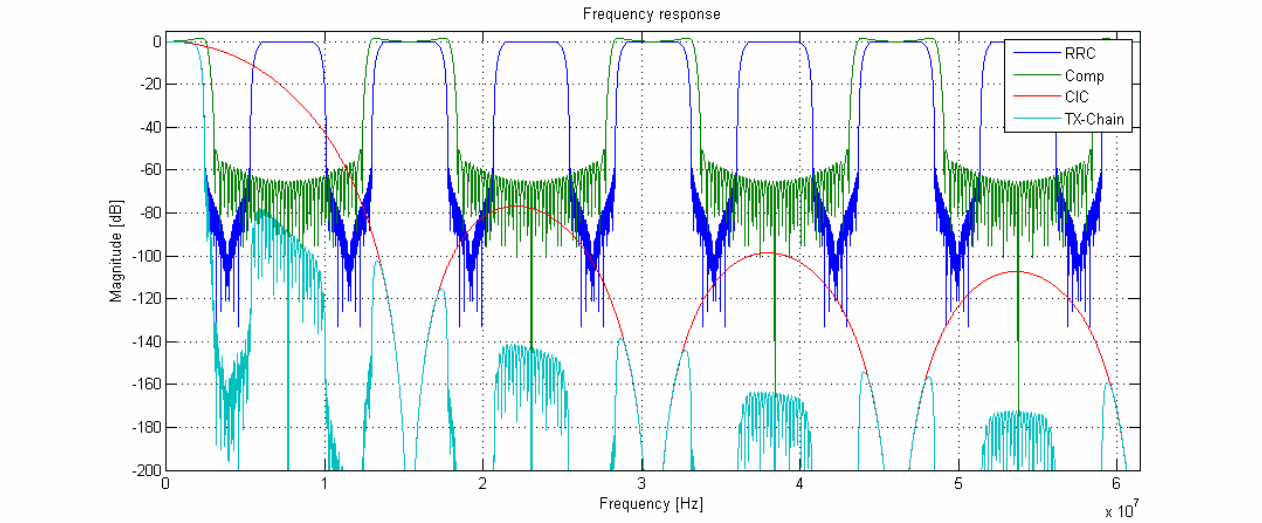

Figure 2-9: Frequency response for TX-chain with six stages and a differential delay of one.

The rejection of the first spectral component is approximately $80dB$, but the ACLR value for that channel will become better, due the average effect over that interval.

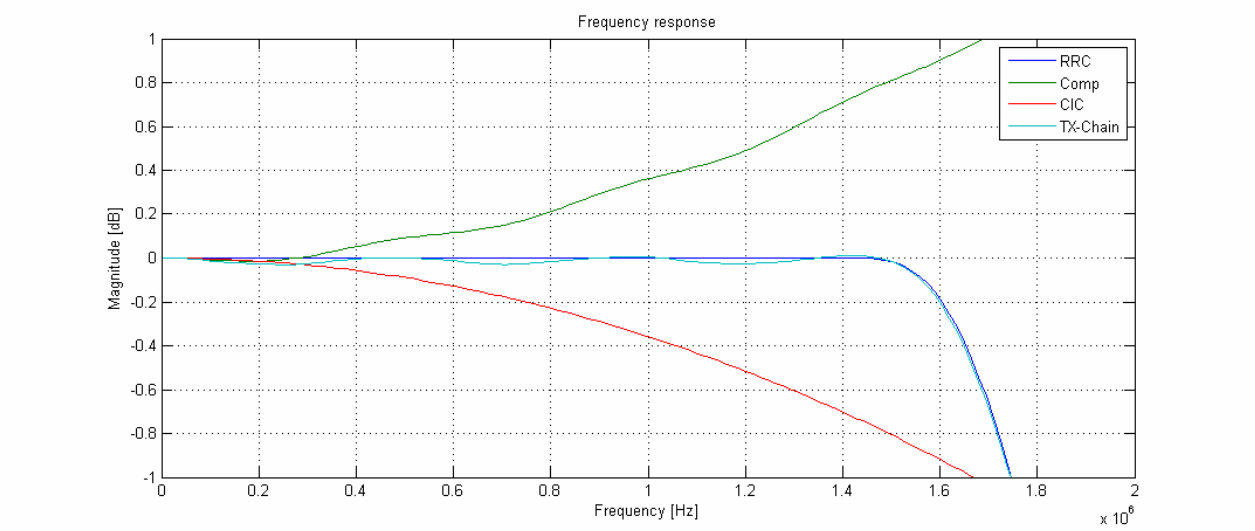

Figure 2-10: The frequency response in passband.

The compensation filter is designed as described in 1.3.6. The order of the compensation filter determines EVM and ACLR value for the first channel. A long order results in small ripple in passband and a high attenuation in stopband.

The hardware cost and performance result for this TX-chain is summarized in Table 2-7 and Table 2-8.

Table 2-7: Hardware cost

Adders relative high clock rate	8.75
Multipliers relative high clock rate	2.00
Memory required*	1824

*(with 16 bits data width of input signal)

Table 2-8: Performance

EVM [%]*	0.18
Maximum ACLR [dB]*	-87.0

*(with 16 bits data width of input signal)

The multipliers are a result of the long order compensation filter. As stated before, for wideband signals and for low resampling factors the CIC may not be the optimal choice. An analysis on that issue will be made in the next section.

2.3.3 The CIC filter versus FIR halfband filters for WCDMA signals

It is interesting to see when it will be profitable to use a TX-chain consisting of a CIC-filter compared with others. As mentioned in the theory section, the relative bandwidth of the signal must be sufficient narrow, therefore a rule of thumb can be stated: Due the main lobe gain reduction usually limits the input signal bandwidth to be less than 25% of the main lobe width **[5]**, which was also performed in section 2.3.1 and 2.3.2.

Hence, the test starts with an oversampling by 8:1 to satisfy the rule of thumb, as illustrated in Figure 2-11 and the specification for all stages is defined according to Table 2-9. For each stage a comparison in hardware cost is performed.

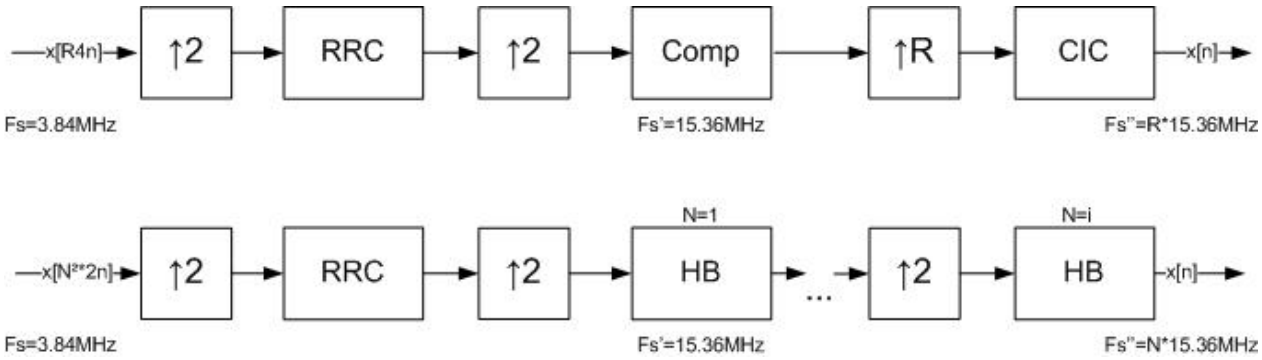

Figure 2-11: Two different TX-chains consisting of a CIC-filter and halfband-filters.

Table 2-9: Specification

EVM	$\leq 0.5\%$
ACLR	$\leq -90dB$
Relative bandwidth, f_{rel}	$2.5/7.68 \approx 1/3$

At this point it can be stated that halfband filters with high rejection in stopband lead to very small ripple in passband. Small ripple in passband combined with a linear phase results in a small EVM. Hence, with high rejection as $\leq -90dB$, the TX-chain consisting of halfband filters has an outstanding EVM. On the other hand, it is possible to archive a similar EVM for the TX-chain consisting of the CIC-filter also, but require a high order compensation filter.

For the case of simplicity both compensation filter and the CIC filter has a fixed length where the latter of $N = 6$, which is allowed as long as satisfy the specification. The halfband filters are of decreasing length. The result of the hardware cost is illustrated in Figure 2-12.

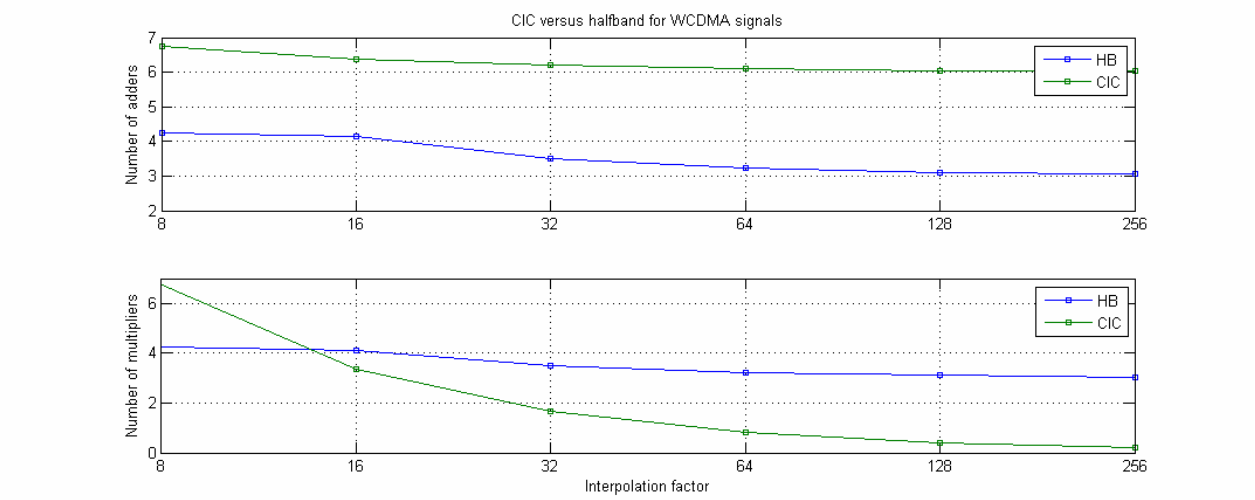

Figure 2-12: Hardware cost

From the figure above it can be stated that interpolation by CIC-filter gives a great reduction of multipliers for larger interpolation rates and that the number of adders converges to the length of the CIC-filter.

2.4 WDF

This section will present the results in terms of hardware cost and performance, i.e. EVM and ACLR, for filter chains consisting of bireciprocal lattice WDFs. The undesirable non-linear phase property inherited from the recursive structure, is solved with using an algorithm according to **[9]**.
Furthermore, a comparison in terms of coefficient sensitivity between FIR half-band and bireciprocal lattice WDF is performed.

2.4.1 Design of the TX-chain – first approach

The first approach for designing a TX-chain consisting of bireciprocal WDF is similar as for FIR halfband. This is shown in Figure 2-13.

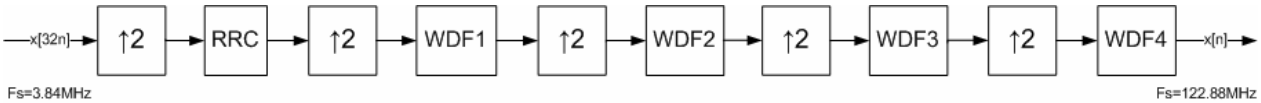

Figure 2-13: The first approach for the TX-chain consisting bireciprocal WDFs.

As usual, the long order pulse-shaping filter is located first followed by the interpolating bireciprocal WDFs. It is not necessary that all filters have the same stopband attenuation, nor same passband width. The specifications for the interpolating filters are shown in Table 2-10 and its respective order. The calculated coefficients are shown in Table 2-11.

Table 2-10: Specifications

	Passband width, ω_c [rad]	Stopband attenuation, $A_{\min}$ [dB]	Resulting order
WDF1	0.33π	70	9
WDF2	0.17π	70	7
WDF3	0.08π	70	5
WDF4	0.03π	70	5

As for FIR halfband, the passband ripple in a bireciprocal WDF is completely determined by the stopband attenuation, $A_{\min}$, due to the anti-symmetry in the bireciprocal filters. When required high attenuation in stopband it will result in an extremely small passband ripple, which is sometimes hard to compute even by double floating point precision. That is why a moderate attenuation, $\leq 70dB$ is chosen. Furthermore, a wide passband combined with high stopband attenuation results in a longer filter order. The cost for adders and multipliers relative high sample-rate will represent mostly by the latter filters, as before.

Table 2-11: Adaptor coefficients

	WDF1	WDF2	WDF3	WDF4
α_1	-0.079879760742188	-0.081527709960938	-0.124755859375000	-0.124755859375000
α_3	-0.283859252929688	-0.315917968750000	-0.562606811523438	-0.562606811523438
α_5	-0.545349121093750	-0.709976196289063		
α_7	-0.834426879882813			

It will result in a filter as shown in Figure 2-14.

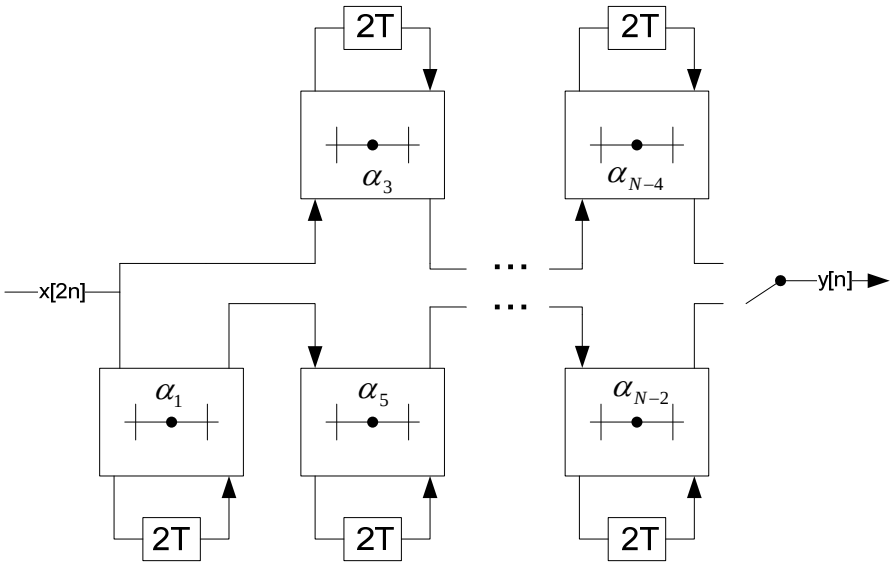

Figure 2-14: A Nth order bireciprocal lattice WDF in polyphase form

The frequency response of the TX-chain is showed in Figure 2-15 and Figure 2-16.

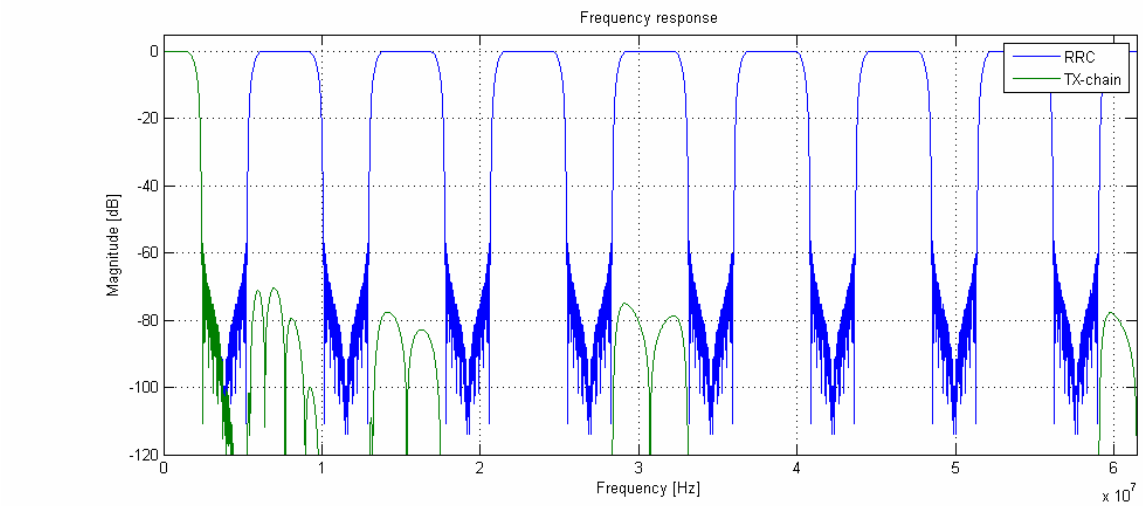

Figure 2-15: Frequency response for TX-chain with different specifications of the WDFs.

The frequency response show pretty good attenuation of imaging components, a descent, but maybe not acceptable ACLR value should be expected.

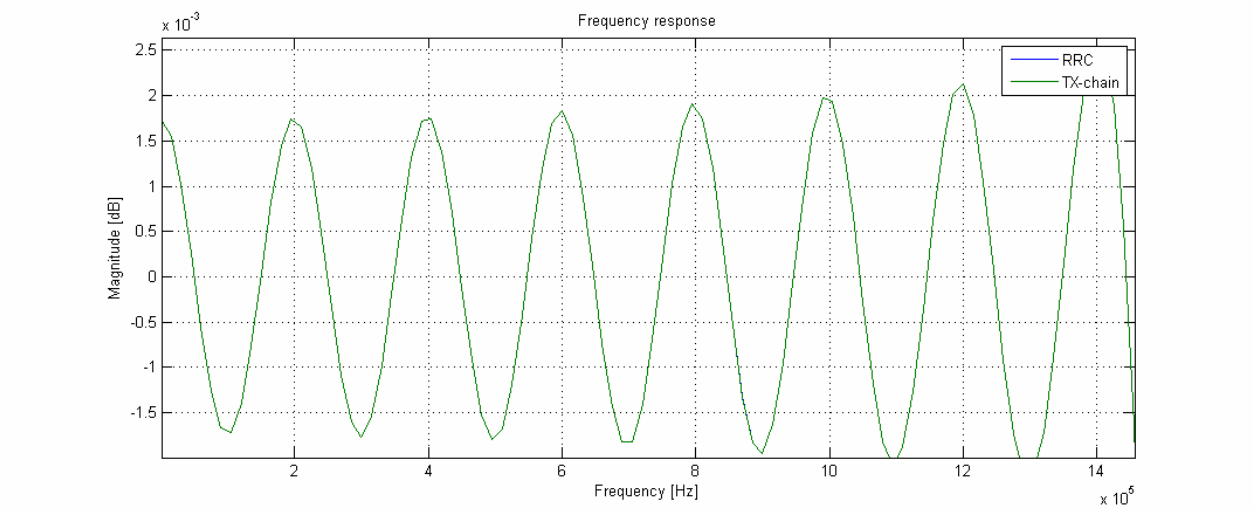

Figure 2-16: An extremely small passband ripple.

As predicted, a small passband ripple is present. By following the argument that a flat passband is optimal for a small EVM, this would be perfect in an EVM perspective. However, it turn out that it is not, due the non-linear phase delay.

Table 2-12: Performance

EVM [%]	1.86
Minimum ACLR [dB]	-142.5
Maximum ACLR [dB]	-78.0

The non-linear phase delay results in a non-constant group delay, for different frequencies it will be different propagation time as shown in Figure 2-17.

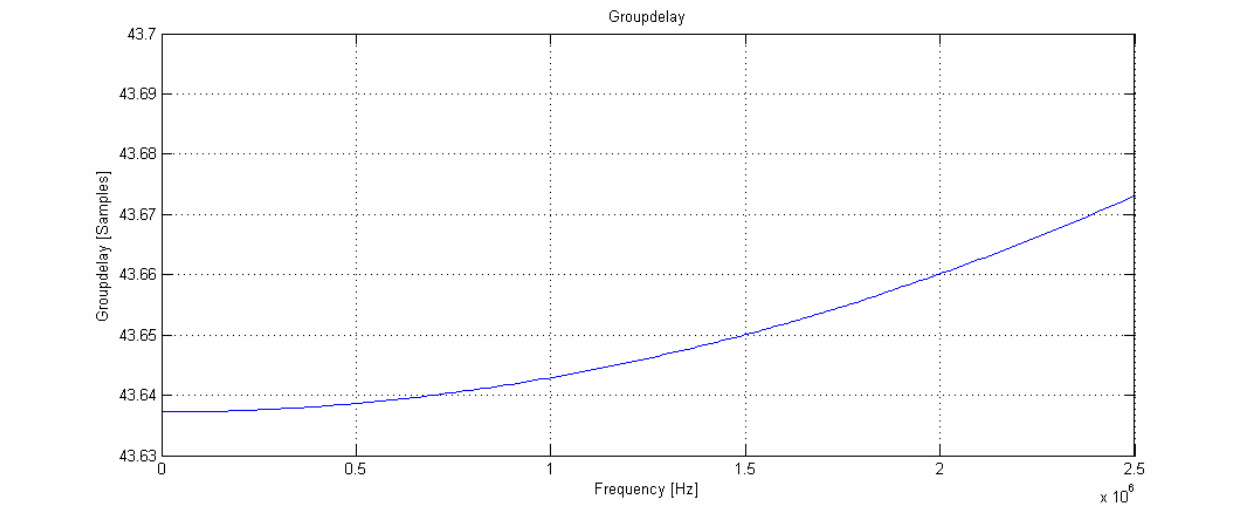

Figure 2-17: Groupdelay in passband

The group-delay outside the passband are neglected, these frequencies are attenuated anyway and will have an insignificant affect of the EVM.

The hardware cost is calculated, as described in the theory section, results are shown in Table 2-13.

Table 2-13: Hardware cost

Adders relative high sample-rate	6.38
Multipliers relative high sample-rate	2.13
Memory required*	363

*(with 16 bits data width of input signal)

The bireciprocal lattice WDF seems to be very efficient in a memory perspective. As mention in the theory, the WDF has very good sensitivity properties. That means that it is possible to quantize the coefficient and receive an even smaller memory cost. A quantization also brings smaller adders and multipliers and that is the strongest argument for using this kind of filters.

To summarize, the bireciprocal lattice WDF is hard to design with high stopband- or low passband attenuation, at least with the standard approximation. Non-linear phase in passband results in a non constant group-delay which affect EVM. To reach an acceptable level on ACLR and EVM it is required to increase stopband attenuation and minimize the phase ripple in passband.

2.4.2 Design of the TX-chain with nonlinear programming – second approach

In the first approach it was established that it is necessary to improve the stopband attenuation and minimize the phase ripple. That is accomplished by using nonlinear programming (NLP) which is a general approach for designing IIR-filters **[18]**.

Hence, NLP can be used to design filters with different requirements, such as magnitude response, phase response and step response. These requirements are handled simultaneously and may results in a satisfying design for all constraints.

The NLP technique is outside this scoop and is not handled here. The interested readers may look in **[18]**. However, an algorithm **[9]** proposed by Johansson and Wanhammar is used to obtain the coefficients for an almost linear phase lattice WDF.

In this algorithm, the filter order determines the stopband attenuation. Hence, try and error is performed until the required specification is reached.

Table 2-14: Specification

	Passband width, ω_c [rad/s]	Stopband attenuation, $A_{\min}$ [dB]	Required order
WDF 1	0.33	90	27
WDF 2	0.17	90	11
WDF 3	0.08	90	7
WDF 4	0.03	90	3

Table 2-15: Adaptor coefficients

	WDF 1	WDF 2	WDF 3	WDF 4
α_1	0.748489068901453	0.556328525667520	-0.467757822896096	-0.333969062723045
α_2	0.100883036880476	0.011038904457442	0.064322079791587	
α_3	0.305588418522756	0.116696953037980		
α_4	0.067976990119664			
α_5	0.147277442201018			
α_6	0.059104745970241			
α_7	0.418966848295443			

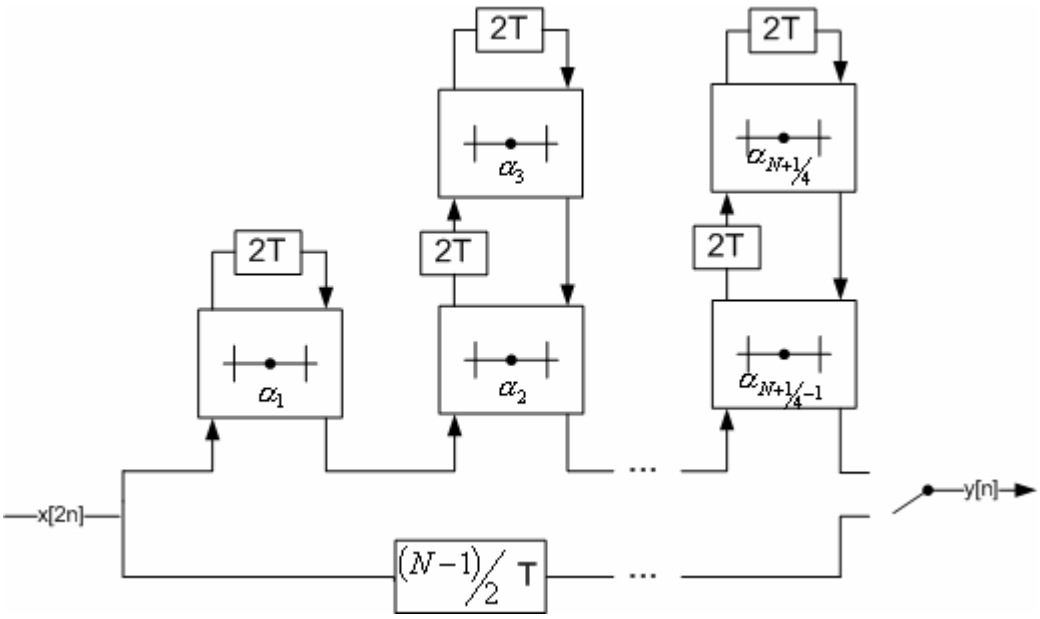

Figure 2-18: An almost linear phase Nth order bireciprocal lattice WDF in polyphase form

By numeric optimization the requirement of both magnitude and phase has been reached. The frequency response is shown in Figure 2-19. However, the most interesting result is the almost linear phase as shown in Figure 2-20.

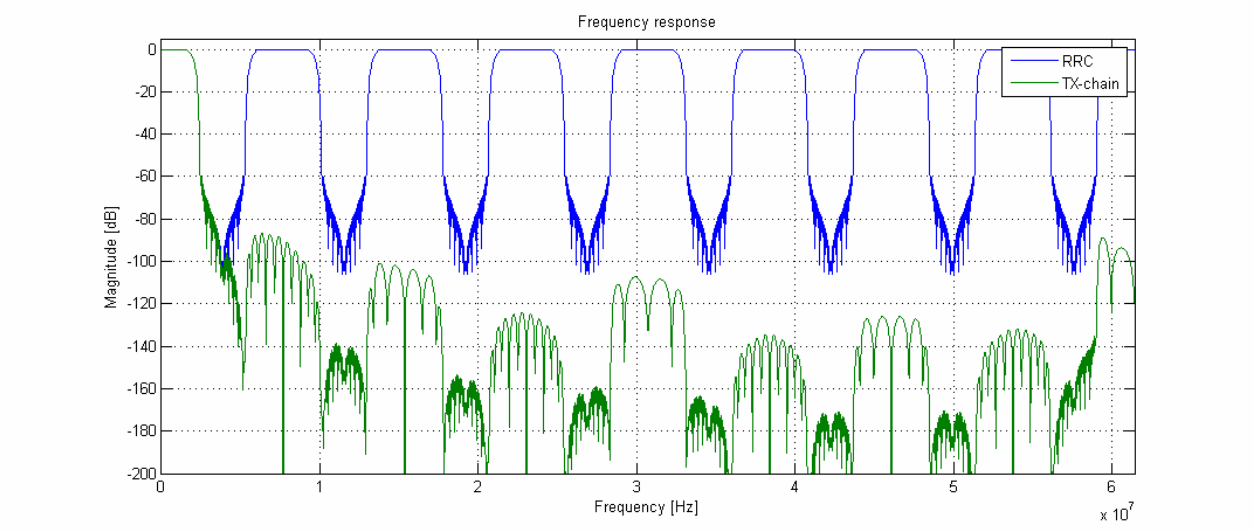

Figure 2-19: Frequency response

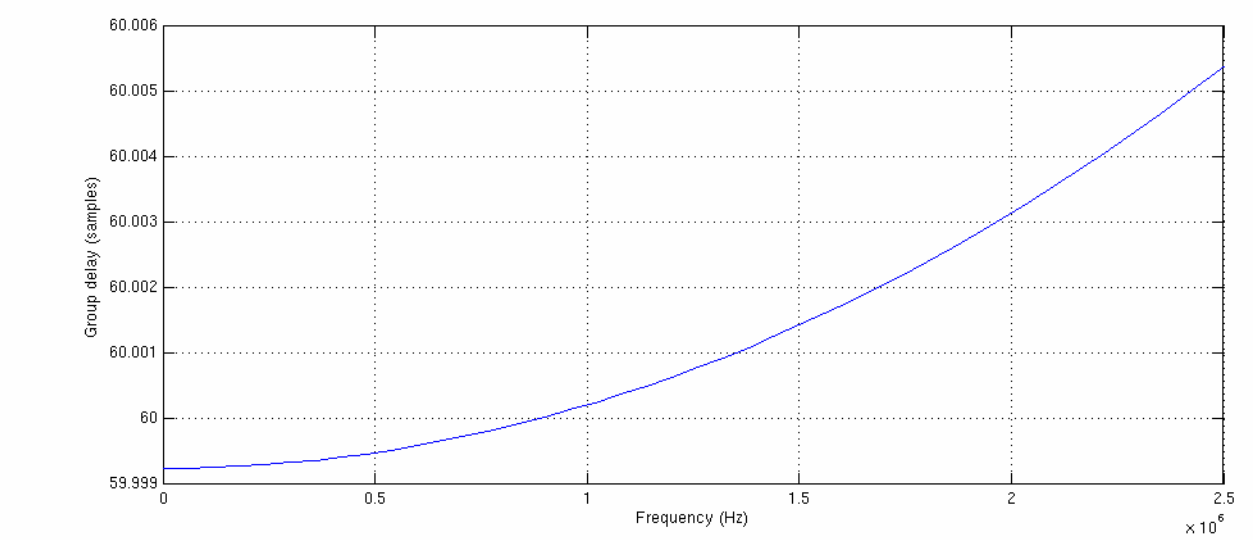

Figure 2-20: Group-delay

It was established that a flat passband is optimal for a low EVM but is also affected by the phase. With an almost linear phase, or equivalent, a constant group-delay, it may be interesting to see how the performance of the TX-chain is affected by quantization. The quantization is not applied on the pulse-shaping filter.

Table 2-16: Quantization and its impact on performance

Quantization [Bits]	EVM [%]	Maximum ACLR [dB]
17	0.15	-88.7
15	0.14	-88.7
13	0.14	-83.7
11	0.12	-69.8
9	0.20	-67.6
7	1.70	-44.6
5	2.04	-36.5

The results of the quantization may confirm the low sensitive property in passband of the lattice WDF structure due the low EVM. In contrast of low EVM is a high ACLR present, which confirm the high sensitivity in stopband.

Table 2-17: Performance (WDF)

EVM [%]	0.13
Maximum ACLR [dB]	-88.5

Table 2-18: Hardware cost (WDF)

Adders relative high sample-rate	5.25
Multipliers relative high sample-rate	1.75
Memory required*	908

To summarize, by using this algorithm an almost linear phase can be obtained at the same time as the magnitude constraint is satisfied, which is necessary to get a good performance.

However, the non-linear programming is hard to understand and similar results may be reached with utilizing of a phase-equalizer i.e. an allpass-filter cascaded with the TX-chain, the interested reader may look in **[21]**.

2.4.3 Bireciprocal lattice WDF versus FIR half-band

One of the most major reasons to use WDF is the low sensitive property in the passband for coefficient quantization, especially the lattice structure. As was established in the theory section and indicated in 2.3.1, the attenuation was clearly affected by quantization. That leads to a question of issue of overall characteristic compared with common half-band FIR filters.

It must be straight out that it is hard to do a comparison of a bireciprocal filter and a FIR half-band due the non-linear phase property and the different depending of the passband- and attenuation requirements.

By using the algorithm as described in 2.3.1 and FIR halfband filter makes it possible to compare them for a determined specification. The first analysis is to compare filters with a fixed passband width, $\omega_c = 0.45$ and see how the requirement of the attenuation affect hardware cost in form of adders and multipliers.

The results are presented in Figure 2-21, which shows that a bireciprocal lattice WDF is more efficient in hardware cost than its corresponding FIR halfband. It may be hard to weight an adder and a multiplier, but the fact that multipliers actually consists of adders, it can be stated that a multiplier always is more expensive than an adder and in what degree is depending on its implementation.

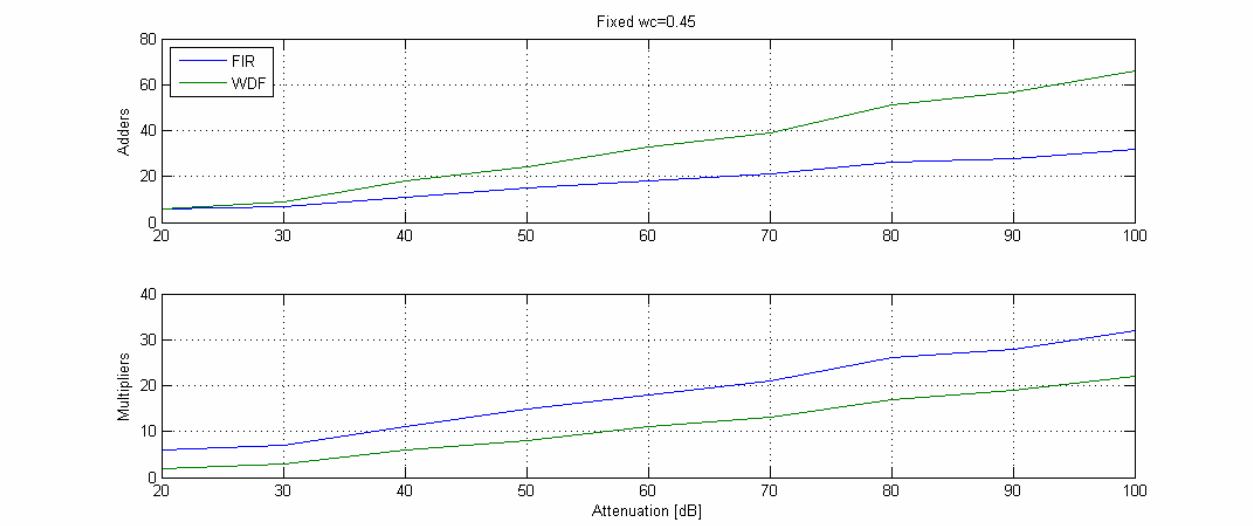

Figure 2-21: Adders and multipliers for different stopband attenuation.

A similar analysis is made but with different passband width for a fixed stopband attenuation of $A_{\min} = -90dB$. The results is shown in Figure 2-22 and reflecting the former result. The bireciprocal lattice WDF is probably a better choice both for variation in passband width and for different stopband attenuation.

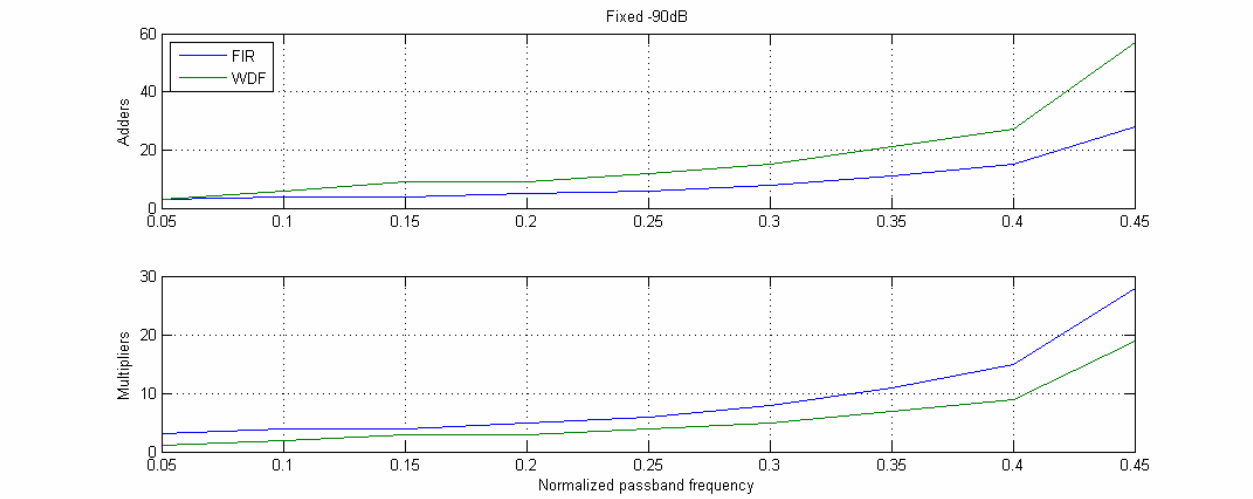

Figure 2-22: Adders and multipliers for different passband width.

Another interesting property may be the low sensitive in lattice WDF. This is shown in Figure 2-23 and Figure 2-24 for stopband and passband respectively.

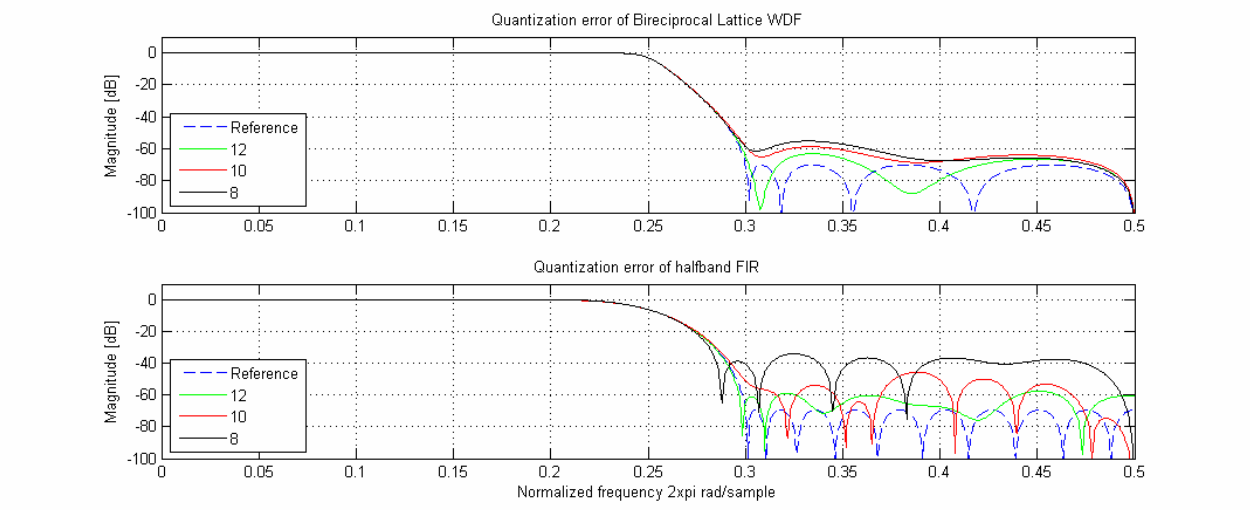

Figure 2-23: Quantization error

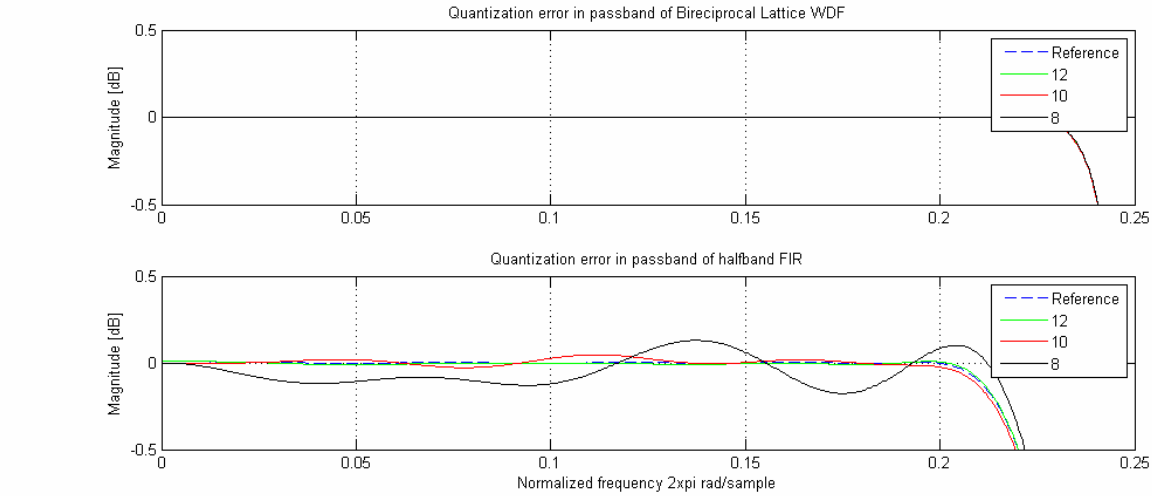

Figure 2-24: Quantization error in passband

Certain conclusions regarding bireciprocal lattice WDF can now be made

- They suffer of non-linear phase which may be solved by NLP, which are hard to understand. Alternative a phase-equalizer could be used instead.

- Good performance for less hardware cost. The bireciprocal lattice WDF may represent the properties for other kinds of filters, i.e. notch, bandpass, highpass.

- Although the bireciprocal lattice structure is sensitive for coefficient quantization in stopband, they are still better than FIR halfband.

3 Discussion and future work

The work progress has not been straightforward, mostly cause of the problem in dealing with what parameters to be considered and how to calculate and compare the hardware. The explanation for comparing chain versus chain, and not filter versus filter is due the fact that the CIC filter does not interpolate or decimate by factor two. Its compensation filter may also be used as RRC-filter. However, that is a future work.

It is hard to find information about WDF in textbooks and even harder to find implementation examples. The theory is based on an article of Fettweis, which can seem a little hard to understand and not really necessary to do. Another author, Gazsi, presents a way of directly designing the filters using formulas instead of designing the analogue filters before the digital without the need of understanding more than the concept of WDFs.

To get answers there have been contacts with people from LiTH and from TuDelft in the Netherlands. One of the main concerns regarding WDFs is why they are not more frequently used or not more mentioned in the literature, there have to be some bad side effects and not just positive ones.

One answer from the contacts is that they are just very hard to understand. But one might think that even if so and if very good alternative to FIR filters, someone would have designed a toolbox in tutorial or commercial purpose. One thought regarding this from Lincklaen from TuDelft. “I can imagine that when WDFs were introduced they were much too computational intensive for the hardware that was available then. Circuit- and-Systems-Theory people and Signal-processing people also did talk different languages. Have you ever tried to implement a WDF on a dsp-chip? Since dsp-chip usually contains a MAC-circuit-implementing a FIR filter is a snap.”

Further, Lincklaen have good future prospects for the WDFs “Lattice WDFs/all-pass implementations have been used more often, and maybe will (re)gain interest with FPGAs becoming more popular.”

So there are some possible answers that to the question of why not WDFs are more commonly used, even if a good alternative to FIR filters.

- Hard to understand
- Not as modular as FIR filters

When implementing the WDFs we had two possible solutions to use. One was to use the bireciprocal lattice WDF with an allpass filter to overcome the problem with the non-linear phase. The other was to use the algorithm and design the almost linear-phase bireciprocal LWDF. We decided to go with the latter one after some trying out. Something that had not really been considered then was the group delay which turned out to be quite large. Perhaps there is a different way to solve this problem that we have not thought of or there are better to use the first solution with the allpass filter which gives a much better group delay.

It would be of great interest to implement these solutions and this is something that could be done in future work. Also having a closer look at the RRC filter to see what, if possible, can be done with this one. This filter is quite large but also is placed in the beginning of the chain.

To sum up everything, both CIC filters and WDFs is shown to be of interest as an alternative to FIR filter but must be considered from case to case, depending on what filter specifications one may have and where in the chain the filter is located.

4 Conclusions

The objective of this work has been to compare two different recursive digital filters considering both hardware cost (i.e. multipliers, adders and memory) and performance (i.e. EVM and ACLR). The filters of interest were the CIC filter and the lattice WDF. Furthermore, also the FIR halfband has been examined, which may be seen as a reference in both hardware cost and performance.

It has also been established what kind of operations these filters are best suited for. Both are lowpass filters, mainly used for interpolation, decimation or in combination, including the FIR halfband. Interpolation- and decimation has been handled in a mathematical way to show the importance of a good lowpass filter in multirate systems. Pulse-shaping and ISI has also been handled because it is of big importance in different kinds of transmission systems.

The CIC filter has great properties such as no multipliers are required and variable interpolation- or decimation factor for the same compensation filter. It suffers of a droop in passband which may set demands on the required compensation filter. However, it turned out that the CIC filter is best suitable for narrowband signals with higher interpolation- or decimation factors, due the extra taps needed for the compensation filter.

The theory behind WDF originates from the microwave theory where voltage-waves and chain- and scattering matrixes are used. This is due to the delay-free loops that will occur if currents and voltages are used as signal parameters instead. By realizing a lossless network, such as a ladder- or lattice structure the desirable properties can be retained. These properties are the low sensitivity for nominal component changes, the guaranteed stability and the usage of the classical design methods and approximations for recursive analog filters.

To reach a fair comparison of the different filters, it was required to define the hardware cost and performance. It is hard to weight multipliers and adders due the fact that the number of adders inside a multiplier are depending on the bit-width and the adder structure, among others. Hence, a separation of adders and multipliers was required. To get a fair comparison, all instances are relative the highest sample-rate in the system. It was also interesting to see how much memory was required for each filter. For performance measurement, EVM and ACLR has been used which is strongly related to the passband- and group-delay ripple and the stopband rejection.

Problems with non-linear phase has been discovered which is an inherited undesirable property at recursive filters. For that problem a non-linear programming algorithm has been used which decrease the group-delay ripple. However, this problem is related only for the WDF and it should be noted that CIC filter does not produce any non-linear phase at all.

In addition to the tests related to the main task, different tests has been performed to archive knowledge when it payoff to use the proposed filters.

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