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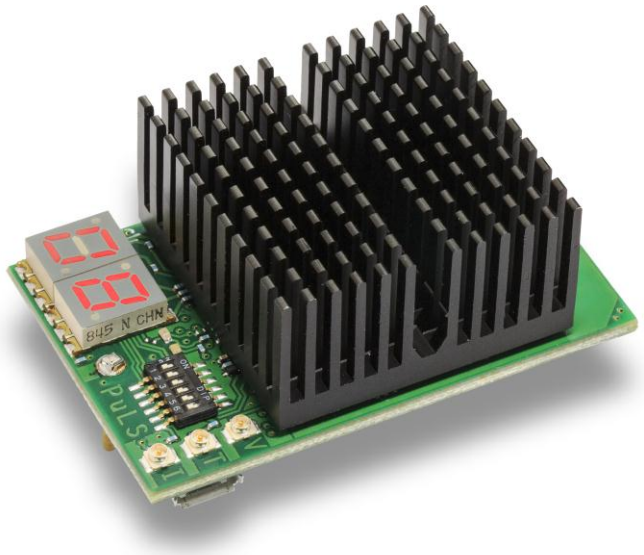

Analysis of the Output Impedance from Switched DC/DC Converters

Development of a new Measurement Method Using a Programmable Load

Master's thesis in Electrical Power Engineering

GUSTAV HANSSON
MARCUS UUSSALU

Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2014

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Cover: A picture of the PuLS taken for Ericsson AB.

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Abstract

The PuLS is a product used at Ericsson AB for performance testing of switched DC/DC converters by applying pulse shaped current waveforms. In this thesis, the PuLS is redesigned to be able to measure output impedance of switched DC/DC converters by drawing a sinusoidally shaped current while measuring the output voltage ripple. Existing measurement methods are investigated, the theoretical output impedance of a buck converter is calculated and simulations of two buck converters are implemented.

Output impedance measurements of two buck converters are done using the redesigned PuLS. The results are compared with an existing impedance measurement method as well as simulations of the buck converters. It is shown that the PuLS is able to measure the output impedance of switched DC/DC converters at frequencies up to 80 kHz with results close to both the simulation and the previously made measurements. At frequencies greater than 80 kHz, the PuLS measurements shows a greater impedance compared to the simulation and the previously made measurements. When measuring passive components it is shown that the PuLS can measure impedance in the frequency range of 0.5-500 kHz.

Index Terms: Active load, Electronic load, Converter, Output impedance, Frequency response.

Acknowledgements

Firstly, we would sincerely like to thank our supervisors Andreas Karvonen, Lukas Rosén and Bahar Motlagh for their time and effort guiding us during our thesis work. We would also like to thank our examiner Torbjörn Thiringer as well as the Power Solutions department for providing the supplies and equipment needed during the thesis work. This thesis has been carried out at Ericsson AB with support from the Department of Energy and Environment at Chalmers University of Technology. Lastly, We would like to thank all other contributes to the thesis not mentioned.

Gustav Hansson
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Abbreviations

AC	Alternating Current
ADC	Analogue to Digital Converter
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DUT	Device Under Test
FPGA	Field Programmable Gate Array
FRA	Frequency Response Analyser
GUI	Graphical User Interface
IC	Integrated Circuit
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
PCB	Printed Circuit Board
PMBus	Power Management Bus
PuLS	Programmable Micro Load
PWM	Pulse Width Modulation
SAADC	Successive Approximation ADC

Contents

1 Introduction

Over 40 percent of the worlds mobile data traffic passes through Ericsson AB networks. These networks, located in more than 180 countries, ramifies into millions of telecommunication sites. Switching DC/DC converters feeding amplifiers and other loads in the base stations at these sites are under constant development in order to improve efficiency and performance. Accurate testing of developed converters is a necessity to guarantee wanted specifications, a process that can be time consuming [1].

This master thesis is dedicated to shorten the verification process of developed converters saving both time and spendings. This is done by implementing an active electronic load as an impedance measuring device.

1.1 Background

The PuLS (Programmable Micro Load) is a small digital active load that is used for verification and testing of switched DC/DC converters developed at Ericsson using pulsed loads with controllable slew rates. As digital loads such as FPGAs (Field Programmable Gate Array) and microcontrollers gets faster and are using higher currents, it is necessary that the performance of the converters feeding these loads are verified for these fast variations. To ensure sufficiently low voltage variations on the output, the output impedance needs to be analysed in the frequency domain. Low output impedance of the design is crucial since any current change will result in a voltage ripple determined by the magnitude of the impedance. Other important design parameters are performance of the feedback loop for the regulator to ensure a fast and stable response of load variations and a well tuned output filter. The output filter can not be too large since it could affect the output impedance in a negative way and would make the system too slow, big and expensive [2].

Measuring the output impedance of a converter is a complicated procedure and can consume a lot of time and effort. To measure the output impedance, either a complete measuring system e.g. Venable or large set-ups with function generators, amplifiers and oscilloscopes/network analysers can be used. The system from Venable is automatic but is quite big and very expensive while other set-ups with oscilloscopes need to be analysed manually for each frequency tested. The observed output impedance is a combination of the output filter and the feedback loop as well as parasitic effects in the circuit.

The current version of the PuLS can only be used to draw a pulsed load. The purpose of this thesis is to investigate if the PuLS could be used as an output impedance measurement device. If it could be used, the advantages could be the easy setup, small size, low parasitic inductance mounting close to the load, fast measurement results and low cost.

1.2 Previous Work

There are several documented ways to measure the output impedance of a converter, although most of them are very alike. The common way to obtain the frequency response of the output impedance is to load a DC current and either inject or load an AC signal. By using this method, the AC characteristics of the output impedance can be obtained for different load levels by changing the DC current amplitude and the frequency of the AC signal.

The reason why the PuLS was developed is the slew rate limitation of commonly used active loads, such as the Chroma 63103A. To connect these big loads, long cables are usually required. These cables often have a relatively large inductance which limits the slew rate. Since the PuLS is a small compact circuit and is directly installed on the DUT (Device Under Test) during testing, the interconnection inductance is much lower. Another advantage with the PuLS is the easy configuration software. The software is used to control the slew rate, the amplitude and the duration time and the time between the pulses.

1.3 Purpose & Objectives

Since new IC (Integrated Circuit) loads e.g. FPGAs are very fast, the current used by them changes rapidly during operation. This means that high demand is put on the converters in terms of stability and speed at various frequencies. To be able to meet these demands, analysis of the converter output impedance is important. The frequency response is not only used to see that the magnitude of the impedance is low enough, it can also be used to see in which frequency range the controller operates in its stable region [2].

The purpose of this thesis is to investigate if the PuLS can be used as an output impedance measurement device for converters, and if so, how reliable the measurements are. Many impedance measurement setups are big and connected with long cables that increase the inductance of the circuit which affects the measurement results. The procedure is also time consuming, a working prototype could save time regarding the verification process of developed converters if a output impedance characteristic is requested.

2 Background

There are several documented ways to perform a frequency analysis of the output impedance of a converter. Some setups are similar and some are using different methods as will be later described in Section 2.4. Analysing this frequency response gives information of the load transient response and system stability. The converters analysed, both practically and theoretically, are in this report 1.8 V and 5 V Buck converters switching at 600 kHz developed by Ericsson. This section will cover the theory of a simple buck converter, its voltage control system and calculations on a buck converters output impedance.

Moreover, the since the PuLS is controlled by a microcontroller, some functions that the microcontroller uses within the specification of the PuLS will also be covered in this section.

2.1 Basic Theory of a Buck Converter

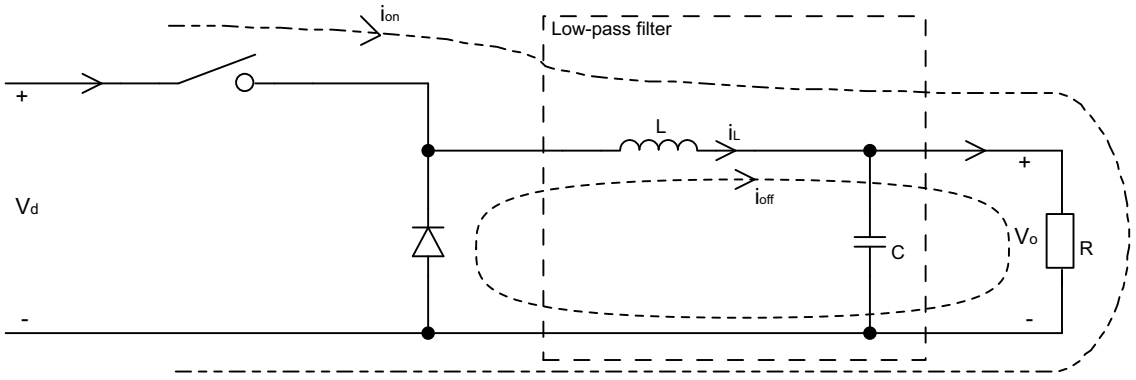

Figure 2.1: Schematics of a simple buck converter showing current paths when the switch is turned on or off.

The basic principle of an ideal buck converter, also called a step-down converter, is to step down the voltage level to a fixed output voltage. As seen in Figure 2.1 the current will take two different paths depending on if the switch is open or closed. Because of the different paths, the output voltage can be changed by controlling the duty cycle of the switches, i.e. the ratio of the time the switch is turned on. In steady state the waveforms must repeat, this means that the integral of one period must be equal to zero. This can then be written as

$$\int_0^{Ts} v_L\,dt = \int_0^{t_{on}} v_{L,on}\,dt + \int_{t_{on}}^{Ts} v_{L,off}\,dt = 0 \tag{2.1}$$

where v_L is the inductor voltage, t_{on} is the time where the switch is closed and T_s is the time of one switching period [3]. While $0 < t < t_{on}$ the voltage over the inductor is $V_d - V_0$ and while $t_{on} < t < T_s$ the voltage over the inductor is $-V_0$ as seen in Figure 2.2. Inserting this into (2.1) gives that

$$(V_d - V_0)t_{on} = V_0(T_s - t_{on}) \Rightarrow \frac{V_0}{V_d} = \frac{t_{on}}{T_s} = D \tag{2.2}$$

where D is the duty cycle.

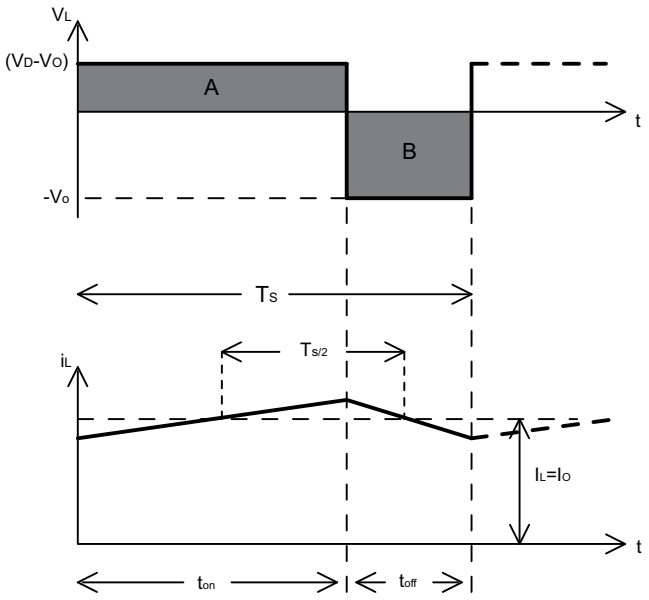

Figure 2.2: On and off states of the converter.

As the converter was considered ideal the input and output power is the same

$$P_d = P_0 \Rightarrow V_d I_d = V_0 I_0 \Rightarrow \frac{I_0}{I_d} = \frac{V_d}{V_0} = \frac{1}{D}. \tag{2.3}$$

Using the relation that the current in an inductor is the integral of the voltage over it and that the voltage over the inductor is $-V_0$ during the off time, the current ripple through the inductor can be calculated as

$$\triangle i_L = \frac{V_0}{L}(1-D)T_s \tag{2.4}$$

where L is the output inductance. The voltage over and the current ripple through the inductor is illustrated in Figure 2.2 and shows the relation between duty cycle, voltage and current ripple.

If the output capacitor is not considered infinitely large as in the previous analysis, V_0 is no longer considered a constant DC voltage. The output voltage has a ripple depending on the output filter. Further, if all the current ripple in the inductor is assumed to flow through the capacitor and its average value through the DC load, the area between i_L and I_0 when $i_L \geq I_0$ during $T_s/2$ as seen in Figure 2.2 is the accumulated charge of the capacitor, $\triangle Q$. The output voltage ripple can be calculated as

$$\triangle V_0 = \frac{\triangle Q}{C} = \frac{1}{C}\frac{1}{2}\frac{\triangle i_L}{2}\frac{T_S}{2} \tag{2.5}$$

where C is the output capacitance. If $\triangle i_L$ from (2.4) is inserted into (2.5) the output voltage ripple can be calculated as

$$\triangle V_0 = \frac{T_S}{8C}\frac{V_0}{L}(1-D)T_s \Leftrightarrow \{T_s = f_s\} \Leftrightarrow \frac{V_0}{8CLf_s^2}(1-D) \tag{2.6}$$

where f_s is the switching frequency. Note that the output voltage ripple is very dependent on the switching frequency where a high switching frequency lowers the output voltage ripple.

2.2 Control of Buck Converters

Since the input voltage and the load of a converter are usually not constant, the output voltage has to be controlled. The voltage is controlled by controlling the gate voltage of the switch, which means that the duty cycle is controlled. This method is called PWM (Pulse Width Modulation) switching. Figure 2.3 illustrates a block diagram of a PWM feed back loop. An amplifier is commonly used to increase the amplitude of the control voltage. The switching frequency is always constant when using PWM switching and the switch control signal is generated by comparing the error in the output voltage, $v_{control}$, with a saw tooth voltage, v_{st}. When $v_{control} > v_{st}$, the switch control signal is on and when $v_{control} < v_{st}$, the signal is off which can be seen in Figure 2.4 [3]. This is adjusted by the comparator.

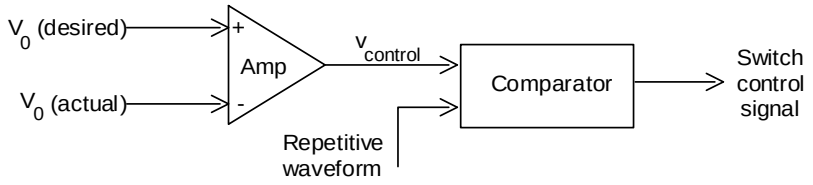

Figure 2.3: Block diagram of a PWM feed back loop.

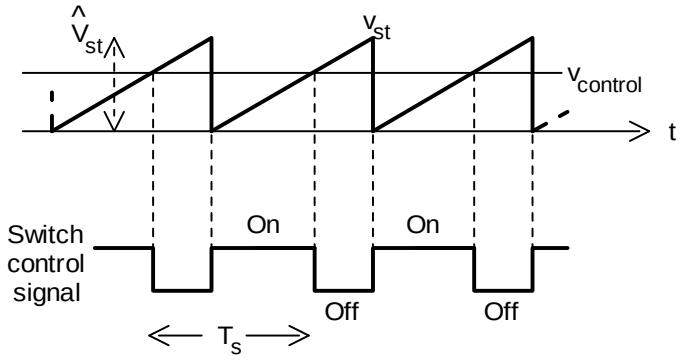

Figure 2.4: Comparator signals of PWM switching with v_{st} as a sawtooth voltage and $v_{control}$ as the amplified error signal.

The duty cycle can be calculated as

$$D = \frac{t_{on}}{T_s} = \frac{v_{control}}{\hat{V}_{st}} \tag{2.7}$$

where $\hat{V}_{st}$ is the peak of v_{st}.

2.3 Theoretical Output Impedance of a Simple Buck Converter

The circuit of a closed loop buck converter is shown in Figure 2.5. The output voltage is controlled to follow the reference voltage in the feedback loop. Gc(s) is the transfer function of the controller and Gp(s) is the transfer function of the open loop converter.

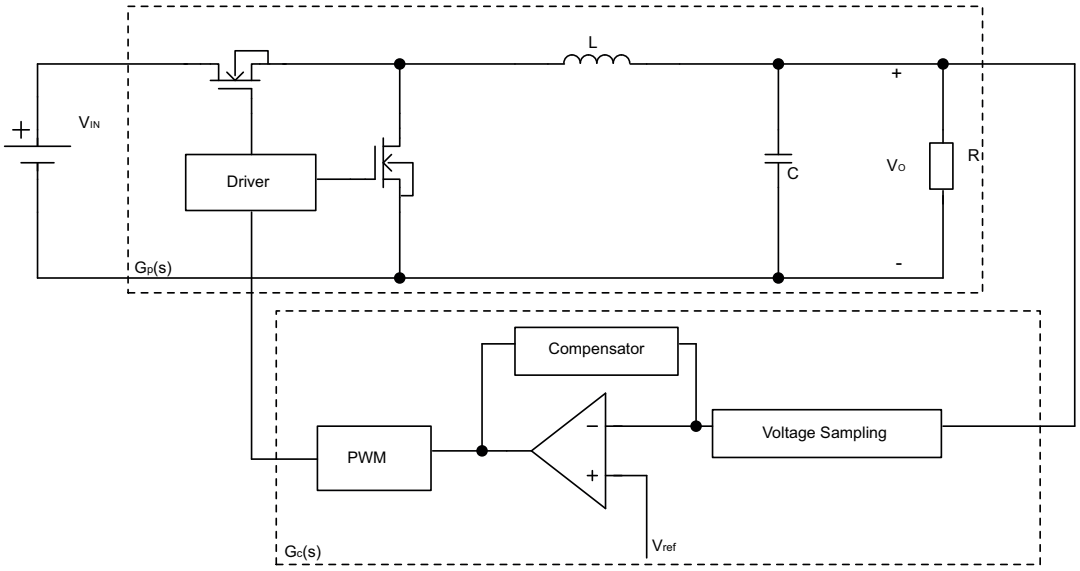

Figure 2.5: Simple model of a buck converter with voltage regulation.

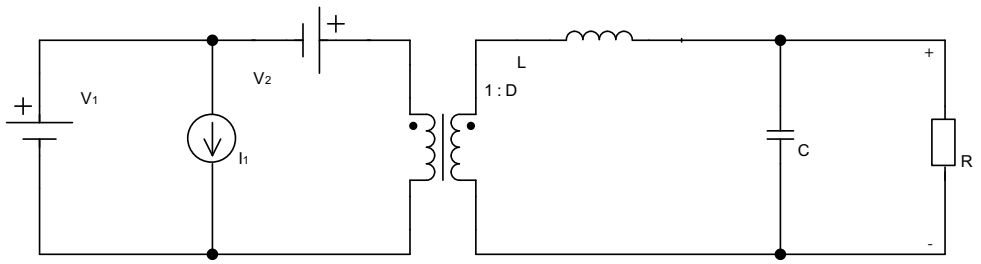

Figure 2.6: Small signal model of a buck converter.

In Figure 2.6, V_1, V_2 and I_1 is expressed as

$$V_1 = V_g + \hat{V}_g(s) \tag{2.8}$$

$$V_2 = \frac{V}{D^2}\hat{d}(s) \tag{2.9}$$

$$I_1 = \frac{V}{R}\hat{d}(s) \tag{2.10}$$

where $\hat{d}(s)$ is a small variation of the duty cycle and V_g is the gate voltage of the switch and R is the load resistance [4]. Considering the small-signal model of the buck converter, shown in Figure 2.6, the output impedance of the converter can be calculated as

$$Z_O(s) = \left.\frac{\hat{V}(s)}{\hat{i}_{out}(s)}\right|_{\hat{v}_g(s)=0,\hat{d}(s)=0} = sL \parallel \frac{1}{sC} \parallel R = \frac{Ls}{LCs^2 + \frac{L}{R}s + 1} \tag{2.11}$$

where C is the output filter capacitance, L is the output filter inductance and R is the load resistance. Using $C = 400\,\mu F$, $L = 1\,\mu H$ and $R = 0.5\,\Omega$, the bode plot of (2.11) is shown in Figure 2.7 where the maximum impedance is approximately 0.5 Ω at 8 kHz for the ideal buck converter. If non ideal parameters are considered, a series resistance R_e of 1.2 mΩ is introduced representing the equivalent

resistive losses in the inductor of the output filter [4]. The output impedance of the open loop can now be expressed as

$$Z_O(s) = R_e \parallel \frac{1}{sC} \parallel R = \frac{R_e}{sR_eC + \frac{R_e}{R} + 1} \tag{2.12}$$

where the bode plot of the non ideal buck converter is compared with the ideal buck converter in Figure 2.7. Note that the impedance of the non ideal buck converter approaches the impedance of the ideal buck converter as the frequency increases.

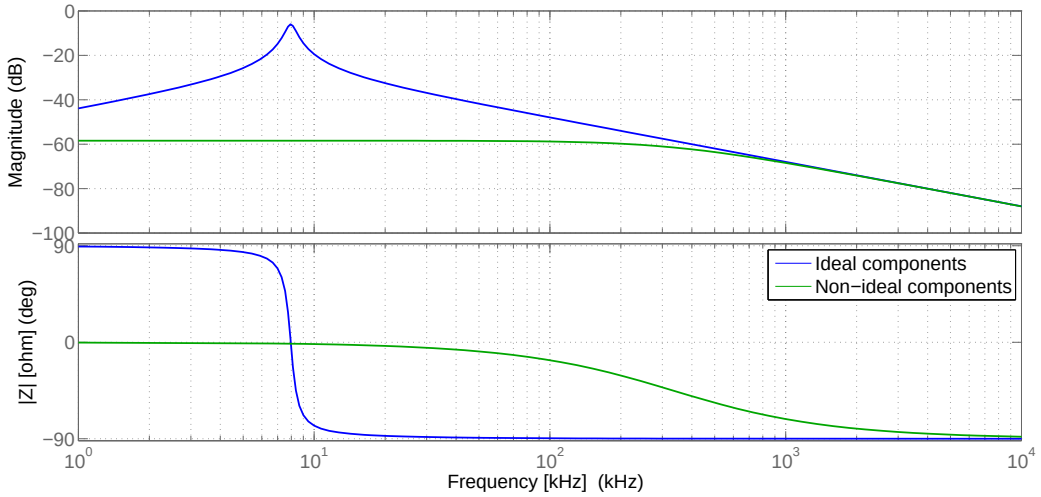

Figure 2.7: The theoretical open loop output impedance of an ideal buck converter and a buck converter with non ideal components.

Considering the schematics in Figure 2.5, the closed loop output impedance is calculated as

$$Z_{OC}(s) = \frac{Z_0(s)}{1 + G_P(s) \cdot G_C(s)} \tag{2.13}$$

where the transfer function of the open loop converter $G_p(s)$ is

$$G_P(s) = \frac{V_{in}}{LCs^2 + \frac{L}{R}s + 1} \tag{2.14}$$

and $G_C(s)$ is the transfer function of the controller.

At high frequencies the open loop output impedance should approach the closed loop output impedance since the control loop has a much lower break point. This is however only true if the capacitors have an ideal and fixed capacitance and a fixed series resistance over frequency.

2.4 Existing measurement methods

There are several different methods to measure the output impedance of power supplies and converters. To obtain the frequency dependant characteristics of the impedance an excitation signal to the output of the DUT is used. This can be done by either loading the DUT with an AC load or by injecting an AC signal into the output. To obtain load dependant characteristics, the measurements are also performed at different DC load levels.

All of the methods studied are executed in a similar way and can be simplified in an equivalent circuit shown in Figure 2.8 where Z_0 is the output impedance of the DUT, v_0 is the output voltage of the DUT and i_0 is the current waveform created by an oscillating load/source.

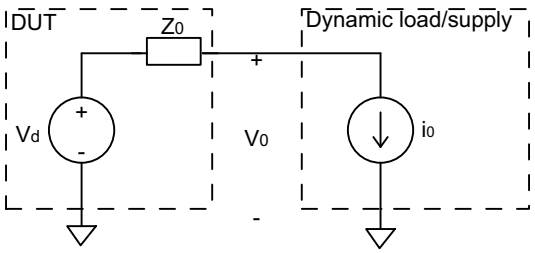

Figure 2.8: Simplified circuit of the general output impedance measurement.

The output current (i_0) consists of two parts as

$$i_0 = I_{0,DC} + i_{0,AC} \tag{2.15}$$

where $I_{0,DC}$ is a DC offset and $i_{0,AC}$ is a sinusoidal AC. From Figure 2.8, the output voltage of the DUT can be calculated using

$$v_0 = V_d - Z_0 i_0 = V_d - Z_0(I_{0,DC} + i_{0,AC}) \tag{2.16}$$

where V_d is the input voltage of the DUT. If only the AC component, i.e. the peak to peak value, of the output voltage is considered, the AC-component can be expressed as

$$v_{0,AC} = |Z_0|\, i_{0,AC} \Leftrightarrow |Z_0| = \frac{v_{0,AC}}{i_{0,AC}}. \tag{2.17}$$

Thus, the output impedance for a certain frequency is calculated by dividing the AC component of the output voltage of the DUT with the AC component of the generated current. Depending on the DC offset amplitude, $I_{0,DC}$, the output impedance is given for different output current levels. This is important since the output current affects the components creating different parasitic effects.

2.4.1 The IEC60478-4 Method

The IEC introduced the IEC60478-4 standard in 1976, illustrated in Figure 2.9. This method uses a variable resistive load that loads the supply with 50 % of the rated DC current. This resistance is connected in parallel with a sine wave creator to introduce the AC characteristics. The current and voltage is measured with an oscilloscope. The drawbacks of this method is that the oscilloscope measures the phase difference poorly and due to the circuit design, it is sensitive to ripple and noise of the power supply [5].

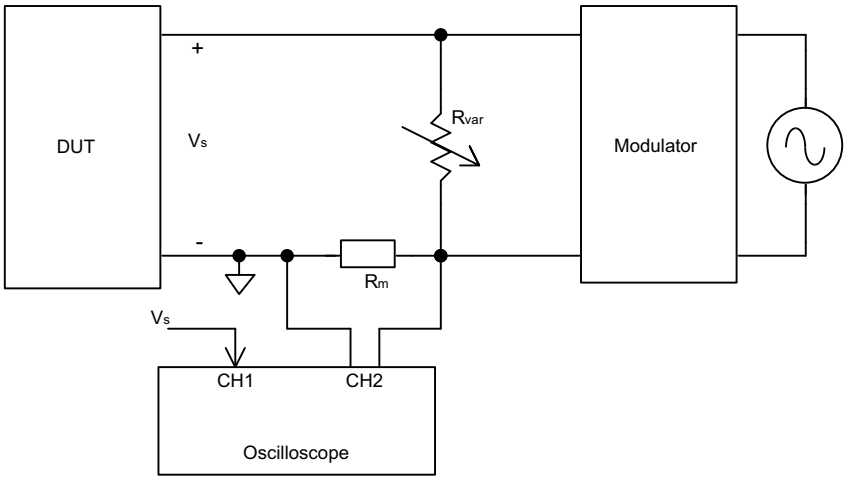

Figure 2.9: Measurement method presented in IEC60478-4.

2.4.2 The Venable Method

Venable suggests a measurement setup showed in Figure 2.10 which is based on their FRA (Frequency Response Analyser), an instrument mostly used for measuring the frequency response of control loops. The FRA sends an AC signal via an amplifier and a transformer to the output of the power supply. The load current as well as the supply and load voltage are measured with the FRA to CH1 and CH2 respectively.

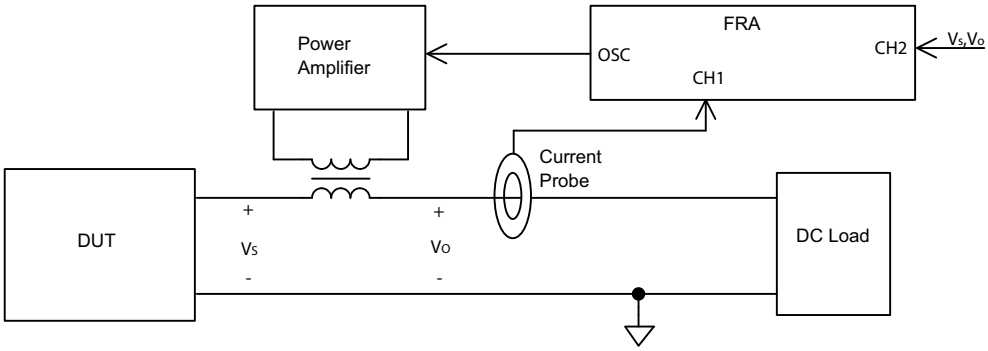

Figure 2.10: Measurement method presented by Venable.

The output impedance is obtained by

$$Z_o = -\frac{CH2}{CH1} \tag{2.18}$$

where CH1 is the output current input and CH2 is the voltage input to the FRA. By measuring V_O at CH2 the output impedance of the DC power source is obtained and by measuring V_s, the input impedance of the DC load is measured. [6].

The drawback of this method is that it is difficult install the measurement setup properly, e.g.. the right position of the current probe and calibrating the scale-factor and polarity correctly [6].

2.4.3 The Ridley and Agilent Method

A measurement method introduced by Ridley and Agilent is shown in Figure 2.11. This method uses an excitation sine wave signal that is injected at the load via a transformer.

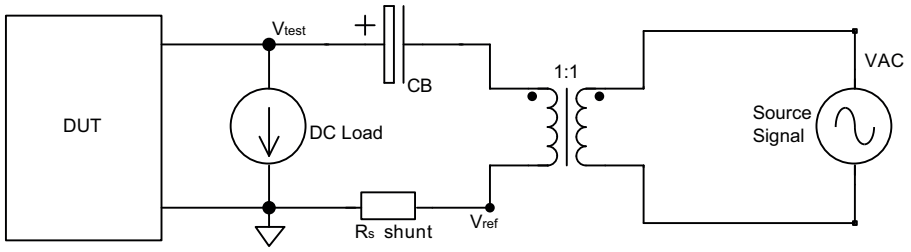

Figure 2.11: Measurement method presented by Ridley and Agilent.

The output impedance is obtained by

$$Z_o = -R_s \frac{V_{TEST}}{V_{REF}} \tag{2.19}$$

where R_s is the current sensing resistor, V_{TEST} is the voltage over the load and V_{REF} is the voltage over the sensing resistor, used to calculate the current through it.

The drawback with this method is that because of the generally low power of the signal generator, the magnitude of the injected current is low which affects the precision of the measurement .

2.4.4 The Ridley Method

Another measurement method introduced by Ridley is shown in Figure 2.12. The difference compared to the previous method is the MOSFET that is used as an amplifier and excitation signal is not galvanically isolated from the DUT. The output impedance is measured in the same way as the Ridley and Agilent method described in Section 2.4.3.

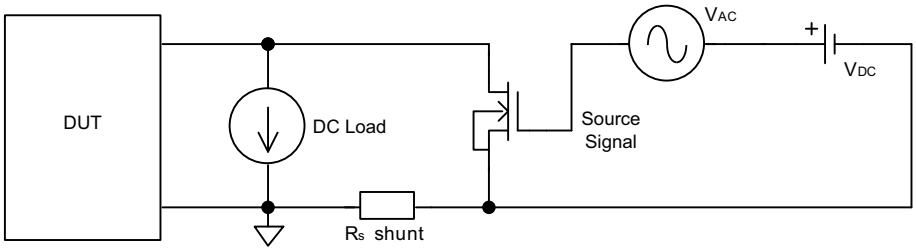

Figure 2.12: Measurement method presented by Ridley.

The Ridley method does not have the same problem with low amplitude excitation signal as the the Ridley and Agilent method since it is amplified by the MOSFET. On the other hand, a drawback for this method is that the MOSFET is powered by the DUT, making measurements while the power supply is turned off impossible.

2.5 The PuLS Measurement System

The easiest way to measure output impedance is to directly connect a device to the output of e.g. a converter without connecting any external measurement instruments. If the PuLS would be able to perform such measurement it needs to measure the voltage constantly and draw oscillating current with good precision. The PuLS has a built in microcontroller that measures the voltage and controls the output signals to draw current. The microcontroller is a fully digital circuit which means that functions that converts digital signals to analog and vice versa are needed. Because of the conversion between digital values and analog signals all measurements or outputs will be affected by the resolution of the conversions done between the two states. This gives a measurement error which leads to that the microcontrollers ability

to detect small differences are therefore limited. Sections 2.5.1 and 2.5.2 will explain the conversions made by the microcontroller between digital and analog signals.

2.5.1 Analog to Digital Converter

An ADC (Analog to Digital Converter) is used to convert an analog voltage to a digital number representing the value of the analog amplitude. In the microcontroller used in the PuLS, an ADC called SAADC (Successive Approximation ADC) is used.

The SAADC has, as all ADCs, a fixed number of possible outputs, each corresponding to a certain fraction of the reference voltage. The basic idea of the SAADC is to use a binary search to find which level the measured voltage corresponds to. A binary search works by comparing to the middle value first, then if it is greater, it compares with the 3/4 value and so on until it reaches the highest resolution. Each stage corresponds to a bit e.g. the first one $V_{ref}/2$ to the MSB (Most Significant Bit), the 3/4 and 1/4 to the next bit and so forth [7]. One of the most common SAADCs is the charge-redistribution SAADC. It consists of an array of capacitors, individually switched and binary weighted, and a comparator as seen in Figure 2.13. The working principle of the charge-redistribution SAADC can be explained in four steps [7]:

1. The capacitor array is discharged via the reset switch to the offset voltage of the comparator. This creates an automatic offset calibration.

2. The capacitor array is switched to V_{in}, this means that the charge for each capacitor will be $(V_{in}\text{-}V_{offset})C/2^N$.

3. The capacitors are switched to apply this charge to the comparators input, creating an input voltage of $-V_{in}$.

4. The conversion starts by switching the capacitor corresponding to the MSB to V_{ref}, this will set the input of the comparator to $V_{ref}/2\text{-}V_{in}$ because of the binary weighting of the capacitors. If V_{in} then is greater than $V_{ref}/2$ the MSB will be set to one. Each capacitor is then tested in the same manner, setting the previous capacitor to zero or keeping the voltage depending on if V_{in} is higher or lower than the capacitor voltages.

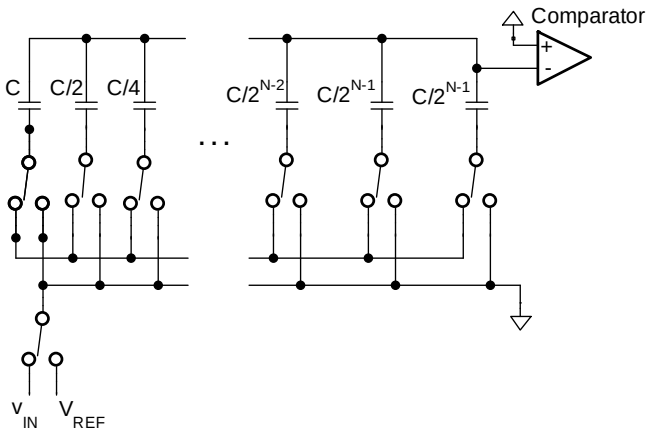

Figure 2.13: The schematics of charge redistribution SAADC.

In this way a digital representation of the input voltage is made as a fraction of the reference voltage. This fraction can easily be recalculated in the microcontroller code to represent the measured voltage

cancelling both external scaling and the scaling done in the ADC [7]. The ADC conversion leads a trade-off between how good the resolution can be and how large the measurable range of the input signal is.

2.5.2 Digital to Analog Converter

A DAC (Digital to Analog Converter) is a converter from a digital number to an analog signal, such as a voltage. This can be done in different ways, e.g. using PWM, oversampling or binary weighted switched resistors.

The STM32F105 microcontroller used in the PuLS has DACs working with integrated resistor strings. The resistor string contains 2^N resistors with the same resistance connected in series between the output supply voltage and the ground. The output from the DAC is basically a voltage division over these resistors. The voltage division is selected using switches between each resistor controlling where the voltage division is made. To lower the output capacitance a binary switch is used with each switch corresponding to one bit in the digital signal, as seen in Figure 2.14, instead of using one switch per resistor to a single output. This does however lower the conversion speed [7].

This architecture provides good accuracy because of the simplicity but low resolution because of the many switches and resistors needed [7].

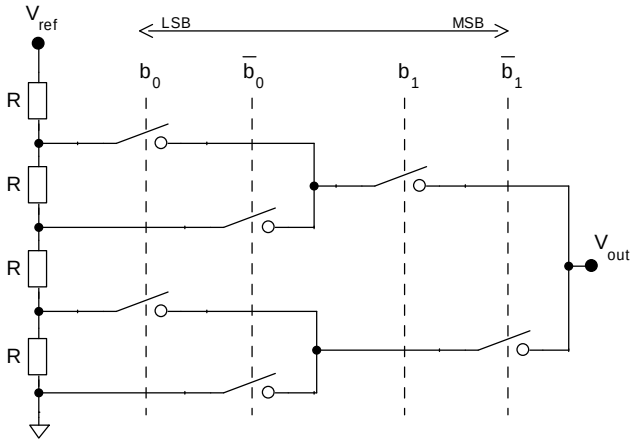

Figure 2.14: Resistor string DAC using a binary switch array.

3 The Current PuLS

PuLS is currently a working product at Ericsson, it is used for testing and verification of DC/DC converters. In its current form, it can only be used as a pulsed load.

3.1 Specification

The PuLS can create current pulse shapes with three different current levels between 0.5 and 45 A with rise and fall slew rates up to 20 A/µs. Each pulse can have a duration of 10-9999 µs and a delay time of 5-1000 ms between each pulse. In its present state, it can only handle load characteristics consisting of one pulse per period with a maximum duty cycle of 50 % and voltages under 20 V [8]. One of the biggest benefits with using the PuLS compared to the active loads used today is that the PuLS is directly installed on the PCB to minimize inductance leading to faster slew rate of the pulses. The PuLS can be powered either through the USB cable or through the PMBus (Power Management Bus) cable. Several PuLS units can also be connected to one controlling computer via the PMBus and can be set to trigger simultaneously [8].

The typical error in the drawn current by the PuLS is greater for lower current amplitudes as seen in Figure 3.1. Under 5 A, the maximum error is 10 % but above 5 A the error is below 1.5 % [9].

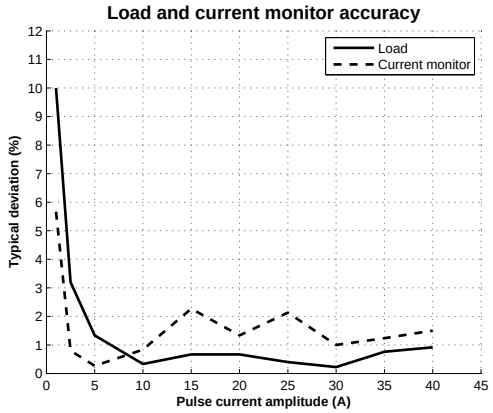

Figure 3.1: Load current and monitor accuracy of the PuLS [9].

Due to the small physical size of the PuLS PCB layout and the small convectionally cooled heat sink conducting the heat, the maximum average power dissipation of the PuLS is 7.5 W corresponding to 85°C as seen in Figure 3.2 [9]. The instantaneous power of a pulsed load can be significantly higher due to the no-load time between each pulse since the delay determines the average power.

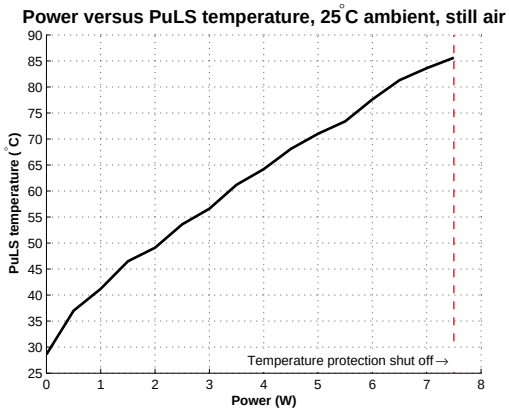

Figure 3.2: Maximum power dissipation of the PuLS [9].

3.2 Hardware & Software

To control the current drawn from the PuLS, the gate voltage of four Power MOSFETs operating in the ohmic region is controlled. The MOSFETs are used in parallel to lower the conduction resistance and to spread out the power dissipation as shown in Figure 3.3, which illustrates the schematics of the load stages. The output current is measured using small current sense resistors connected in series with each MOSFET. The voltage over the sense resistors are compared with the reference voltage set by the microcontrollers DAC and regulates the gate voltages to the corresponding current level. The control of the MOSFETs gate voltage is done with error amplifier circuits using operational amplifiers. To be able to measure the input voltage from the supply a voltage divider is installed to keep the voltage from exceeding the rated measurable level of 3.3 V to the microcontrollers ADC pin [10].

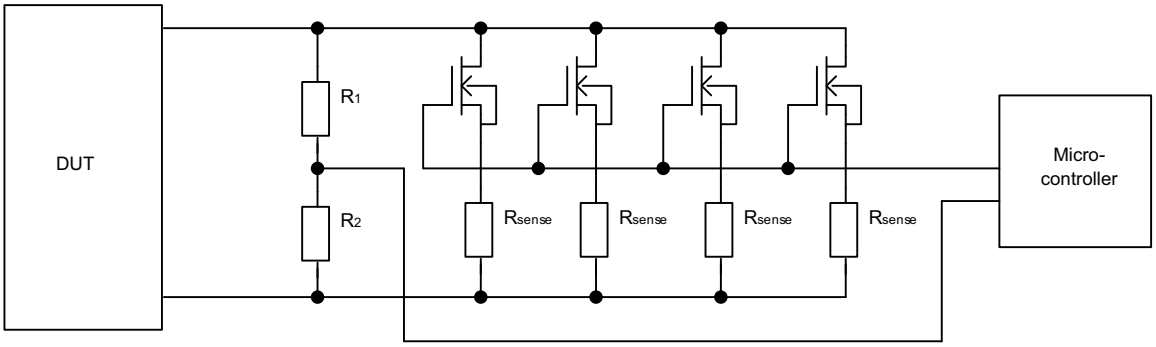

Figure 3.3: The four load stages of the PuLS.

The desired shape of the current drawn by the PuLS is programmed in a computer application called "PuLS Control". This pulse shape is configured by setting start amplitude, pulse amplitude, stop amplitude, start slew rate and stop slew rate as well as the time between the pulses. When these settings are sent to the microcontroller in the PuLS, it calculates the pulse shape and creates a series of samples used to control the gate voltage of the MOSFETs for a specific current pulse. To prevent damage to the PuLS, input current and voltage limitations are also implemented as well as a temperature trigger circuit which triggers at 92°C [8].

To use the microcontroller to its full potential, the waveform is sampled and then fed to the microcontrollers DAC using the DMA (Direct Memory Access). The DAC then puts out the sampled values converted to a gate voltage reference for the MOSFETs.

When controlling the MOSFETs in the ohmic region and using DAC, all that is needed to create custom waveforms is a list of samples. While it is hard to implement a function that enables the ability to create

any waveform from the GUI (Graphical User Interface), custom waveforms with some changeable parameters can be coded directly into the PuLS. The original GUI can be seen with examples of changeable parameter can be seen in Figure 3.4.

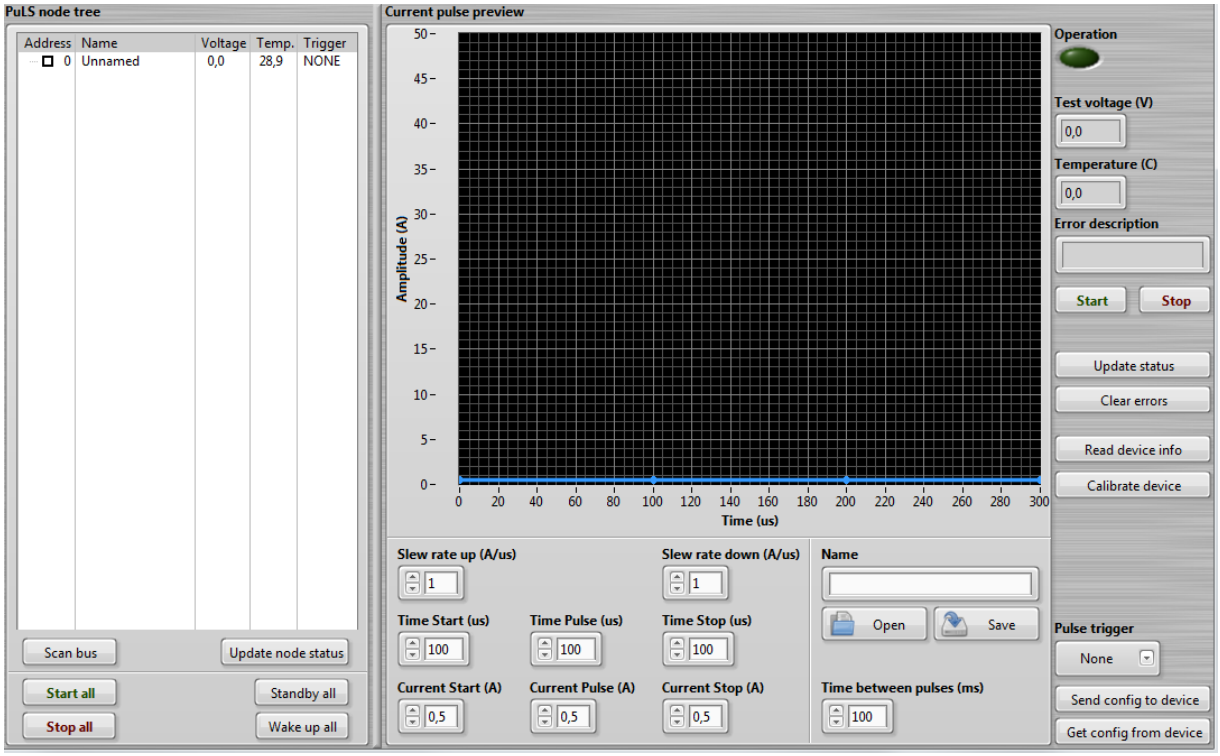

Figure 3.4: The original GUI of the user controlled software “PuLS Control”.

3.3 Comparison with other programmable loads

When the PuLS was designed, the focus was put on creating a load with a high slew rate. The maximum slew rate of the PuLS is 20 A/µs according to [8]. In [10], an earlier version of the PuLS is compared with conventional loads such as Chroma 63103A. The Chroma has a maximum slew rate of 2.5 A/us which is significantly lower than the maximum slew rate of the PuLS [11].

Another programmable load is the Agilent N3306A which was the fastest found from Agilent. The N3306A has a maximum slew rate of 10 A/us when the input voltage is higher than 3 V. When the voltage is lower than 3 V the maximum slew rate is 1 A/us [12]. This abrupt change in the maximum slew rate at 3 V is probably software controlled to ensure the specification.

When comparing the specification of the loads it is seen that the PuLS has a slew rate that is over 12 times as high as the Chroma load at 3.3 V (32 A/us vs. 2.5 A/us) and over 3 times as high as the Agilent load at 3.3 V (32 A/us vs. 10 A/us). When looking at the slew rate it is also seen that the PuLS slew rate is sensitive to low voltages, at 0.2 V the slew rate is only 2 A/us. This is still in the higher region of the Chromas capability and over the Agilent loads capability for this voltage [10].

One of the mayor differences between the programmable loads and the PuLS is that the PuLS is mounted very close to the DUT. This allows the slew rate to be higher due to the low interconnection inductance, this is especially important at low voltage levels. Another big difference between the PuLS and other programmable loads is the power dissipation capacity. The PuLS can only withstand low power and is therefore not suitable for constant current or long pulses. This is mainly because of the small size of the PuLS. The small MOSFETs and the compact placing of these as well as a small heat sink all contributes to low power dissipation capacity.

3.4 Using the PuLS to Measure the Output Impedance

The original PuLS can only draw pulse shaped loads but if the current PuLS would be able to draw a sinusoidal current, it could be used as a excitation sine wave signal for output impedance measurements. Since the microcontroller can measure voltage it is possible to extract the voltage over the DUT while it draws the load creating a possibility to measure output impedance. If the frequency of the excitation sine wave can be swept, the output impedance of each frequency could be calculated and automatically create a table of values from the measurements. A drawback with using the PuLS to measure the output impedance is that it is not possible to measure the phase. Another drawback is that the DUT has to be on during the testing, and therefore the output filter alone can not be measured.

The PuLS is able to draw loads up to 45 A. This means that it can draw a very large excitation current. According to [13] a high excitation current is needed when measuring the output impedance on devices that have a high rated output currents or have very low impedance, such as batteries.

4 Redesign of the PuLS

To be able to measure the output impedance of converters or power supplies, changes in both the hardware and the software of the PuLS had to be made. These changes will be explained in this section.

4.1 Hardware

The maximum frequency of the current sine waves that the PuLS will draw is limited to 500 kHz in this thesis. This is because the current waveform becomes distorted and the voltage measurement is too slow to measure over 500 kHz. This is explained more in depth in Section 4.4.

As described in Section 3.2, the voltage measurement is done via a ADC converter in the microcontroller. The original PuLS only measured static voltages and because of this the noise filter was overdimensioned with a breakpoint at approximately 1.5 kHz at the measuring leg of the microcontroller. To make 500 kHz measurement possible without dampening the signal, the measuring filter had to be redesigned with a higher breakpoint. The original PuLS also had a Zener diode for protection of the input. This Zener diode had a notable leakage current close to the maximum rating of the input voltage of the microcontrollers measuring leg in the PuLS which affects the voltage measurement. Thus, the Zener diode was replaced with another Zener diode with higher Zener voltage (3.9 V) closer to the maximum rating of the microcontroller. To increase the sensitivity of the measurements, the voltage divider in the filter was changed so that the rated maximum voltage of the PuLS (25 V) corresponded to a voltage just below the rated measurable voltage of the input (3.3 V). The replaced filter at the microcontrollers measuring leg is shown in Figure 4.1.

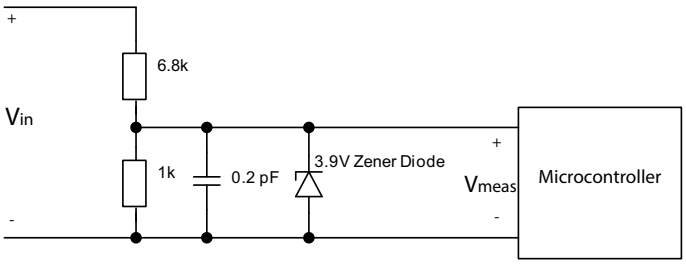

Figure 4.1: The filter at the microcontrollers voltage measuring leg.

The number of uniformly distributed voltage measure points for the microcontrollers measuring leg is 4095 between 0 and 3.3 V as described in Section 2.5.1 and the voltage dividing factor is 7.8 [14]. The resolution of the voltage measurement can be then be calculated with

$$V_{sens} = \frac{V_{measured,max} \cdot 7.8}{4095} = \frac{3.3 \cdot 7.8}{4095} = 6.3\,\text{mV} \tag{4.1}$$

which means that voltage changes below 6.3 mV will not be registered.

4.2 Software

To measure the output impedance, the PuLS must be able to draw a sinusoidal current from the DUT. To accomplish this, the PuLS had to be reprogrammed so that it can send and receive the parameters needed to calculate the samples from an algorithm. The algorithm for calculating the samples receives the following input variables; frequency, amplitude, number of periods and DC-offset. The period time is calculated first, since the DMA to DAC has a fixed transfer rate the number of samples per period is

calculated by multiplying the period time with the transfer rate. The sine wave samples is then calculated as

$$y(n) = A \cdot \sin(\frac{2\pi}{k}n - \frac{\pi}{2}) + O \tag{4.2}$$

where k is the number of samples for one period, n is an integer $0 \leq n \leq k$, A is the amplitude and O is the DC-offset. The phase offset is used for starting at the lowest possible value. To get a good shape of the sine wave at high frequencies and to limit the use of memory at low frequencies, the samples are calculated for one period only. If the DMA is set to circular mode, the output will automatically repeat the sample array until it is turned off. After each transfer, the flag "Transfer complete" is set. When the flag is detected a counter is increased by one and the flag is cleared. When the counter reaches the set number of periods the transfer is stopped and the PuLS waits for the previously set time between transfers before it starts the transfer again. Figure 4.2 illustrates a block diagram of the output impedance measurement procedure of the PuLS.

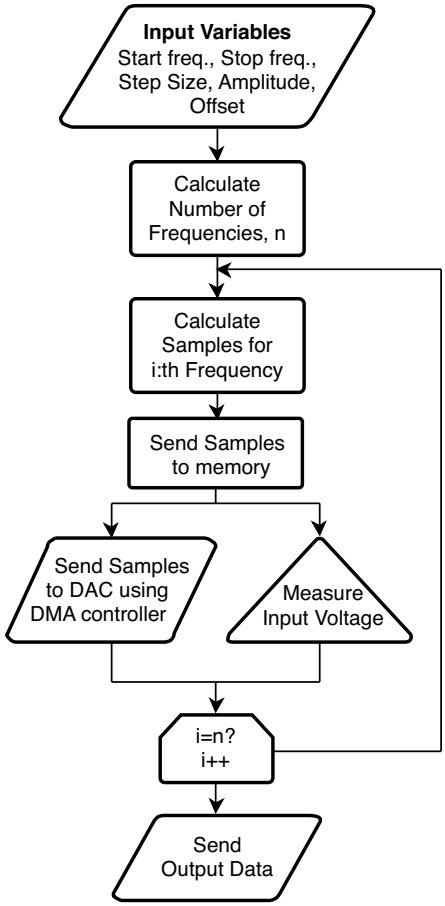

Figure 4.2: Block diagram of the output impedance measurement procedure of the PuLS.

Additional variables had to be added to be able to measure the impedance for several frequencies in one sweep; start frequency, stop frequency and step size. The measurement starts from the lowest frequency and then increases the frequency with the specified step size until the stop frequency is reached. During the sine wave periods, the voltage is measured at several points with the highest possible frequency by an ADC. The counter used for stopping the transmission of the drawn current is also used to start and stop the measurement of the voltage. Since the voltage will dip in the beginning because of the offset, the measurements have to wait until the voltage has reached steady state before measuring the peak-to-peak value by subtracting the minimum value from the maximum value. Over 20 periods was considered

sufficient to reach steady state for frequencies up to 500 kHz. The voltage measurement gather sampling points at a certain frequency limited by the microcontroller to approximately 850 kHz [14]. Because of this limitation, the voltage must be measured over several periods to be able to reach a sufficient number of points to extract the maximum and minimum values of the voltage wave form. The number of periods where the voltage measurement is on were chosen to 20 periods in the end of the transmission which means that the total number of periods of each transmission is 40 periods.

4.3 Graphical User Interface

To be able to use the PuLS for impedance measurements the GUI had to be changed as well. The parameters, explained in Section 4.2 are controlled in the GUI and then sent to the PuLS. When the measurement series is performed the results of the voltage ripple at different frequencies is sent back to the computer program which calculates the impedance corresponding to the amplitudes of the current and voltage. It presents the results in a table as seen in Figure 4.3 where the GUI with the impedance measurement tab is shown. It also saves the results in a CSV-file (Comma Separated Values).

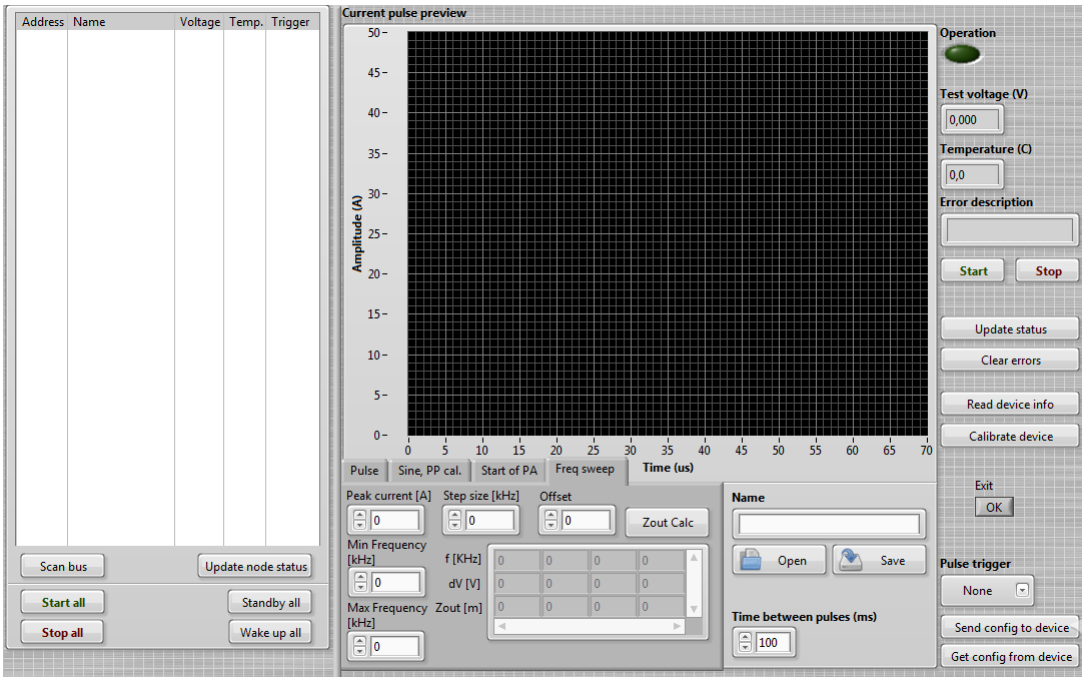

Figure 4.3: The GUI of the user controlled software “PuLS Control”.

4.4 Limitations

Considering the design of the PuLS, drawing a sine wave current comes with some limitations. These limitations are discussed in this subsection. The limitations are depending on both the specifications of the microcontroller, such as the clock frequencies and the memory sizes and hardware such as slew rate limitations.

4.4.1 Slew Rate

Since the maximum slew rate of the PuLS is 20 A/µs as described in Section 3.3, limitations in the created sine wave can be expected if the wanted sine wave requires a higher slew rate than the PuLS can deliver. An arbitrary sine wave can be calculated as

$$i = A\sin(\omega t) + O = A\sin(2\pi f t) + O \tag{4.3}$$

where A is the amplitude, ω is the angular frequency, O is the offset and f is the frequency. The maximum slew rate of the sine wave is the time derivative of (4.3) when t = 0. If the slew rate is expressed in A/µs, it can be expressed as

$$\frac{di}{dt} = \frac{2\pi f A}{10^6}. \tag{4.4}$$

Limitations in the frequency and amplitude depending on the maximum slew rate of the PuLS is shown in Figure 4.4 where the slew rate as a function of the frequency is illustrated for several amplitudes of the sine wave. Looking at (4.4) it is obvious that greater amplitudes give a higher slew rate for the same frequency which is also seen in Figure 4.4. Frequencies above 500 kHz will not be used in this thesis because of limitations described in Section 4.1, this means that current amplitudes up to 6 A can be used over the whole frequency spectrum.

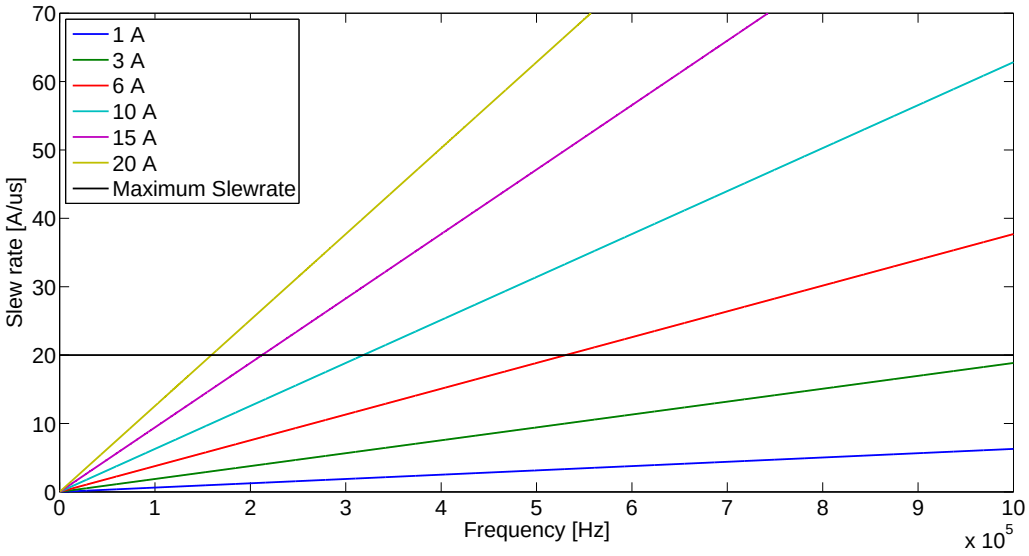

Figure 4.4: Slew rate vs. frequency at different current levels.

4.4.2 DMA to DAC Output Frequency

When using the DMA to output samples through the DAC, the time between each output is 0.2232 µs which corresponds to a frequency of about 4.5 MHz. The sampled points for a 100 kHz sine wave is compared to an ideal sine wave using MATLAB seen in Figure 4.5. To create the sample points, the same algorithm as used in the PuLS for calculating the samples, from (4.2), was used in MATLAB. Due to the high number of sampling points ($\sim$45), the shape of the sampled sine wave is very close to the ideal sine wave.

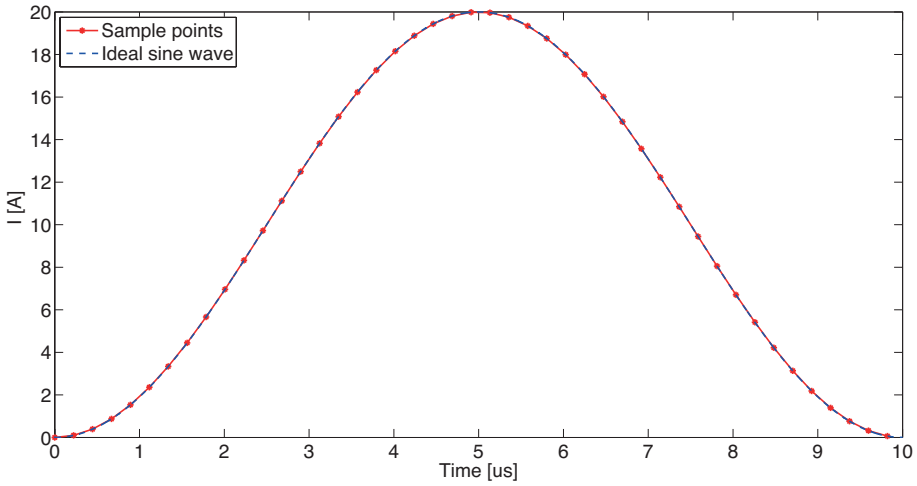

Figure 4.5: Sample points of the current sine wave drawn by the PuLS and an ideal sine wave at 100 kHz.

If the frequency is increased to 500 kHz, the number of points is further reduced to 9. Both the purity and amplitude of the sine wave is heavily affected by the low number of points as seen in Figure 4.6. This fact is also a reason to limit the maximum frequency for the PuLS during operation.

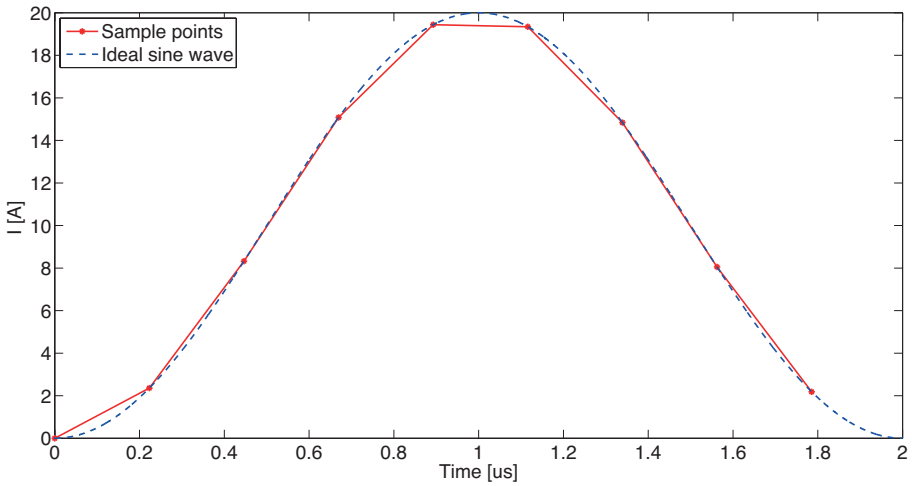

Figure 4.6: Sample points of the current sine wave drawn by the PuLS and an ideal sine wave at 500 kHz.

The amplitude error of the sine wave current was measured for several frequencies at different current amplitudes. As seen at the peak of the sine wave in Figure 4.6 and as measured, the amplitude of the sine wave decreased as the frequency increased. Since the error depending on the frequency had a non-linear dependency (the amplitude decreased more drastically for the highest frequencies), a function was extracted using the polyfit function in MATLAB to compensate for this error. The function that were used depending on the frequency is illustrated in

$$F_f = -4.97 \cdot 10^{-9} f^3 + 2.22 \cdot 10^{-6} f^2 - 4.74 \cdot 10^{-5} f + 0.9998 \tag{4.5}$$

where f is the wanted frequency set in the GUI. This function was multiplied with the amplitude of the sine wave current. Another error depending on the amplitude of the sine wave set in the GUI was also compensated for. For lower current amplitudes, the error of the sine wave was greater compared to higher

current amplitudes. In the same way as the frequency compensation in (4.5), a function using the polyfit function in MATLAB was extracted as

$$F_A = -3.6 \cdot 10^{-4} I_{p-p}^4 + 0.0122 I_{p-p}^3 - 0.1417 I_{p-p}^2 + 0.7922 I_{p-p} + 0.3887 \tag{4.6}$$

where $I_{p\text{-}p}$ is the wanted current amplitude set in the GUI. This function was added to the set amplitude of the current.

In addition to the limitations at higher frequencies, the fixed sampling rate of the DMA and DAC creates problems at low frequencies. At frequencies lower than 500 Hz, the DMA memory is too small to handle all the sampling points and will not work. Therefore the minimum frequency when creating sine waves is limited to 500 Hz.

5 PuLS Verification Measurements

In order to verify the purity of the sine waves drawn by the PuLS and the peak-to-peak voltage measured, verification measurements had to be done with ideal considered references for different frequencies.

5.1 Verification of the Sine Wave created by the PuLS

Even though the amplitude error of the sine wave current drawn by the PuLS was compensated for as explained in Section 4.4.2, a small error in amplitude and phase is still present in the waveform. To verify the sine wave created by the PuLS, comparison with an ideal sine wave was made in MATLAB. The sine waves created by the PuLS was measured with a current probe (Le Croy AP015) into an oscilloscope (Le Croy Wavesurfer 44MXs-A) with the measurement setup shown in Figure 5.1. The Power Supply used was a Delta Elektronika SM70-22, to get a higher output slew rate two capacitors were connected with a combined capacitance of 18.1 mF.

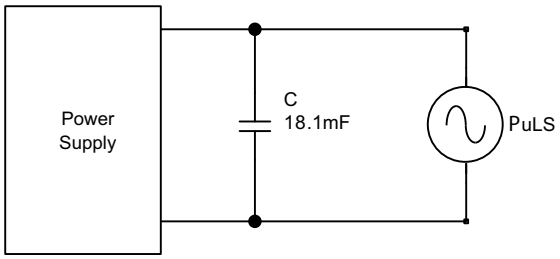

Figure 5.1: PuLS directly connected to the power supply.

Figures 5.2-5.5 illustrates the ideal sine wave and the sine wave created by the PuLS at 50 kHz and 500 kHz with a peak-to-peak amplitude of 10 A. Ten periods of the sine wave current drawn by the PuLS and an ideal sine wave at 50 kHz is shown in Figure 5.2. It can be seen in the figure that the PuLS sine wave has a bit higher frequency at values over the mean value and lower frequency on the values under the mean value which leads to small phase errors in the lower regions.

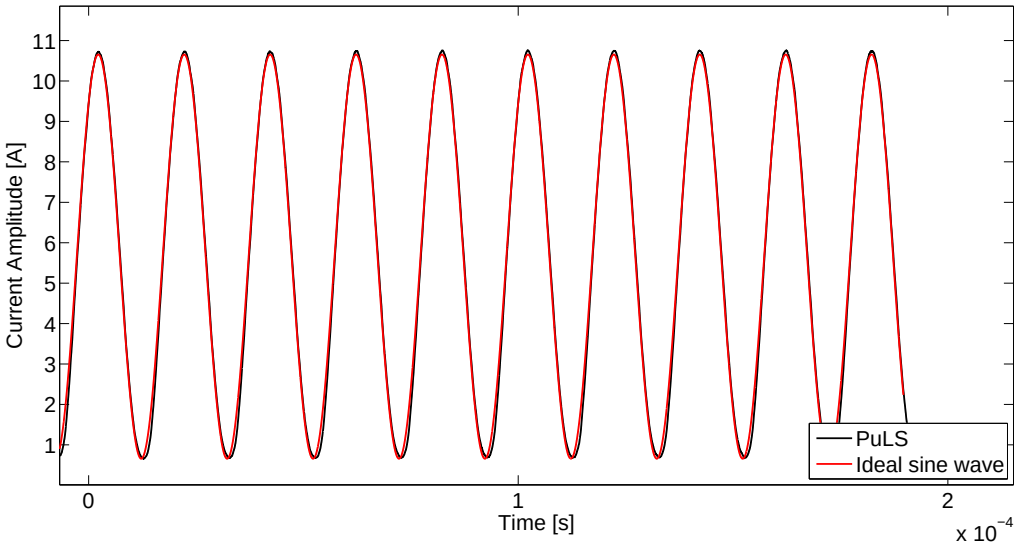

Figure 5.2: Comparison between an ideal sine wave and the PuLS sine wave at 50 kHz for ten periods

To compare the amplitude and phase error and to see the shape of the drawn current, zooms of the peaks of the first and tenth period from Figure 5.2 are shown in Figure 5.3. The peaks are where the PuLS sine

wave deviates the most from the ideal sine wave and the first and tenth period is used to see if any phase shift is present. Note that the axes have different limits for the two peaks. The phase error at the peak is neglectable and the amplitude is approximately 0.05 A greater for the PuLS sine wave.

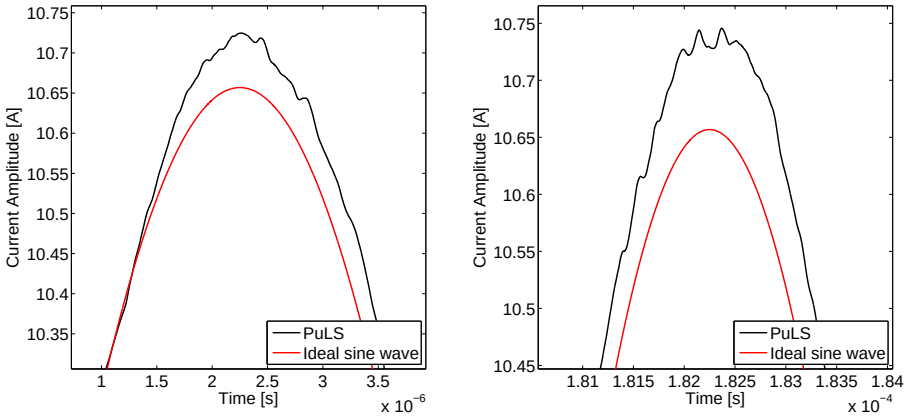

Figure 5.3: The first and the last period peak of the PuLS sine wave compared to the ideal sine wave at 50 kHz.

Figure 5.4 illustrates ten periods of the sine wave current drawn by the PuLS and an ideal sine wave at 500 kHz. The amplitude error of the PuLS sine wave for 500 kHz is observed to be slightly greater compared to the 50 kHz analysis for the PuLS sine wave.

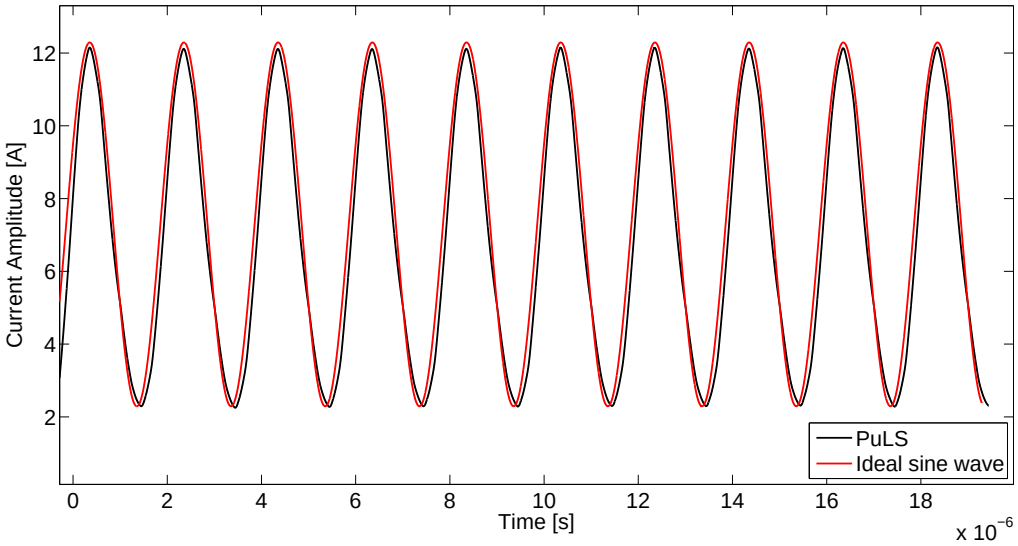

Figure 5.4: Comparison between an ideal sine wave and the PuLS sine wave at 500 kHz for ten periods.

To compare the amplitude and phase error and to see the shape of the drawn current, zooms of the first and tenth period peaks from Figure 5.4 is illustrated in Figure 5.5. The phase of the PuLS sine wave is slightly faster but less than 5 ns per period. Compared to the other frequencies analysed, the amplitude error of the PuLS sine wave is approximately 0.12 A at 500 kHz.

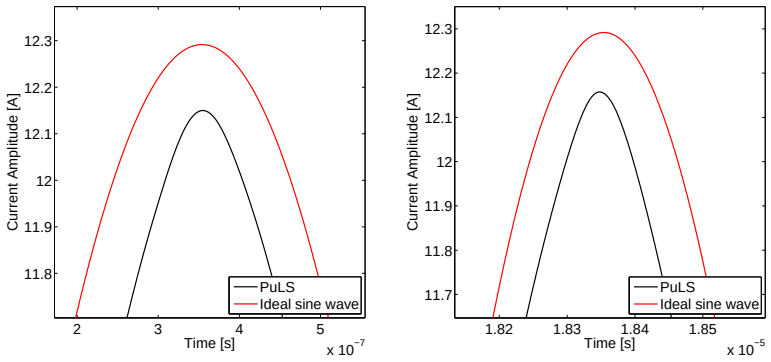

Figure 5.5: The first and the last period peak of the PuLS sine wave compared to the ideal sine wave at 500 kHz.

The maximum amplitude error was 0.12 A in the frequency range of 0.5-500 kHz and the phase error was considered neglectable due to the very small time difference. Another thing to notice is that the shape of the sine wave created by the PuLS has a little lower frequency in the lower current amplitude region and a bit higher in the higher current amplitude region compared to the ideal sine wave, especially for higher frequencies. This indicates that the PuLS has a slight difficulty with delivering the proper amplitude of the current under 5 A as discussed in Section 3.1. Another thing that is worth mentioning is the specification of the power supply that might have limitations like high output inductance or limited slew rate which may affect the current wave form drawn by the PuLS.

5.2 Verification of the PuLS Voltage Measurement

To verify the PuLS voltage peak-to-peak measurement system, a comparison with oscilloscope (Le Croy Wavesurfer 44MXs-A) measurements was made. Using the measurement setup seen in Figure 5.1, the input voltage was set to 15 V and the amplitude of the current sine wave drawn by the PuLS was 10 A. Figure 5.6 illustrates both voltage measurements for different frequencies between 10-400 kHz. The deviation of the PuLS voltage measurement, if the oscilloscope measurements are considered ideal, is relatively small even if the deviation peaks at -8 % at 400 kHz. This is not ideal, since the error is greater at higher frequencies and thus not easily compensated for, but the voltage measurement is considered sufficiently good for a fair approximation for measurement of the output impedance.

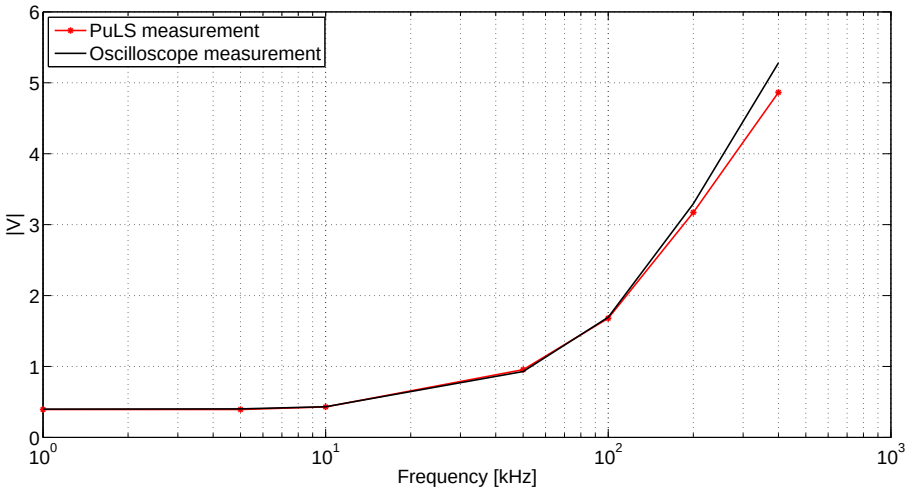

Figure 5.6: Comparison between the PuLSs and the oscilloscopes voltage measurements.

5.3 Reference Inductor Measurements

To verify the impedance measurement of the PuLS, two inductors; a 1 µH inductor from Pulse (PG0702.102NL) and a and 1.4 µH from Etal Group (300889) were selected as reference objects. The 1 µH inductor is the same inductor used for the 1.8 V buck converter analysed in Section 7, the 1.4 µH inductor is not used in the analysed converters but the specified inductance is similar to the one in the 5 V converter. Due to big deviations in the inductance and resistance specified in the datasheet [15] for the 1 µH inductor, the inductors were measured by a LCR-meter (Agilent E4980A Precision LCR Meter) with 2 V over the inductors. The parameters measured was the inductance and series resistance for different frequencies, see Table 5.1. It is noted from the measurements that the series resistance increases and the inductance decreases with frequency for frequencies greater than 20 kHz.

Table 5.1: Measured inductance and series resistance of a 1 µH and a 1.4 µH inductor using a LCR-meter.

Frequency [kHz]	1 µH		1.4 µH	
	Inductance [nH]	Series resistance [mΩ]	Inductance [nH]	Series resistance [mΩ]
1	947.29	6.40	1448.01	7.44
10	950.54	9.05	1430.17	10.02
20	943.43	12.72	1405.03	13.80
50	911.73	26.45	1368.69	25.27
100	872.93	45.93	1338.68	42.66
130	860.58	54.13	1327.68	50.94
200	844.68	68.23	1312.31	66.24
500	824.41	113.75	1292.94	111.12

The PuLS measurements was done using two different setups. Firstly, the output impedance of the power supply was measured with the measurement setup shown in Figure 5.1, secondly the same measurement was executed with the the reference inductor connected in series with the PuLS as seen in Figure 5.7. To get a higher output slew rate two capacitors were connected with a combined capacitance of 18.1 mF. The impedance of the reference inductor can then be calculated using

$$Z_{PuLS} = Z_{L,PuLS} - Z_{PS,PuLS} \tag{5.1}$$

where $Z_{L,PuLS}$ is the output impedance of the power supply (Delta Elektronika Power Supply SM 70-22) with the reference inductor connected in series with the PuLS and $Z_{PS,PuLS}$ is the output impedance of the power supply without the inductor connected.

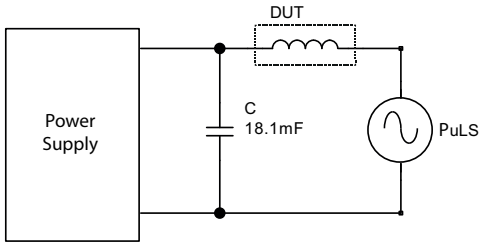

Figure 5.7: The measurement setup for the impedance measurement of the inductor.

A comparison between the impedance measurement of the 1 µH reference inductor from the LCR-meter in (5.2) and from the PuLS in (5.1) is shown in Figure 5.8. The magnitude of the impedance of the reference inductor can be calculated using

$$\mid Z_{LCR_{meter}} \mid = \mid j\omega L + R_s \mid = \sqrt{(2\pi f L)^2 + R_s^2} \tag{5.2}$$

where L is the inductance, R_s is the series resistance and f is the frequency. Seen in Figure 5.8, the impedance magnitude measured with the PuLS follows the measurements with the LCR-meter good at most frequencies but deviates around 100 kHz. The measurements done by the PuLS are slightly lower in this frequency region.

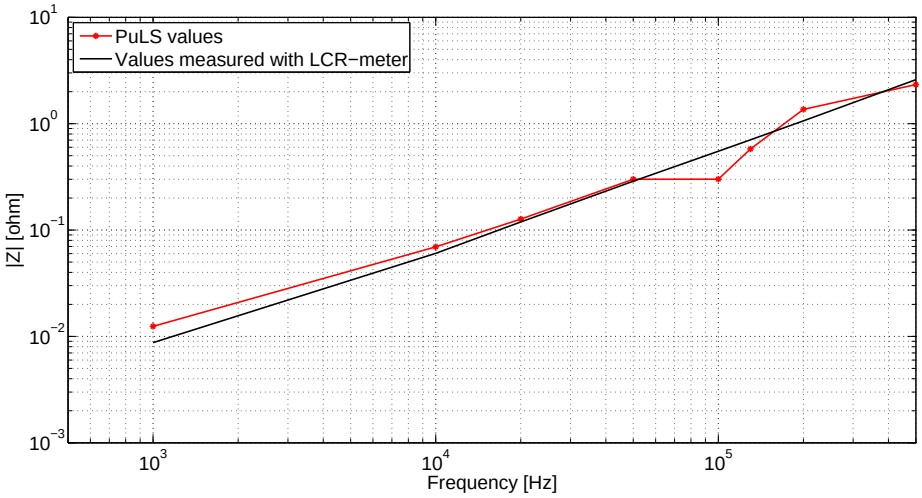

Figure 5.8: Impedance of the 1 µH reference inductor measured by a LCR meter and the PuLS.

These measurements show that the PuLS works quite good in the intended frequency range for measuring the magnitude of the impedance. It is hard to explain the deviation at 100 kHz but it should be noted that the measurements are performed with big differences in current and voltage levels which could lead to parasitic effects affecting the measurements differently. It could also be because of resonance in the circuit.

A comparison between the impedance measurement of the 1.4 µH reference inductor from the LCR-meter and from the PuLS is shown in Figure 5.9. The deviation that was noted in the 1 µH measurement at 100 kHz is not seen for the 1.4 µH inductor. Instead, the measured impedance by the PuLS is greater than the LCR-meter impedance for this frequency. Generally, the impedance measured by the PuLS is slightly greater compared to the one measured by the LCR-meter except between 20-50 kHz, where the measured impedance by the PuLS is equal to the LCR-meters.

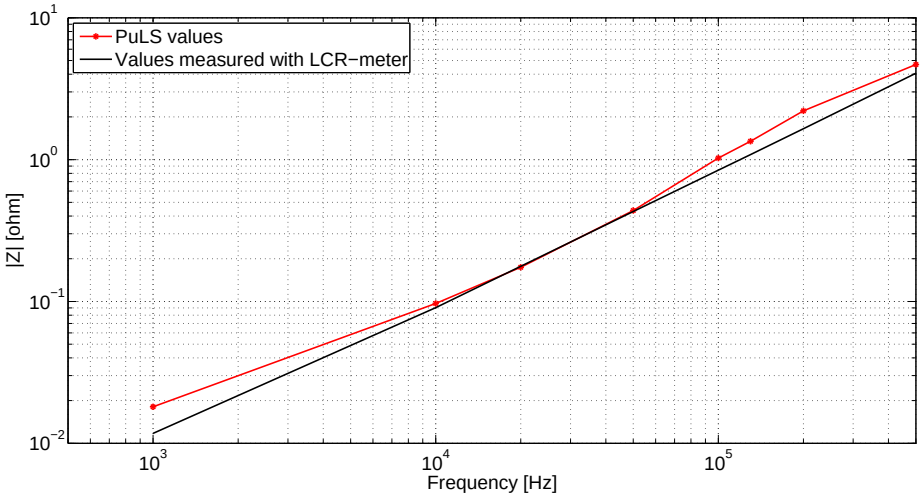

Figure 5.9: Impedance of the 1.4 µH reference inductor measured by a LCR meter and the PuLS.

6 Simulations

Simulations of the output impedance were performed of a 1.8 V and a 5 V buck converter. Basic theory of a buck converter and its controller can be found in Section 2. The simulations were done in Orcad Capture CIS Lite and the schematics used is shown in Figure 6.1 for the 1.8 V converter and Figure 6.2 for the 5 V converter. The simulation profile used was "Time domain (transient)" with the run time selected to 3 ms and the data collection started after 2 ms for each frequency simulated. To get the frequency response, I_2 was sweeped in time domain. Since the amplitude of the current is 1 A, the peak-to-peak voltage ripple at the output of the converter will be the output impedance for the given frequency according to (2.17). For a more realistic simulation, the following changes were made for the 1.8 V buck converter to the specified parameters:

- The value of the output filter capacitance was decreased by 15 % from 400 µF accounting for the value of the DC-bias voltage according to [16].
- The ESR of the output filter capacitors manually adjusted for each frequency simulated according to [16].
- The inductance decreases with frequency as stated in Table 5.1 and because of the high switching frequency in the converter affecting the inductance, the inductance parameter was decreased by 20 % from 1 µH [15].

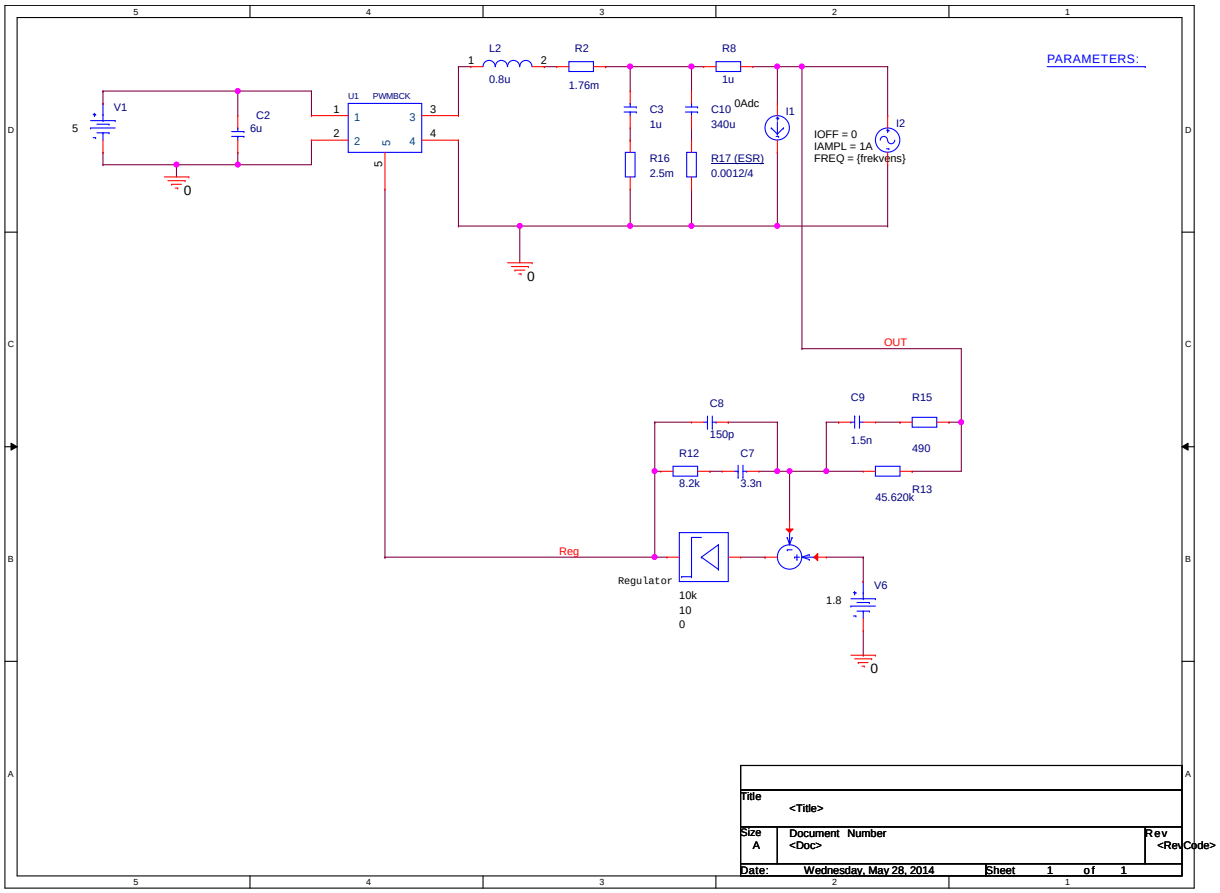

Figure 6.1: Schematics of the simulated 1.8 V buck converter.

For the 5 V buck converter, the following changes were made to the specified parameters:

- The value of the output filter capacitance was decreased by 15 % from 276 µF according for the value of the DC-bias voltage according to [16].
- The ESR of the output filter capacitors manually adjusted for each frequency simulated according to[16].
- As for the 1.8 V buck converter, the inductance was decreased by 20 % from 1.4 µH [15].

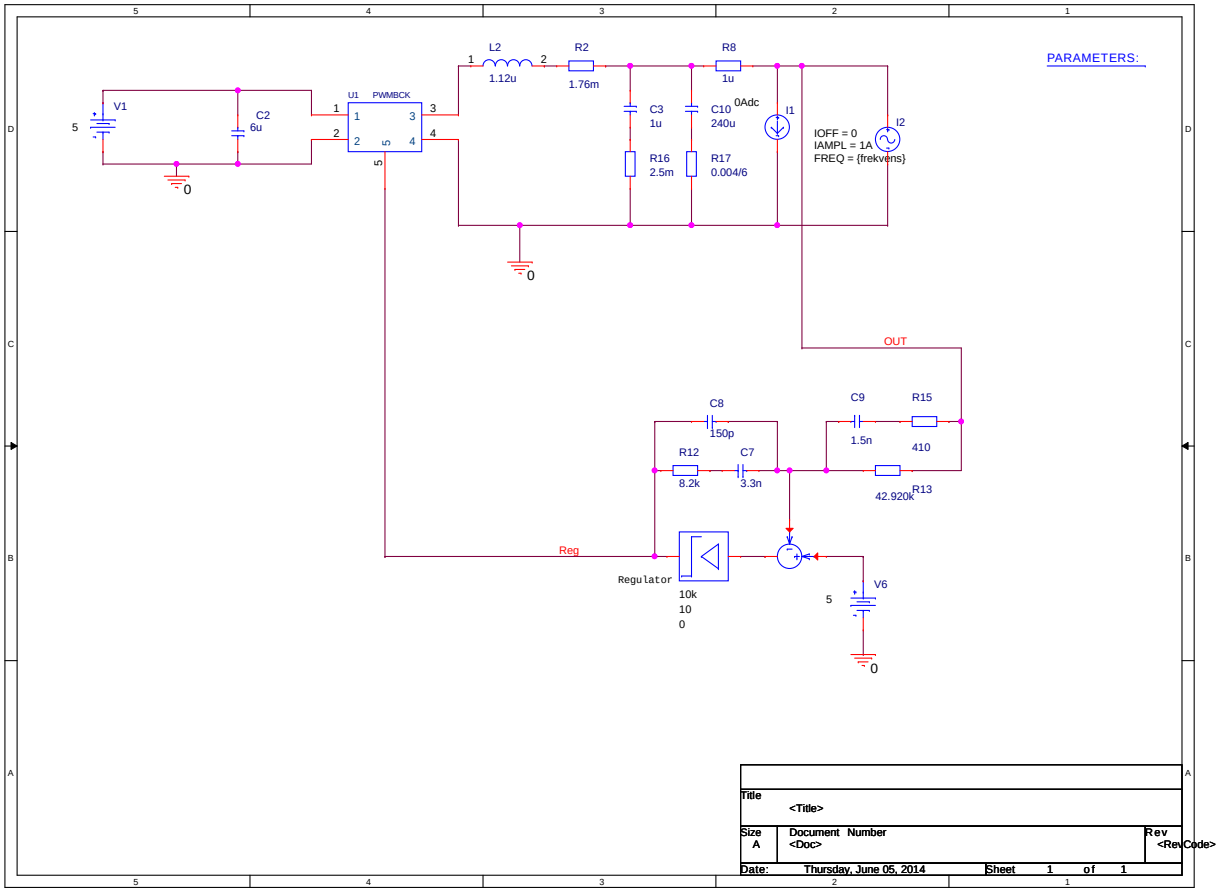

Figure 6.2: Schematics of the simulated 5 V buck converter.

The results of the simulation for the 1.8 V converter can be seen in Figure 6.3 together with the results of a simulation done without changing the ESR, which was fixed to 4 mΩ of the output capacitors for each frequency simulated. The main difference between the two curves is that the one with fixed ESR does not increase over 400 kHz but approaches zero as the frequency increases as in the theoretical case seen in Figure 2.7.

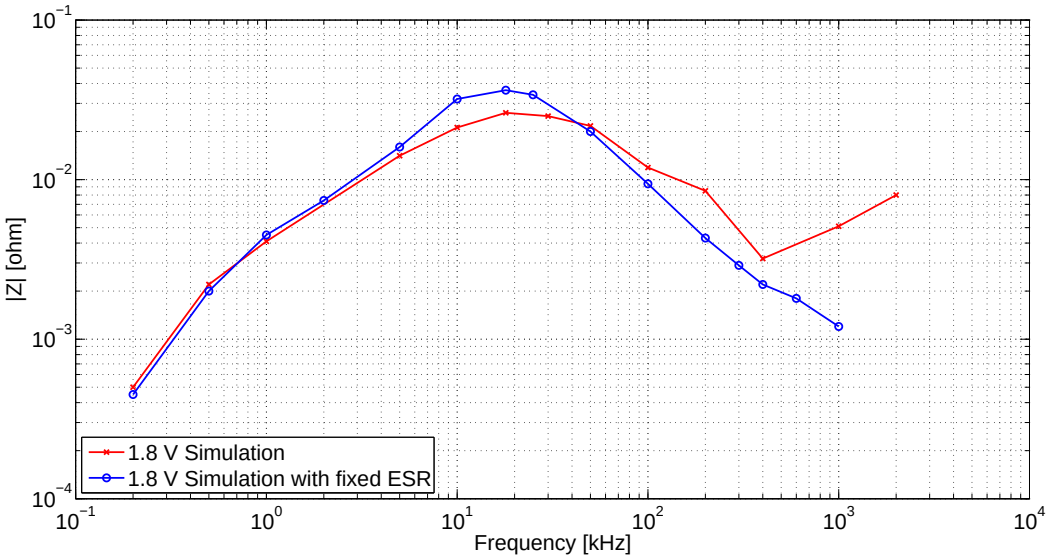

Figure 6.3: Simulation of the 1.8 V buck converter with frequency dependant and fixed ESR of the output capacitors.

The results of the 5 V converter simulation can be seen in Figure 6.4. Compared to the 1.8 V results, it has a generally higher output impedance. It does however have values very close to the 1.8 V for frequencies lower than 1 kHz and higher than 1 MHz.

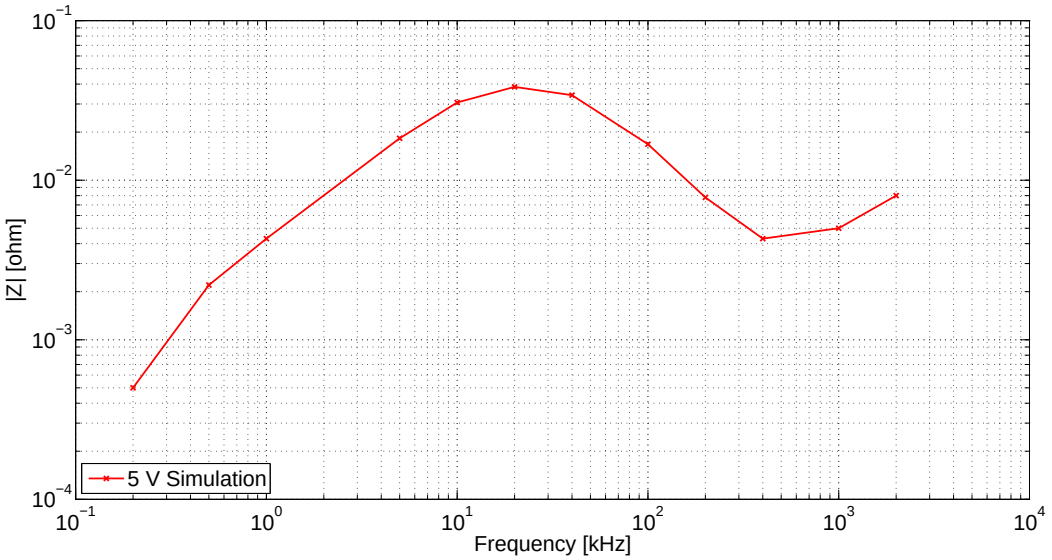

Figure 6.4: Simulation of the 5 V buck converter with frequency dependant ESR of the output capacitors.

The impedance characteristics can be divided into three parts as seen in Figure 6.5. The first rise (1), the fall (2) and the second rise (3).

1. The first rise in the impedance is dependent on the voltage compensation feedback loop, which basically is a low pass filter with a cut-off frequency much lower than the switching frequency. At low frequencies the compensation works good and makes the output ripple very small but as the frequency gets higher the compensation is not fast enough and a higher output ripple is created and thus a higher output impedance.

2. At slightly higher frequency than the cut-off frequency of the feedback loop, the converter has its peak impedance. After this it is the output filter that determines the output ripple. At first, the output

impedance is decreasing with frequency as could be expected because of the relatively large output capacitors.

3. After a certain frequency the impedance starts to rise again, this is because of the ESR in the capacitors which increases with frequency at this point, thus counteracting with the capacitance in the capacitors.

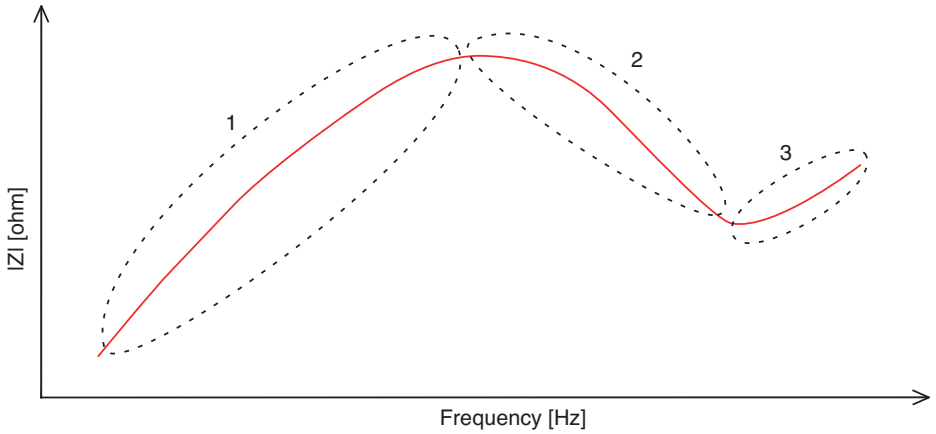

Figure 6.5: Typical output impedance characteristics of a DC/DC converter.

7 Analysis of the PuLS Output Impedance Measuring System

The purpose of this thesis was to investigate methods of measuring the output impedance of switched DC/DC converters. In this section, simulated values, reference measurements and PuLS measurements of the output impedance for the 1.8 and 5 V buck converters will be compared, analysed and discussed.

7.1 Measurement Setup

This section handles different setups used when measuring the output impedance of the 1.8 V and 5 V buck converters.

7.1.1 The Reference Measurement Setup

The impedance measurement that was compared with the PuLS impedance measurements of the buck converter called the reference measurement was measured in a similar way as the Ridley and Agilent method seen in Section 2.4. However, the reference method differs in some ways as can be seen in Figure 7.1 where $C_C = 100\,\mu F//1\,\mu F//100\,nF//1\,nF//10\,pF$. The reason why several capacitors were used is to allow AC signals to pass through C_C with a high frequency range. The difference in this method is that the injected signal, which is 45 mA peak-to-peak, is not galvanically protected by a transformer. Since the value of R_s is known, and only AC current can flow through it, the current can be obtained. The output impedance can be obtained with

$$\frac{V_{R_s}}{R_s} = \frac{V_{test}}{Z_{out}} \Leftrightarrow Z_{out} = \frac{V_{test}R_s}{V_{R_s}} \tag{7.1}$$

where $R_s = 50\,\Omega$ in the measurements of the 1.8 V and the 5 V buck converters [17][18].

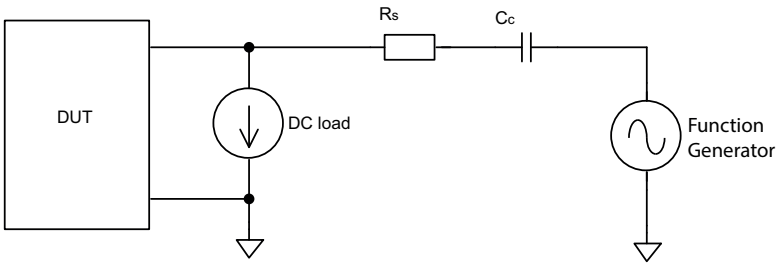

Figure 7.1: Reference output impedance measurement method.

A list of the instruments used to measure the output impedance for the buck converters in the reference method is found in Table 7.1.

Table 7.1: Table of used instruments in the reference impedance measurement method.

Name	Function
LeCroy Wavesurfer 44MXs-A	400 MHz Oscilloscope, 2.5 GS/s
Agilent 33250A	80 MHz function/arbitrary generator
LeCroy AP015	50 MHz Current Probe
Delta Elektronika SM 70-AR-24	Power Supply
Chroma 63102A	DC Electronic Load

7.1.2 The PuLS Measurement Setup

The PuLS impedance measurement method is measured with the setup found in Figure 7.2 and the instruments used for the measurement is listed in Table 7.2. As seen in the table the only instrument needed to measure the output impedance is a power supply that supplies the DUT.

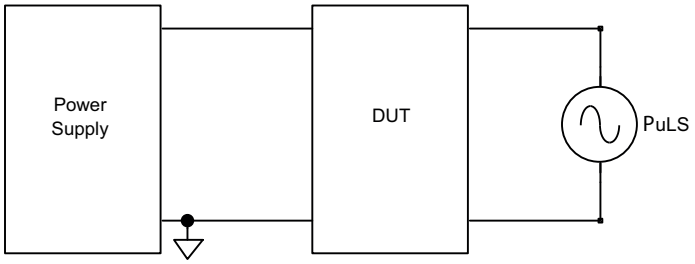

Figure 7.2: PuLS connected to the DC/DC converter.

Table 7.2: Table of used instruments in the PuLS impedance measurement method.

Name	Function
PuLS	Programmable Electronic Load
Delta Elektronika SM 70-22	Power Supply

7.2 Output Impedance Measurements

This section presents the results and analysis of the output impedance measurements of the 1.8 V and the 5 V buck converters made by the PuLS. The measurement by the PuLS is also compared with the reference measurement method and simulated values of the impedance.

7.2.1 Measurement Results

A comparison between the PuLS measurement, the reference measurement and the simulated values of the output impedance of the 1.8 V buck converter is shown in Figure 7.3. The amplitude of the sine wave current drawn by the PuLS was 7 A. For frequencies below 10 kHz, the PuLS measurements conforms with the simulated values more than the reference method which measured a higher output impedance. Between 10 - 80 kHz, the impedance curves are very similar but at 130 kHz the PuLS measurement of the output impedance starts to increase in comparison to the simulated values and the reference measurement which continues to decrease to approximately 400 kHz.

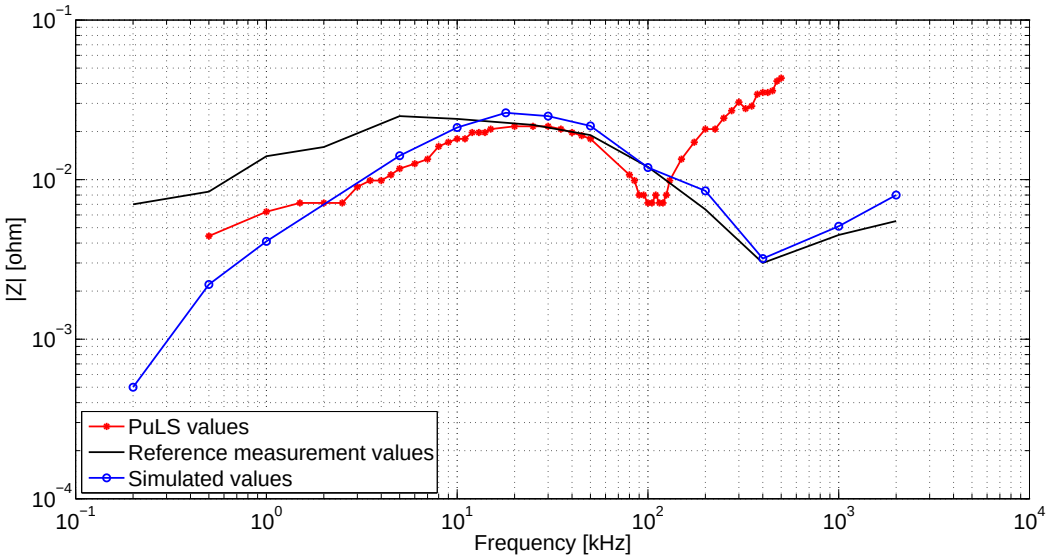

Figure 7.3: Comparison between the PuLS measurements, the reference measurements and simulated values of the output impedance of the 1.8 V buck converter.

Due to the discrepancy of the PuLS measurement over 130 kHz, a control measurement was made using an oscilloscope (LeCroy waveSurfer 44MXs-B). The amplitudes of the voltage ripple measured by the oscilloscope corresponded to the same values registered by the PuLS. This means that the sudden increase at 130 kHz is not due to incorrect measurements by the PuLS.

In the same way as the previous evaluation of the 1.8 V buck converter, the output impedance of the 5 V buck converter is shown in Figure 7.4. The measured impedance by the PuLS conforms with the simulated values from 1-80 kHz while the reference measurement shows a significantly higher output impedance for frequencies below 8 kHz. At 130 kHz, the measured impedance by the PuLS starts to increase in the same way as for the 1.8 V converter. For frequencies greater than 200 kHz, the reference measurements do not follow the simulated values as closely as for the 1.8 V buck converter, but are still closer to the simulated values than the impedance measured by the PuLS.

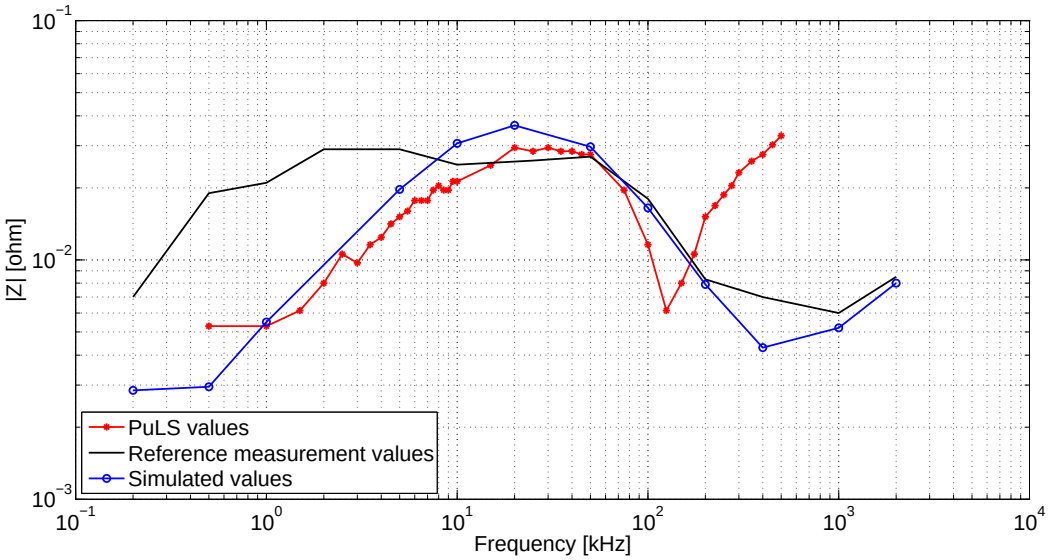

Figure 7.4: Comparison between the PuLS measurements, the reference measurements and simulated values of the output impedance of the 5 V buck converter.

In the same way as for the 1.8 V buck converter, the voltages and current amplitudes were measured with an oscilloscope and confirmed with the values registered by the PuLS. As seen in Figure 7.4, the PuLS measurement and the simulated values of the output impedance is approaching its highest values over 2 kHz and [19] states that the crossover frequency for the feedback loop is 45 kHz. This insinuates that the load should not have AC contents above 2 kHz to ensure that the output voltage ripple of the converter is kept low. To remain within the stable region of the controller, the load must not have AC contents above 45 kHz.

Almost the exact same results were obtained when different amplitudes (0.5-7 A) of the ripple current during the PuLS impedance measurement was used. Something worth noticing is that the lowest amplitude used by the PuLS was 0.5 A, which is about ten times higher than the amplitude of the reference measurements excitation current of 45 mA stated in Section 7.1.1.

7.2.2 Analysis of the Control Systems Effect on the Output Impedance

Considering the fact that the PuLS impedance measurement of the reference inductor in Section 5.3 showed a relatively trustworthy result. There is no reason to believe that the impedance measurement of passive components are wrong and are therefore not seen as the reason for the deviation in the PuLS output impedance measurement of the buck converters compared to the reference method.

A reason why the reference measurements and the measurements made by the PuLS did not match above 130 kHz for either the 1.8 V or the 5 V buck converter could be the fact that the controller of the buck converters are to slow to compensate for the large current drawn by the PuLS leading to relatively large voltage ripple. Figure 7.5 illustrates the gate voltage of the buck converter with the ripple current drawn from the PuLS at 130 kHz. It can be seen that the voltage control tries to regulate the output voltage since the duty is not constant.

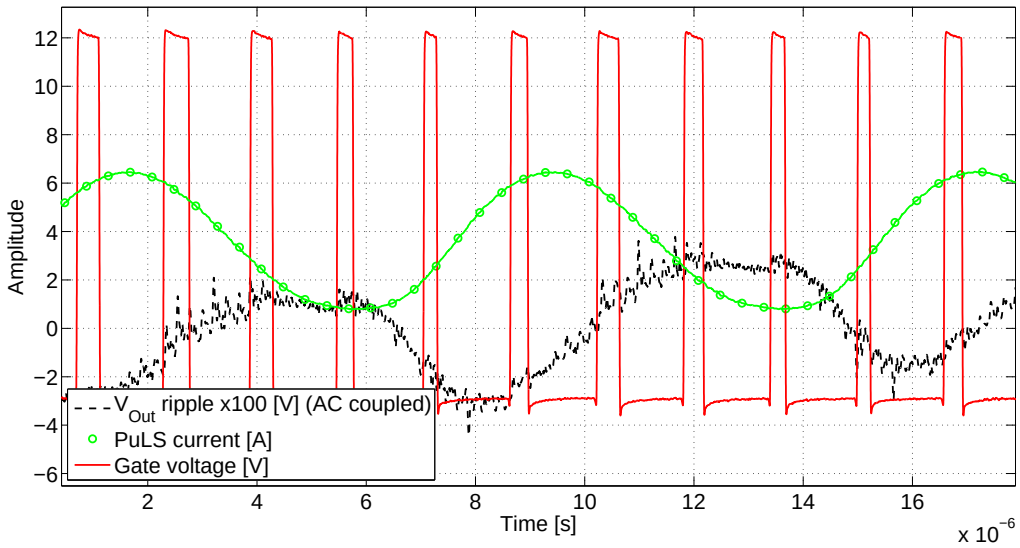

Figure 7.5: Gate voltage, output voltage and the output current 1.8 V buck converter at 130 kHz.

On the other hand, at 200 kHz test current as seen in Figure 7.6, the controller does not seem to regulate the duty cycle at all, this insinuates that the voltage ripple that arises from the PuLS sine waves is totally uncompensated for. Since the current ripple injected in the reference measurements was of the magnitude 45 mA compared to 6 A from the PuLS, the output voltage ripple from the converters is significantly higher. Because of the high excitation current, the PuLS might be better suited for loads with high rated current or converters with very low output impedance, such as batteries.

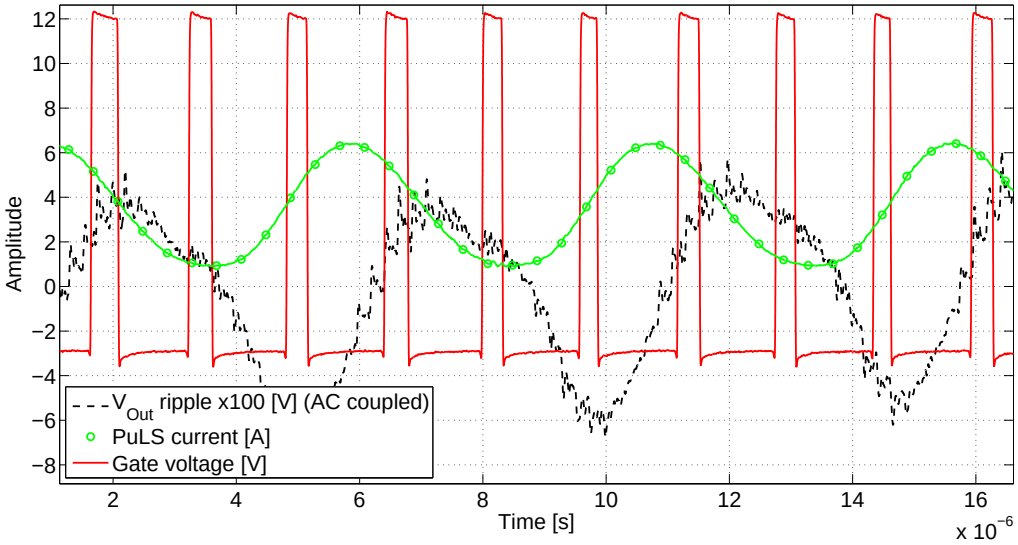

Figure 7.6: Gate voltage, output voltage and the output current 1.8 V buck converter at 200 kHz.

8 Conclusion

In this thesis a product called PuLS has been redesigned to be able to measure the output impedance of switched DC/DC converters. Existing measurement methods of the output impedance have been investigated with the conclusion that all the existing methods operates with the same principle, either injecting or loading a excitation current at the load and measuring the output voltage ripple. The theoretical output impedance of a buck converter has been calculated, although only considering the open loop of the converter. To see what the expected output impedance should be, simulations of simple buck models were performed. Measurements of the output impedance of two buck converters were made using the redesigned PuLS. The results were compared with an already existing impedance measurement method and with the simulation of the buck converters.

It has been shown that the PuLS can be used for output impedance measurements for switched DC/DC converters up to 80 kHz. The measurement of the reference inductors shows that the PuLS measures the impedance with sufficient accuracy between 500 Hz and 500 kHz. The analysed method is a fast and semi-automatic method which requires nothing more than just a computer, a power supply and a PuLS unit. The method can be used for converters with fairly slow loads as a quick way to analyse the output impedance. It can also be used for stability checks when loads with a known input impedance is used.

An advantage with the PuLS is the close connection to the tested device. This means the interconnection inductance are small in comparison with other methods and should lead to a more accurate measurement of the real impedance in the circuit. Other advantages with using the PuLS is the fast installation, the possibility to load several waveforms and the possibility to connect several PuLS devices and load them simultaneously. The method of sampling current waveforms means that any waveform can be created with high slew-rate. The choice to use the linear region of the MOSFETs and not using PWM gives that the harmonic content in the current is low even if no filter is used.

For the measured output impedance for the buck converters, it is uncertain if the measurement results are trustworthy at frequencies over 80 kHz since the method deviates from the reference method and the simulation over this frequency. Why the deviation occurs is not answered in this thesis but a couple of probable reasons have been discussed as causes for incorrect measurements. The most probable reason is that the high excitation current used by the PuLS makes the output filter or controller to behave in a different way than with a small excitation current.

The waveforms produced by the PuLS closely resembles the wanted waveforms at lower frequencies but due to the sampling within the microcontroller, small deviations in amplitude and phase are introduced at higher frequencies. These errors are caused by not hitting the absolute top of the sine wave with a sample point or missing a point where the slew rate is at its highest point. The low resolution of the voltage measurement used by the PuLS is another disadvantage. It makes voltage variations difficult to detect without using a high excitation current. Another disadvantage is the power dissipation due to its compact design and cooling, which makes very long pulses or constant current load operation difficult for power levels greater than 7.5 W.

9 Future Work

The PuLS voltage measuring system is insensitive to very small voltage variations. To improve the sensitivity of the measurement, an additional circuit can be added to the design that only measures the ripple voltage. This can be done with an AC filter which consists of a transformer or capacitors to filter out the DC voltages. Using an AC filter would mean that only the ripple voltage would be measured and a higher resolution can be used. Since the maximum input voltage to the microcontroller is 3.3 V, the voltage dividing circuit would rather increase the ripple voltage magnitude since it most often is in the mV range for switched DC/DC converters.

When considering the different current waveforms created by the PuLS, it is clear how flexible it can be as an arbitrary waveform current load. Practically any waveform can be drawn with some modification to the software of the PuLS. This ability to draw any current waveform can be used to simulate a various number of loads to certify requirements of many devices. The easiest way to create any waveform wanted is to adjust a graphical representation of the current shape in the GUI. To implement this, an algorithm for loading the sample points to the DMA is needed to be able to replicate the current set in the GUI.

The original as well as the redesigned PuLS can only draw positive current. If the PuLS would be able to inject current or create a sine wave with zero offset, the measurements could be performed on non operating converters. This would mean that an external power source would have to be implemented and with that a complete redesign of the PuLS to e.g. a four-quadrant converter is needed.

The DMA to DAC transfer rate of the microcontroller used in this thesis was 4.5 MHz. Due to the low number of points in the sine wave current drawn by the PuLS at higher frequencies, a microcontroller with a faster DMA to DAC transfer rate can be used to increase the quality of the sampled sine wave. In this way, the amplitude error might be decreased. Further, the minimum frequency of the current drawn from the PuLS is 500 Hz. To be able to draw currents below this frequency, the transfer rate has to be lowered or the memory of the controller increased. From an output impedance point of view, frequencies under 500 Hz are not usually cared for but such low frequencies can be used for impedance measurement of other devices such as passive components.

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