

Class D Power Amplifier Design in 22 nm CMOS for RF BP $\Delta\Sigma$ Modulated Signals

Master's thesis in Wireless, Photonics and Space Engineering

BJÖRN LANGBORN

MASTER'S THESIS 2020

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CHALMERS
UNIVERSITY OF TECHNOLOGY

Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience
CHALMERS UNIVERSITY OF TECHNOLOGY, Gothenburg, Sweden 2020

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Master's Thesis 2020

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Cover: Visualization of class D power amplifier in the context of $\Delta\Sigma$ -over-fiber. On the left-hand side, a $\Delta\Sigma$ modulator encodes an information signal to be transmitted over a fiber link. A photodetector receives the signal, driver amplifiers follow and finally the class D stage amplifies and filters out the analog information signal to be transmitted in the antenna.

Typeset in L^AT_EX
Gothenburg, Sweden 2020

Abstract

For future communication and sensor systems, energy efficient transmitters are essential to achieve good system performance. To this end, this thesis has investigated the efficiency, frequency, power and bandwidth limitations of Class D power amplifiers for bandpass $\Delta\Sigma$ modulated signals. Herein, bandpass $\Delta\Sigma$ modulation (BPDSM) allows for digitization of analog information signals, which is attractive from a system perspective, whereas Class D power amplifiers are suitable for digital signals and has an ideal efficiency of 100%. This paper will begin with theory on $\Delta\Sigma$ modulation, choice of semiconductor process technology, amplifier topology, and operational and design principles. From this theory, design equations are found that determine the limitations on the achievable output power and drain efficiency. Key parameters for the BPDSM and class D stage are highlighted. Three loss mechanisms for the class D stage are identified and quantified, namely switching, conduction and short circuit losses. Simulation studies have been performed, for the circuit in *Cadence's Virtuoso Analog Design Environment* (CVADE) using *GlobalFoundries* 22 nm FDSOI CMOS technology, and for the BPDSM in MATLAB using R. Schreier's *Delta Sigma Toolbox*. The simulations in CVADE were performed using Super Low-Voltage Threshold (SLVT) transistors. These simulations included transistor characterization by DC and S-parameter simulations, and circuit performance comparison between a class D stage using SLVT transistors with a switch model class D stage. From the design equations, the output power is seen to be limited by the BPDSM coding efficiency η_c , transistor on-resistances R_{on} and the process technology limiting the drain voltage V_{DD} . Furthermore, it is suggested that both the output power P_L and the drain efficiency η_d will be especially limited by high R_{on} , resulting in conduction loss, if the class D transistor widths are small. On the other hand, large transistor widths are expected to yield dominant switching losses at higher frequencies, due to parasitic capacitances, thus reducing η_d . The oversampling ratio $R_c = f_s/(2f_c)$ of the BPDSM is determined a key performance factor, because of its impact on both η_c and the switching losses. These theoretical results are confirmed in simulations. Additionally, it is found that η_c is limited by the input signal peak amplitude and Peak-to-Average Ratio (PAR), for signal preservation through the BPDSM and class D stage. However, no conclusive bandwidth limitation of the BPDSM class D PA is found in this study. Approaches to address the respective limitations, and alternative topologies that could improve performance, are mentioned.

Keywords: Class D RF Power Amplifiers, Delta-Sigma Modulation, Sigma-Delta Modulation, CMOS.

Acknowledgements

Many thanks to my supervisors Christian Fager, Lars Svensson and Jonas Fritzin. Additional thanks to Ibrahim Can Sezgin for help me with $\Delta\Sigma$ modulation in MATLAB. Final thanks to Infineon, for lending us Jonas and welcoming me to the office in Munich, and to GlobalFoundries for the access to the 22 nm FDSOI CMOS design kit.

Björn Langborn, Gothenburg, June 2020.



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1

Introduction

For future 5G systems, massive Multiple Input Multiple Output (MIMO) is considered a highly promising alternative to achieve high capacity networks. Research on transmitters to realise these networks have so far mostly focused on active antenna arrays with co-located antennas. However, this solution comes with the difficult issues of handling heat dissipation and integration. An alternative to this is to spatially distribute the active antennas, in a so-called Distributed Massive MIMO system, seen in Figure 1.1. Aside from removing the said issues with co-located active antennas, this also allows for benefits such as cell-free wireless communication systems [1], joint communication and wireless power transfer [2], drastically improved radar accuracy [3] and more.

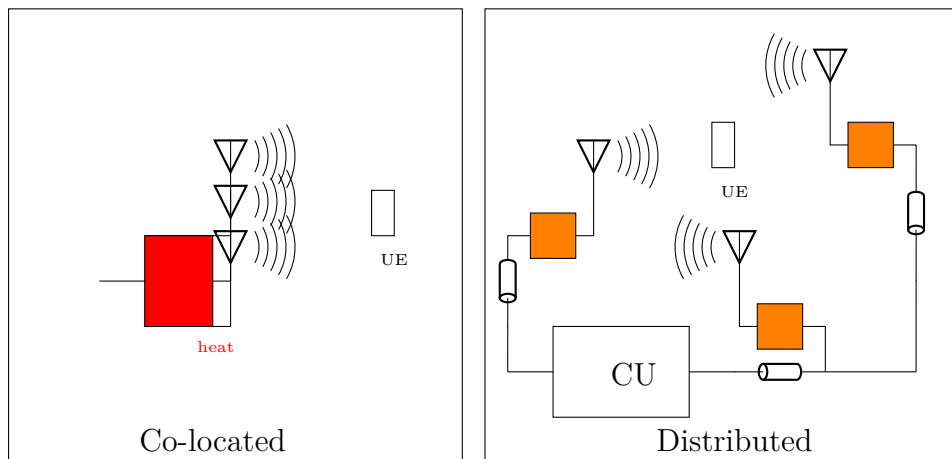


Figure 1.1: A transmitter in a co-located massive MIMO system, compared to transmitters in the distributed massive MIMO system.

For the distributed massive MIMO (DMIMO) system, the transmitters should be lightweight and energy efficient. This could be enabled by the rapid advance in modern CMOS technology, which can allow for digital signals to be processed at radio frequencies (RFs). While the distribution network in a DMIMO system could be realised with transmitting analog signals over fiber, digital realizations such as $\Sigma\Delta$ -over-fiber has shown promising results for high data rate, real-time applications using fewer components and having reduced electrical-to-optical sensitivity [4]. Transmitters using $\Delta\Sigma$ -modulation have the additional benefit of using signals with a constant signal envelope, which could potentially allow for Switch-Mode Power Amplifiers (SMPA) operating at high efficiency to be used, and quantization noise that falls outside of the signal bandwidth, which allows for relatively good signal quality [5]. Figure 1.2 exemplifies the transmit chain in such a system.

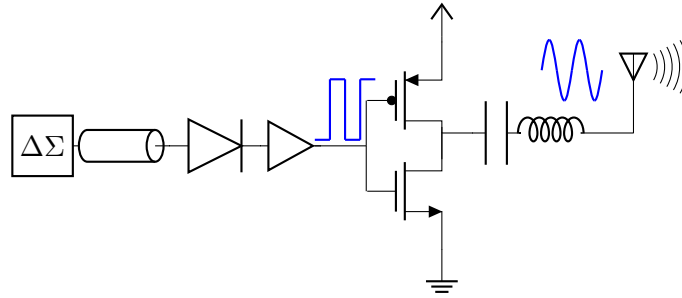


Figure 1.2: Example of $\Delta\Sigma$ -over-fiber transmit chain.

As for the SMPA implementation, the class D topology is of special interest. Compared to e.g. class E, the class D topology has higher output power capability and lower voltage stress across the transistors [6][7], whilst class F are more area demanding and complicated to realise. Implementing it differentially would have the additional benefit of increased output power and suppression of even order harmonics.

In this project, simulation studies have been performed to reach an understanding of the frequency, power, bandwidth and efficiency limitations of class D power amplifiers for RF $\Delta\Sigma$ -modulated signals. To see if operation around 26 GHz is feasible is one project goal that was investigated.

This work did not concern itself with any circuit design that comes prior to the main stage (including drivers) for the class D amplifier, nor to any circuit design coming after. This work involved $\Delta\Sigma$ modulators, but was limited to only study 1-bit bandpass $\Delta\Sigma$ modulated signals due to their attractiveness from a wireless system perspective [8] and suitability for switch-mode power amplifier driving.

Fabrication of the circuit was not be possible within the time scope of this thesis, therefore the work was limited to simulation studies.

This project aimed to answer the following questions:

- Is it possible to make a class D power amplifier operational for high RF (e.g. 26 GHz) $\Delta\Sigma$ modulated signals in 22 nm FDSOI CMOS technology?
- What is the achievable drain efficiency for the design? What output power and bandwidth is attainable?

2

Theory

In the following sections, the key concepts and theory for understanding this work will be presented. This includes a brief introduction to $\Delta\Sigma$ modulation, theory on the circuit process technology that is used for this work, how to model and characterize the transistors, the class D circuit topology, operational principles and governing equations.

2.1 $\Delta\Sigma$ modulation

$\Delta\Sigma$ modulation is a coding technique which can be used to re-code an analog signal into a digital pulse train. Specifically, information that for the analog signal is contained in continuous amplitude, phase and frequency variations are reshaped to discrete amplitude values, and discrete times, of the digital pulse train. This makes 1-bit $\Delta\Sigma$ modulation, having only two discrete amplitude values, suitable for using with switch-mode power amplifiers (SMPAs), who typically operates with binary input signals that either turn the switches on or off.

$\Delta\Sigma$ modulators can be made in different types, but they typically contain three key blocks: Filtering, quantization and feedback. Filtering is necessary to ensure we only encode the band of interest in our input signal. Quantization, on the other hand, is what codes the analog signal into a digital one. Quantizers can operate with a resolution of multiple bits, or with a single bit, as seen in Figure 2.1. Regardless of number of bits, the output of a quantizer will never exactly replicate the analog input signal. This discrepancy is called the quantization error.

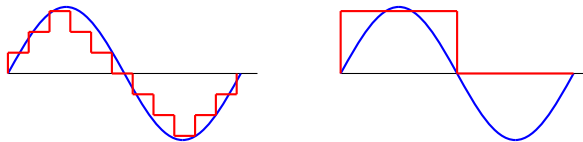


Figure 2.1: Example of multibit and one-bit quantization respectively.

Feedback is used in a $\Delta\Sigma$ modulator partly to suppress the quantization error within the signal bandwidth. If the quantizer has only one bit of resolution, the feedback is also necessary to actually retain sufficient amplitude information. This is because, if $x[n] = A[n] \sin(2\pi f_c n t_s)$, $A[n] > 0$ and the comparator is in reference to a voltage

level of 0, then

$$\begin{aligned}
 y[n] = x[n] + e[n] &= \begin{cases} V_{\text{dd}}, & \text{when } \sin(2\pi f_c n t_s) > 0, \\ 0, & \text{otherwise.} \end{cases} \\
 e[n] = y[n] - x[n] &= \begin{cases} V_{\text{dd}} - A[n] \sin(2\pi f_c n t_s) & \text{when } \sin(2\pi f_c n t_s) > 0, \\ -A[n] \sin(2\pi f_c n t_s) & \text{otherwise.} \end{cases}
 \end{aligned} \tag{2.1}$$

We see that the output $y[n]$ is independent of $A[n]$. As such, the output does not preserve the amplitude information of $x[n]$. The comparator can only distinguish between $A[n] = 0$ and $A[n] \neq 0$ in regards to amplitude modulation. However, when using feedback and oversampling this can be remedied.

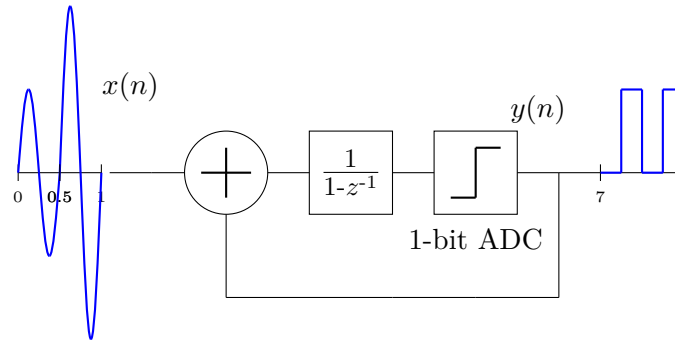


Figure 2.2: Schematic of a lowpass $\Delta\Sigma$ modulator.

A basic $\Delta\Sigma$ modulator is the low-pass $\Delta\Sigma$ modulator, seen in Figure 2.2. Solving this in the z -domain for $Y(z)$ we get

$$Y(z) = \underbrace{z^{-1} X(z)}_{\text{STF}} + \underbrace{(1 - z^{-1}) E(z)}_{\text{NTF}}, \tag{2.2}$$

where $Y(z)$ is the output signal, $X(z)$ input signal and $E(z)$ the error that is introduced by quantization. STF here stands for Signal Transfer Function and NTF for Noise Transfer Function. To understand that this modulation does preserve amplitude information, consider the special case when $z = e^{j2\pi f t_s}$. Then, the z -transform becomes a discrete Fourier transform and

$$X(e^{j2\pi f t_s}) = A[2\pi f t_s] * \frac{\pi}{j} \sum_{l=-\infty}^{l=\infty} [\delta(2\pi(f - f_c)t_s - 2\pi l) - \delta(2\pi(f + f_c)t_s - 2\pi l)], \tag{2.3}$$

where $*$ denotes convolution. Then,

$$Y(e^{j2\pi f t_s}) = e^{-j2\pi f t_s} X(e^{j2\pi f t_s}) + (1 - e^{-j2\pi f t_s}) E(e^{j2\pi f t_s}). \tag{2.4}$$

Now note that the zero placement of the NTF is at $z = 1$, equivalently $e^{-j2\pi f t_s} = 1$, which occurs at $f = 0$ i.e. DC for frequencies f below the sampling frequency $f_s = 1/t_s$. Thus, the error has been removed from the DC component, which is good since the signal baseband information is centered around DC. However, we want the

noise to be low for the entire baseband. Thus, consider that the baseband's highest frequency is greatly oversampled such that $f_s = 1/t_s \gg f_c$. Then

$$e^{-j2\pi ft_s} \approx 1 - j2\pi ft_s \dots, \quad (2.5)$$

and

$$Y(e^{j2\pi ft_s}) \approx X(e^{j2\pi ft_s}) - 2j\pi ft_s(E - X), \quad (2.6)$$

where the second term is negligible in terms of magnitude. Figure 2.3 shows the magnitude $|\text{NTF}|^2$ of such a transfer function, where it is seen that noise is pushed away from the baseband.

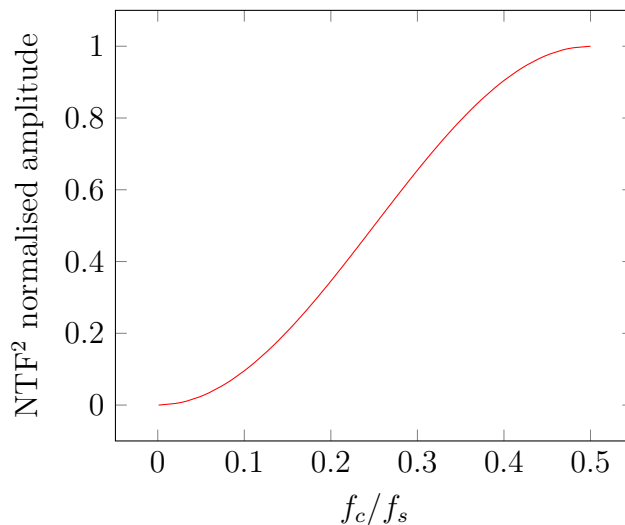


Figure 2.3: Example of noise transfer function squared $|\text{NTF}|^2$ for lowpass $\Delta\Sigma$ modulator as in (2.2).

In a bandpass $\Delta\Sigma$ modulator (BP $\Delta\Sigma$ M), the stopband for the NTF is centered at the carrier frequency and covering the bandwidth to the greatest extent possible. A simplified schematic of a BPDSM is seen in Figure 2.4. The carrier frequency can in theory be placed anywhere between DC and $f_s/2$ for BP $\Delta\Sigma$ Ms, but there are several considerations for optimal placement. The realization of the analog path loop, the bandpass architecture synthesis and digital mixing can all be simplified in a practical implementation with the choice of $f_s = 4f_c$ [9]. However, in [10] a BPDSM with sampling frequency of 5 GS/s for a carrier at 2.2 GHz ($f_s \approx 2.27f_c$) is implemented with a two-fold motivation. Firstly, the switch-mode power amplifier (SMPA) that follows the BPDSM in this work is implemented with transistors that have a rise and fall time that would not allow them to turn on the transistors in time if $f_s = 4f_c$ was chosen. Instead, lowering f_s allows for a frequency of operation otherwise not achievable. Secondly, lowering the sampling frequency at the BPDSM reduces the switching losses for the SMPA. This is highly relevant in order for high frequency operation to be feasible, and will be detailed further in section 2.3.4.

To realize a BP $\Delta\Sigma$ M, a transformation $z^{-1} \rightarrow -z^{-2}$ must be made to be able to place the NTF zeros at other frequencies than DC. Thus, the order of the modulator

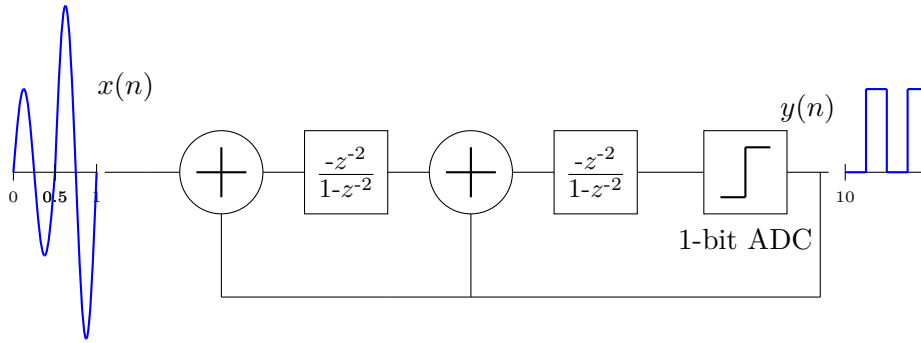


Figure 2.4: Schematic of a bandpass $\Delta\Sigma$ modulator.

needs to be at least 2. Higher order modulators can also be implemented, which have the benefit of reducing quantization noise but at the cost of complexity and risk of instability [11].

2.1.1 Coding Efficiency

In the process of quantization and recoding from an analog signal to a digital pulse train, quantization noise is added. To quantify this noise, the term *coding efficiency* can be defined as [12][11]

$$\eta_c = \frac{P_{\text{sig}}}{P_{\text{sig}} + P_{\text{qn}}}, \quad (2.7)$$

where P_{sig} denotes the power of the signal of interest, and P_{qn} denotes the quantization noise power. As an example, this quantity is for a Non-Return-to-Zero (NRZ) 50% duty cycle pulse train, with frequency f_c , equal to $8/\pi^2 \approx 81\%$ [12]. This is seen by taking a Fourier series of a NRZ 50% duty cycle voltage wave and noting the amplitude of the fundamental component

$$\text{sgn}(\sin(2\pi f_c t)) = \underbrace{\frac{4}{\pi}}_{V_{f_c}} \sin(2\pi f_c t) + \frac{4}{\pi} \frac{1}{3} \sin(3 \cdot 2\pi f_c t) + \dots, \quad (2.8)$$

such that (normalizing the load, $R = 1$) $P_{\text{sig}} = (V_{f_c}/\sqrt{2})^2 = 8/(\pi^2)$, and $P_{\text{qn}} = (4/(\sqrt{2} \cdot 3\pi))^2 + (4/(\sqrt{2} \cdot 5\pi))^2 + \dots = (1 - 8/\pi^2)$ and as such from (2.7), $\eta_c = 8/\pi^2$.

However, the coding efficiency for a general $\Delta\Sigma$ modulated signal can not be stated as easily in a directly analytically solvable equation. Special cases, such as when the input signal is a pure sinusoidal tone, exists where the coding efficiency can be determined or estimated analytically. Appendix A.2 elaborates on the case of a sine ton. But in general it is not easy. This is simply because the pulse train has a frequency that varies aperiodically between DC and the sampling frequency f_s , depending on the input signal. Additionally, it varies with a number of factors such as the oversampling factor $R_c = f_s/(2f_c)$, rise and fall time of the pulse τ_r , τ_f and variations (e.g. amplitude, bandwidth) in the input signal [12]. Also, it depends on if the pulse train is a NRZ pulse or Return-to-Zero (RZ). Redoing the Fourier series

of (2.8) for a RZ pulse we get

$$\frac{1}{2} + \frac{1}{2} \operatorname{sgn}([\sin(2\pi f_c t)]) = \frac{1}{2} + \underbrace{\frac{2}{\pi}}_{V_{f_c}} \sin(2\pi f t) + \frac{2}{\pi} \frac{1}{3} \sin(3 \cdot 2\pi f t) + \dots, \quad (2.9)$$

from which a maximal coding efficiency

$$\eta_c = \frac{(2/(\sqrt{2}\pi))^2}{(2/(\sqrt{2}\pi))^2 + (1/2)^2 + (2/(3 \cdot \sqrt{2}\pi))^2 + \dots} = \frac{2/\pi^2}{1/2} = \frac{4}{\pi^2}, \quad (2.10)$$

which is half the coding efficiency of a NRZ pulse train, due to the DC level that was not present for the NRZ pulse train. With all this in mind, the coding efficiency for a $\Delta\Sigma$ signal can be calculated given e.g. power spectral density S_{yy} of the pulse train according to

$$\eta_c = \eta_{DT} [\operatorname{sinc}(1/[2R_c]) \cdot \operatorname{sinc}(f_c T_{r,f})]^2, \quad (2.11)$$

where

$$\eta_{DT} = \frac{1}{P_{\text{tot}}} \int_{f_c - \text{BW}/2}^{f_c + \text{BW}/2} S_{yy}(f) df. \quad (2.12)$$

Here, η_{DT} denotes the discrete time coding efficiency, $T_{r,f}$ denotes the rise and fall time of the pulse (assumed equal), f_c the carrier frequency and P_{tot} the total pulse train power [12].

An example of how the oversampling ratio affects the coding efficiency, according to (2.11), is in Figure 2.5.

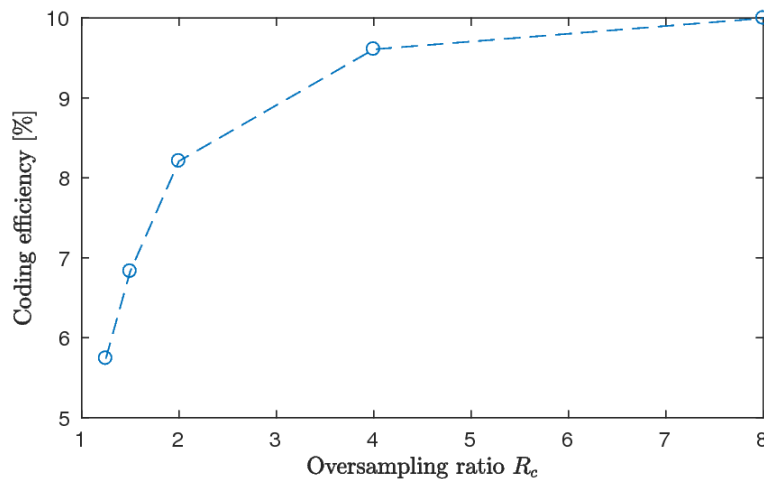


Figure 2.5: Coding efficiency plotted against the oversampling ratio R_c .

2.2 Circuit Technology

This section will start with details on the Fully Depleted Silicon-On-Insulator (FD-SOI) Complementary Metal-Oxide-Semiconductor (CMOS) circuit technology that has been used in this work. After that, theory on how to model the transistor behaviour is presented.

2.2.1 FDSOI Circuit Technology

Fully Depleted Silicon-On-Insulator (FDSOI) Complementary Metal-Oxide-Semiconductor (CMOS) transistor technology is a type of MOS technology for Field-Effect Transistors (FETs), characterized by a number of unique properties. Firstly, the FDSOI channel is typically undoped to eliminate random dopant fluctuations in the channel, which reduces variability in the threshold voltage V_{th} [13][14]. Additionally, this enables good short channel control and a reduction of gate-induced-drain-leakage [14][15]. Secondly, below the channel a Buried Oxide (BOX) is placed instead of having a bulk well of the reverse polarity as in conventional MOSFETs. This, amongst other things, reduces parasitic capacitances from source to drain, C_{ds} , via junction capacitance through the bulk [13][14].

Back biasing, which is easier attainable for buried oxide devices [15], in FDSOI allows for adjusting V_{th} to suit the application. For high frequency applications, the transistors must be fast at switching. Therefore, one typically uses the super low-voltage threshold transistors in the 22nm design kit, in which the back gate is forward biased [14].

2.2.2 Transistor modelling

Class D power amplifiers are so-called switch-mode power amplifiers, and as such it is natural to model the transistors as switches. Generally when characterizing a transistor, a transistor model is assumed and one tries to extract model parameter values such that the model behaves similarly to the real transistor. Depending on the application, one might need to characterize the transistor over a smaller or wider range of possible voltage and current levels at the respective terminals. In this work, the transistor in FDSOI technology (seen in Figure 2.6) is characterized in reference to a simplified transistor model as in [16], seen in Figure 2.7. However, only the parasitic capacitances C_{gs} between gate and source, C_{gd} between gate and drain, C_{ds} between drain and source, and the drain-to-source resistance r_{ds} were practically used. Additionally, the characterization for transistors used for switch-mode power amplifiers is most critical for the two states of operation: On and off-state.

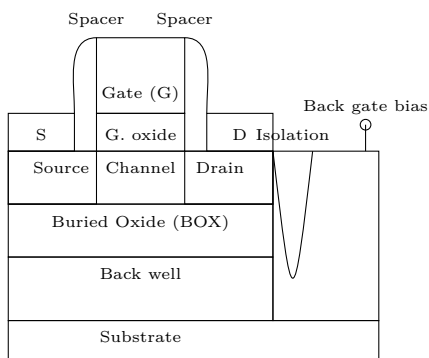


Figure 2.6: Schematic view of FDSOI transistor structure.

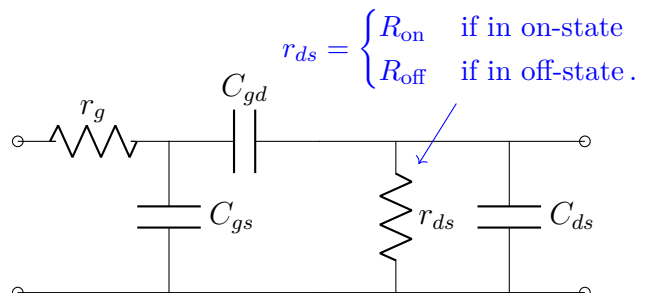


Figure 2.7: Equivalent circuit model for the transistors.

Both r_{ds} and the capacitances will change under various biasing conditions. One way to simplify the gate capacitances is to consider them as

$$\begin{aligned} C_{gs} &= C_{ov}W + C_{gcs}(V_{GS}, V_{DS})W \\ C_{gd} &= C_{ov}W + C_{gcd}(V_{GS}, V_{DS})W \end{aligned} \quad (2.13)$$

where C_{ov} is a constant capacitance due to overlap between the gate metal to source and drain regions (including fringing field effects), W the transistor width and C_{gcs} , C_{gcd} are capacitances from gate to source and drain via the formed channel when the transistor is on. These capacitances are therefore functions of the DC bias voltages (V_{GS} , V_{DS}). A simplified model for the channel capacitances of an NMOS transistor is found in [17] (with the width W accounted for in (2.13))

$$\begin{aligned} C_{gcs}(V_{GS}, V_{DS}) &\approx \begin{cases} 0 & \text{Device off, } V_{GS} < V_{thn} \\ \frac{1}{2}C_{ox}L & \text{Device in linear region, } V_{GS} > V_{thn}, V_{DS} < V_{GS} - V_{thn} \\ \frac{2}{3}C_{ox}L & \text{Device in saturation region, } V_{GS} > V_{thn}, V_{DS} \geq V_{GS} - V_{thn} \end{cases} \\ C_{gcd}(V_{GS}, V_{DS}) &\approx \begin{cases} 0 & \text{Device off, } V_{GS} < V_{thn} \\ \frac{1}{2}C_{ox}L & \text{Device in linear region, } V_{GS} > V_{thn}, V_{DS} < V_{GS} - V_{thn} \\ 0 & \text{Device in saturation region, } V_{GS} > V_{thn}, V_{DS} \geq V_{GS} - V_{thn} \end{cases} \end{aligned} \quad (2.14)$$

where $V_{thn} > 0$ is the threshold voltage for an NMOS, and for the PMOS transistor

$$\begin{aligned} C_{gcs}(V_{GS}, V_{DS}) &\approx \begin{cases} 0 & \text{Device off, } V_{GS} > V_{thp} \\ \frac{1}{2}C_{ox}L & \text{Device in linear region, } V_{GS} < V_{thp}, V_{DS} > V_{GS} - V_{thp} \\ 0 & \text{Device in saturation region, } V_{GS} < V_{thp}, V_{DS} \leq V_{GS} - V_{thp} \end{cases} \\ C_{gcd}(V_{GS}, V_{DS}) &\approx \begin{cases} 0 & \text{Device off, } V_{GS} > V_{thp} \\ \frac{1}{2}C_{ox}L & \text{Device in linear region, } V_{GS} < V_{thp}, V_{DS} > V_{GS} - V_{thp} \\ \frac{2}{3}C_{ox}L & \text{Device in saturation region, } V_{GS} < V_{thp}, V_{DS} \leq V_{GS} - V_{thp} \end{cases} \end{aligned} \quad (2.15)$$

where $V_{thp} > 0$ is the threshold voltage for the PMOS transistor. From this we note that the gate to drain, and gate to source, capacitance of a device will increase when turned on due to formation of the channel. Additionally, C_{gcs} for an NMOS and C_{gcd} for a PMOS are maximal during saturation. However, simplifying the analysis to on and off-state, only the linear region and off-state are of interest.

Other capacitances that could be considered, e.g. junction capacitance, are deemed negligible in comparison to the ones mentioned. E.g. neglecting junction capacitance is motivated by the buried oxide in the process, which isolates the substrate [13][14].

When the NMOS or PMOS are turned on in the class D configuration, they will initially be in saturation with low channel resistance and in that state will be able to drive a large current to discharge the output capacitances. As the output capacitances discharge, the transistor operation goes into the linear region. The transition is very brief. The linear region is where the transistor operates for the most part during a cycle, and thus the resistance of the device in this region is necessary to know

for estimating output power and conduction losses. A well-known expression for the on-resistance of an NMOS transistor in the deep linear region ($V_{DS} \ll 2(V_{GS} - V_{thn})$) is [18]

$$R_{on,n} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{thn})} \quad (2.16)$$

From this we see that the on-resistance is dependent on the overdrive voltage $V_{GS} - V_{thn}$, the width to length ratio W/L of the transistor, the oxide capacitance C_{ox} and electron mobility μ_n . For a given process technology, only W/L and the overdrive voltage can be altered by the designer to lower the on-resistance. This formula is analogous for PMOS transistors.

2.2.3 Transistor characterization

Accurate transistor modelling and characterization is a difficult task, especially for large-signal models. Luckily, characterization for a limited bias range is simpler. For a limited bias range, the model can be linearized. This allows us to use S-parameter simulations in order to determine the parasitic capacitances as

$$\begin{aligned} C_{gs} &= \text{Im}\{Y_{11} + Y_{12}\}/\omega \\ C_{gd} &= -\text{Im}\{Y_{12}\}/\omega \\ C_{ds} &= \text{Im}\{Y_{22} + Y_{12}\}/\omega \end{aligned} \quad (2.17)$$

where ω is the angular frequency. These formulas are derived in Appendix A.1. To find the on-resistance on the other hand, DC simulation to obtain the $I_{ds} - V_{ds}$ curves can be made. Keeping V_g at a level where the transistor is on, and varying V_{ds} , the on-resistance will be

$$\frac{1}{R_{on}} = \frac{\Delta I_{ds}}{\Delta V_{ds}}, \quad (2.18)$$

measured in the deep linear region for the respective transistor. As such, R_{on} is equal to the inverse linear slope of the $I_{ds} - V_{ds}$ curves.

2.3 Class D Circuit Design

Different switch-mode power amplifier (SMPA) topologies have different properties and operational principles, making them more or less suitable for amplifying digital signals. The classes D, E and F (and their inverses) are all common SMPA topologies. In this work, a voltage mode class D power amplifier was chosen for study over the current mode class D power amplifier simply due to the slightly more intuitive circuit topology. Class E could have been interesting to investigate, but was not elected over class D as the main focus of study due to the high voltage stress $V_{ds} = 3.56 V_{DD}$ that is exerted on the transistor [19] and lower output-power capability [7]. However, finite inductance in the DC feed and common-gate switching as in [20], or cascoding as in [21][22] (though here implemented for class D) could alleviate the voltage stress issue. Class F on the other hand was considered too bulky, area consuming, and complicated given its multi-harmonic resonance requirements in the output network.

In the following subsections, the voltage mode class D stage's operational principles and equations will be detailed, and an equivalent switch model will be introduced.

2.3.1 Voltage mode class D

A class D voltage-mode power amplifier implemented with NMOS and PMOS transistors, driven by a periodic 50% duty cycle pulse train, is seen in Figure 2.8, with corresponding ideal current and voltage waveforms seen in Figure 2.9. The class D topology in general is characterized by having two switches (here, the PMOS and NMOS devices) and an output network that is resonant at a desired frequency $f_c = 1/(2\pi\sqrt{L_f C_f})$. At any given time, one of the switches is on and the other one is off. When Q2 is on current is delivered from the source V_{DD} to the resonant circuit consisting of C_f and L_f . When Q1 is on, current is drawn from the resonant circuit through Q1 and to ground. Due to the output network resonance, the current has a periodicity of f_c so that it becomes zero in each switching instance of the voltage. Therefore, since the current through, and voltage over, any switch is never non-zero at the same time no power is lost in the transistors.

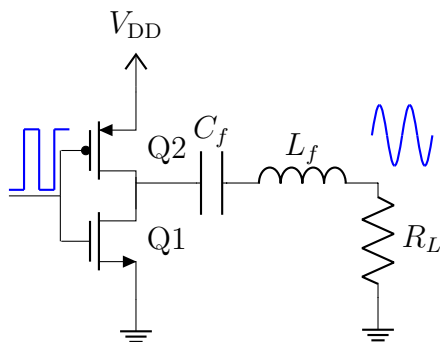


Figure 2.8: Class D topology, using NMOS (Q1) and PMOS (Q2) transistors.

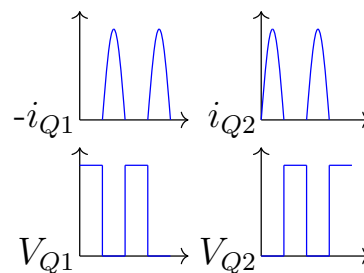


Figure 2.9: Current and voltage waveforms of a class D PA.

2.3.2 Switch model

A simplification of the class D inverter stage as in Figure 2.8 is to model the transistors as switches with on-resistance and constant parasitic capacitances, as in Figure 2.10.

2.3.3 Ideal Class D Circuit Analysis

In the class D topology, as seen in Figure 2.8, the ideal assumptions made should be elaborated upon to understand the available output power and drain efficiency η_d . The ideal circuit assumptions are that the transistors Q1 and Q2 have zero on-resistance, no parasitic capacitances are present, the rise and fall times of the pulses are zero, and that L_f and C_f have no resistance. With a $\Delta\Sigma$ input signal, the fundamental tone will be reduced due to the coding efficiency η_c as understood

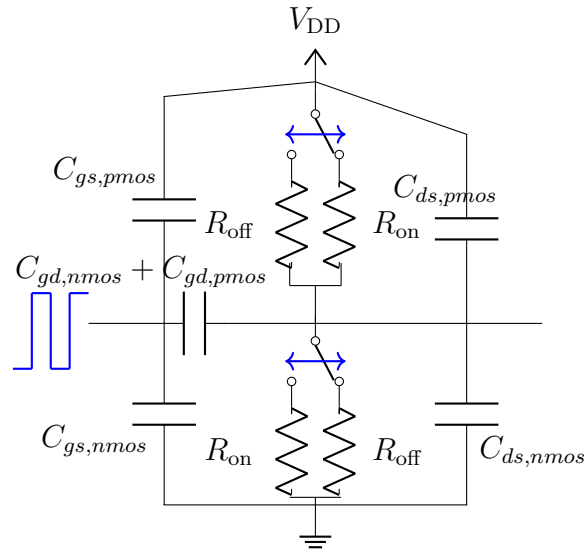


Figure 2.10: Switch model of the class D topology. The blue arrows above the switches indicates that the input signal controls the state that the switch is in.

by (2.7). Thus the fundamental peak voltage will be $V_{\text{fund}} = \sqrt{\eta_d} V_{DD}$ in the output node shared by Q1 and Q2, the RMS voltage $V_{\text{fund, RMS}} = \sqrt{\eta_d} V_{DD} / \sqrt{2}$ and thus

$$P_L = \eta_c \frac{(V_{DD}/\sqrt{2})^2}{R_L}, \quad (2.19)$$

will be the power delivered to the load R_L . The drain efficiency will be 100%, since there is no loss mechanism involved. A derivation of this for periodic signals can be found in e.g. [23], but with no loss mechanism involved it clearly holds also for non-periodic signals.

2.3.4 Non-ideal Class D Circuit Analysis

By introducing resistances in the transistors and LC -network, the output power delivered to the load will change from (2.19) to

$$P_L = \eta_c \frac{(V_{DD}/\sqrt{2})^2 R_L}{(R_{LC} + R_{\text{on}} + R_L)^2}. \quad (2.20)$$

where $V_{DD}/\sqrt{2}$ is the RMS-voltage squared for a 50% duty cycle square wave with frequency f_c , $R_L/(R_{LC} + R_{\text{on}} + R_L)^2$ is from voltage division over the load R_L and on-resistance R_{on} plus LC -network resistance, and η_c takes into consideration the coding efficiency, i.e. how much the fundamental power is in relation to the total pulse train power. This formula also holds when introducing moderate parasitic capacitances, and non-zero rise and fall times. The rise and fall times are considered in the expression for η_c when it comes to output power, but was necessary to keep zero in the ideal analysis to exclude short-circuit losses (which will be explained later on). The parasitic capacitances can also be introduced without invalidating (2.20),

if moderate in magnitude so that they do not overwhelmingly distort the waveforms at the inverter output.

With non-idealities introduced, η_d will no longer be 100%. In the following subsections, each loss mechanism that deteriorates the performance will be addressed.

2.3.4.1 Switching losses

The switching losses in the class D stage is essentially the power that is lost by charging and discharging parasitic capacitances. A visualization can be seen in Figure 2.11. This process consumes supply current, but does not contribute to the output power. The switching loss P_{sw} can in a more general form be given by e.g. [12]

$$P_{sw} = 2f_{av}E(W_Q), \quad (2.21)$$

where f_{av} is the average switching frequency and $E(W_Q)$ is the expected value of the change in stored energy W_Q in the circuit capacitances. Explicitly,

$$W_Q = \Delta W_{gs} + \Delta W_{ds} + \Delta W_{gd}, \quad (2.22)$$

i.e. the change in energy stored over the gate-to-drain (gs), the drain-to-source (ds) and the gate-to-drain (gd) of the class D stage. However, this can be simplified and more easily calculated making two assumptions¹. First, assume that the voltage at the inverter input and output nodes are constant and either V_{DD} or 0 in each switching instant. This is approximately valid if we have small on-resistances, since the voltage drops across the transistors are then small, and for moderate rise and fall times of the pulse train as to avoid overshoot from cross coupling via C_{gd} [24]. Secondly, assume that the transistor capacitances are constant for each transition and in accordance with the following:

When the input transitions from $V_g = 0$ mV to 900 mV, the NMOS is initially off, PMOS on and inverter output node voltage approximately 900 mV. In this transition, $C_{gs,NMOS,off}$, $C_{ds,PMOS,on}$, $C_{gd,NMOS,off}$ and $C_{gd,PMOS,on}$ are charged whereas $C_{gs,PMOS,on}$, $C_{ds,NMOS,off}$, but also $C_{gd,NMOS,off}$ and $C_{gd,PMOS,on}$ are discharged. Similarly, when the input transitions from $V_g = 900$ mV to 0 mV, the NMOS is initially on, PMOS off and inverter output node voltage approximately 0 mV. Then, $C_{gs,PMOS,off}$, $C_{ds,NMOS,on}$, $C_{gd,NMOS,on}$ and $C_{gd,PMOS,off}$ are charged, but $C_{gs,NMOS,on}$, $C_{ds,PMOS,off}$, $C_{gd,NMOS,on}$ and $C_{gd,PMOS,off}$ discharge. The reoccurring inclusion of the gate-to-drain capacitances is consistent with the Miller effect, which is known to effectively double the gate-to-drain capacitance over the whole signal transition [25]. This is then because of how C_{gd} each transition not only discharges fully but afterwards recharges with opposite polarity. This reasoning also gives consistent power analysis with e.g. [26]. From these statements we can define the total capacitance that is charged in each transition as

$$\begin{aligned} C_{tot, V_g \text{ low to high}} &= C_{gs,NMOS,off} + C_{ds,PMOS,on} + C_{gd,NMOS,off} + C_{gd,PMOS,on}, \\ C_{tot, V_g \text{ high to low}} &= C_{gs,PMOS,off} + C_{ds,NMOS,on} + C_{gd,NMOS,on} + C_{gd,PMOS,off}. \end{aligned} \quad (2.23)$$

¹The assumption made here are similar, but not identical to those in [12].

Making these assumptions, (2.21) reduces to

$$P_{sw} = f_{av} V_{DD}^2 \frac{1}{2} (C_{tot, V_g \text{ low to high}} + C_{tot, V_g \text{ high to low}}), \quad (2.24)$$

The factor 1/2 comes from the fact that f_{av} includes both rise and fall transitions, and accounts for the fact that both total capacitances are included in the formula. Note that this is similar to the equation for power consumption in an inverter by charging of a single load capacitor, where in a single transition [27]

$$P_{V_{DD}, 0 \rightarrow 1} = \int i_{C_L} V_{DD} dt = V_{DD} C_L \int_{V_{C_L}=0}^{V_{DD}} \frac{\partial V_{C_L}}{\partial t} dt = V_{DD}^2 C_L \quad (2.25)$$

such that the average power consumption scales with the average transition frequency f_{av} as

$$P_{V_{DD}} = V_{DD}^2 C_L f_{av}, \quad (2.26)$$

which is also well-known from literature [7]. With known conduction loss and short-circuit loss in a circuit, P_{sw} is also obtainable by solving

$$\eta_d = \frac{P_L}{P_L + P_{sw} + P_{sc} + P_{cond}} \quad (2.27)$$

for P_{sw} which gives

$$P_{sw} = \frac{P_L(1 - \eta_d) - \eta_d(P_{sc} + P_{cond})}{\eta_d}. \quad (2.28)$$

Note that the output filter capacitance, C_f in Figure 2.8, does not contribute to switching losses. The current through the series LC has a forced periodicity at the fundamental frequency, and the inductor L_f prevents any rapid discharges of current from C_f , even when the inverter output node voltage drops.

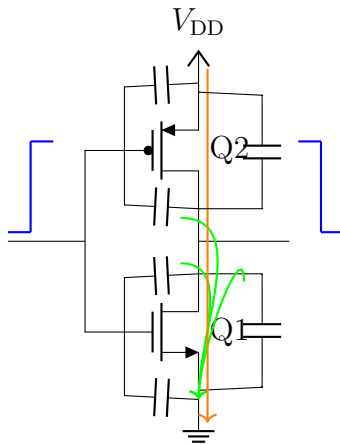


Figure 2.11: Inverter part of class D stage with short-circuit current losses and switching losses visualized, in orange and green lines respectively.

2.3.4.2 Short-Circuit Current Losses

Short-circuit current losses occur when both the NMOS and PMOS transistors are active at the same time, so that current has a direct path from the supply V_{DD} to ground, as visualized in Figure 2.11. This loss mechanism is inherent to inverters in general, and not specific to class D power amplifiers. Additionally, it is a quantity that relatively simply can be estimated from static conditions (i.e. DC simulations) [28], even though consideration to circuit dynamics lead to more accurate results [29].

2.3.4.3 Conduction Losses

Conduction loss is the unintended power loss due to resistive circuit components. Two ways of equating the conduction loss are mentioned in [12], namely solving

$$\eta_d = \frac{P_L}{P_L + P_{\text{cond}}}, \quad (2.29)$$

for P_{cond} in a setting when all other losses are non-existent, or alternatively calculating

$$P_{\text{cond}} = i_{L,\text{RMS}}^2 (R_{\text{on}} + R_{LC}), \quad (2.30)$$

which is valid in the presence of other loss mechanisms. This can also be expressed as

$$P_{\text{cond}} = P_L \frac{R_{\text{on}} + R_{LC}}{R_L}, \quad (2.31)$$

which is seen in comparison with (2.20), since the peak load voltage V_L and peak current through the on-resistance to the load i_L is

$$\begin{aligned} V_L &= \sqrt{\eta_c} V_{DD} \frac{R_L}{R_L + R_{\text{on}} + R_{LC}} \\ \implies i_L = V_L / R_L &= \sqrt{\eta_c} V_{DD} \frac{1}{R_L + R_{\text{on}} + R_{LC}} \\ \implies P_{\text{cond}} &= (i_L / \sqrt{2})^2 (R_{\text{on}} + R_{LC}) = P_L \frac{R_{\text{on}} + R_{LC}}{R_L}. \end{aligned} \quad (2.32)$$

With the design equations derived in this theory section, it will be possible to quantify the output power and the loss mechanisms, and ensure consistency between the expected circuit behaviour and simulated results.

3

Method

In this section the procedure for this thesis to investigate class D PAs for $\Delta\Sigma$ modulated signals will be detailed. Firstly, the procedure of generating $\Delta\Sigma$ modulated signals in MATLAB will be described. After that, the characterization of transistors in comparison to an assumed transistor model will be described. The design procedure of the class D power follows, and lastly the circuit evaluation will be presented.

3.1 Generating $\Delta\Sigma$ modulated signals

Whilst not part of the circuit design, the task of signal generation is critical. This entails generating a modulated analog signal, encoding it with $\Delta\Sigma$ modulation and ensuring that the obtained $\Delta\Sigma$ signal preserves the signal content sufficiently. This was done in the following manner.

First, one sets the key parameters of the circuit. This includes the carrier frequency f_c , sample frequency of the modulator $f_s = 2R_c f_c$, where R_c is the oversampling ratio in relation to the carrier, and order M (and modulator architecture) of the $\Delta\Sigma$ modulator. After that, one determines a modulation format, e.g. 64QAM, and generates a number of bits to be recoded to symbols. For realistic simulations, these bits are random, but test cases may use deterministic bit patterns. After generating symbols, filtering with e.g. a raised cosine filter is made using `rcosdesign`[30] and normalized so that the maximum amplitude is 1. Upconversion to the carrier frequency is then done, real part is taken, and the analog signal given to a $\Delta\Sigma$ modulator. In this work, the 'Delta Sigma Toolbox' [31][32] is used. Consider the input analog signal amplitude carefully, as the SNQR of the BPDSM improves with increasing input amplitude until a certain point where it drastically decays[12]. Too large of an input amplitude will result in clipping after the reconstruction filter in the amplifier, and can cause instability in the $\Delta\Sigma$ modulator [8]. To ensure that the analog signal bandwidth is sufficiently preserved, it is useful to after this compare the frequency content of the two signals. Additionally, ensuring power preservation via Parseval's theorem is also a good sanity check of the results. If something is awry, e.g. the $\Delta\Sigma$ output being too narrowband, the modulator parameters can be altered. A Return-to-Zero (RZ) pulse train is used for the input, since the class D inverter output will be RZ and the NMOS transistor threshold voltage is positive.

Once these steps have been made, the coding efficiency can be calculated in accordance with (2.11), and the predicted output power of the circuit in accordance with (2.20) calculated. It can also be useful to compare to the in-band power of the signal

here with (2.20) but η_c replaced with η_{DT} , and $R_{\text{on}} = 0$, since these should be about equal. η_{DT} is used since the conversion to continuous time has not been made at this point.

The average transition frequency f_{av} mentioned in 2.21 is calculated practically as $\# \text{transitions for entire signal duration} / (\text{entire signal duration})$ which in MATLAB gives `sum(diff(sig)~=0)/(t(end)-t(1))`, i.e.

$$f_{\text{av}} = \frac{\#(\text{transitions during time } T)}{T}. \quad (3.1)$$

3.1.1 $\Delta\Sigma$ coding dependence on input signal variations

To study how the coding efficiency depends on the input signal variations, several types of input signals were generated and fed to the $\Delta\Sigma$ modulator. Specifically, QPSK and various degrees of M-QAM were used. Once the analog signal was generated, additive white Gaussian noise was added. Then, after $\Delta\Sigma$ modulation the Signal-to-Noise Ratio (SNR) and coding efficiency were calculated for the output signal. The SNR is calculated by taking the Fourier transform of the output signal, and calculating the mean power within the signal bandwidth divided by the mean noise power in the near vicinity of the signal bandwidth. Specifically, the noise band was chosen as $\{f_c - 2\text{BW} < f < f_c + 2\text{BW}\} \setminus \{f_c - \text{BW}/2 < f < f_c + \text{BW}/2\}$, i.e. the first set of frequencies excluding the second set. The noise power is calculated near the carrier, and not over the whole frequency span, to get as good an estimate as possible for the in-band noise. This is similar to the SNR calculation in the Delta-Sigma toolbox.

3.2 Transistor characterization

In order to quantify circuit losses, and investigate the validity of replacing the transistors in the class D topology with simpler switch models, it is necessary to characterize the transistor. In this work, the transistors are modelled as in [16], seen in Figure 2.7. To achieve fast switching and high on-currents [14], super low-voltage threshold (SLVT) transistors from the design kit are used.

The parasitic capacitances were extracted through S-parameter simulations on the transistors, under on and off-bias conditions. On and off-bias conditions refer to the bias conditions that the transistors will have in the class D inverter configurations during respective states. On-bias for the NMOS transistor that means $V_g = 900 \text{ mV}$, $V_d \lesssim 100 \text{ mV}$ and $V_s = 0 \text{ mV}$. On-bias for the PMOS transistor that means $V_g = 0 \text{ mV}$, $V_d \gtrsim 800 \text{ mV}$ and $V_s = 900 \text{ mV}$. On the other hand, off-bias for the NMOS transistor that means $V_g = 0 \text{ mV}$, $V_d \gtrsim 800 \text{ mV}$ and $V_s = 0 \text{ mV}$. Off-bias for the PMOS transistor that means $V_g = 900 \text{ mV}$, $V_d \lesssim 100 \text{ mV}$ and $V_s = 900 \text{ mV}$. From the S-parameter measured data, conversion to Y-parameters is made, and the parasitic capacitances are extracted as in (2.17).

The on-resistance of the devices was characterized both using the S-parameter data as in [16], but also from DC simulation, which is a more intuitive approach. In a

DC simulation, IV-characteristics were measured for each device when they were in the linear region, by sweeping V_{ds} over the device with a fixed V_g . The slope of the IV-curve in this region corresponds to the on-resistance, in agreement with (2.16). Both ways of characterizing the on-resistance gave the same results.

3.3 Loss characterization

This section is dedicated to describing how the conduction, switching and short-circuit current losses were quantified.

3.3.1 Conduction losses

One approach to estimate the conduction loss is via the class D switch model, as seen in Figure 3.1. Here, since the switches can be made to have no overlap in on-states there will be no short-circuit current. Additionally, the parasitic capacitances are set to zero to remove switching losses. All the losses that arise during simulations are then conduction losses, via the switch on-resistances. As such, a simulation with a $\Delta\Sigma$ modulated signal was performed and the output power and drain efficiency measured. From (2.29) or (2.31), the conduction loss can be calculated. This was measured for various R_{on} , corresponding to the on-resistances calculated in section 3.2, for transistor widths from $16\ \mu\text{m}$ to $128\ \mu\text{m}$.

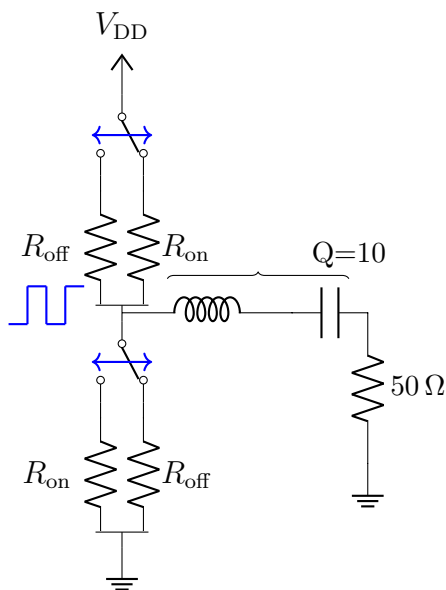


Figure 3.1: Switch model with only resistances included, for conduction loss simulations.

This approach assumes that the loss mechanisms are independent, so that if switching and short-circuit loss mechanisms are added to the circuit this will not change the conduction loss. Additionally, it is a simplification to assume a single R_{on} for the entire on-duration of the switch since the on-resistance will vary. This is especially true during the transition, when the transistor transitions from off-state to

saturation and finally to the linear region, but also since there are slight variations of R_{on} in the linear region also. Still, the assumptions are assumed to yield relatively accurate results.

3.3.2 Switching losses

The switching losses can, once transistor characterization has been made according to section 3.2 and once an average transition frequency f_{av} has been calculated according to (3.1), be estimated with (2.24).

The equation (2.24) is verified in simulation using the switch model of the class D by adding each parasitic capacitance C_{gs} , C_{gd} and C_{ds} separately. This switch model is seen in Figure 3.2. Once a parasitic capacitance is added, an input signal with known f_{av} is used and the η_d and P_L of the circuit obtained. Adding all the parasitic capacitances simultaneously is also a simulation setting, which yields the total switching loss.

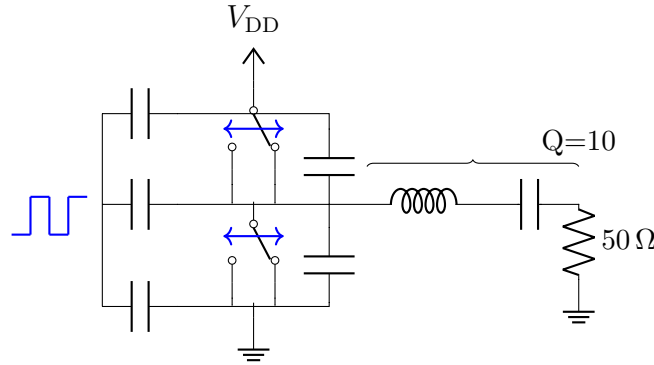


Figure 3.2: Switch model with only parasitic capacitances, to simulate switching losses.

3.3.3 Short-circuit current losses

The short-circuit current loss in a class D stage can be estimated from the static behaviour of an inverter, as in [28], visualized in Figure 3.3. However, that report arrives at a closed form equation by assuming a well-defined threshold voltage V_{th} of the transistors. An exact value for V_{th} is not easily chosen for the SLVT transistors in the 22 nm FDSOI technology though, due to relatively low subthreshold swing.

Instead, one can from the $I_{ds} - V_g$ curves, given a V_{ds} , of the inverter determine the overlap in on-state for the transistors and what current is short-circuited for a given V_g . This is seen in Figure 3.4. Thus, from simulated I_{ds} and V_g one obtains the instantaneous power loss at a given V_g as

$$P_{\text{inst,sc},V_g = V_{g,i}} = |I_{ds}(V_g = V_{g,i})|V_{DD}, V_{g,i} \in [0, V_{DD}] \quad (3.2)$$

Then, assume that the rise of V_g from 0 to V_{DD} occurs over a rise time t_{rise} . Each step in V_g will then correspond to a time step t_{step} . As such, the energy loss in

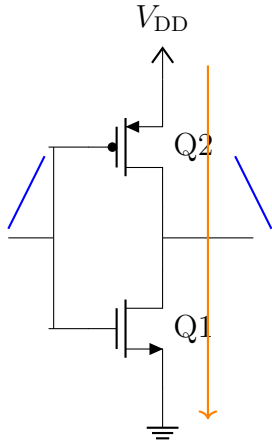


Figure 3.3: Setup for static simulation of inverter short-circuit current loss. Blue lines imply voltage levels, whereas the orange arrow is the short-circuit current.

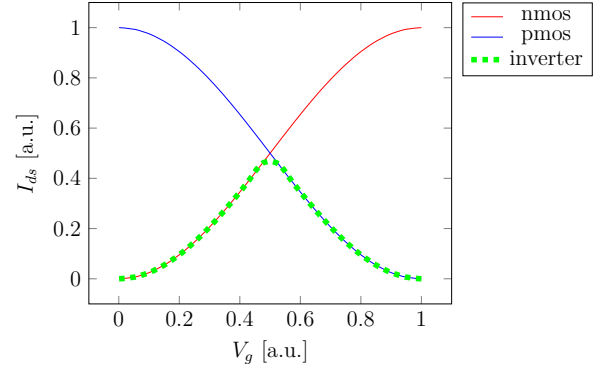


Figure 3.4: Static current behaviour of an inverter. The blue line is the $I_{ds} - V_g$ curve from a pmos device, the red one from an nmos and the green is the inverter short-circuit current.

discrete time interval is

$$E_{\text{inst,sc},i} = P_{\text{inst,sc},V_g = V_{g,i}} t_{\text{step}}, \quad (3.3)$$

and the total energy lost over the full rise time

$$E_{\text{loss,sc,rise}} = \sum_i P_{\text{inst,sc},i} t_{\text{step}}. \quad (3.4)$$

Dividing this by the period time of the carrier T_c gives the average power loss due to short-circuit loss, from rise time. By symmetry, this power loss is equivalent when V_g transitions from V_{DD} to 0. As such, the average short-circuit power loss will be

$$P_{\text{sc,loss,av}} = \frac{E_{\text{loss,sc,rise}}}{T_c} \cdot \frac{f_{\text{av}}}{f_c}, \quad (3.5)$$

where f_{av} is the average transition frequency of the $\Delta\Sigma$ signal. Note that (3.5) increases with t_{rise} via t_{step} . Given that N values for V_g are used to characterize to static behaviour as in Figure 3.4, the sum (3.4) consists of N terms and $t_{\text{step}} = t_{\text{rise}}/N$.

4

Results

In this section, key results will be presented. This includes the $\Delta\Sigma$ coding efficiency for various modulated signals, the results of transistor and loss characterization, and the performance of a class D stage implemented with FDSOI super low voltage threshold transistors.

4.1 $\Delta\Sigma$ coding efficiency for various input signals

The coding efficiency and SNR varies with the input signal peak voltage and Peak-to-Average Power Ratio, as in Figure 4.1 where $R_c = 2$. Here we see that increasing the input amplitude increases SNR and coding efficiency, up to a point of SNR collapse. This SNR collapse can be understood by the fact that the output voltage waveform starts clipping when the input signal amplitude is too high. Additionally, we note that for signals with lower PAPR the coding efficiency is higher. The optimal operating point is slightly below 0 dBV peak input amplitude. Quantitatively speaking, the obtainable coding efficiencies at around 10 % are drastically lower than for a constant sinusoidal tone. This significantly reduces the achievable average output power of the class D PA.

4.2 Switch model simulations

In this section, the simulations performed for the switch model as in Figure 2.10 will be detailed. This includes the determination of circuit element values by transistor characterization and loss characterization.

4.2.1 Transistor characterization

The on-resistances for NMOS and PMOS with varying transistor widths are seen to the right in Figure 4.2, where the $I_{ds} - V_{ds}$ curves to the left indicate the V_{ds} region of validity for this obtained on-resistances. It is seen that the on-resistances are slightly smaller for the NMOS transistors, for a given width, but also that the on-resistances are large enough to be non-negligible in any circuit analysis.

In Figure 4.3, the parasitic capacitances for NMOS and PMOS transistors in their respective on and off-states are seen. Firstly, we note that in general the parasitic capacitances for NMOS and PMOS devices are quite similar but with a number of exceptions. The respective on-state drain-to-source capacitances differ quite much in the on-state. This also applies for the gate-to-drain capacitances both in on

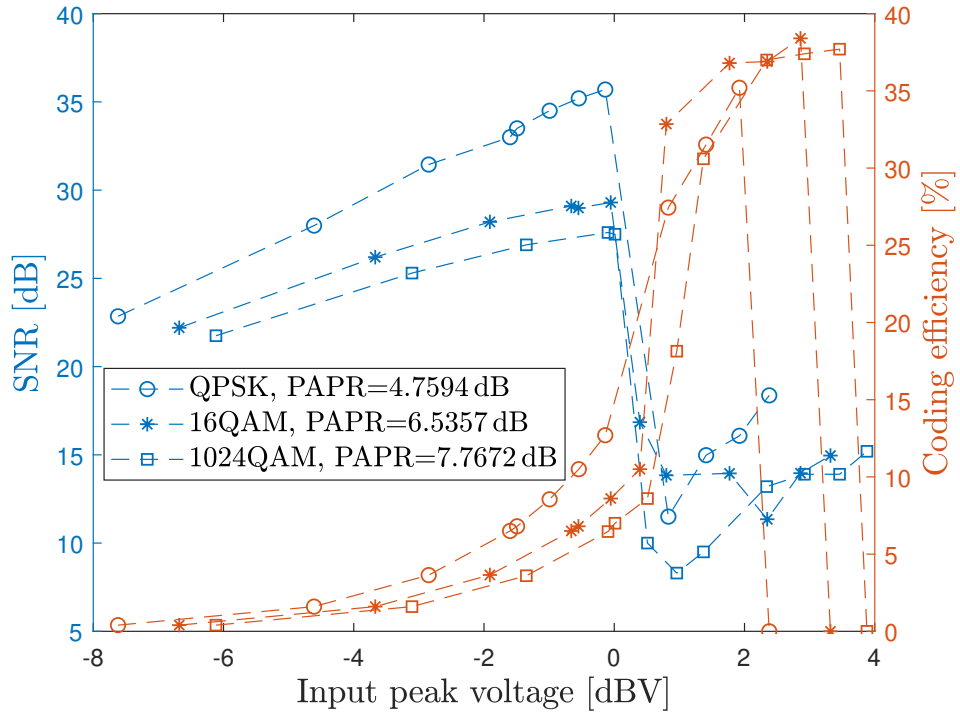


Figure 4.1: SNR and coding efficiency plotted against the peak input signal amplitude. The bandwidth is 30 MHz for each signal.

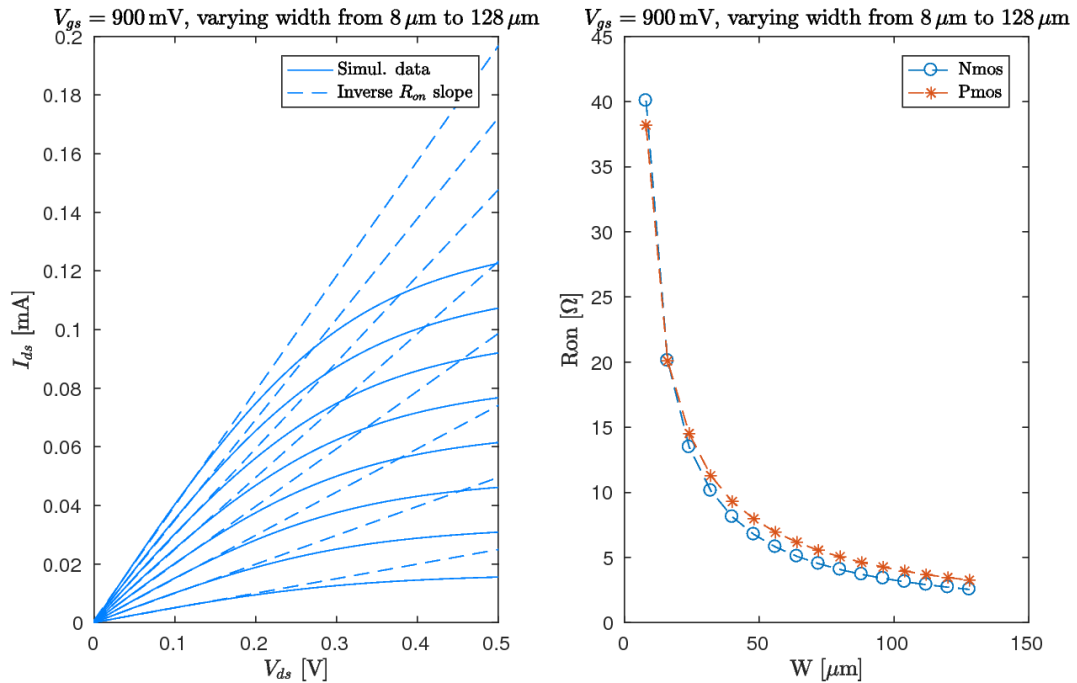


Figure 4.2: On-resistance characterization from $I_{ds} - V_{ds}$ curves along with the obtained on-resistances, for NMOS and PMOS devices with varying widths.

and off-state. Secondly, we note that the parasitic capacitances increase when the devices become larger. Thirdly, the gate capacitances C_{gs} and C_{gd} increase in the on-state relative to the off-state. This agrees with the transistor capacitance model in (2.14) and (2.15). Comparing to these equations, one would obtain the approximate constants

$$\begin{aligned} C_{ov,gs,n} &\approx 0.34 \text{ fF}/\mu\text{m} \\ C_{ov,gd,n} &\approx 0.26 \text{ fF}/\mu\text{m} \\ C_{gcs,n} &\approx 0.59 \text{ fF}/\mu\text{m} \\ C_{gcd,n} &\approx 0.61 \text{ fF}/\mu\text{m}, \end{aligned} \quad (4.1)$$

for the overlap and gate-to-channel capacitances, for the NMOS device, and

$$\begin{aligned} C_{ov,gs,p} &\approx 0.34 \text{ fF}/\mu\text{m} \\ C_{ov,gd,p} &\approx 0.38 \text{ fF}/\mu\text{m} \\ C_{gcs,p} &\approx 0.59 \text{ fF}/\mu\text{m} \\ C_{gcd,p} &\approx 0.61 \text{ fF}/\mu\text{m}, \end{aligned} \quad (4.2)$$

for the PMOS device, for fitting the off and on-state regions.

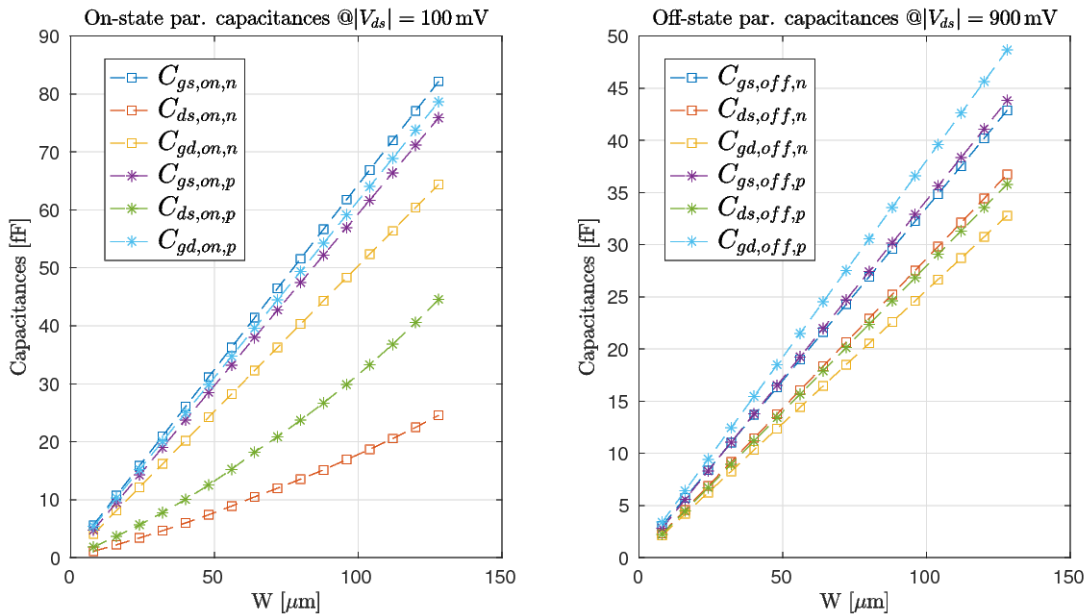


Figure 4.3: Parasitic capacitance characterization for varying transistor widths W .

4.2.2 Loss characterization

In this section, the results of the loss characterizations will be presented.

4.2.2.1 Conduction loss

The conduction loss for varying transistor widths, corresponding to varying on-resistances, is seen in Figure 4.4. In blue, the conduction loss from (2.29) is seen using both simulated η_d and P_L results, whereas in red (2.31) is used with the simulated P_L . In yellow, (2.31) is used with the estimated P_L from (2.20).

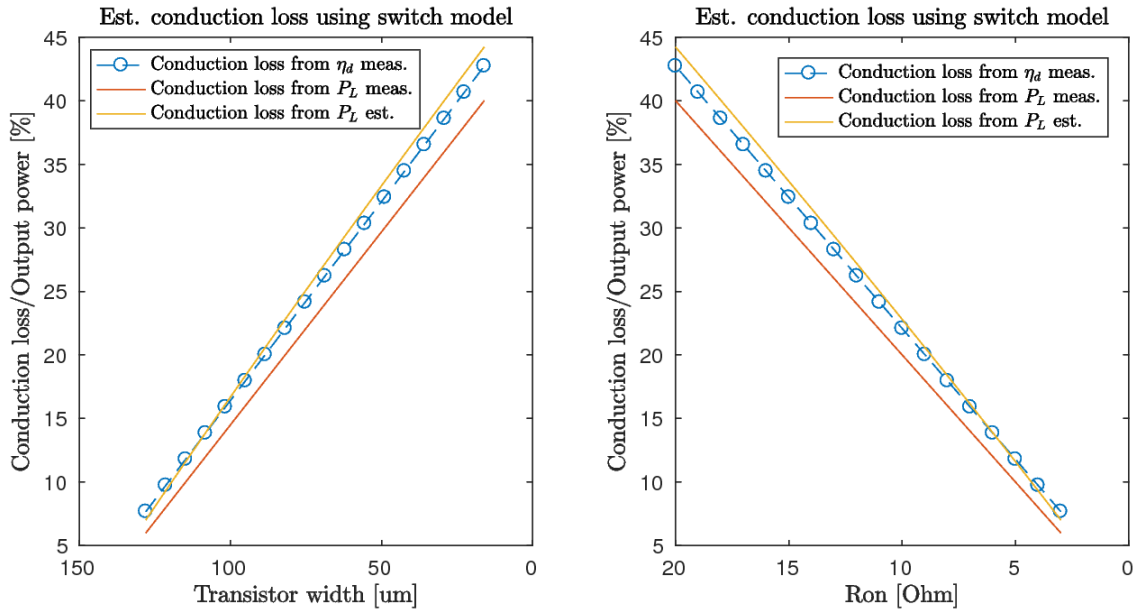


Figure 4.4: Conduction loss normalized to the output power, on the left hand side versus decreasing transistor and on the left hand side versus decreasing on-resistance R_{on} .

4.2.2.2 Switching loss

The switching loss results entails first verifying the switching loss equation (2.24). Then, applying the equation to varying transistor widths (which varies capacitance) and varying switching frequencies, yields an understanding of realistic switching losses.

4.2.2.3 Verifying the switching loss equation

The switching loss for varying magnitudes of parasitic capacitances, corresponding to varying transistor widths, are seen in Figure 4.5 for simulation with a BPDS signal that has $f_{av} \approx 50$ GHz corresponding to $f_s = 4f_c$, $f_c = 25$ GHz. To the left, the simulated η_d is compared to η_d as calculated if the switching losses are given by (2.24), for separately added C_{ds} and C_{gd} in the switch model in Figure 3.2. To the right, the corresponding switching loss is seen. Firstly, we note that (2.24) gives good agreement with simulated data for estimating switching losses in the simplified switch model. Secondly, we note that the switching losses are highly significant at this high frequency. Already for transistor widths of about $28 \mu\text{m}$, the switching loss at the output is equal to the output power. Finally, the impact of C_{gd} is seen. The slope is fourfold relative to C_{gs} and C_{ds} , as expected from (2.23).

4.2.2.4 Varying transistor width and frequency

Varying R_{on} , C_{ds} , C_{gs} and C_{gd} in accordance with the transistor characterization for varying transistor widths in section 4.2.1, we find that the switching losses increase with frequency as in Figure 4.6. Here, $V_{DD} = 900$ mV, $f_s = 4f_c$ and the input signal

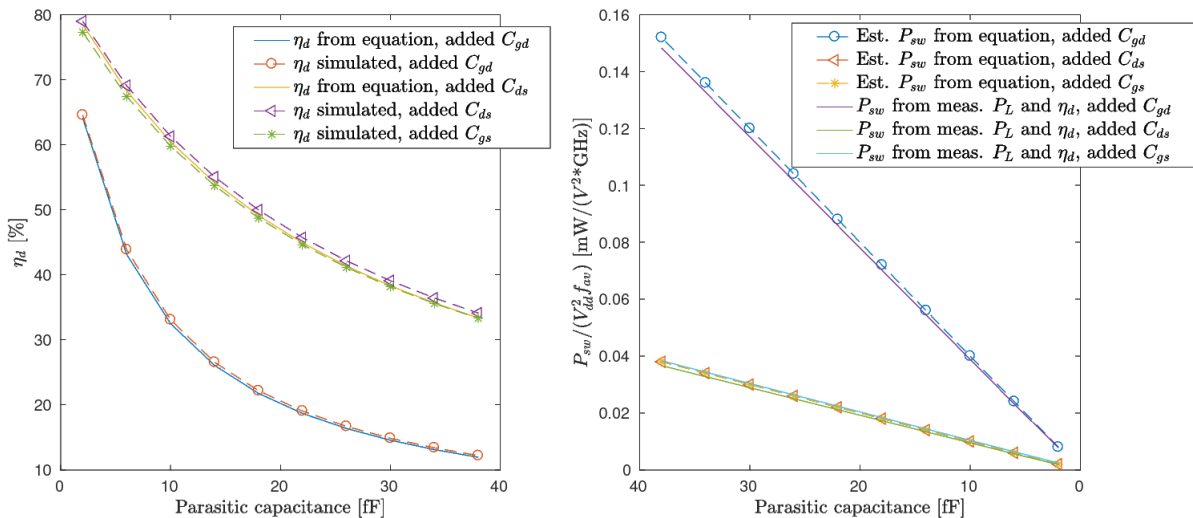


Figure 4.5: Simulated results, using the switch model, of η_d and the switching loss normalised to $V_{DD}^2 f_{av}$ in comparison to theoretical equations (2.24) and (2.28). The input signal is a $\Delta\Sigma$ signal with $f_c = 25$ GHz, $f_s = 100$ GHz, $f_{av} \approx 50$ GHz. Each parasitic capacitance C_{gs} , C_{gd} and C_{ds} is assumed constant, and are evaluated separately, to see their relative impact on the results. In the right figure, it is interesting to note the fourfold times larger slope of C_{gd} compared to C_{gs} , C_{ds} which clearly states the impact of that capacitance.

is a $\Delta\Sigma$ modulated signal of an analog QPSK-modulated signal with bandwidth $BW \approx 0.15f_c$, $PAPR \approx 4.8$ dB, $\eta_c \approx 16\%$ over time $T = 100$ ns.

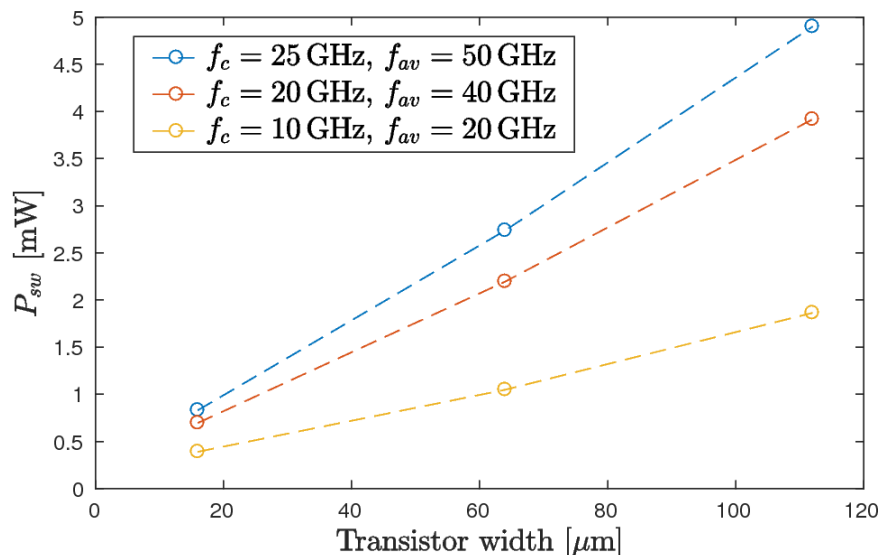


Figure 4.6: Switching loss P_{sw} in mW as a function of varying R_{on} , C_{ds} , C_{gs} and C_{gd} , corresponding to different transistor widths as characterized in section 4.2.1, and varying frequency.

4.2.2.5 Short-circuit loss

The normalized short-circuit power loss, as a function of the transistor width, is seen in Figure 4.7 for varying rise and fall times $t_{\text{rise}} = t_{\text{fall}}$ relative to the sampling period time T_s . It is seen that for larger transistor widths and larger t_{rise} , t_{fall} , the short-circuit losses increase. For more frequent switching (higher f_{av}) the loss also increases.

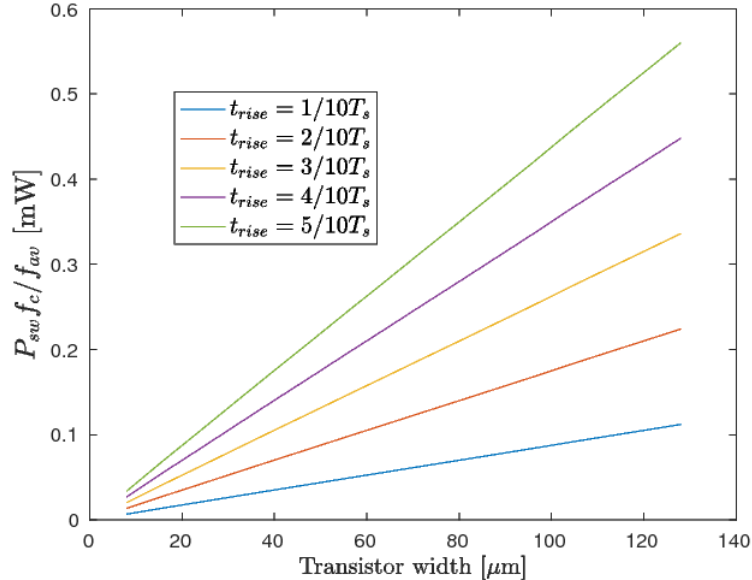


Figure 4.7: Normalized short-circuit power loss as a function of the transistor width, and for varying rise and fall times $t_{\text{rise}} = t_{\text{fall}}$ relative to the sampling period time T_s . The loss is normalized by f_c/f_{av} , i.e. the number of transitions per RF cycle.

4.3 Transistor model simulations

Firstly, a typical output waveform of the transistor simulations using a $\Delta\Sigma$ modulated input signal can be found in Figure 4.8, with loss mechanisms highlighted. Secondly, the output power P_L and drain efficiency η_d for varying transistor widths at $f_c = 25$ GHz and $R_c = 2$, in comparison to the corresponding switch model, are seen in Figure 4.9, for $V_{DD} = 900$ mV and a $\Delta\Sigma$ signal with rise time $1/10 T_s$. The agreement overall is quite well between transistor and simulation results for larger transistor widths, with the most significant error seen for $8 \mu\text{m}$ and $16 \mu\text{m}$ transistor widths. This is discussed in section 5. For the derived theory to hold, the resulting P_L and η_d should be consistent with equations (2.20), (2.24), (2.27), (2.31) and (3.5). For these to be calculated, the parameters $\eta_c = 16.9\%$, $f_{\text{av}} \approx 2f_c$ were given when generating the $\Delta\Sigma$ signal in MATLAB. The resulting values for equating the output power P_L , switching loss P_{sw} , conduction loss P_{cond} and short-circuit current power loss P_{sc} and drain efficiency η_d are seen in Table 4.1. These are obtained from equations (2.20), (2.24), (2.31), (3.5) and (2.27), along with Figure 4.2, Figure 4.4

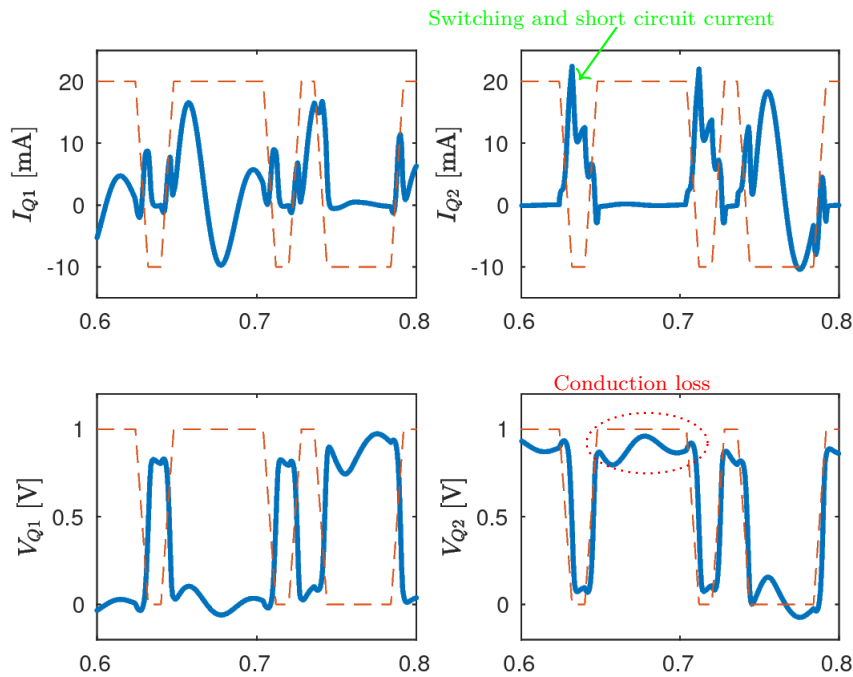


Figure 4.8: Output waveforms of class D stage driven by a $\Delta\Sigma$ modulated signal.

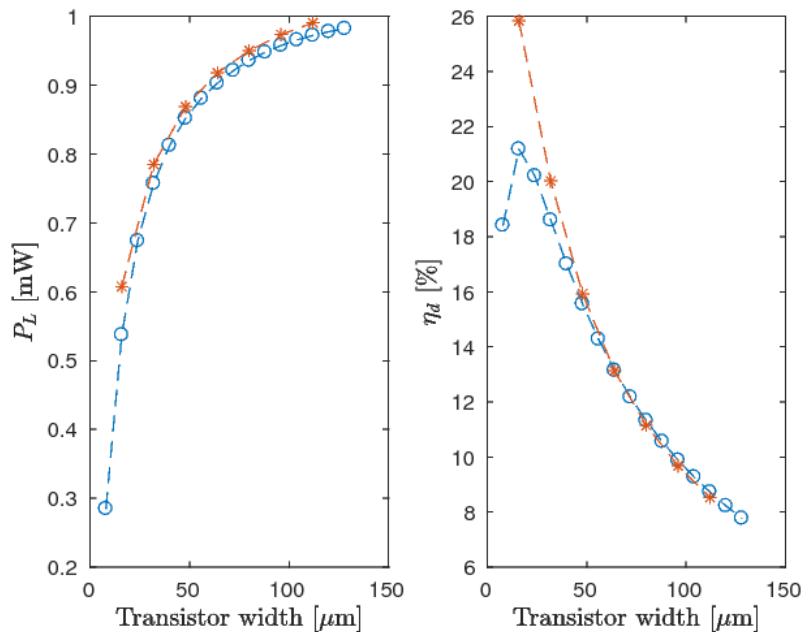


Figure 4.9: Output power P_L and drain efficiency η_d for varying transistor widths and frequencies, in comparison to corresponding switch model, at $f_c = 25$ GHz.

and Figure 4.7. There is mainly a difference in the drain efficiency when comparing the simulated results to the design equations, which is discussed in section 5.

Lastly, the output power and drain efficiency, as a function of both varying frequency and transistor widths, can be found in Figure 4.10. The output power is seen

4. Results

Table 4.1: Resulting P_L and η_d from simulation using SLVT transistors, in comparison to expected results from equations (2.20), (2.24), (2.27), (2.31) and (3.5). The equation for P_L agrees well, but for each width the equations underestimate the losses. A possible cause of error is mentioned in section 5.

W [μm]	8	16	24	32	40	48	56	64	...	112	120	128
P_L theor. [mW]	0.35	0.56	0.67	0.75	0.80	0.83	0.86	0.89		0.96	0.97	0.98
P_L simul. [mW]	0.29	0.54	0.67	0.76	0.81	0.85	0.88	0.90		0.97	0.98	0.98
P_{cond} [mW]	0.27	0.22	0.19	0.16	0.14	0.12	0.11	0.10		0.07	0.06	0.06
P_{sw} [mW]	0.48	0.94	1.4	1.9	2.3	2.8	3.3	3.7		6.7	7.2	7.7
P_{sc} [mW]	0.007	0.014	0.021	0.028	0.035	0.042	0.049	0.056		0.098	0.105	0.112
η_d theor. [%]	31.3	32.3	29.5	26.8	24.3	21.9	20.1	18.5		12.3	11.7	11.1
η_d simul. [%]	18.4	21.2	20.2	18.6	17.0	15.6	14.2	13.1		8.7	8.2	7.8

to be independent of frequency, whereas the losses increase at higher frequencies. Peak drain efficiency is obtained for transistors with width around $20 \mu\text{m}$ for higher frequencies and around $40 \mu\text{m}$ for lower frequencies.

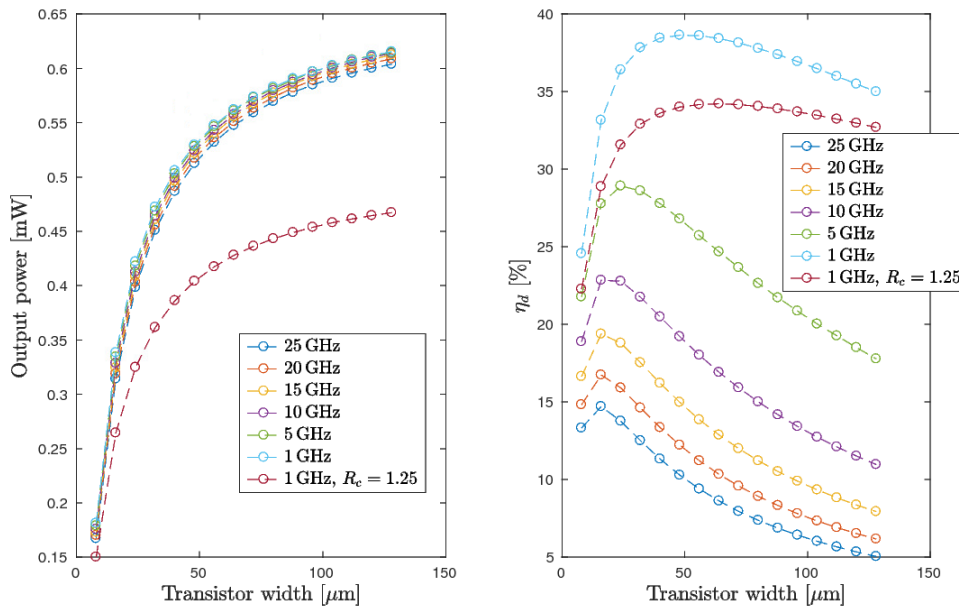


Figure 4.10: Output power P_L and drain efficiency η_d varying with transistor width W and carrier frequency f_c , for a $\Delta\Sigma$ modulated 16 QAM input signal with PAPR of 6.83 dB. An oversampling ratio of $R_c = 2$ is used, except for one measurement series as noted in the legend. For each f_c , the input signal bandwidth in relation to carrier frequency BW/f_c is constant and Q-factor for the filter is always 10. The output power is seen to be constant for varying frequencies therefore, and increasing with the transistor width. Lowering R_c lowers P_L . The drain efficiency is seen to increase when the frequency is lowered, and peak around $W \approx 35 \mu\text{m}$.

5

Discussion

This discussion is divided into two parts. Firstly, a few of the results will be commented on further. Secondly, an attempt to realize a circuit topology that addresses the issue with switching losses will be discussed, along with suggestions on future work.

5.1 Discussion of results

The differences in η_d that was seen in Table 4.1, when comparison between equations and simulation results, is another topic for discussion. The author believes that the cause of error is the observed overshoot voltages at the inverter output node of the class D stage in the simulation, which invalidates the assumptions made in (2.24). The overshoot voltages were observed to peak above 1 V for sharp transitions and undershoot below 100 mV. If considering this as an effective voltage over the capacitors to discharge, the switching losses would be far closer to the simulated results. However, the overshoot effect was a bit too complex to take into consideration, in the given time span remaining, once observed. Further study of e.g. [24] would be necessary. However, overshoot is less likely to occur in a real system since the sharp transitioning pulses used in simulation are less likely to occur in reality. However, simulating with less sharp transitions was difficult when using switch component drivers. Driving the signal directly from a voltage source would remove the discharge path on the input side, whereas drivers with realistic circuit behaviour would make isolation of losses belonging to the main class D stage difficult.

On the same note, the difference in P_L and η_d in Figure 4.9 is worth discussing. The discrepancy of η_d at lower transistor widths could possibly be due to the short-circuit current loss' relative impact. The switch model doesn't include short-circuit current losses, and features no on-state overlap. This effect becomes more visible at lower widths where the switching losses are lower and each loss mechanism contributes more significantly. The discrepancy in P_L might also be due to the switch model not considering the short-circuit current. Both the short-circuit current and the discharge current distorts the output waveforms, which can have an impact on the fundamental tone. This is especially true for slower discharge processes, which occurs when R_{on} is high, since the current spike's frequency content is broadened to lower frequencies (which can include the fundamental frequency).

In Figure 4.10, we see that very low output power is attained. This is largely due to the input signal's high PAPR, which forces the BPDSM to operate at a low coding efficiency. However, for such a high PAPR the drain efficiency is quite acceptable

at lower carrier frequencies. In comparison to e.g. [12] where $\eta_d \approx 50\%$ at 1 GHz for a $\Delta\Sigma$ signal with PAPR of 7.1 dB, the peak $\eta_d \approx 40\%$ is worse but comparable. The cause for obtaining a lower η_d could be partly that the transistor widths were not optimized, and that their work is implemented in a different circuit technology with different parasitic capacitances. In this sweep, the NMOS and PMOS devices were equal always in widths. From Figure 4.2 it can be noted that this results in different on-resistances, for example.

Another matter than can be seen from when $f_c = 1$ GHz in Figure 4.10 is the fact that whilst lowering R_c yields a decrease in switching loss, the corresponding reduction in output power due to R_c lowering η_c still results in a reduction of η_d . However, the steeper slope of η_d when $R_c = 2$ rather than the case $R_c = 1.25$ suggests that if larger transistor widths W were used, then the lower R_c might be better in terms of η_d . These curves will likely have varying curvatures and slopes in other process technologies, and as such a lower R_c might prove beneficial there.

An alternative way to estimate the switching loss (and the short-circuit losses), if (2.24) is assumed invalid but confidence is held in the extracted parasitic capacitances, would be to add a controllable parasitic capacitance C_{load} at the output and then vary it. From this, one can extrapolate to a total capacitance equal to zero to obtain the short-circuit current loss. After that, both the conduction loss and short-circuit current loss can be subtracted from the total loss given for $C_{load} = 0$ to obtain the switching losses. However, this analysis was left undone due to time limitations.

5.2 Future work

It is made clear from this work that voltage mode class D power amplifiers have severe output power and efficiency limitations when implemented in this technology and for $\Delta\Sigma$ modulated signals. The main limiting factor to the drain efficiency is switching losses, whereas the main limiting factors for the output power is the coding efficiency and drain voltage. The coding efficiency and drain voltage limitations are inevitable given the chosen $\Delta\Sigma$ modulation, and might be hard to improve upon. Instead, attempts to address the switching losses were made first. Firstly, the class DE topology [33] as seen in Figure 5.1 was considered as it includes the parasitic capacitances in its design, but with a peak voltage of V_{DD} across drain-to-source of transistor. Unfortunately, the requirements on 25% duty cycle pulse train input with a frequency f_c were incompatible with the aperiodicity of a directly applied $\Delta\Sigma$ coded pulse train. As such, an attempt to parallelize the signal, as in Figure 5.2. Here, given that $f_s = 4f_c$ the requirements for 25% duty cycle and frequency f_s would be fulfilled for each separate class DE stage. This is mathematically possible, because of the linearity of the Fourier transform which ensures that the input signal is equivalent to the added separate drive signals even after filtering and recombination. This was also demonstrated in MATLAB. However, the reconstruction network proved difficult to realise because of the relative phase shift between the signals. Because of load modulation in the recombination when the signals are

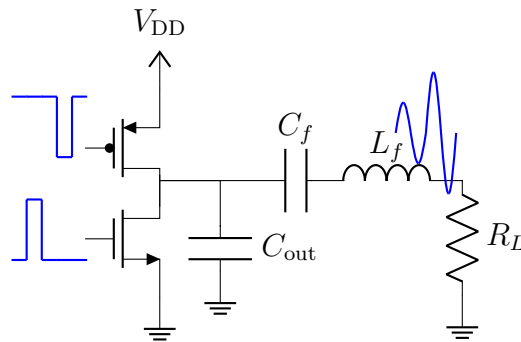


Figure 5.1: Class DE topology.

added together directly (using e.g. Wilkinson combiners), poor efficiency and output power is obtained. At the same time, attempts to adjust the relative phase difference between V_1, \dots, V_4 , would ruin the original signal after reconstruction. The output analog signal would as such have some sort of deterministic, though complex, relation to the input analog signal but exactly how to model that is beyond the author's understanding.

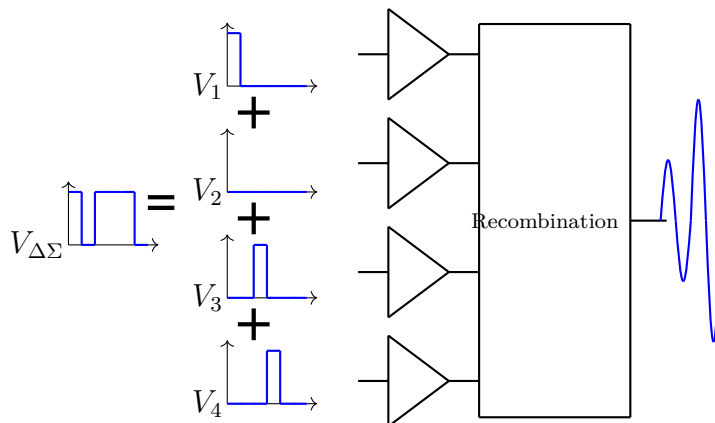


Figure 5.2: Parallelization of input signal, where V_1 to V_4 then proceeds to separately drive a Class DE stage each, followed by some recombination network.

Differential implementation of the voltage mode class D stage is relatively straightforward conceptually, but was omitted in this report due to time constraints. The implementation involves driving one side with the original $\Delta\Sigma$ modulated signal, and the other side with the first signal's inverse. The respective outputs of each class D stage is then recombined using a transformer, which yields the differences of the voltages at each input node. Thus, the expected result when going from a single sided class D stage to a differential one is an increase in the output power, but also an increase in losses, by a factor of about 2.

Though no conclusive bandwidth limitation could be found in this work, bandwidths greater than 150 MHz [34] have not been found in the literature for BPDSM. Therefore, to achieve higher bandwidths (500 MHz) parallel low-pass $\Delta\Sigma$ modulators as in [4] might be preferred.

Current mode class D would be very interesting to investigate, to address the switching losses. With ideal periodic driving, it can achieve zero-voltage switching (meaning that the switch turns on with $V_{ds} = 0$) which would remove switching losses. Even if zero-voltage switching can not be achieved for $\Delta\Sigma$ modulated signals due to aperiodicity, discharging the parasitic capacitances from a lower voltage level than V_{DD} will reduce the switching loss quadratically, as seen from (2.24). The benefit of current mode class D, instead of voltage mode, is mentioned by e.g. [35]. The theory in this report could likely be translated to the current mode class D topology. Alterations to the capacitance expressions and discharge voltage level would have to be made, and no short-circuit current loss will be had.

6

Conclusion

This work concludes that the design equations and simulation results agree quite well with previous work [12] and theory [7][35]. The results show that voltage mode class D power amplifiers are not well suited to high RF BPDSM signals, due to circuit non-idealities. The most dominating non-ideal effect is the switching loss mechanism, wherein the losses increases linearly with both the frequency and transistor width, but also quadratically with the drain voltage. As a consequence of the dominating switching losses, relatively modest transistor widths are required at higher frequencies to limit parasitic capacitances. However, this comes in conflict with the desire to increase output power and reduce conduction losses by increasing the transistor widths. Furthermore, low achievable output power, due to low coding efficiencies and drain voltages, limits the application area to where small output power requirements are had.

The final loss mechanism, short-circuit current loss, was concluded non-negligible for wider transistors, and especially when the rise- and fall times of the pulses are a significant fraction of the total pulse width. This work contributes to future work by providing some additional insight into the modelling of the loss mechanisms, and their impact at higher frequencies.

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Appendix 1

A.1 Derivation for parasitic capacitance extraction from S-parameters

Given a transistor model as in 2.7, we know that

$$Y_{11} = \left. \frac{i_1}{V_1} \right|_{V_2=0}. \quad (\text{A.1})$$

Then,

$$V_1 = i_1 \left(r_g + \frac{\frac{1}{j\omega C_{gs}} \frac{1}{j\omega C_{gd}}}{\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C_{gd}}} \right) = \dots = i_1 \left(r_g + \frac{1}{j\omega C_{gs} + C_{gd}} \right). \quad (\text{A.2})$$

From this (A.1) becomes

$$Y_{11} = \frac{1}{r_g + \frac{1}{j\omega C_{gs} + C_{gd}}} = \dots = \frac{\omega^2 (C_{gs} + C_{gd})^2 r_g + j\omega (C_{gs} + C_{gd})}{1 + r_g \omega^2 (C_{gs} + C_{gd})^2}. \quad (\text{A.3})$$

Thus,

$$\text{Im} \left\{ \frac{Y_{11}}{\omega} \right\} = \frac{(C_{gs} + C_{gd})}{1 + r_g \omega^2 (C_{gs} + C_{gd})^2} \xrightarrow{\omega \rightarrow 0} (C_{gs} + C_{gd}). \quad (\text{A.4})$$

Then,

$$Y_{12} = \left. \frac{i_1}{V_2} \right|_{V_1=0}. \quad (\text{A.5})$$

The transistor model then reduces to a π -net (see e.g. [36]), from which

$$Y_{12} = -j\omega C_{gd}. \quad (\text{A.6})$$

Thirdly,

$$Y_{22} = \left. \frac{i_2}{V_2} \right|_{V_1=0}. \quad (\text{A.7})$$

From the reduced network, it is directly obtained that

$$Y_{\text{out}} = Y_{22} = \frac{1}{Z} + \frac{1}{r_{ds}} + j\omega C_{ds}, \quad (\text{A.8})$$

where

$$Z = \frac{1}{j\omega C_{gd}} + \frac{1}{1/r_g + j\omega C_{gs}}. \quad (\text{A.9})$$

From this,

$$Y_{22} = \frac{j\omega C_{gd} - \omega^2 C_{gs} C_{gd} r_g}{1 + j\omega C_{gs} r_g + j\omega C_{gd} r_g} + \frac{1}{r_g} + j\omega C_{ds}, \quad (\text{A.10})$$

and

$$\text{Im} \left\{ \frac{Y_{22}}{\omega} \right\} \xrightarrow{\omega \rightarrow 0} C_{gd} + C_{ds}. \quad (\text{A.11})$$

With these results we see

$$\begin{aligned} C_{gs} &= \text{Im}\{Y_{11} + Y_{12}\}/\omega \\ C_{gd} &= -\text{Im}\{Y_{12}\}/\omega \\ C_{ds} &= \text{Im}\{Y_{22} + Y_{12}\}/\omega. \end{aligned} \quad (\text{A.12})$$

A.2 Derivation of coding efficiency for sinusoidal tone

Given a sine tone at frequency f_c with amplitude 1, it will have a mean power of $P_{\text{sig}} = (1/\sqrt{2})^2 = 1/2$. If modulated into a binary NRZ $\Delta\Sigma$ pulse train, this pulse train will have a mean power of 1. Since the quantization noise at the fundamental tone f_c of the $\Delta\Sigma$ can be shaped to be zero, the fundamental power in the binary NRZ $\Delta\Sigma$ pulse train will be $1/2$. As such, the coding efficiency $\eta_{\text{DT}} = \frac{1/2}{1} = 0.5$, and given an oversampling rate R_c , and a rise and fall time $T_{r,f}$, η_c is also easily determined. This result is expected to hold approximately for similar input signal, i.e. little amplitude variation from 1 and small bandwidth, and as such could be used as an estimation there.