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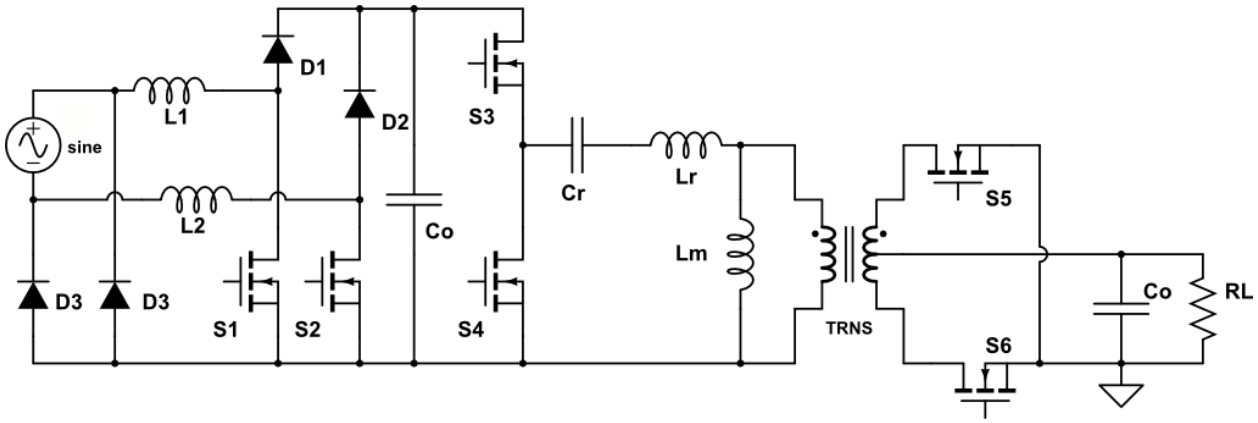

Investigation of optimized topology for AC/DC Power supply unit in telecom industry

Master of Science Thesis

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Department of Energy and Environment
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2019

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A Master of Science thesis in which different AC/DC converter topologies are studied and compared in terms of efficiency, power density and cost.
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Cover: AC/DC converter made of bridgeless PFC and half bridge LLC converters
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Abstract

Nowadays most power electronics converters are becoming more efficient and cost effective, and yet there is always a room left for improvement. This Master thesis deals with AC/DC power supply units in telecom industry which is implemented by a two-stage approach, which includes a power factor correction (PFC) stage followed by an isolated DC/DC stage.

A literature study has been conducted to choose suitable topology candidates for telecom industry for power levels around 500W, 1kW and 2kW. The topology selection has been done considering efficiency, power density and cost. Active boost/-classical boost, interleaved and bridgeless PFC are chosen to be suitable for further studies. Similarly, half bridge, full bridge and interleaved half bridge LLC resonant converters have also been selected for further study. This study indicates that, the bridgeless PFC converter, at 230V input, shows high efficiency across the given power range and has a peak efficiency of 98.5%. The half bridge LLC resonant converter is chosen to be efficient and cost effective for around 500W with a peak efficiency of 97.5%. The full bridge LLC resonant converter is chosen for power levels around 1kW with a peak efficiency of 97.5%. For a power range around 2kW, the interleaved half bridge LLC resonant converter is chosen with a peak efficiency of 97.7%.

The combination of the PFC stage and LLC stage gives the AC/DC power supply unit (PSU). With the selected topology combinations, this converter can achieve a peak efficiency of 96.0%, 95.9% and 95.6% around 500W, 1kW and 2kW respectively.

Keywords: PFC, LLC, PSU, LLC, Resounant converters

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Contents

1
Introduction

1.1 Background

Power supply units (PSU) are used almost in every application that uses electrical power as a primary source. In most of the applications, the contribution of the PSU is very important in energy savings, thus saving money. One of the major areas that involves the use of an AC/DC power supply units is telecom industry.

The 5G network, the Fifth-generation wireless network, is the latest technology in telecom industry which will increase the data transfer and responsiveness of wireless networks. Advanced Antenna System (AAS) and Antenna Integrated Radio (AIR) unit are important products of 5G. To achieve higher system integration, higher power density and higher efficiency are required for the power supplies of AAS and AIR products, and such requirements bring more challenges to the design of the AC/DC PSU used in telecom industry.

The AC/DC PSU in telecom industry is usually implemented by a two-stage approach, which includes a power factor correction (PFC) stage followed by an isolated DC-DC stage [1]. To improve the PSU's efficiency and power density, the switching frequency of both stages shall be pushed to higher frequency regions, then the selection of the most optimized topology becomes one of the critical issues that should be investigated for an AC/DC PSU design.

1.2 Aim

The aim of this thesis work is to investigate the most optimized topologies for AC/DC power supply units with different power levels, for example below 500W, around 1kW and 2kW by considering efficiency, power density and cost.

1.3 Delimitations

Theoretical and simulation models shall be investigated for selected AC/DC converter topologies based on previous work and literature review for different power rating. Analysis will be made based on efficiency, power densities and cost and the optimized converter topology will be selected for different power levels. As a constraint the following limitations are set:

- This masters thesis does not include hardware design of the selected topologies.

- The topologies are going to be simulated in open loop control since the design of closed loop control is out of scope.

- For the DC/DC stage only LLC converters of different topologies will be studied and other DC/DC converter topologies are excluded.

1.4 Problem description

Due to high frequency operation of 5G antennas in telecom industry the operation ranges of this antennas might be limited to short distance ranges. Due to easy availability of AC grid and unavailability of DC supply voltage in the streets, an optimized topology of AC/DC converters should be investigated in terms of their efficiency, cost and power density. Based on literature studies, key topologies will be selected and further investigation. The efficiency curves and power losses shall be calculated and verified via simulation to find the most optimized topology.

1.5 Environmental and ethical aspects

This thesis work deals with optimized topology of AC/DC converters which deals, mostly, with efficiency of the converters. The use of optimized converters in terms of efficiency saves energy and money in the long run. The way electricity is consumed also affects the environment. The power consumption consumed by one converter might be very low, but with the presence of millions of these converters connected to the grid will have a huge impact on the grid and consequently on the environment one way or another.

In US, studies indicate that about half of the electricity generated will be processed by some kind of electronics device and in case of extreme power quality failure, the cumulative effect can lead to power outage as in 2003 in New York[2]. To decrease the effect of low power quality, standard like IEEE 519 and IEC 1000-3-2 should be considered and the converters should meet the EMC certifications. Another perspective is to understand and to minimize the environmental impact based on how the raw materials are extracted for the specific topology design and different choices or designs should be considered which affects the environment less.

Many developed countries have a long term commitment fighting global warming and reduce carbon impact. For example, in Britain in 2014, BT Group plc (trading as BT and formerly British Telecom) developed a rectifier replacement program in the UK network, a trial of Huawei's super high efficiency rectifier within a BT operational site is to be implemented. The efficiency of the new front end rectifiers were 98% which replaces the old ones with efficiency 96%[3]. The study indicates that, in 5 years investment view, the rectifiers with efficiency of 96% has a return on investment of 55 weeks whereas the rectifiers with 98% efficiency has a return on

investment of 52 weeks. Furthermore, the study indicates that cumulative savings over 5 year's use of 98% efficiency rectifiers achieves £9M more savings than using 96% efficiency rectifiers. This shows efficient power converters have a great impact on environment and have a huge operational benefit.

2

Theory

2.1 Background on AC/DC converters

Alternating current (AC) supply is a very efficient way of transferring electrical power and since most of electronic devices work in direct current (DC) power supply, the AC source should be converted to DC. The easiest way of converting AC to DC is to use four diodes as in bridge rectifier and connecting a capacitor as filter as shown in Figure 2.2. But this kind of rectifiers does not meet harmonics standards like IEC6000-3-2[4] and have low efficiency. Furthermore, there is no way of controlling the current in the rectifier. These drawbacks and limitations give rise the development of high efficiency AC/DC converters.

Nowadays, two stage approach of AC/DC converters are implemented in telecom industry with a basic layout as shown in Figure 2.1. The EMI filter, usually made of passive components, reduces high frequency noises and helps only the fundamental component of the AC current passes through the converter. The PFC block shapes the input current in such a way that it has the same waveform as the rectified AC voltage and help the converter have a power factor close to 1.

The DC/DC converter changes the DC output of the PFC converter and changes to a regulated and required voltage level. This stage can be implemented with switch mode power supply or with resonance converters. Resonant converters provide high efficiency operations since the switch in the converter works in zero voltage and zero current switching, which reduces the switching loss of the switch. To have a high power density and efficiency of the DC/DC stage different resonant converter topologies are available as it will be explained more in the coming sections. The efficiency and performance of the AC/DC converter is then determined by the combined efficiency and performance of the PFC and LLC stages.

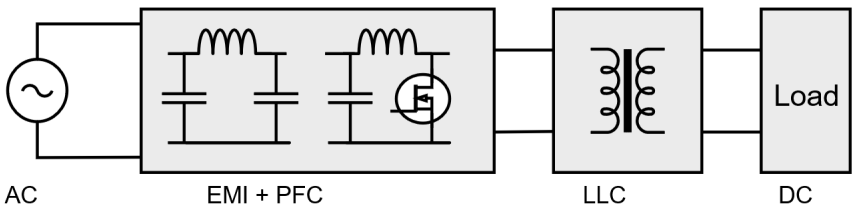


Figure 2.1: General layout of AC/DC converters

2.2 Overview on active PFC topologies

As it has been introduced in the previous section, the AC/DC power conversion usually implemented in two power stages. The first stage consists of a power factor correction stage and the second stage being a DC/DC converter. The classical AC/DC conversion circuit uses four diodes as in a bridge rectifier configuration to rectify the sinusoidal AC voltage and a capacitor connected to the output to filter out the voltage ripple as shown in Figure 2.2.

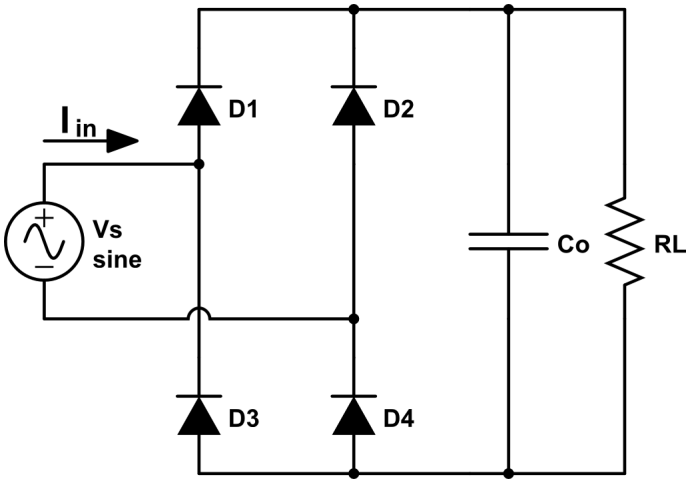


Figure 2.2: Bridge rectifier circuit

The current from the supply flows to the output only when the capacitor voltage is less than the input voltage. Consequently, the current consumed is not sinusoidal and is rather distorted as shown in Figure 2.3. The power factor of this type of converter is usually around 0.7 [5], which greatly affects the power quality and does not meet industry standards.

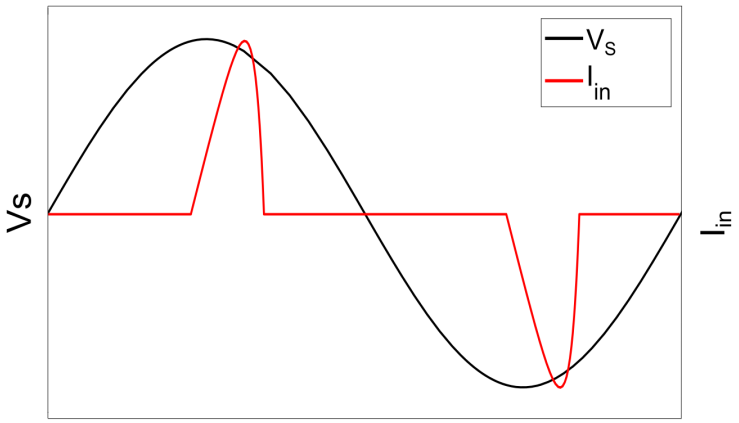


Figure 2.3: Voltage and input current of bridge rectifier circuit

In order to reduce the total harmonic distortion (THD) of the input current and to improve its power factor, power factor corrector (PFC) circuits are implemented.

Passive versus active
PFCs broadly classified as passive and active PFC controllers. Passive PFC controllers use passive devices like inductors to shape the current waveform and do not use any control mechanism whereas active PFC controllers use different control mechanisms to shape the current input. Usually passive PFCs are not implemented if the power level is higher than 400W because of their bulky size, high cost and poor performance [6].

Active PFC converters provide a much better power factor of the current and they can be implemented in so many different typologies. Many of the topology implementations depend on the type application such as input/output voltage requirements. One way of classifying PFC converters is by the use of diode rectifier bridge as a means of changing the AC/ voltage to DC voltage waveform and control the input current. The most commonly used PFC topology of these kind is the active boost PFC converter, whereas PFCs based on flyback converter, SEPIC converter and CUK converter can also be implemented as PFC depending on the application[7]. The use of diode bridge rectifier increases the conduction losses in the PFC and creates a thermal stress in the bridge and usually requires a heat sink.

Bridgeless
The used of bridge circuit brings issues with power loss and thermal management. PFC converters that does not need bridge rectifier are known as bridgeless PFC converters. These converter typologies have higher efficiency as compared with the previous group of PFC topologies. Basic bridgeless PFC, Semi bridgeless PFC and back to back bridgeless PFC can lie into this category[8]. As stated in [8], most of these type of topologies experience a higher level of electro-magnetic interference (EMI) issues because of their topology. Different modifications and types of bridgeless topologies are implemented to decrease this EMI issues and semi-bridgeless PFC is one of those.

Interleaved
Another group of PFC can be classified as interleaved PFCs. Interleaving means channeling the power flow from the input to the output into two or more separate paths and add them at the output point. By doing this, the current ripple on both at the input and at the output of the converter is reduced. As the number of interleaved branches increase the power rating also increases. Another advantage of this approach is better thermal performance as it uses two inductors which are half the size of the basic active boost PFC as will be explained later. The use of two inductors can increase the thermal performance of the converter as well.

Wide band-gap switches: SiC and GaN
The bottleneck with increasing the switching frequency to decrease the size of passive devices is that it increases the switching losses of the MOSFETs significantly. The development of new types of switches such as gallium nitride (GaN) and Silicon carbide (SiC) switches, lead the PFC converter to different types of topology known as the totem pole PFC. In wide gap switch, because of the absence reverse recovery charges (Q_{rr}), the switching losses significantly reduces and the switching frequency

can be pushed to a higher level resulting small converter size and increased power density[9].

Table 2.1 shows some of the PFC topologies that have high efficiency. The table does not include all the PFC topologies but summarizes the most common PFC topology implementations with their reference document.

Table 2.1: High Efficiency PFC converters

No	Topology	Feature	Power (W)	Peak Efficiency (%)	Ref.
1	Buck	High gain	500	98.5	[10]
		Cascaded	2000	97	[11]
2	SEPIC	Uses SiC MOSFETs	1000	95.3	[12]
3	Cuk	Synchronous rectifier	150	95	[13]
4	Active boost	Soft switching	500	97	[14]
		Interleaved	700	98.4	[15]
5	Bridgeless active boost	Phase shifted	1000	98.6	[16]
		Three level; Interleaved	3000	98.6	[17]
		Dual-boost	3200	99.33	[18]
6	Totem pole	Uses MOSFETs	1600	98.05	[19]
		Uses SiC MOSFETs	2000	98.5	[20]
		Uses GaN	3000	99.1	[9]

2.3 Active PFC converters and their mode of conduction

As it has been mentioned earlier, the main goal of this PFC converter is to charge and discharge the inductor by controlling the switch to control the average current flowing through the inductor, i.e. input current, have the same shape as the rectified voltage waveform. The mode of conduction in PFC converters refers to state or value of the current in the boost inductor. In continues conduction mode (CCM) the current in the inductor will not reach zero in one switching period. which implies that the difference between the RMS and peak currents through the inductor are minimum which makes this mode of conduction popular at higher power levels. Furthermore, the EMI filter design is simplified since the input current through the PFC is always continues. In this conduction mode, hard switching takes place which apparently increase the losses in switch and diode as will be explained in the following sections. Figure 2.4 show the waveforms in CCM where V_{rect} is the rectified voltage, I_L is instantaneous inductor current and I_{avg} is the average current of inductor.

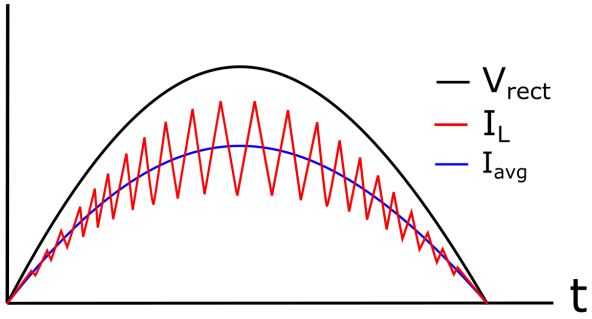


Figure 2.4: PFC waveforms in continues conduction mode

The second conduction mode, critical or boundary conduction mode (BCM), is a type of conduction in which the next switching cycle starts when the inductor current reaches zero as shown in Figure 2.5. One advantage of this conduction mode is that the reverse recovery loss of the boost diode is almost negligible and the turn on losses in the switch will be zero since the current reaches zero prior to turning on the MOSFET. Although this conduction mode provides soft switching while turning on the MOSFET, it exposes the switch, the diode and the inductor to high current stress. Another disadvantage of this mode of conduction comes when designing EMI filter. For example to keep the same size of EMI filter in DCM mode, which operates in CCM with a switching frequency in kHz range, is to push the switching frequency in range of MHz, apparently, this results in large switching losses[21].

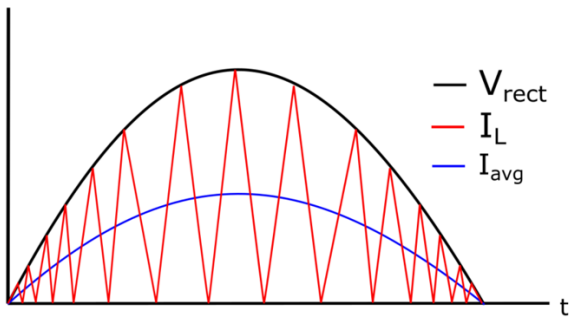


Figure 2.5: PFC waveforms in boundary conduction mode

Discontinues conduction mode (DCM) is when the current through the inductor is discontinues. While implementing DCM, using one control loop is enough to assure good power factor while maintaining constant output power. Because of the reason that the MOSFET, the inductor and the boost diode stress and problems with conducted emission, the use of converters operating in DCM is limited to low power range, i.e $<$ 250W[22]. The waveforms in DCM are shown in Figure 2.6.

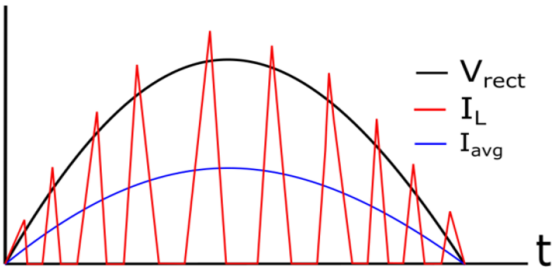


Figure 2.6: PFC waveforms in discontinues conduction mode

2.3.1 Active boost PFC

Active boost PFC converter uses a diode bridge to rectify the AC voltage to pulsating DC and then use an active boost DC to DC converter to control the input current i.e. controlling the power factor. The active boost PFC topology is the most used topology because of its simple power circuit and easy control of the input inductor current so that the current will have the same waveform of the rectified ac voltage [23]. This topology is also a basic topology as most of other PFC converters are derived from this topology.

Active boost PFC converter is an ideal PFC controller especially if the voltage at the output is required to be higher than the input and if another DC/DC stage is connected to the PFC output. This is because the PFC stage will act as a pre-voltage regulator for the DC/DC stage. There are different ways of controlling the input current in the boost configuration by controlling the switch shown in Figure 2.7. Average current control mode, hysteresis current control mode and peak current control mode are ways of controlling the current in the inductor but average current control mode is commonly used one because of the simplicity[6].

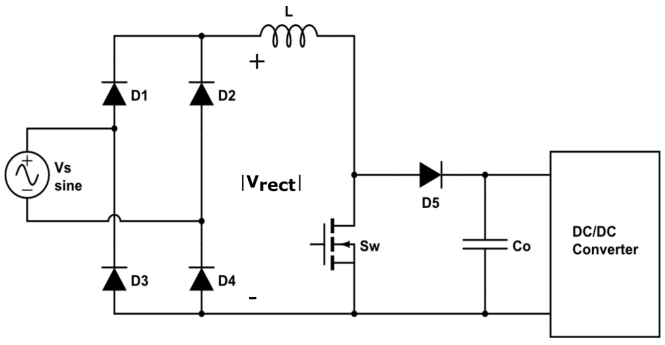
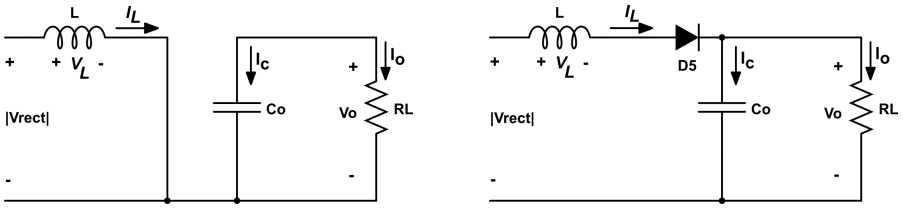


Figure 2.7: Boost PFC circuit

The main operation of an active boost PFC is the same as a DC/DC boost converter. The difference is that the input for the PFC is a pulsating DC voltage. In some PFC designs, an input capacitor is connected after the bridge rectifier to decrease the current ripple in the boost inductor. This will help in reducing the physical size

of the inductor. Figure 2.8 shows the current paths when the switch, *Sw*, closes and opens. In Figure 2.8a, the current from V_{in} will charge up the inductor and the charge stored in the capacitor makes the current flow to the load. In Figure 2.8b the current stored in the inductor starts to flow to the output capacitor and charges it.



(a) Turn on **(b)** turn off

Figure 2.8: The current paths when the switch turns on and turns off

From the fact that the average inductor voltage over one time period is zero, if CCM is considered, applying KVL in Figure 2.8a when the switch is on, and Figure 2.8b when the switch is off, we get

$$V_{rect}t_{on} + (V_{rect} - V_o)t_{off} = 0 \tag{2.1}$$

where t_{on} is the on time period for the switch and t_{off} is the off time period for the switch. Rearranging (2.1), the ratio between V_{in} and V_o can be found as follows

$$\frac{V_o}{|V_{rect}|} = \frac{1}{1-d} \tag{2.2}$$

where d is the duty cycle and and V_{rect} is the rectified voltage. Based on the equations derived above, the average model of the active boost PFC can be drawn as shown in Figure 2.9.

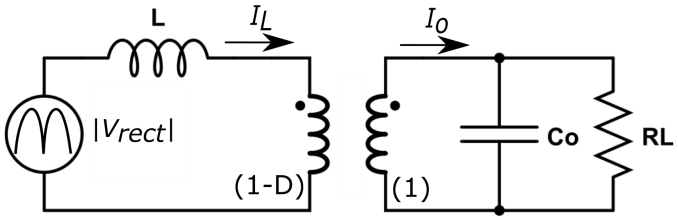


Figure 2.9: Average model of active boost PFC in CCM

In CCM, the boost diode, *D5*, in Figure 2.7, turns off by interrupting the current flowing through it which causes reverse recovery losses in the diode. This phenomena also imposes higher turn on losses in the switch, *Sw*. Furthermore, this topology requires good EMI filter since the current ripple in the inductor is the same as the input current ripple. This topology is usually used for power range of less than 1kW.

2.3.2 Interleaved boost PFC

Interleaving approach is used to channel the current flowing path into two or more phases so that the output current is the sum of each individual phases. Figure 2.10 shows single phase two leg interleaved PFC topology. The two switches, *Sw1* and *Sw2*, operates 180° out of phase. The input current will flow in both inductors, *L1* and L_2, and the total current will be the sum of the currents passing through the two inductors.

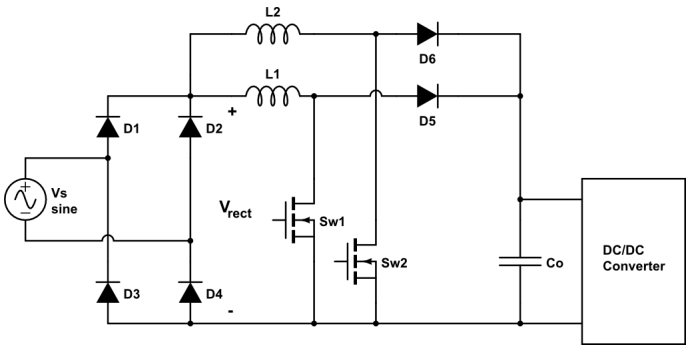


Figure 2.10: Interleaved PFC converter

The operational principles of an interleaved boost PFC is exactly the same as the active boost PFC and for one leg, for example for inductor, *L1*, and switch *Sw1*, Figure 2.8 can be used to see the current flowing paths. Since this topology uses two inductors, L1 and L2, each with half size of the boost PFC, the thermal performance of the converter will improve. The efficiency of this converter is also higher as compared with the active boost PFC since the power is channeled through two paths which decreases the conduction losses of the inductor, the boost diode and the MOSFET by half. Furthermore, the stress across the switches reduces. Interleaved operation is usually preferred over the active boost PFC if the power level is higher than 1kW.

The inductor current ripple in active boost PFC is the same as the input current ripple while in the interleaving approach, the ratio of the supply ripple current to inductor's ripple current can vary depending on the duty cycle. Current ripple cancellation both in the input and output side of interleaved PFC is considered as the major advantage over the active boost PFC. The ripple in the input current, Δi_{in}, can be written as (2.3) for duty cycle greater than 0.5 and less than 0.5[24].

$$\Delta i_{in} = \begin{cases} \Delta i_L \frac{1-2D}{1-D}, for D \leq 0.5 \\ \\ \Delta i_L \frac{2D-1}{D}, for D \geq 0.5 \end{cases} \tag{2.3}$$

Figure 2.11 show how the ripple current cancels in the two legs as a function of duty cycle. Consequently, the size of the EMI filter reduces as a result of ripple current cancellation.

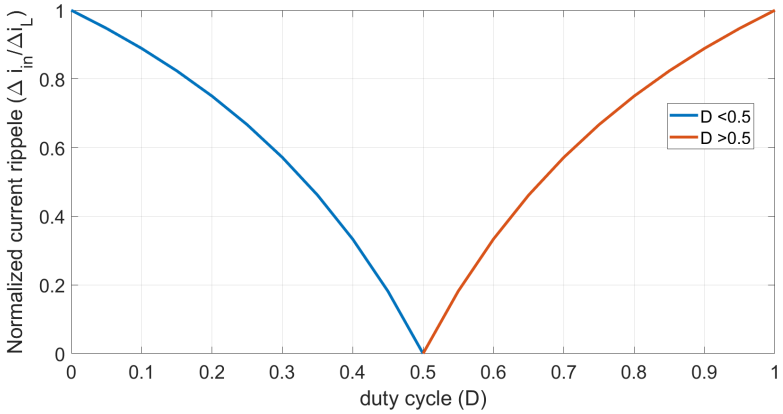


Figure 2.11: Inductor ripple current cancellation

2.3.3 Bridgeless boost PFC

In the bridgeless PFC, the diode bridge used to rectify the AC input voltage is not needed. The bridgeless PFC discussed in [16], which is the same as the one shown in Figure 2.12 without diode *D3* and *D4*, has a major disadvantage of high EMI due to a switch voltage changing from negative to positive values which is usually not recommended for telecom applications. The solution is to use two diodes *D3* and *D4* as a current return path and connects the input neutral to the output neutral as shown in Figure 2.12. Due to these diodes, and because of the presence of two boost inductors this topology is also known as the semi-bridgeless PFC or dual-boost semi-bridgeless PFC. Consequently, this topology can achieve higher efficiency as it reduces the number of components in the current flowing path. In addition to high efficiency, this topology also has high power density and better heat spot distribution and this provides less cooling effort[25].

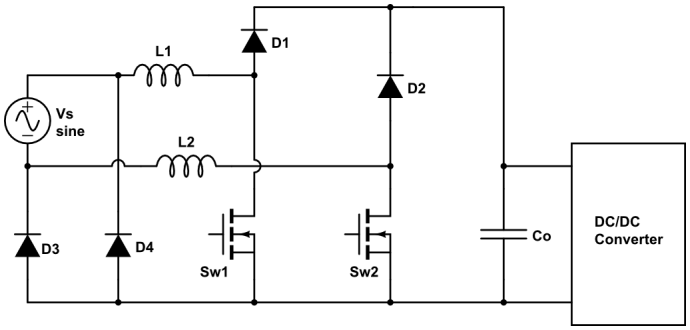


Figure 2.12: Bridgeless PFC

The operation principles of the bridgeless PFC for the positive AC cycle and negative AC cycle are symmetrical, thus only the positive half cycle is discussed here. The classification for positive and negative AC cycles comes from the absence of the bridge rectifier.

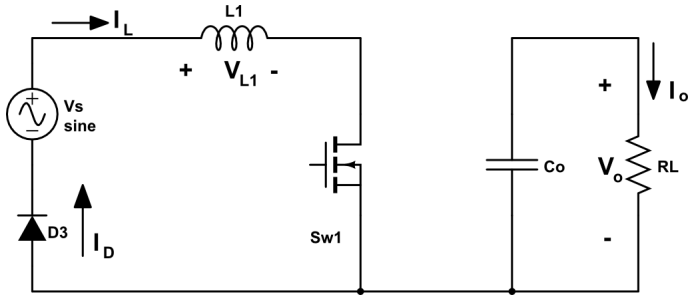


Figure 2.13: For positive AC cycle and SW1 is on and SW2 is off

When the switch, *Sw1*, is conducting, the inductor, *L1*, will charge up and the return current flows back to the source through *D3*. The return current also uses the body diode of the second switch, *Sw2*, although it can be ignored when explaining the working principle of this PFC. Since the flow of the reverse current through these two separate channels, through one diode and body diode of one of the MOSFETs, will reduce the losses in the diode and increase the MOSFET losses. The current flows through the body diode just because of the circuit configuration. Meanwhile, the voltage stored in the output capacitor flows to the load. During this interval the voltage across inductor *L1* can be expressed as

$$V_{L1} = L\frac{di_{L1}}{dt} = V_s \tag{2.4}$$

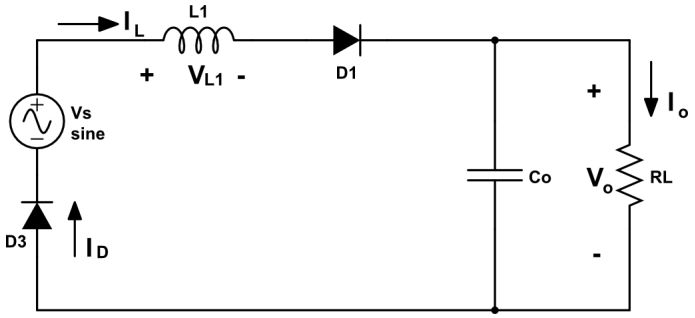


Figure 2.14: For positive AC cycle and both switches are off

When the switch, *Sw1*, is open then the energy stored in the inductor flows to the load as shown in Figure 2.14. Which basically results in the same operating phenomenon as the active boost PFC. For the negative AC cycle the same operation continues for the second inductor, *L2*.

2.4 Losses and component sizing of PFC stage

The sizing of components in the PFC depends on different parameters like maximum power output, maximum voltage and current capabilities of the converter. The efficiency of the AC/DC converters directly related to the losses in the components that build up the converter. All the three topologies contain diode bridge rectifier (also known as slow diodes in bridgless PFC), inductor, MOSFETs, boost diode

and output capacitor. The sizing of each device and the losses associated with each component will be in this section.

2.4.1 Diode bridge

The diode bridge in active boost and interleaved PFC stages are used to rectify the AC voltage in to a pulsating DC waveform so that it is easier to shape the current through an inductor have the same waveform as the rectified DC. The maximum break down voltage or reverse voltage of the diode rectifier should be at least equal to the output voltage of the boost PFC circuit. If, for example, the output voltage of the PFC is 400V, then the reveres voltage capability should be 450V or 500V so that the bridge rectifier can perform better with less voltage stress. Another criterion choosing the bridge rectifier is that it should have a low voltage drop and low forward resistance as much as possible so that the losses would be minimized.

Diode losses can be classified into conduction losses, which comes from the resistive part of the diode while its conducting, and turn off loss which is caused by the reverse recovery of the diode. Figure 2.15 show a representation of a power loss in a diode due to its forward resistance, R_f and due to its forward voltage drop V_f.

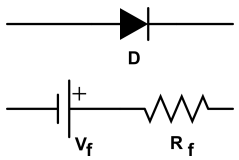


Figure 2.15: Representation of a diode

The turn off losses of diode or reverse recovery losses are caused by the release of charges when the diode goes from conducting state to blocking state. For grid connected bridge rectifiers, where the mains frequency is 50 or 60 Hz, the reverse recovery losses are usually ignored as the switching takes place naturally and the current through the diode is zero while switching, and during forward biased the typical voltage drop, V_f, is 0.8V. The power loss of the diode can be given by (3.2.1) as a function of temperature where I_{av} and I_{rms} are the average input current and RMS value of the current passing through the diode when it is forward biased.

$$P_{diode,c} = V_f(T)I_{av} + R_f(T)I_{rms}^2 \tag{2.5}$$

The diode parameters, V_f and R_f, can be found from the diode specification or datasheet.

For bridgeless PFC, the losses due to the slow diodes can also be calculated using (2.5) but the average current passing through the diode changes as nearly half of the current will return back through the body diodes of the MOSFET. This further will be explained in the next chapter.

2.4.2 Boost Inductor

The inductor in any PFC topology is the most important circuit component because of the reason that the current in the inductor will neither go to zero nor will reach rated value instantaneously, so its evident that it is possible to shape the current passing through it. The size of the inductor, apart from the RMS current through it, can be determined from the ripple current that is allowed to pass through it. Usually the ripple current can be given as the percentage of the maximum input current. For all the three topologies discussed above, the inductor size can be determined as follows. From (2.1), when switch *Sw* is off, the inductor voltage can be, respectively expressed as

$$V_L = (V_{rect} - V_o)t_{off} \tag{2.6}$$

Equation (2.6) holds true for both active boost and interleaved PFC topologies. For bridgeless topology, the rectified voltage, V_{rect}, should be replaced with the supply voltage, V_s. (2.6) can also be expressed as

$$V_L = L\frac{di_L}{dt} = (V_{rect} - V_o)t_{off} \tag{2.7}$$

During turn off, the inductor voltage is decreasing which mean V_L will have a negative value. Replacing the off period by *(1-d)/fs*, where *fs* is switching frequency and rearranging (2.7) gives

$$L = (V_o - V_{rect})\frac{(1-d)}{\Delta i_L fs} \tag{2.8}$$

Equation (2.8) can be used to determine the size of the inductor. Furthermore, in [26], the maximum ripple current is experienced in the inductor when the input voltage is at its peak. Then, for active boost and interleaved PFC topologies, (2.8) can be written as

$$L = (V_o - \sqrt{2}V_{rect})\frac{(1-d)}{\Delta i_L fs} \tag{2.9}$$

where Δi_L is the ripple current in the inductor and it can be given by the following equation where η is the efficiency of the PFC, % ripple is the ripple current in the inductor in percentage

$$\Delta i_L = \frac{P_o}{\eta V_{rect,min}}\%ripple \tag{2.10}$$

by combining (2.9) and (2.10), for active boost and interleaved PFC, the minimum inductor size can be given as

$$L = \frac{1}{\%ripple}\frac{1}{\eta}\frac{V_{rect,min}^2}{P_o\, fs}(1 - \frac{\sqrt{2}V_{rect,min}}{V_o}) \tag{2.11}$$

and for bridgeless PFC, the minimum inductor size can be expressed as

$$L = \frac{1}{\%ripple}\frac{1}{\eta}\frac{V_{s,min}^2}{P_o\, fs}(1 - \frac{\sqrt{2}V_{s,min}}{V_o}) \tag{2.12}$$

In practice, the size of the inductance value for the PFC stage is slightly higher than the one calculated using (2.12).

Inductor core selection
Power inductors require a core and air gap within the core structure to increase the energy stored in the inductor and preventing the core from saturation. The core should be chosen in such a way that it should have less volume and less core loss.

The air gap in the core can be distributed all over the core as in powdered cores or it can be discrete as in ferrite cores. In powdered core the air gap is distributed in the core since the core is made of different materials powdered together as an alloy. One advantage of powdered core is that it decreases fringing loss. This loss is due to the scattering of magnetic flux lines out of the core path and is emitted into the air. Ferrite cores uses discrete air gap in the core structure which leads to low AC core loss at high frequency but are expensive as compared with powdered cores[27].

Inductor wire selection
The inductor wire will form a turn around the core and is selected based on the maximum current. It should meet the requirements that one it should be thick so that the resistance is small and two its should be possible to form the required number of turns around the core.

Inductor losses
Inductor losses can be divided into core losses and copper losses. The core loss in an inductor can be found from the following Steinmetz's equation(2.13), which is an empirical formula used to calculate the core loss per unit volume.

$$P_{core} = k\ f_s^a\ B_{max}^b \tag{2.13}$$

where f_s is switching frequency, B_{max} is the maximum flux density. k, a and b are constants which depends on the type of core.

Another way of calculating or estimating the core loss at specific switching frequency is to use core suppliers' curve fit equations. This way of calculating core loss is explain in the next chapter.

Copper losses are basically the resistive losses present in the copper winding of the inductor. Once the type of inductor wire is selected, then the resistance of the copper wire can be calculated by

$$R_{DC} = \frac{\rho l}{A} \tag{2.14}$$

where ρ is the resistivity of the copper wire, L is the length of to form the required turns in the inductor and A is the cross sectional area of the copper wire selected. Then the copper loss can be easly calculated using (2.15), where $\mathrm{i}_{L,rms}$ is the RMS current through the inductor

$$P_{copper} = i_{L,rms}^2 R_{DC} \tag{2.15}$$

2.4.3 Switching element

The selection of switching element in a PFC depends on different parameters. The first requirement is the switching frequency of the system. Usually IGBT switches are used in high voltage low switching frequency applications while MOSFETs are usually used in high switching frequency low voltage applications. The switching frequency of the PFC itself should optimize the size of passive components and switching losses. Usually the switching frequency in a PFC is chosen to be between 25kHz and 150kHz. As mentioned in[28] most of DC to DC and AC to DC converters usually fail to meet the requirements of electromagnetic compatibility (EMC) certification in their first design loop. If size is an issue the switching frequency should be pushed higher to decrease the size of passive components and a proper size of EMI filter should be designed.

The most important parameters selecting a MOSFET are drain to source voltage rating, rated drain to source current rating V_{DS}, the on state resistance, $R_{DS,on}$ and the gate charge, Q_g. Furthermore, in order to have as low switching losses as possible, the turn on and turn off transient times should have be low.

MOSFET losses
Ideally, MOSFETs are represented as an ideal switch i.e. zero resistance while it's in on state and infinite resistance when it's in off state. In real scenarios this is a wrong assumption and a proper MOSFET model should be investigated to determine the losses associated with the it.

MOSFETs have four types of losses. These are switching losses, conduction losses, gate losses, and MOSFET's output capacitance or MOSFET's body diode losses. These losses can be determined using three methods[29]. The first method can be equating the turn on and turn off time transients to estimate the losses. The second method is to use the datasheet information to approximate MOSFET losses. The last method is to physically model MOSFET's parameters such as doping density, geometry, and to use finite element analysis software like COMSOL to evaluate the losses.

Conduction losses in MOSFETs are caused by the continues voltage drop in the MOSFET while it is conducting because of the presence of the on time resistance of a MOSFET, $R_{DS,on}$ and is given by (2.17). For active boost and bridgeless PFC the drain to source current of a MOSFET can be given by

$$I_{DS,rms} = \frac{P_{out}}{\eta V_{rect}} \sqrt{2 - \frac{16 V_{rect}}{3\pi V_o}} \tag{2.16}$$

For interleaved PFC the drain to source current is half of the one given in (2.16). Although it takes a few nano seconds for the MOSFET to turn on and to turn off, switching losses of a MOSFET are significant, because of their high switching frequency applications. These MOSFET switching losses are caused by the voltage and current overlap area while the MOSFET turns on and turns off as it will be clearly explained below. This way of switching MOSFETs is called hard switching.

There are ways of implementing the PFC switch to operate in zero voltage and zero current switching by using additional circuit components[14]. This type of switch operation is called soft switching and help reduce the switching losses. As a result, the switching frequency can be pushed to a few MHz range to increase the efficiency and power density.

$$P_{conduction} = i^2_{DS,rms} R_{DS,on} \tag{2.17}$$

2.4.3.1 MOSFET switching waveforms

MOSFET turn on

Turn on MOSFET waveforms are shown in Figure 2.16. Before the time period t_1, i.e. t_0, the MOSFET was turned off and the current passing through it I_{DS}, was zero. During the delay time, t_1, the gate to source voltage, V_{GS} increase from 0 to the threshold voltage V_{th}. Once this voltage level is reached, then the current start to flow from gate to source.

The time period t_2 is called current rise period. Since V_{GS} is above V_{th} value and the current keeps flowing and reaches its final value by the end of this period, and the voltage increase from V_{th} to plateau voltage V_{pl}. During voltage fall period, t_3, the gate to source voltage, V_{GS}, is constant since the MOSFET inters into saturation region. The time period, t_4 is called gate voltage rise time. In this interval the gate voltage increases to its final value to decrease the on time resistance of the MOSFET.

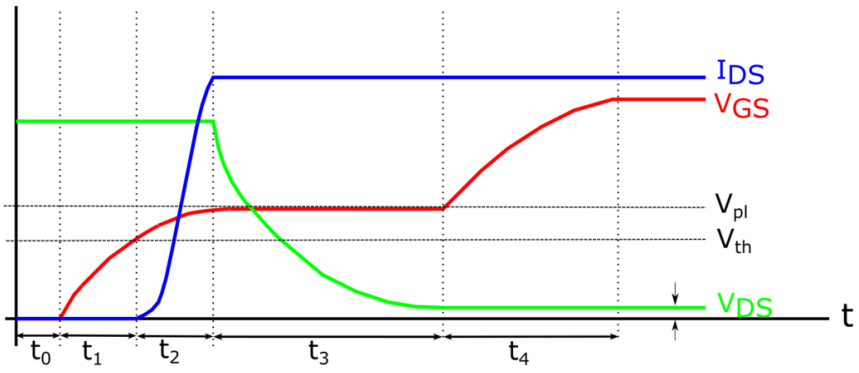


Figure 2.16: Turn on switching transients of MOSFET

It is evident that from Figure 2.16, the turn on losses occur during current rise time, t_2 and voltage fall time, t_3.

$$t_{on} = t_{ir} + t_{vf}$$

$$t_{ir} = C_{iss} R_g ln(\frac{V_g - V_{th}}{V_g - V_p l}) \tag{2.18}$$

$$t_{vf} = C_{rss} Rg \frac{V_{ds} - V_{pl}}{V_g - V_{pl}} \tag{2.19}$$

now the turn on losses can be expressed as

$$P_{on} = \frac{1}{2} i_{in} V_o t_{on} f_s \tag{2.20}$$

where i_{in} is the input current, V_o is the output voltage and f_s is the switching frequency.

MOSFET turn-off
Figure 2.17 shows the turn off transients of a MOSFET. During turn off the reverse sequence of the turn on process repeats. During the turn-off delay time interval, t_5, the gate voltage, V_{GS}, is decreasing to V_{pl} and the resistance of the channel increases. Whem V_{GS} reaches its V_{pl} value, textitV_{DS} starts to increase. The time period t_6 is called voltage rise time.

The time period t_7 is the current fall period. The current I_{DS} decreases to zero and the current will be transferred to the free-wheeling diode. The time period t_8 is called Gate voltage fall time. The turn off process is completed at the end of t_7 but the voltage V_{GS} decrease to zero as the charge stored in C_{iss} discharges slowly.

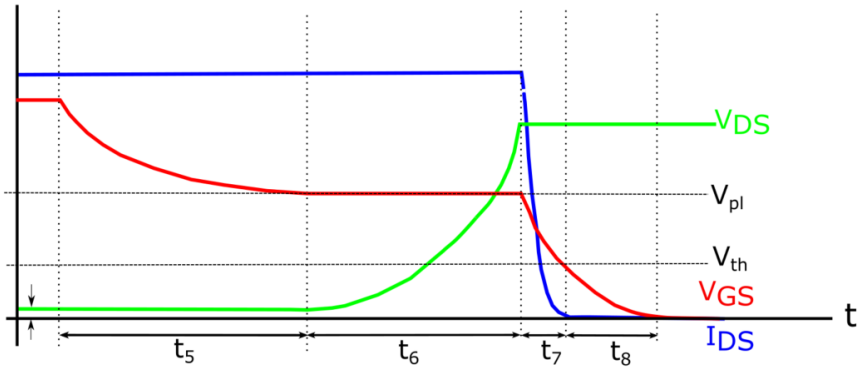


Figure 2.17: Turn off switching transients of MOSFET

From Figure 2.17, the turn off losses only occur during voltage rise time, t_6 and current fall time t_7 which can be expressed as

$$t_{off} = t_{vr} + t_{if}$$

$$t_{vr} = C_{iss} R_g ln(\frac{V_{pl}}{V_{th}}) \tag{2.21}$$

$$t_{if} = C_{rss} Rg \frac{V_{ds} - V_{pl}}{V_{pl}} \tag{2.22}$$

then the turn off loss can be given by

$$P_{off} = \frac{1}{2} i_{in} V_o t_{off} f_s \tag{2.23}$$

The gate loss, which is the power loss dissipated while energizing the gate charges present in the MOSFET can be given by

$$P_{gate} = Q_g V_g f_s \tag{2.24}$$

where Q_g is the gate charge and V_g is the gate voltage. The loss dissipated by the output capacitance of the MOSFET can be, respectively, given by

$$P_{coss} = e_{oss} f_s \tag{2.25}$$

where e_{oss} is the energy stored in the output capacitor of the MOSFET.

2.4.4 Boost diode

The selection or sizing of the boost diode in PFC depends on the ability to block the reverse voltage from the output and on the average current requirement. Furthermore, the reverse recovery charge of the boost diode Q_{rr}, and the on time resistance and the voltage drop across the diode while conducting should considered.

Boost diode losses

The losses associated with the boost diode can be divided into conduction and switching losses. During turn on, a diode can be considered as ideal switch as it turns on very fast[5], but when it switches off, it has to release the charges, stored while it was conducting, for some time period called reverse recovery time, t_{rr}. Figure 2.18 shows the reverse recovery current of boost diode in PFC converter.

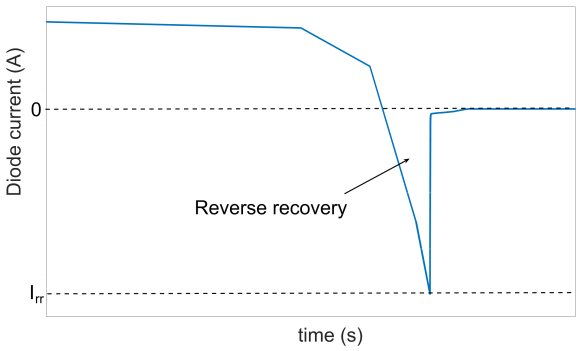


Figure 2.18: Diode reverse recovery current,I_{rr}

The amount of charge stored during conduction period, also known as capacitive charge, depends on the type of the diode selection. The reverse recovery loss is then calculated from Q_{rr} found on the datasheet of the diode and this reverse recovery loss directly depends on the switching frequency. The switching losses of the boost diode can be calculated from (2.26)

$$P_{drc} = \frac{1}{2} V_o Q_{rr} f_{sw} \tag{2.26}$$

where V_o is the voltage it has to block, in this case, it is the output voltage, and f_{sw} is the switching frequency of the PFC. Conduction losses of the boost diode can be calculated using the same equation used to calculate the conduction losses of the diode bridge, as given in (2.5).

2.4.5 Output capacitor

The output capacitor is the energy storage device and helps to smooth out the ripple voltage present at the output. It should be properly dimensioned considering hold up time requirement or allowable voltage ripple consideration. If both requirements should be considered, then the larger size should be chosen.

The equation to calculate the size of the capacitor is derived from the power equation and by the amount of energy that is needed during the hold up time. Equation (2.27) is based on hold up time requirement and (2.28) is based on allowable output voltage ripple.

$$C_o = \frac{2\ P_o\ T_{holdup}}{{V_o}^2 - V_{oholdup}^2} \tag{2.27}$$

$$C_o = \frac{P_o}{2\pi f_g \Delta V V_o} \tag{2.28}$$

In practice, the actual capacitance value used is a little bit higher than the one calculated in (2.27) and (2.28). This is to make sure that the voltage ripples as minimum as possible and the converter has to provide energy for at least for the hold up time. Capacitors are usually categorized based on the type of dielectric used.

Ceramic capacitors have ceramic dielectric and aluminum electrolytic capacitors has a thin film of aluminum oxide film that cover the capacitor plates. Usually aluminum electrolytic capacitors are used where high power density is required, because of their small volume. These types of capacitors are also preferred in PFC applications since they provide high capacitance value with low equivalent series resistance (ESR).

Capacitor losses
The ESR of a capacitor represents the equivalent resistance present in the capacitor. ESR of a capacitor can be determined from three methods. The first method is to measure it on the physical capacitor using ESR meter, the second way is to use dissipation factor, which is the ratio of the ESR and capacitive reactance which is roughly between 10% to 20%, at specific frequency, *f*, using (2.29)

$$ESR = \frac{DF}{2\pi f C_o} \tag{2.29}$$

where DF is the dissipation factor, C_o is the capacitor value and f is a test frequency which typically 120Hz for aluminum electrolytic capacitors[30]. The third method is to use the ESR value of a capacitor from the datasheet. Once the ESR is determined, the power loss can be calculated using

$$Pcap = {i_{crms}}^2 ESR \tag{2.30}$$

where $i_{c,rms}$ is the RMS current through the capacitor.

2.4.5.1 Hold up time requirement in telecom

Hold up time comes from the reason that even if the input voltage level is zero because of a power outage or any other reason the circuit should provide the load for a specific amount of time called hold up time. For PFC circuits in telecom industry the hold-up time requirement is usually 20ms and for LLC it is usually 16ms. The hold up time for LLC is smaller than the PFC this is because of the reason that the PFC provides as an input for LLC, so the hold up time of the PFC should be higher or at least equal to the hold up time of the LLC so that the LLC can provide the proper amount of energy during the hold up time.

2.5 Small signal model of PFC converters

In order to evaluate the losses in the PFC, an open loop control system is established to control the current input. For CCM and average current control mode, the open loop transfer function can be expressed as

$$TF_{OL}(s) = G_v(s)\frac{G_{cc}(s)G_i(s)}{1 + G_{cc}(s)G_i(s)} \tag{2.31}$$

where $G_i(s)$ is inductor current to duty transfer function, $G_v(s)$ is voltage to current transfer function and G_{cc} is the current compensator or current controller.

In addition to the input current, if the output voltage level is required to be controlled, voltage controller should be implemented with feedback system as shown in Figure 2.19. In this case the closed loop controller will have internal current control loop, which should be very fast, and an outer loop voltage controller which should be very slow.

$$TF_{CL}(s) = \frac{G_{vc}(s)TF_{OL}(s)}{1 + G_{vc}(s)TF_{OL}(s)LP(s)} \tag{2.32}$$

where $LP(s)$ is the transfer function of the low pass filter which is required to filter out high frequency components since the output voltage might contain high frequency components from the switching action. TF_{OL} is the open loop transfer function given in (2.31).

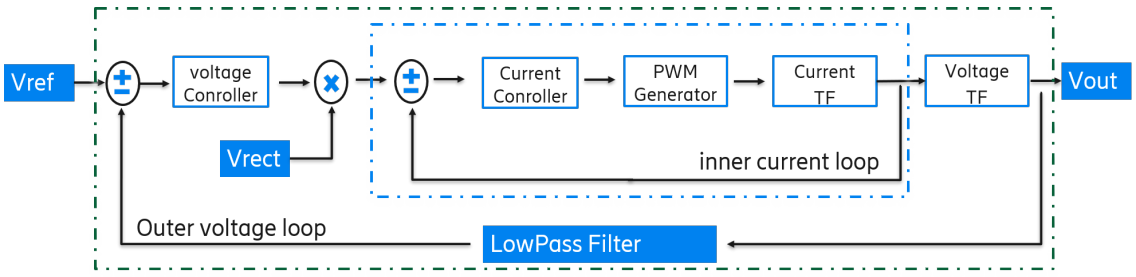


Figure 2.19: block diagram of control block for PFC in CCM

The inductor current to duty transfer function, $G_i(s)$ and the output voltage to current transfer function, $G_v(s)$, can be found by deriving state space equation for respective PFC topologies as explain in the next subsection.

Once the transfer functions are derived, for loss analysis purpose, the compensator can be designed using MATLAB's single input single output controller design tool. The bode plot of open loop and closed loop transfer functions for each PFC converter is plotted and can be found in the appendix at the end of this document.

2.5.1 Small signal model of active boost PFC

Because of the non-linearity of active boost converter, the open loop transfer function of active boost PFC can be determined by state space averaged technique. As shown in Figure 2.8, the boost PFC converter has two operating modes, one is when the switch is on and the other when the switch is off. In time domain, when the switch is on, the inductor voltage and capacitor current of active boost PFC can be written in the following two equations

$$\frac{di_L(t)}{dt} = \frac{v_{rect}}{L} \tag{2.33}$$

$$\frac{dv_o(t)}{dt} = -\frac{v_o(t)}{CR_L} \tag{2.34}$$

and when the switch is off

$$\frac{di_L(t)}{dt} = \frac{v_{rect}}{L} - \frac{v_o(t)}{L} \tag{2.35}$$

$$\frac{dv_o(t)}{dt} = \frac{i_L(t)}{C} - \frac{v_o(t)}{CR_L} \tag{2.36}$$

The above four equations can be combined together to form large signal model of the active boost PFC using state space averaged technique as explained in [31][32].

$$\frac{di_L(t)}{dt} = \frac{v_{rect}}{L} - \frac{(1-d)v_o(t)}{L} \tag{2.37}$$

$$\frac{dv_o(t)}{dt} = \frac{(1-d)i_L(t)}{C} - \frac{v_o(t)}{CR_L} \tag{2.38}$$

The above two equation can be linearized by assuming that the variables (i_L, v_{rect}, v_o, and d) by a steady state values a very small signal perturbation. This small signal model can then be used to describe the operation of converter around the steady state operation point. By replacing i_L, v_{rect}, v_o, and d by steady state variable and small signal perturbation where $i_L = I_L + \hat{i_L}$, $v_{rect} = V_{rect} + \hat{v_{rect}}$, $v_o = V_o + \hat{v_o}$, and $d = D + \hat{d}$.

$$\frac{d(I_L + \hat{i_L})}{dt} = \frac{(V_{rect} + \hat{v_{rect}})}{L} - (1 - D - \hat{d})\frac{V_o + \hat{v_o}}{L} \tag{2.39}$$

$$\frac{d(V_o + \hat{v_o})}{dt} = (1 - D - \hat{d})\frac{I_L + \hat{i_L}}{C} - \frac{V_o + \hat{v_o}}{CR_L} \tag{2.40}$$

Neglecting the stead state values and from the fact that the product of two small number gives even a very small number and hence ignoring those the above equation reduces to

$$\frac{\hat{i_L}}{dt} = \frac{\hat{v_{rect}}}{L} - (1-D)\frac{\hat{v_o}}{L} + V_o\frac{\hat{d}}{L} \tag{2.41}$$

$$\frac{d\hat{v_o}}{dt} = (1-D)\frac{\hat{i_L}}{C} - I_L\hat{d} - \frac{\hat{v_o}}{CR_L} \tag{2.42}$$

rearranging the above two equations gives

$$\begin{bmatrix} \dot{\hat{i_L}} \\ \dot{\hat{v_o}} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & -\frac{1}{CR_L} \end{bmatrix} \begin{bmatrix} \hat{i_L} \\ \hat{v_o} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{V_o}{L} \\ 0 & -\frac{I_L}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_{rect} \\ \hat{d} \end{bmatrix} \tag{2.43}$$

Equation 2.43 represents small signal AC model of active boost PFC and Figure 2.20 shows the small signal model of the PFC using dependent voltage and current sources. The small signal model diagram is drawn using [33] as a reference for one phase only. The voltage across the output, i.e. across RL in the figure below, represents the output voltage which is assumed to be constant for the small signal representation.

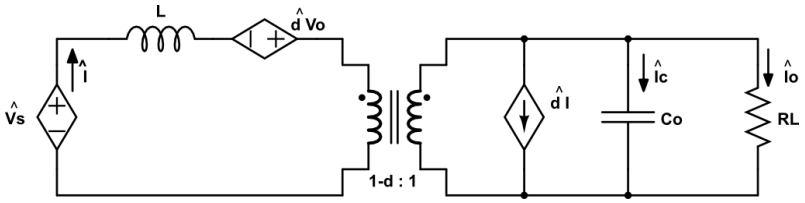


Figure 2.20: Small signal model of boost PFC

From (2.43), it is possible to derive an output to input transfer function using state space equations. Once the transfer functions are determined, then it is possible to design a compensate or a controller according to the required cut over frequency and phase margin. The cut over frequency determines the range of frequencies up to which the controllable is working or responsive and frequencies above the cut over frequencies are attenuated. The phase margin of the transfer function determines if the system is stable or not. It also shows how quickly the system responds to transient events.

$$G_i(s) = \frac{\hat{i_L}}{\hat{d}} = \frac{sCV_o + \frac{V_o}{R} + (1-D)I_L}{s^2LC + s\frac{L}{R_L} + (1-D)^2} \tag{2.44}$$

in canonical form

$$G_i(s) = \frac{\hat{i_L}}{\hat{d}} = \frac{2V_o}{R_L(1-D)^2}\frac{1 + \frac{sCR_L}{2}}{1 + \frac{sL}{R_L(1-D)^2} + \frac{s^2LC}{(1-D)^2}} \tag{2.45}$$

The voltage controller transfer function can be given as the output voltage to inductor current transfer function

$$G_v(s) = \frac{\hat{v_o}}{\hat{i_L}} = \frac{V_o(1-D) + sLI_L}{sCV_o + 2(1-D)I_L} \tag{2.46}$$

2.5.2 Small signal model of interleaved boost PFC

The small signal modelling of the interleaved PFC can be derived the same way as explain for the small signal modeling of active boost PFC using state space averaging technique. Unlike active boost PFC, interleaved PFC does not only have two operating modes, instead it has four and if the average duty cycle is less than 0.5, both switches will not be turned on at the same time which results in three operating modes. This is because of the reason that interleaved PFC contains two separate boost PFC converters operating 180 degrees out of phase. These two separate legs are assumed to operate identically to derive the transfer function of the model. The first operating states is when *Sw1* is on and *Sw2* is off in Figure 2.10. The equations governing this state are given by the following set of equations.

$$\frac{di_{L1}(t)}{dt} = \frac{v_{rect}}{L_1} \tag{2.47a}$$

$$\frac{di_{L2}(t)}{dt} = \frac{v_{rect}}{L_2} - \frac{v_c}{L_2} \tag{2.47b}$$

$$\frac{dv_o(t)}{dt} = -\frac{i_{L2}}{C} - \frac{v_o(t)}{CR_L} \tag{2.47c}$$

The second operating mode is when *Sw1* is off and *Sw2* is on, and the equation governing these states are

$$\frac{di_{L1}(t)}{dt} = \frac{v_{rect}}{L_1} - \frac{v_c}{L_1} \tag{2.48a}$$

$$\frac{di_{L2}(t)}{dt} = \frac{v_{rect}}{L_2} \tag{2.48b}$$

$$\frac{dv_o(t)}{dt} = \frac{i_{L1}}{C} + \frac{i_{L1}}{C} - \frac{v_o(t)}{CR_L} \tag{2.48c}$$

The third operating mode is when both *Sw1* and *Sw2* are off, and the equation governing these states are

$$\frac{di_{L1}(t)}{dt} = \frac{v_{rect}}{L_1} - \frac{v_o}{L_1} \tag{2.49a}$$

$$\frac{di_{L2}(t)}{dt} = \frac{v_{rect}}{L_2} - \frac{v_o}{L_2} \tag{2.49b}$$

$$\frac{dv_o(t)}{dt} = \frac{i_{L1}}{C} + \frac{i_{L2}}{C} - \frac{v_o(t)}{CR_L} \tag{2.49c}$$

Equations from (2.47a) to (2.49c) can be combined together into one average state space equation using state space averaged method[34][32], in the same way as used to derive for active boost PFC previously, to give

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L} \\ 0 & 0 & -\frac{1-d}{L} \\ \frac{1-d}{C} & \frac{1-d}{C} & -\frac{1}{CR_L} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{rect} \\ d \end{bmatrix} \tag{2.50}$$

Equation 2.50 represents the large signal model of interleaved PFC. The small signal model can be derived from the large signal model by introducing a small signal perturbation to the state values, i.e. replacing i_L, v_{rect}, v_o, and d by steady state variable and small signal perturbation where i_L=I_L+$\hat{i_L}$, v_{rect}= V_{rect}+$\hat{v_{rect}}$, v_o=V_o+$\hat{v_o}$, and d=D+$\hat{d}$. Then the small signal model can be obtained by neglecting stead state values to get

$$\begin{bmatrix} \dot{\hat{i}}_{L1} \\ \dot{\hat{i}}_{L2} \\ \dot{\hat{v}}_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1-D}{L} \\ 0 & 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & \frac{1-D}{C} & -\frac{1}{CR_L} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{V_o}{L} \\ \frac{1}{L} & \frac{V_o}{L} \\ 0 & \frac{i_{L1}+i_{L2}}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_{rect} \\ \hat{d} \end{bmatrix} \tag{2.51}$$

The two leg inductor currents are assumed to be identical so, the current to control (duty cycle) can be written as

$$G_i(s) = \frac{\hat{i_{L1}}}{\hat{d}} = \frac{\hat{i_{L2}}}{\hat{d}} = \frac{sR_LCV_o + 2V_o}{s^2LCR_L + sL + 2(1-D)^2R_L} \tag{2.52}$$

and the output voltage to inductor current transfer function can be derived in same way to get

$$G_v(s) = \frac{\hat{v_o}}{\hat{i_L}} = \frac{v_{rect}}{s2V_oC} \tag{2.53}$$

2.5.3 Small signal model of bridgeless PFC

A bridgeless boost PFC has four operation modes as interleaved PFC. For the positive half cycle of supply voltage V_s, the switch *Sw1* changes its state while switch *Sw2*, in figure 2.12, stays off and vice versa for the negative half cycle of V_s. Assuming identical inductors (L_1 and L_2), boost diodes (D_1 and D_2), slow diodes (D_3 and D_4) and switches ($Sw1$ and ($Sw2$), the following equations can be derived for the four operating modes. If one of the switches is open and the other is off, the equation governing the states are the same regardless of the positive or negative cycle of V_s and can be written as

$$\frac{di_L(t)}{dt} = \frac{v_s}{L} \tag{2.54a}$$

$$\frac{di_L(t)}{dt} = -\frac{v_c}{CR_L} \tag{2.54b}$$

when both of the switches are off, regardless of the positive or negative cycle of V_s, the equation governing the states are the same and can be written as

$$\frac{di_L(t)}{dt} = \frac{v_s}{L} - \frac{v_c}{L} \tag{2.55a}$$

$$\frac{dv_c(t)}{dt} = \frac{i_L}{C} - \frac{v_c}{CR_L} \tag{2.55b}$$

In the same way as showed previously, these equations, (2.54) and (2.55), can be written into a one state state space equation using state space averaging technique[35] and gives the averaged large signal model of the bridgeless PFC as

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-d}{L} \\ \frac{d-1}{C} & -\frac{1}{CR_L} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \begin{bmatrix} v_s \\ d \end{bmatrix} \tag{2.56}$$

The large signal model of the bridgeless PFC, (2.56), can be liberalized into a steady state operating value by introducing small signal perturbations into the large signal model state values, i.e. replacing i_L, v_s, v_o, and d by steady state variables and a small signal perturbation where i_L=I_L+$\hat{i_L}$, v_s= V_s+$\hat{v_s}$, v_c=V_c+$\hat{v_c}$, and d=D+$\hat{d}$. Then removing the multiplication of the perturbations and steady state values, it is possible to derive the following small signal model of the bridgeless PFC.

$$\begin{bmatrix} \dot{\hat{i_L}} \\ \dot{\hat{v_c}} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & -\frac{1}{CR_L} \end{bmatrix} \begin{bmatrix} \hat{i_L} \\ \hat{v_c} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{V_s}{L(1-D)} \\ 0 & -\frac{V_s}{(1-D)CR_L} \end{bmatrix} \begin{bmatrix} \hat{v_s} \\ \hat{d} \end{bmatrix} \tag{2.57}$$

Equation (2.57) represents the small signal model of the bridgeless PFC and the current to duty cycle transfer function can be derived as

$$G_i(s) = \frac{\hat{i_L}}{\hat{d}} = \frac{2V_s + V_s R_L C s}{R_L LC(1-D)s^2 + L(1-D)s + R_L(1-D)^3},$$

in canonical form

$$G_i(s) = \frac{V_s(2+sCR_L)}{R_L(1-D)^3} \frac{1}{s^2\frac{LC}{(1-D)^2} + s\frac{L}{R_L(1-D)^2+1}} \tag{2.58}$$

and the output voltage/capacitor voltage to inductor current transfer function can be derived in same way to get

$$G_v(s) = \frac{\hat{v_o}}{\hat{i_L}} = \frac{V_s}{2V_c} \frac{1}{2V_c R_L C s + 1} \tag{2.59}$$

2.6 Overview on isolated DC-DC converter topologies

This DC/DC stage comes after the PFC converter i.e. the outputs of the PFC stage are connected to the inputs of the DC/DC converter. There are many factors that drive to select a suitable topology for a power supply. Some of the important factors are output power level, efficiency, power density, isolation, cost (related to number of power devices), input voltage range and output voltage.

Some of the basic topologies that are usually used for isolated DC/DC power converters can be listed from lower to higher power application as flyback, forward, push-pull, half-bridge LLC and full-bridge LLC resonant and phase shifted full-bridge converters [36].

The most common topologies among many available resonant converter topologies

are series resonant converter (SRC), parallel resonant converter (PRC)and LLC resonant converter. In all the resonant topologies, the working principle is essentially the same.

Series resonant converter (SRC)
In series resonant converter, the tank circuit is a series connection of one inductor and one capacitor. The tank circuit is connected in series with the load. The fact that, an SRC works as a voltage divider between the resonant circuit and the load, the output voltage regulation is difficult at light or no load for this converter[37].For this converter, the maximum DC gain is 1 and this happens at the resonant frequency where the resonant tank impedance is minimum. Due to its insufficient capability of output voltage regulation and high circulating current at higher switching frequency, this converter is not a good choice for telecom application[38].

Parallel resonant converter (PRC)
In a parallel resonant converter, the resonant circuit (one capacitor and inductor connected in parallel) is connected in parallel with the load and this acts as a band stop filter. This converter has better voltage regulation as compared to SRC but larger amount of circulating current requirement as the input voltage increases. There converter topology difficult to apply for applications which need smaller size components and large load variations.
Some of the high efficiency resonant converter topologies for the intended application are shown in Table 2.2. Only LLC resonant topology of these isolated type will be discussed in this chapter while the other topologies are deemed to be not suitable for this study.

Table 2.2: High Efficiency resonant converters

No	Topology	Feature	Power(W)	Peak Eff.(%)	Ref.
1	Series resonant converter (SRC)	Phase shifted, Diode rectification	2000	95.6	[39]
2	Half bridge LLC	Diode rectification	350	96.3	[40]
		SR rectification	600	97.8	[41]
		Uses GaN switches	1000	97.6	[42]
3	Full bridge LLC	Phase shifted, SR rectification	1000	97.6	[43]
		Uses GaN	3000	98.4	[44]
4	Interleaved half bridge	SR rectification	2700	98	[45]
5	Hybrid full bridge-half bridge	Diode rectification	3700	98.3	[46]

2.7 LLC resonant converters

Nowadays, LLC resonant converters are receiving much attention because of their potential to achieve both higher switching frequencies and higher efficiency. However, the fact that LLC resonant converters are frequency controlled brings more

challenges in their design as compared to pulse width modulated converters. Essentially, all the LLC resonant circuit contains the following basic function blocks:

- Switching bridge
- LLC tank
- Transformer and rectifier circuit
- Output filter capacitor

The first function block which is the switching bridge, generates a square wave to excite the resonant tank section. The LLC resonant tank block, has the role to generate a resonant sinusoidal current which will get scaled by the transformer and rectified by the rectifier circuit. The fourth block, which is the output section of the circuit contains an output capacitor to filter the rectified sinusoidal current and produces a DC output voltage.

The three LLC resonant topologies selected for further discussion are half bridge, full bridge and interleaved half bridge resonant converters, and their mode of operations are explained as follows.

Operating modes
Depending on the load conditions and input voltage, the operation of the LLC resonant converter can be seen in three modes. The operating modes of the LLC resonant converter is based on the relationship between the switching frequency, f_s, and series resonant frequency, f_o.

Below resonance, when the switching frequency is below the series resonant frequency. In this mode of operation, the converter works in boost mode. Figure 2.21 shows the current wave forms for frequencies below resonant frequency. Between times t1 and t2 the resonant current and the magnetizing current are equal, and no energy is delivered to the load at this time. In this time interval, drain to source capacitance of the primary MOSFET switches helps to discharge the magnetizing current to achieve zero voltage switching. In this operating mode, the magnitude of the resonant current is high and so is the conduction loss.

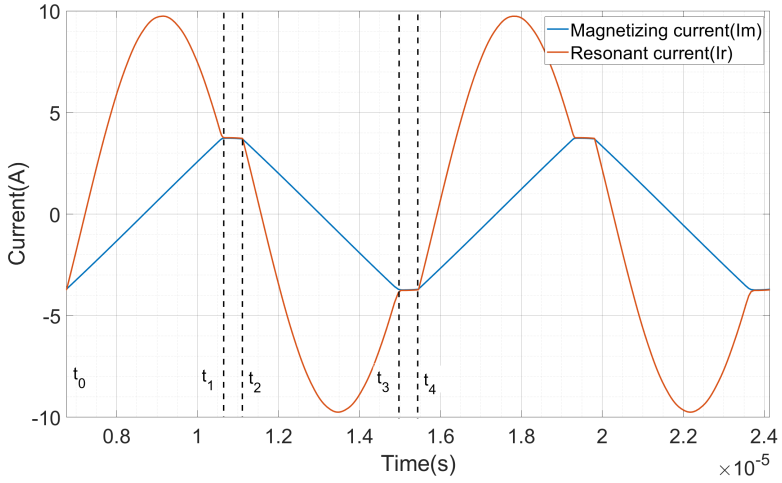


Figure 2.21: When witching frequency is below resonance frequency

At resonant frequency, when the switching frequency is the same as the series resonant frequency. The input voltage is at its nominal value and the transfer function of the resonant network is not sensitive to load variation. In this mode of operation, the impedance of the resonant tank is minimum, and the converter achieves its highest efficiency. Figure 2.22 shows the tank current wave forms at resonant frequency.

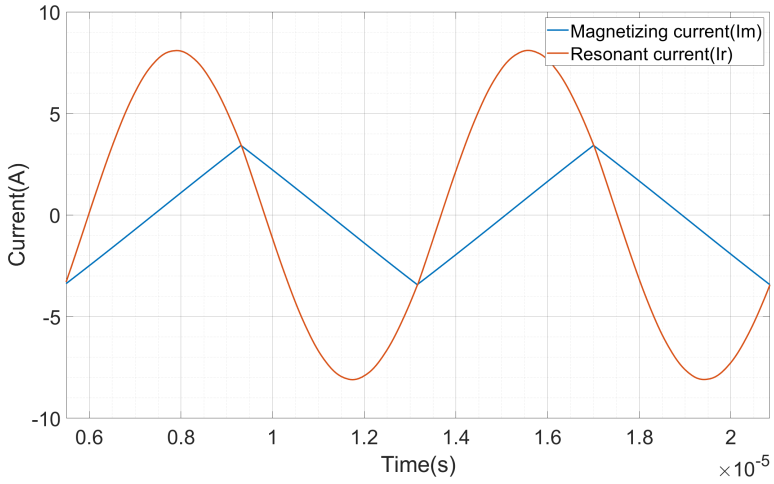


Figure 2.22: When witching frequency is equal to resonance frequency

Above resonance, when the switching frequency is above the series resonant frequency. The magnetizing inductance, Lm, is clamped by the out voltage and it doesn't participate in the resonance. In this mode of operation, the converter works in buck mode depending on the resonant tank component values. Figure 2.23 shows the tank current wave forms at resonant frequency.

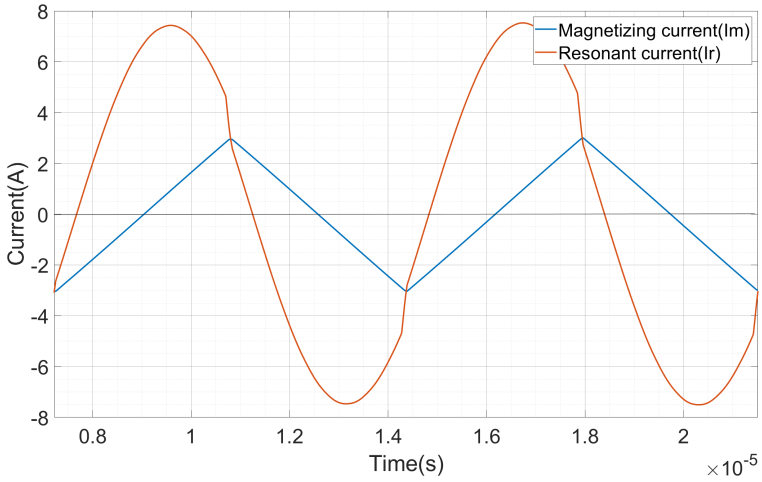


Figure 2.23: When witching frequency is above resonance frequency

2.7.1 Half-bridge LLC resonant converter

Due to its simple structure and capability to achieve soft switching over the entire load range the half bridge LLC resonant converter is commonly used in medium power applications. It has also an advantage of a smaller number of switches in the current flowing path which results in less conduction loss as compared to the full bridge converter. Figure 2.24 shows a typical half bridge LLC resonant converter circuit configuration.

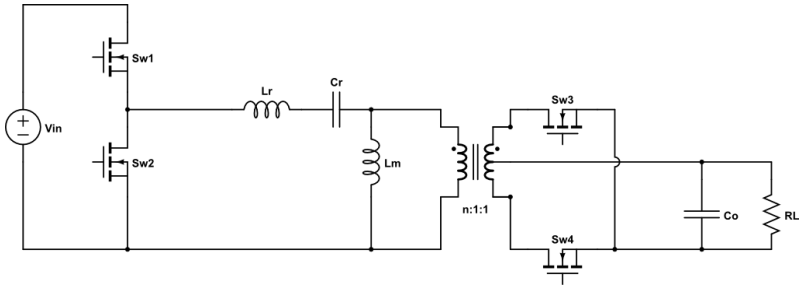


Figure 2.24: Half bridge LLC resonant converter

2.7.2 Full-bridge LLC resonant converter

This topology is basically the same with half bridge LLC resonant converter except there are four semiconductor devices in the switching bridge. The switching bridge generates a periodical square wave which varies between V_{in} and $-V_{in}$. For the same power level, the current in the primary side of the circuit is reduced as compared to half bridge LLC resonant converter. Therefore, the conduction loss of full bridge is less than the half bridge LLC resonant converter.

Similar to half bridge LLC resonant converter, the output capacitance, C_{oss}, of the MOSFET switches in full bridge LLC resonant converter should be fully charged and discharged to achieve zero voltage switching. Thus, sufficient current through the MOSFET during the dead time, t_d, is required[47].

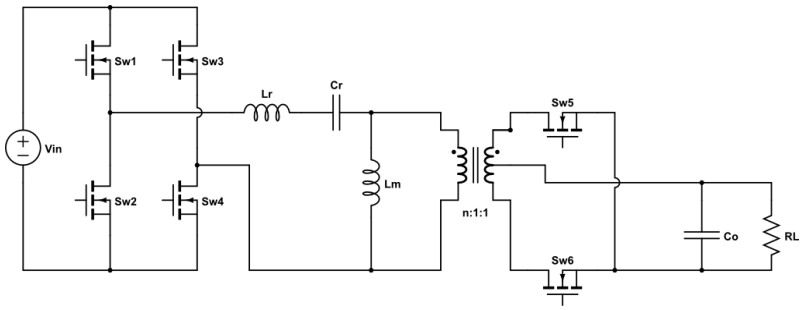


Figure 2.25: Full bridge LLC resonant converter

2.7.3 Interleaved half bridge LLC converter

The Parallel-configuration of LLC resonant converter is a good way to increase the output power rating. The output current and voltage ripple can be reduced

by introducing an interleaved operation between the two half bridge LLC resonant converters connected in parallel. This helps to achieve higher efficiency[48]. With this topology, high efficiency can reach up to 98% around 2kW output power [45].

The output current from the rectifier switches of the two half bridge LLC is summed up at the output side. As such, the filter capacitor ripple current magnitude is then reduced, which will lead to higher efficiency.

Introducing a 90° phase shift between the two legs of the two parallel connected half bridge LLC converters, is a good way to effectively reduce the magnitude of the filter capacitor ripple current. Figure 2.26 shows the circuit configuration of interleaved half bridge LLC resonant converter.

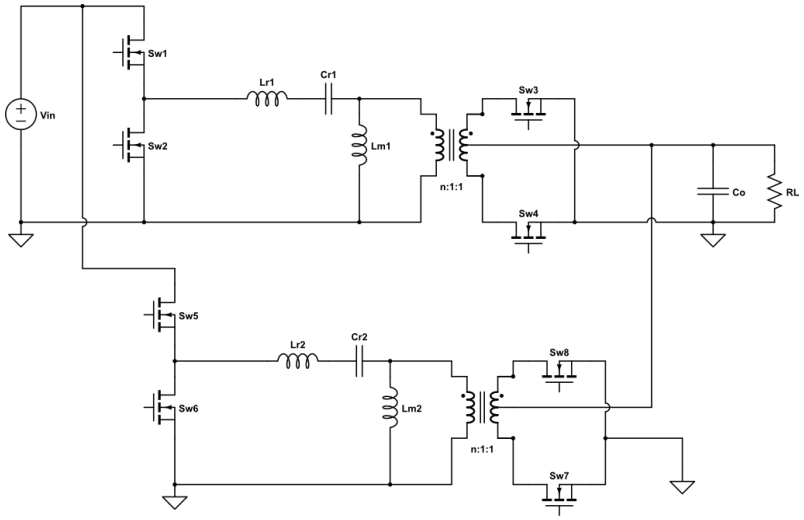


Figure 2.26: Interleaved LLC half bridge resonant converter

2.8 Losses and component sizing of LLC stage

The power loss in the resonant converter is mainly from conduction losses, copper losses, switching losses of MOSFETs, and transformer core loss. The loss model of each component in the half bridge resonant converter is shown in Figure 2.27.

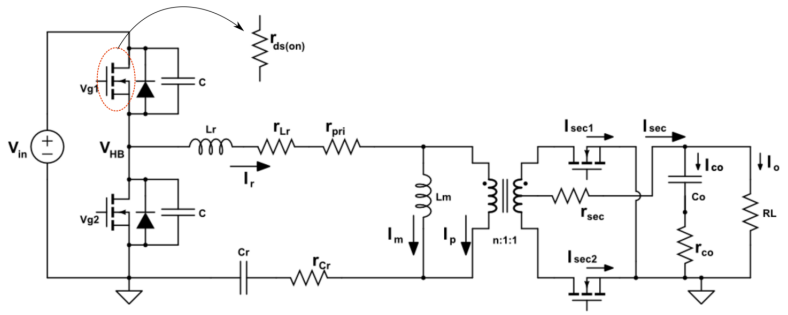


Figure 2.27: Conduction loss model of the LLC resonant converter

2.8.1 MOSFETs

The selection of the primary side MOSFETs is critical in the LLC converter. The output capacitance of the MOSFETs needs to be low with less focus on the MOSFET on resistance, as for the total loss of the converter is more advantageous to have a low output capacitance, which will result in a lower energy needed to achieve ZVS. With low MOSFET output capacitance, the value of the magnetizing inductance in the transformer can be made to be high to have low circulating current which will reduce the conduction loss and improve the efficiency.

As can be seen from Figure 2.28, during the dead time interval, t_{dead}, the magnetizing current and the resonant current are equal, which indicates that the magnetizing current, I_m, circulates through the drain to source capacitances, C_{ds1} and C_{ds2} shown in Figure 2.27.

To ensure ZVS, there has to be sufficient inductive energy that can charge and discharge the two capacitance's. The dead time, t_{dead}, that can ensure this requirement can then be calculated as:

$$\frac{1}{2}(L_m + L_r)I^2_{m_{peak}} \geq \frac{1}{2}(2\,C_{eq})V^2_{in} \tag{2.60a}$$

$$t_{dead} \geq 16\,C_{eq} f_s\,L_m \tag{2.60b}$$

where C_{eq} is the drain to source capacitance of each MOSFET with some parasitic capacitance's added to it and f_s is the switching frequency.

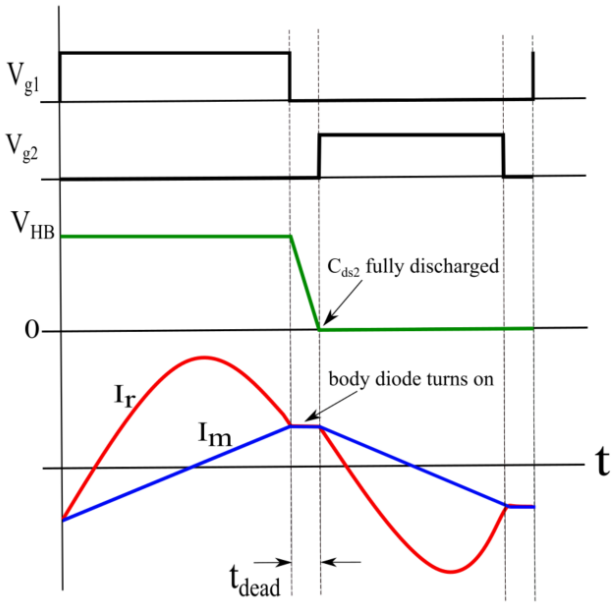


Figure 2.28: ZVS timing for LLC resonant circuit.

As can be seen from the wave form in Figure 2.28, the magnetizing inductance

current,i_m can be approximated to be an ideal triangle and it can be expressed as:

$$i_m = \begin{cases} \frac{n\,V_o}{L_m}(t - \frac{T_s}{4}) + \frac{i_{sec}}{n} \;\; , 0 \leq t < \frac{T_s}{2} \\ \\ \frac{n\,V_o}{L_m}\,\frac{T_s}{4} - \frac{n\,V_o}{L_m}(t - \frac{T_s}{2}) - \frac{i_{sec}}{n} \;, \frac{T_s}{2} \leq t < T_s \end{cases} \tag{2.61}$$

where T_s, f_o, i_{sec} and n represent the switching period, resonant frequency, current through the secondary MOSFETs and turns ratio of transformer respectively.

For the secondary side MOSFETs, the value of the MOSFET on resistance is more important than the output capacitance, but with the requirement that those are also easy to drive, low gate capacitance.

The conduction loss associated with each component can be calculated based on the loss model shown in Figure 2.27. The switching loss of the LLC resonant converter comes mainly from the turn-off switching action. As the LLC resonant converter achieves ZVS, the MOSFET's turn-on action does not contribute to the switching loss. Therefore, the loss calculation is based on the switching transition waveform shown in Figure 2.29.

The loss associated with the MOSFET on resistance can be given by

$$P_{rdson} = I_{Lrms}^2\, r_{ds(on)} \tag{2.62}$$

The gate driving loss of each MOSFET is given by

$$P_{gate} = \frac{1}{2} C_{gs} V_{gs}^2 f_s \tag{2.63}$$

where V_{gs} and C_{gs} are the driving signal voltage level and gate to source capacitance respectively. The body diode loss of each MOSFET is given by

$$P_{body} = V_{bf}\,[\frac{n\,V_o}{L_m}(\frac{1}{4}\frac{1}{f_s} - t_{dis})]\,t_{body(on)}\,f_s \tag{2.64}$$

where t_{dis}, $t_{body(on)}$ are the discharge time of drain to source capacitance and conduction time of a body diode.

During turn-off transition the rising voltage across the MOSFET and magnetizing current can be assumed to be linear[49]. The drain to source voltage and current can then be expressed as

$$v_{ds(t)} = V_{ds(on)} + \frac{V_{in} - V_{ds(on)}}{t_{dis}} t \tag{2.65}$$

$$i_{ds(t)} = \frac{n\,V_o}{L_m}\frac{1}{4\,f_s}(1 - \frac{t}{t_{dis}}) \tag{2.66}$$

The turn-off loss of each MOSFET is given by

$$P_{toff} = f_s \int_0^{t_{dis}} v_{ds(t)} i_{ds(t)} dt = \frac{n\,V_o\,t_{dis}\,(V_{in} + 2V_{ds(on)})}{24 L_m} \tag{2.67}$$

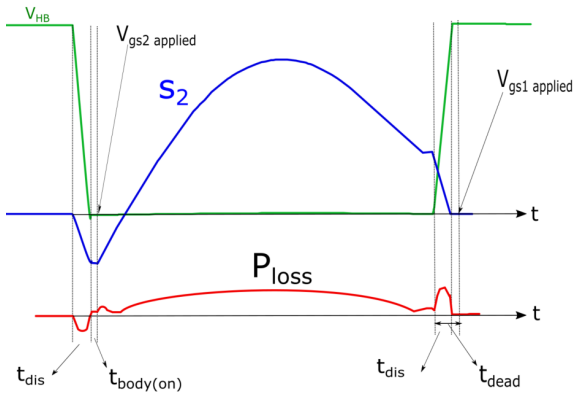


Figure 2.29: Switching transition of LLC resonant converter

2.8.2 Resonant tank inductor and capacitor ESR losses

As can be seen from the current waveforms in figure **??**, the rms value of the current through the resonant tank is close to that of MOSFET current. The loss in the resonant tank can then be calculated as

$$P_{tank} = I_{Lrms}^2 \left(r_{Lr} + r_{Cr}\right) \tag{2.68}$$

2.8.3 Transformer

To calculate the the losses in a transformer, both core related losses and winding losses are considered. The transformer primary winding loss is given by

$$P_{pri} = I_{Lrms}^2 \, r_{pri} \tag{2.69}$$

The transformer secondary conduction loss is

$$P_{sec} = I_{sec\,rms}^2 \, r_{sec} \tag{2.70}$$

The total conduction loss of the transformer is given by

$$P_{cu} = P_{pri} + P_{sec} \tag{2.71}$$

The transformer core loss is given by

$$P_{tf} = K_h \, B_{ac}^n \, f_s^m \, M_{core} \tag{2.72}$$

where B_{ac} is the magnetic field strength in Tesla, M_{core} is the mass of the core material in kilogram, n and m depend on the material and operating frequency range. The total loss in the transformer can then be given as

$$P_{cu} = P_{cu} + P_{tf} \tag{2.73}$$

2.8.4 Output capacitor

The output capacitor power loss is caused by the equivalent series resistance of the output capacitor, r_{co}, as shown in Figure 2.27. This capacitor power loss can be given as

$$P_{rco} = I^2_{Corms}\, r_{co} \tag{2.74}$$

where I_{Corms} is the RMS current through the output capacitor.
Depending on the ripple current magnitude through the capacitor, parallel connection of the output capacitors can be used to reduce the output capacitor loss.

2.8.5 Small signal model of LLC resonant converter

Unlike for pulse width modulation (PWM) converters where an averaging modeling technique can be used, for the LLC resonant converters a different modeling technique is used which is called Extended Describing Function (EDF). With the EDF technique, the small and large signal modeling of LLC resonant converters are derived in [50] as follows.

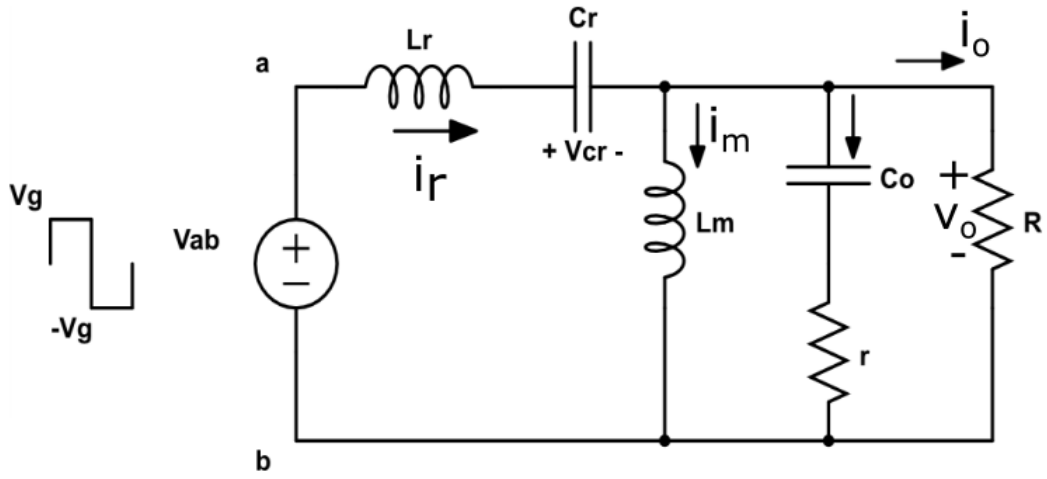


Figure 2.30: Non-linear equivalent circuit of LLC resonant converter

The non-linear state equations of the LLC converter in Figure 2.30 is given by

$$v_{ab} = L_r \frac{di_r}{dt} + v_{Cr} + L_m \frac{di_m}{dt} \tag{2.75a}$$

$$L_m \frac{di_m}{dt} = sgn(i_r - i_m)vo \tag{2.75b}$$

$$i_r = C_r \frac{dv_{Cr}}{dt} \tag{2.75c}$$

$$C_o \frac{dV_{co}}{dt}(1 + \frac{r}{R}) + v_{co}\frac{1}{R} = |i_r - i_m| + i_o \tag{2.75d}$$

$$v_o = \frac{r.R_i}{r+R_i}(|i_r - i_m| + i_o) + \frac{R}{R+r}v_{co} \tag{2.75e}$$

$$i_g = \frac{1}{T}\int_0^T i_r \frac{v_{ab}}{v_g} d(t) \tag{2.75f}$$

where i_r, i_m, v_{Cr}, v_{co} are state variables and v_o and i_g are output variables.
Approximating the resonant currents and voltages with their fundamental harmonics:

$$i_r = i_{rs}(t)sin(w_{st}) + i_{rc}(t)cos(w_{st}) \tag{2.76a}$$

$$i_m = i_{ms}(t)sin(w_{st}) + i_{mc}(t)cos(w_{st}) \tag{2.76b}$$

$$v_{Cr} = v_{Crs}(t)sin(w_s t) + v_{Crc}(t)cos(w_{st}) \tag{2.76c}$$

Extended Describing function
The corresponding EDFs for the non linear equations are derived in [50] and obtained as:

$$f_1(v_g, d) = \frac{4}{\pi}sin(\pi d)v_g \tag{2.77a}$$

$$f_2(i_{rs} - i_{ms}, v_{co}) = \frac{4}{\pi}\frac{i_{rs} - i_{ms}}{i_p}v_{co} \tag{2.77b}$$

$$f_3(i_{rc} - i_{mc}, v_{co}) = \frac{4}{\pi}\frac{i_{rc} - i_{mc}}{i_p}v_{co} \tag{2.77c}$$

$$f_4(i_{rs} - i_{ms}, i_{rc} - i_{mc}) = \frac{2}{\pi}i_p \tag{2.77d}$$

$$f_5(i_{rs}, d) = \frac{2}{\pi}i_p \tag{2.77e}$$

where i_p is

$$i_p = \sqrt{(i_{rs} - i_{ms})^2 + (i_{rc} - i_{mc})^2} \tag{2.78a}$$

Where d is the duty cycle, set to a fixed value.

Harmonic balance
The frequency of the small signal perturbation is much lower than the switching frequency and the converter can be considered to be in steady state operation. (2.79)can be found by substituting (2.76) to(2.79) into (2.75) and rearranging the

coefficients of the sine, and cosine terms,

$$L_r(\frac{di_{rs}}{dt} - w_s i_{rc}) + v_{Crs} + L_m(\frac{di_{ms}}{dt} - -w_s i_{mc} = \frac{4}{\pi} sin(\pi d) v_g \tag{2.79a}$$

$$L_r(\frac{di_{rc}}{dt} + w_s i_{rs}) + v_{Crc} + L_m(\frac{di_{mc}}{dt} + w_s i_{ms}) = 0 \tag{2.79b}$$

$$L_m(\frac{di_{ms}}{dt} - w_s i_{mc}) = \frac{4}{\pi} \frac{i_{rs} - i_{ms}}{i_p} v_{co} \tag{2.79c}$$

$$L_m(\frac{di_{mc}}{dt} - w_s i_{ms}) = \frac{4}{\pi} . \frac{i_{rc} - i_{mc}}{i_p} v_{co} \tag{2.79d}$$

$$C_r(\frac{dv_{Crs}}{dt} - w_s v_{Crc}) = i_{rs} \tag{2.79e}$$

$$C_r(\frac{dv_{Crc}}{dt} - w_s v_{Crs}) = i_{rc} \tag{2.79f}$$

$$(1 + \frac{r}{R}) C_o \frac{dv_{co}}{dt} + \frac{1}{R_i} V_{co} = \frac{2}{\pi} i_p + i_o \tag{2.79g}$$

$$v_o = \frac{r.R}{r+R}(\frac{2}{\pi} i_p + i_o) + \frac{R}{r+R} v_{co} \tag{2.79h}$$

$$i_g = \frac{2}{\pi} i_{rs} sin(\pi d) \tag{2.79i}$$

In steady state operation the derivatives of the constant value state variables in (2.75) is zero.

Perturbation and linearization
By adding a small perturbation signal to the variables as v_g=v_g+$\hat{v_g}$, i_o=0+$\hat{i}_o$, d=D+$\hat{d}$, $\omega_s = \omega_s + \hat{\omega_s}$ and linearizing the equations, the small signal model of LLC converter can be represented as shown in Figure 2.31 [51].

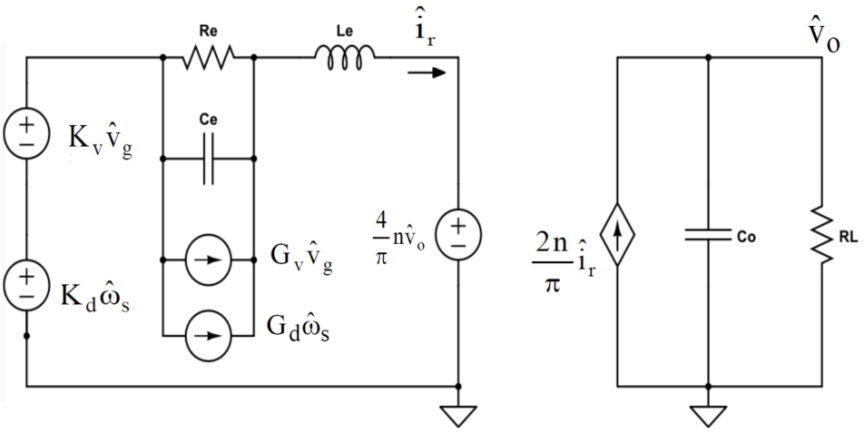


Figure 2.31: Small signal model of LLC resonant converter

For the switching frequency greater than or equal to the series resonant frequency,

the variables in the small signal model circuit is derived in [51] as

$$G_d = \frac{2V_g}{\pi}\frac{L_n}{w_o}\frac{1}{R_e}\left(\frac{\frac{1}{w_n}(\frac{1}{w_n^2}-w_n^2)(\frac{\pi^2}{8}QL_n)^2-(L_n+1-\frac{1}{w_n^2})(\frac{2}{w_n^3})}{\left[\sqrt{(L_n+1-\frac{1}{w_n^2})^2+(\frac{1}{w_n}-w_n)\frac{\pi^2}{8}QL_n)^2)}\right]^3}+\frac{2}{L_n^2}\right) \tag{2.80a}$$

$$G_v = \frac{1}{\pi}\frac{X_{eq}}{\sqrt{X_{eq}^2+R_{eq}^2}} \tag{2.80b}$$

$$K_d = \frac{4V_g}{\pi}\frac{1}{w_o L_n} \tag{2.80c}$$

$$K_v = \frac{4}{\pi^2}\frac{V_g L_n w_n}{R_{eq}}\frac{L_n+1-\frac{1}{w_n^2}}{\sqrt{(L_n+1-\frac{1}{w_n^2})^2+((\frac{1}{w_n}-w_n)\frac{\pi^2}{8}QL_n)^2}} \tag{2.80d}$$

$$L_e = (1+\frac{1}{w_n^2})L_r \tag{2.80e}$$

$$R_e = \frac{L_e X_{eq} w_s - w_o}{R_{eq}} \tag{2.80f}$$

$$C_e = \frac{1}{(w_s-w_o)^2} \tag{2.80g}$$

$$R_{eq} = \frac{8}{\pi^2}n^2 R_L \tag{2.80h}$$

$$X_{eq} = w_s L_r - \frac{1}{w_s C_r} \tag{2.80i}$$

$$L_n = \frac{L_m}{L_r} \tag{2.80j}$$

From (2.80) the transfer function of the LLC resonant converter for the switching frequency greater than the series resonant frequency can then be expressed as

$$\frac{\hat{V}_o(s)}{\hat{\omega}(s)} = G_d\frac{X_{eq}^2+R_{eq}^2}{(s^2L_e+sL_eR_{eq}+X_{eq}^2)(1+R_LC_os)+R_{eq}(sL_e+R_{eq})} \tag{2.81a}$$

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{n^2.R_L} \tag{2.81b}$$

For the switching frequency less than the series resonant frequency, the variables in

the small signal model circuit is derived in [51] as

$$G_d = \frac{2V_g}{\pi}\frac{L_n}{w_o}\frac{1}{R_e}\left(\frac{\frac{1}{w_n}(\frac{1}{w_n^2}-w_n^2)(\frac{\pi^2}{8}QL_n)^2-(L_n+1-\frac{1}{w_n^2})(\frac{2}{w_n^3})}{\left[\sqrt{(L_n+1-\frac{1}{w_n^2})^2+((\frac{1}{w_n}-w_n)\frac{\pi^2}{8}QL_n))}\right]^3}+\frac{2}{L_n^2}\right) \tag{2.82a}$$

$$G_v = \frac{1}{\pi}\frac{X_{eq}}{\sqrt{X_{eq}^2+R_{eq}^2}} \tag{2.82b}$$

$$K_d = \frac{2V_g}{\pi}\frac{L_n}{w_o}\frac{\left[(\frac{1}{w_n^2}-w_n^2)(\frac{\pi^2}{8}QL_n)^2-(L_n+1-\frac{1}{w_n^2})(\frac{2}{w_n^2})\right]\frac{1}{w_n}\cdot\frac{1}{sin(w_n\frac{\pi}{2})}+\left(\frac{-\pi}{2}\frac{cos(w_n\frac{\pi}{2})}{sin^2(w_n\frac{\pi}{2})}\right)}{\sqrt{(L_n+1-\frac{1}{w_n^2})^2+((\frac{1}{w_n}-w_n)\frac{\pi^2}{8}QL_n)^2}} \tag{2.82c}$$

$$K_v = \frac{2}{\pi}\frac{L_n}{sin(w_n\frac{\pi}{2})}\frac{1}{\sqrt{(L_n+1-\frac{1}{w_n^2})^2+((\frac{1}{w_n}-w_n)\frac{\pi^2}{8}QL_n\frac{1}{sin(w_n\frac{\pi}{2})})^2}} \tag{2.82d}$$

$$L_e = (1+\frac{1}{w_n^2})L_r+(1-w_n)L_m \tag{2.82e}$$

$$R_e = 0 \tag{2.82f}$$

$$C_e = \frac{1}{(w_s-w_o)^2} \tag{2.82g}$$

$$R_{eq} = \frac{8}{\pi^2}n^2R_L \tag{2.82h}$$

$$X_{eq} = w_sL_r-\frac{1}{w_sC_r} \tag{2.82i}$$

$$L_n = \frac{L_m}{L_r} \tag{2.82j}$$

From (2.82) the transfer function of the LLC resonant converter for the switching frequency less than the series resonant frequency can then be expressed as

$$\frac{\hat{V}_o(s)}{\hat{\omega}(s)} = G_d\frac{1}{1+\frac{s}{Q_pw_p}+\frac{s^2}{w_p^2}} \tag{2.83a}$$

$$Q_p = \frac{8n}{\pi^2}R_L\sqrt{\frac{C_o}{L_e}} \tag{2.83b}$$

$$w_p = \sqrt{\frac{1}{L_e\frac{\pi^2}{8n^2}C_o}} \tag{2.83c}$$

3
Method

3.1 Modeling of the selected AC/DC converter topologies

In order to model the AC/DC converter topology we can model the PFC stage and LLC stage separately. Some of the topologies of the PFC stage and LLC stage may not be compatible or practical which will be discussed later. Since the efficiency of the combined stage will be the multiplication of each individual topology, for a certain power range, if both stages achieve a higher efficiency, then the combined efficiency will be higher.

The voltage inputs of the AC/DC converter are 85-275V with 47 to 63Hz of frequency and the output is a DC voltage of 48V. The PFC and LLC converters topologies are going to studied separately and in the next chapter the loss distribution plots will be presented separately, and the efficiency of the cascaded topologies are presented together. Finally, based on analytical and simulation results, the topology comparison in terms of efficiency, cost and performance the topology selection will be made for around 500W, 1kW and around 2kW of power levels.

3.2 Modeling of the PFC stage

Many topologies can be implemented as a front-end rectifier. Based on the literature study, active boost, interleaved and bridgeless PFC topologies are going to be modeled and will be studied for further analysis in performance, efficiency and cost perspectives. Other topologies were deemed not suitable in this study.

As the efficiency of each topology depends on the type of components chosen, the same type of components that can function for the given power ranges should be chosen. This methodology will make it easier to understand the power loss of each component implemented in different topology and will simplify the efficiency comparison. The output of the front-end PFC will then be the input to the LLC converter.

The components chosen in this study can function properly for specifications listed in Table 3.1. Some of the loss calculations might consider a 230V input and 50Hz of frequency as a way of design. The input voltage range and frequency are chosen base on telecom requirement or universal input voltage range. The typical output

of the PFC stage is 400V, but the LLC design consider a certain voltage range as its input. The output power is the range at which this study is based and the switching frequency is chosen considering switching losses and size of passive devices. Table 3.1 summarizes the input and output specification of the PFC stage.

Table 3.1: Input and output specifications of PFC stage

Input Voltage	85-275	V
Output voltage	400	V
Grid Frequency	47-63	Hz
Output power	500-2000	W
Switching frequency	100	kHz

3.2.1 Diode bridge rectifier

The diode bridge for active boost and interleaved PFC topologies should be selected in such a way that it can handle the maximum current through it, when the voltage is minimum and the maximum voltage across its terminals. Furthermore, the on time resistance and the voltage drop across the diode that made up the bridge rectifiers should be considered. For minimum voltage input, 85V RMS, and maximum output power, 2000w and assuming converter efficiency of 98%, the average current through the diode can be calculated as

$$I_{in,avg} = \frac{2\sqrt{2}}{\pi}\frac{P_{o,max}}{V_{in,min}\eta} = 0.9\frac{2000}{85 \cdot 0.98} = 21.6A,$$

The average current capability of the bridge rectifier should then be at least 22A. Since the output voltage is 400, the bridge rectifier should block at least 400V. The selected diode bridge can block 560V of reverse voltage and has 25A average current flow capability which is suitable for simulation and loss analysis study.

The power loss in the diode bridge can be calculated using (2.5) and the datasheet information. For an output power of 1kW, assuming efficiency of 98%, and input of 230V RMS with 50Hz, the average and the RMS current will be 4A and 4.44A respectively. The forward voltage drop, V_f of the bridge rectifier per diode is around 0.9 around 4A and the forward resistance is around 0.025Ω at 26°C. Due to natural turn off the diodes in the bridge have a negligible reverse recovery losses.

$$P_{diode,c} = 2 \cdot (V_f I_{av} + R I_{rms}^2) = 8.2W.$$

The bridge rectifier loss can be done for different power rating and voltage input using the same procedure.

For bridgeless PFC, the average and RMS current are the same as active boost and interleaved PFC. But, as discussed in the previous chapter, the current return path is through body diode of one of the MOSFETs and through the slow diode. The loss due to the body diode will be discussed in MOSFET losses MOSFET losses. If roughly half of the current passes through the slow diode then, the power loss is

$$P_{slowdiode,c} = V_f I_{av} + R I_{rms}^2 = 1.93W.$$

3.2.2 Boost inductor

The inductor size mainly depends on the amount of ripple current allowed, and ripple current depends on the type of conduction mode of the PFC. Considering CCM, usually 15% to 40% of ripple current is considered for boost inductor design. In some designs, a small capacitor is connected right after the diode bridge to decrease the ripple current in the inductor[7].

Allowing 20% current ripple, the minimum inductor size for active boost and interleaved PFC can be calculated using (2.11) and for bridgeless using (2.12) which basically results in the same minimum inductor size of 257 μH. In the simulation a standard value of 300 μH is used in the simulation.

The core selection should be in such a way that the number of copper wire turn should result in the same inductance value. The core selection can be made through different methods. For this study, the core is selected from the supplier's, Magnetic-inc®, catalog based on Li_L^2, where L is inductance value and I_L peak inductor current. A powdered core of type Kool Mu with part number 0077071A7HT15 is selected. Table 3.2 shows the properties of the selected core.

Table 3.2: Main properties of selected core material

Inductance nH/T^2	OD Length [mm]	Le Path Length [mm]	Ae Cross Section [mm^2]	Ve Volume [mm^3]
80	33.66	81	86	7000

The number of turns to get 300μH can be calculated as

$$N = \sqrt{\frac{L}{Inductance}}$$

this yields a turn ratio of around 61.
The core loss can be determined from two curve fit equations from the core suppliers guide. The first one determines the maximum and minimum magnetic field strength, H, from the minimum and maximum currents through the inductor using

$$H = \frac{4\pi N I_L}{L_e} \tag{3.1}$$

where N is number of turns, I_L is inductor current and Le is the path length.
The second curve fit equation uses the magnetic the power density based on average magnetic flux density, B, of around 0.05T. This will give a power loss of 159.8mW per cubic centimeter at 1kW of power level. Multiplying this with the volume of the core Ve gives a core loss of around 1.12W. Other core materials like 3C95 are also evaluated using Steinmetz equation to give nearly the same results.

The copper loss of an inductor depends on the type of wire used. By choosing the type of inductor wire and determining its length, it is possible to determine its direct current resistance, DCR.

$$R_{DC} = M_{LT} N R_L \tag{3.2}$$

where M_{LT} is the mean length of turn, N is the number of turns and R_L is the resistance per unit length of the copper wire selected. AWG 18 wire is selected and it has 0.021 mΩ/m, the mean length of turn is nearly 6.3 cm/turn, which gives an R_{DC} of 80 mΩ.

In active boost and bridgeless PFC, the RMS current through the inductor is the same as the input RMS current which can be express as

$$I_{L,rms} = \frac{P_{out}}{\eta V_{in}} \tag{3.3}$$

For 1kW of power the conduction losses of the inductor in active boost and bridgeless PFC will be

$$P_{L,cond} = R_{DC} {I_{L,rms}}^2 = 1.57W$$

For interleaved PFC the input RMS current will be channeled into two separate legs which basically reduces the inductor's conduction loss by half.

3.2.3 MOSFET

The MOSFET losses are mainly switching and conduction losses. The conduction losses can be found by first calculating the RMS current through the MOSFET. For active boost and bridgeless PFC, which can be found by evaluating (2.16), for 1kW, of power which gives 2.64A. For interleaved PFC it will be 1.32A. The conduction loss of the active boost and bridgeless PFC gives 1.32W.

The switching frequency for active boost and bridgeless PFC is the same as system/converter frequency, 100kHz. For interleaved PFC, if the system frequency is assumed to be 100kHz, then the effective switching frequency will be doubled as the switches are 180° phase shifted from each other. To keep the same effective frequency of the switch, the system frequency of the interleaved PFC is 50kHz. Consequently, the switching losses remain the same in all the three PFC topologies while the conduction loss will be half in interleaved PFC and additional body diode losses are present in bridgeless PFC. The turn on and turn off switching losses, can be evaluated using (2.20) and (2.23) respectively and the parameters can be found from the datasheet.

For 1kW of power, the total switching loss for all three PFCs topologies gives 3.25W. The total loss comprised of switching loss, conduction loss, gate loss and body diode loss associated with the MOSFET gives 5W for active boost. For interleaved it is found to be 3.97W. For bridgeless PFC, since the return current flows though one slow diode and one body diode of the MOSFET, the MOSFET losses are 6.44W, which are higher than the MOSFET losses of active boost PFC.

3.2.4 Boost diode

The boost diode selection is also critical since its losses also impose additional losses into the MOSFET and output capacitor. Taking this into consideration, a low reverse recovery silicon carbide/SiC, boost diode is selected. The selected boost diode has a reverse blocking capability of 650V, and total capacitive charge, and voltage drop of 1.5V at 8A average current.

The total losses, can then be calculated using (2.26) and (2.5) to get 4.15W for the active boost and bridgeless PFCs. For the interleaved PFC, the switching losses remain the same and the conduction losses will be roughly half. Which gives a total power loss of 2.37W.

3.2.5 Output Capacitor

The size of the capacitor is calculated based on the equation explained in the theory chapter. The size of the capacitor is greatly affected by the power rating. For 1kW power based on hold up time requirement, using (2.27) of 20ms, the capacitor size becomes 490 μF and based on the ripple voltage requirement, using (2.28), considering 3% of voltage ripple the size becomes 497.4μF. The largest should be chosen as the minimum size of the capacitor. A 330μF Aluminum electrolyte capacitor is selected from Vishay. Two of these capacitors shall be connected up to 1kW and three of them shall be connected in parallel for 2kW.

Once the type of capacitor is selected, its losses can be calculated using (2.30). Connecting the capacitor in parallel reduces the capacitor loss by half and increases thermal performance. For 1kW, the capacitor power loss for the active boost and the bridgeless PFC is around 0.605W and for interleaved topology it becomes 0.340W. The difference is due to the reduction of RMS current in interleaved PFC.

Power losses from 200W to 2200W levels are computed using the same method as explained above. Table 3.3 summarizes the selected components in all the three PFC topologies. At 2kW of power the number of capacitors shall be increased to three in all topologies.

Table 3.3: Quantity of components used

Components	**Part no.**	**Active boost**	**Interleaved**	**Bridgeless**
Diode bridge	GBJ2508	4	4	2
MOSFET	R6020PNJ	1	2	2
Boost diode	FFSB0865A	1	2	2
Capacitor	MAL225957331E3	2	2	2
Inductor/core	0077071A7HT15	1	2	2
Total no. of components		9	12	10

The diode bridges in the bridgeless PFC are slow diodes and are not used for rectification purpose.

3.2.6 Simulation model of PFC

The simulation model used for determining the losses was developed in LTspice using the devices mention in the circuit components in Table 3.3. Some of the component's model were downloaded from the suppliers and some of them can be found in LTspice database. For the inductor, the LTspice model could not be found and the DC resistance calculated above were inserted into the inductor's default model and similarly, the ESR was inserted into the capacitors data in the LTspice default component model.

3.3 Modeling of LLC resonant converter

The input voltage of the LLC converter is the output of PFC stage which is 400V. Even if the output voltage of the PFC is assumed to be constant because of unknown reasons the voltage might fluctuate, so to insure safe operating area of the LLC stage an input range of 370-430V is considered to model the converter.

Table 3.4: Specification and design parameters

specification and Parameters	Value	Unit
DC bus voltage range V_{in}	370-430	V
Output voltage V_{out}	48	V
Rated output power $P_{o,rated}$	500-2000	W

To design an output voltage regulated variable energy transfer converter, a mathematical relationship between input and output voltage is a must. The LLC resonant converter operates in the vicinity of a series resonance which indicates that the circulating current can be assumed to be a pure sinusoidal of a single frequency.

The analysis is based on the First Harmonic Approximation method, in which only the fundamental harmonic component of the square wave input voltage is considered while ignoring the higher order harmonics to design the resonant converter. As long as the switching frequency is at, or close to, the resonant frequency the result obtained with this method is valid[37].

The voltage transfer function can then be developed with the FHA method, representing the LLC resonant converter with its AC equivalent circuit model as shown in Figure 3.1. All variables are referred to the primary side.

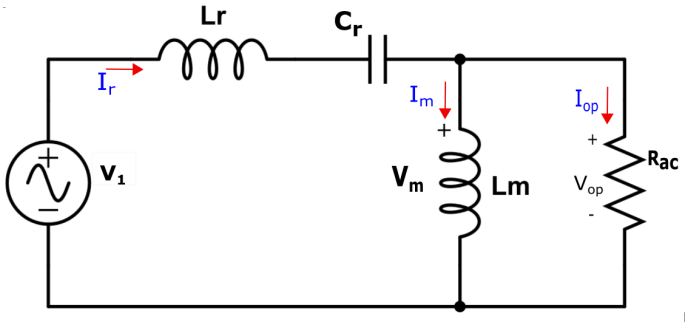


Figure 3.1: AC equivalent model of LLC resonant converter.

The RMS voltage on the input side is

$$V_1 = \frac{\sqrt{2}}{\pi} V_{in} \tag{3.4}$$

The RMS voltage on the output referred to the primary side is

$$V_{op} = \frac{2\sqrt{2}}{\pi} V_o \tag{3.5}$$

The RMS output current referred to primary is

$$I_{op} = \frac{\pi}{2\sqrt{2}} \frac{1}{n} I_o \tag{3.6}$$

The AC equivalent load resistance can be calculated as

$$R_{ac} = \frac{V_{op}}{I_{op}} = \frac{8n^2}{\pi^2} R_L \tag{3.7}$$

where n is the turns ratio of the transformer and it is given by

$$n = \frac{\frac{V_{in-nom}}{2}}{V_{o-nom}} \tag{3.8}$$

The input to output voltage gain function can be expressed in a normalized format to give a general description of design issues. To do this, inductance ratio, L_n, normalized frequency, f_n and quality factor, Q are define as follows:
Normalized frequency

$$f_n = \frac{f_{sw}}{f_o} \tag{3.9}$$

inductance ratio

$$L_n = \frac{L_m}{L_r} \tag{3.10}$$

quality factor of series resonant circuit

$$Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \tag{3.11}$$

The resonant frequency, f_o, is calculated as:

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.12}$$

The input-output transfer function can then be expressed as

$$M_g = |\frac{L_n f_n^2}{[(L_n+1)f_n^2 - 1] + j[(f_n^2 - 1)f_n Q L_n]}| \tag{3.13}$$

Depending on the load and gain requirements for a specific application, reasonable values of inductance ratio, L_n and quality factor, Q can be selected. Figure **??** shows how to how to select the value of the inductance ratio depending on our gain requirement. Figure 3.2 shows M_g and Q values for different inductance ratio, L_n.

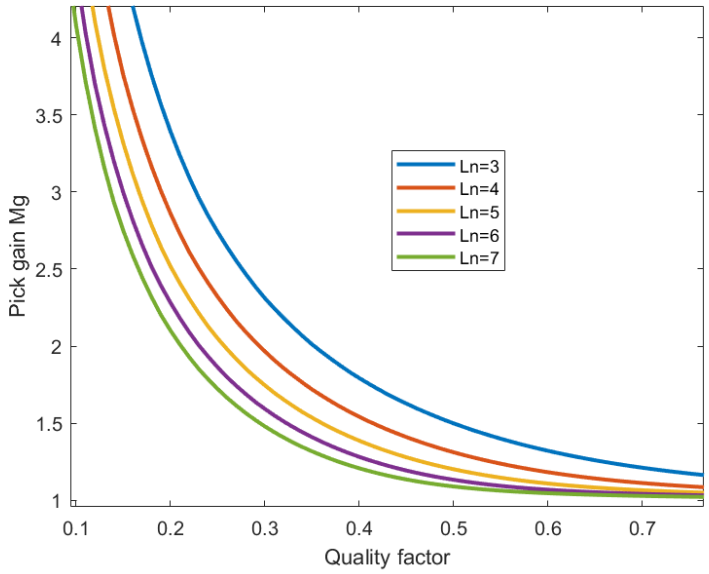


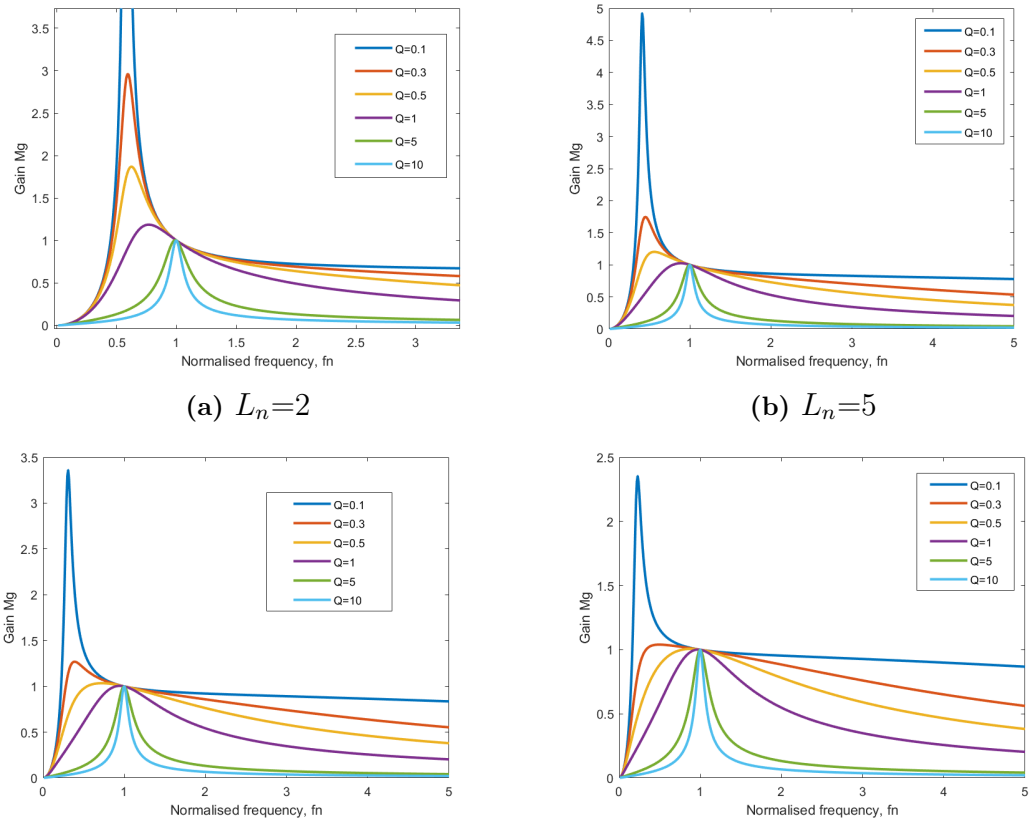
Figure 3.2: Inductance ratio, L_n, selection.

There is a trade of between higher and lower inductance ratio, L_n, selection. Higher inductance ratio means higher monetizing inductance, this has an advantage of having smaller circulating current in the resonant circuit which will help us to have higher efficiency, but this will lead to have low gain. To get the required gain we must go to a relatively low frequency.

On the other hand, smaller inductance ratio, L_n, has an advantage of higher boost gain and narrow frequency range. But this will increase the conduction loss, meaning at the end, reduce the efficiency. Therefore, an inductance ratio between L_n=4

and L_n=7 is practical and kind of optimum value to choose in this design.

A plot of voltage gain with respect to normalized frequency shown in Figure 3.3 is one good way to explain how the voltage gain behaves for different factors such as LLC tank parameters, switching frequency and load. A family of curves are presented in the same figure to show how the gain curve can be reshaped by changing Ln and Q. With the proper selection of the LLC tank parameters, it is possible to make the impedance of the tank inductive. As such, the primary side MOSFET zero voltage switching (ZVS) can be achieved over the complete range of operation.



(a) L_n=2 **(b)** L_n=5

(c) L_n=10 **(d)** L_n=20

Figure 3.3: Voltage gain vs normalized frequency at different inductance ratio values.

According to the different values of design parameters, $L_n = 5$ and $Q = 0.4$ is chosen for this design and the voltage gain curve of full bridge LLC resonant converter is shown in Figure 3.4. The voltage gain curve of half bridge is done essentially the same way except the value of the transformer ratio is different.

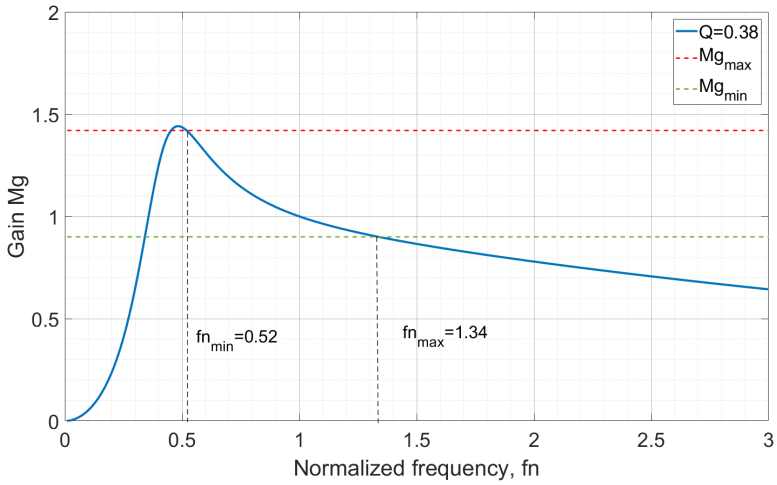


Figure 3.4: Voltage gain curve of full bridge LLC resonant converter

The normalized frequency, f_n. at the maximum gain cross or Mg_{max} in Figure 3.3 decides the minimum switching frequency we can have and f_n at the minimum gain cross or Mg_{min} in Figure 3.3 decides the maximum switching frequency we can have.

The design parameters are calculated according to the design equations and tabulated in Table 3.5 .

Table 3.5: Design parameters of LLC resonant converter

Parameters	**Values**	
	Half bridge LLC	**Full bridge LLC**
Magnetizing inductance, L_m	160μH	350μH
Series resonant inductor, L_r	30μH	60μH
Series resonant capacitor, C_r	60nF	30nF
Transformer turns ratio, n	4.16	8.33
Output capacitor, C_o	560μF	560μF
Resonant frequency, f_o	130 kHz	130 kHz

The size of the resonant inductor and capacitor is different for half bridge and full bridge LLC resonant converters. The resonant inductor and capacitor part numbers given in this table are for half bridge LLC resonant converter. However, this difference is considered to be negligible when comparing the number of components.

Table 3.6: Components used in the LLC resonant converter design

Components	Part no.	HB LLC	Int. HB LLC	FB LLC
Primary MOSFET	R6020PNJ	2	4	4
Transformer material	EQ30-3C94	1	2	1
Secondary MOSFET	R6020PNJ	2	4	2
Resonant capacitor	C0402C563K7PAC	1	2	1
Resonant inductor	DAMT2-26-11	1	2	1
Output capacitor	MAL225957331E3	1	1	1
Total no. of components		8	15	10

Int. HB LLC referes to interleaved half bridge LLC converter.

3.3.1 Simulation model of LLC

The simulation model used for determining the losses was developed in LTspice with the circuit components in Table 3.6 and circuit parameters in Table 3.5. The MOSFETs used are based on what is available in LT-spice database, they are not the best choice when it comes to MOSFET selection for LLC resonant converters, but they are still fine for topology comparison. One can model or search for other MOSFETs with low turn on resistance and low output capacitor value to have a good loss distribution with reduced power loss in the MOSFETs. Some of the components ESR values are taken from the LTspice and some are calculated and inserted into the inductor's default model.

4

Results

Three front end PFC topologies and three LLC resonant converter topology has been studied for their power loss distribution, efficiency, power density and cost. The analytical loss calculation models where developed and verified with simulation models. The results for the power loss distribution for the PFC stage and LLC stage are presented here, separately, and the efficiency graphs are plotted for the combination of selected PFC and LLC stages.

4.1 Loss distribution of the PFC stage

The losses in the converter were calculated using nearly a power factor of one. In order to determine the losses via simulation, the current waveform/the power factor should be acceptable, >0.98. At 230V and 1kW of power, which has a power factor of 0.9882, Figure 4.1 shows the input current and the supply voltage waveforms of this PFC. For the interleaved and bridgeless PFCs, the supply current waveforms can be found in the appendix.

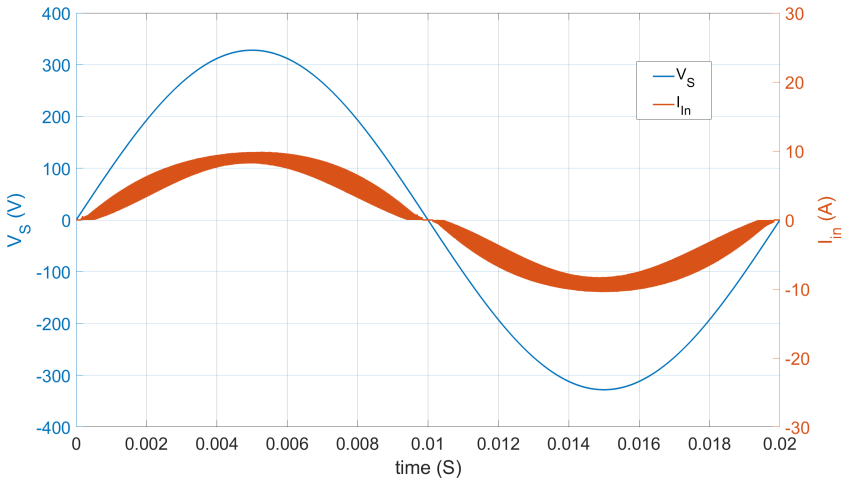
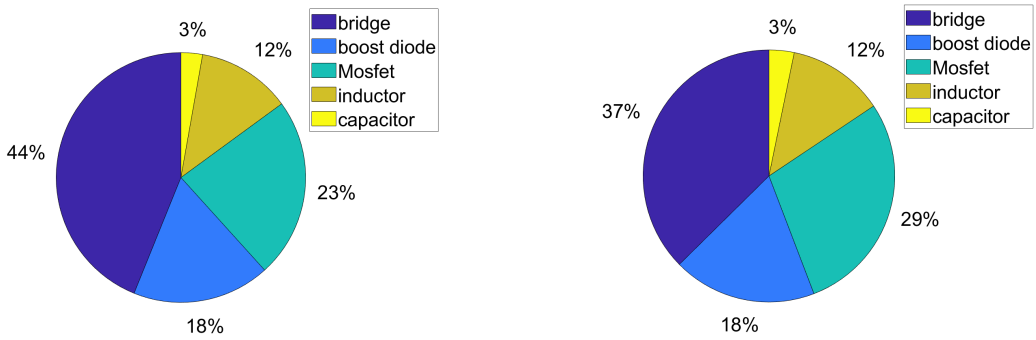


Figure 4.1: Current and voltage waveforms of active boost PFC at 1kW

The analytical and simulation results for the Active boost PFC show that the loss distribution in the converter is mainly because of the bridge rectifier and the MOSFET switch as shown in Figure 4.8. This similarity is common for all the three topologies of PFC. The results indicate that, as the load increases, the conduction

losses become dominant especially the bridge losses and the efficiency start to drop after 600W as shown in Figure 4.6. This is due to the reason that the conduction losses in the converter are related to the square of the current through the converter.



(a) analytical loss distribution **(b)** simulation loss distribution

Figure 4.2: Loss distribution of the active boost PFC

In LTspice, the power loss in a component can easily be found by integrating the voltage and current overlapping areas via built in LTspice functions. This can be done by; one, measuring the voltage across the component and the current through it and integrate the area and two, by holding left Alt key and clicking left mouse key on the component which the power loss is measured. Both methods give the same results and after measuring the power losses in each component a bar graph can be plotted. Figure 4.3 shows the quantitative power loss of each component in all the three topologies at 500W, via simulation.

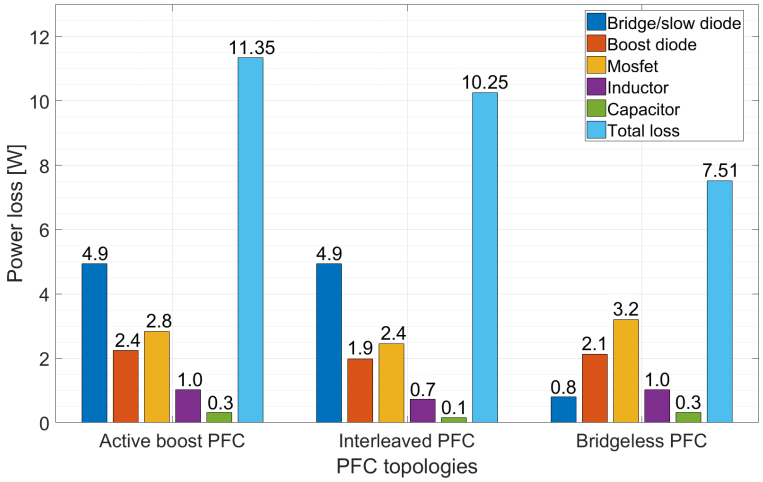


Figure 4.3: Power loss distribution at 500W

The power losses in the active boost PFC are higher since it has more components in the current direction and the interleaved PFC shows a reduced power loss as

compared with the active boost as it has two separate power channel which reduces the conduction losses. The bridgeless PFC has the lowest power loss as it has fewer number of components in the current flowing path.

Figure 4.4 shows the power loss distribution at 1kW. The results indicate that reduction of conduction losses in the MOSFET, inductor and boost diode is now more visible as compared with the results at 500W.

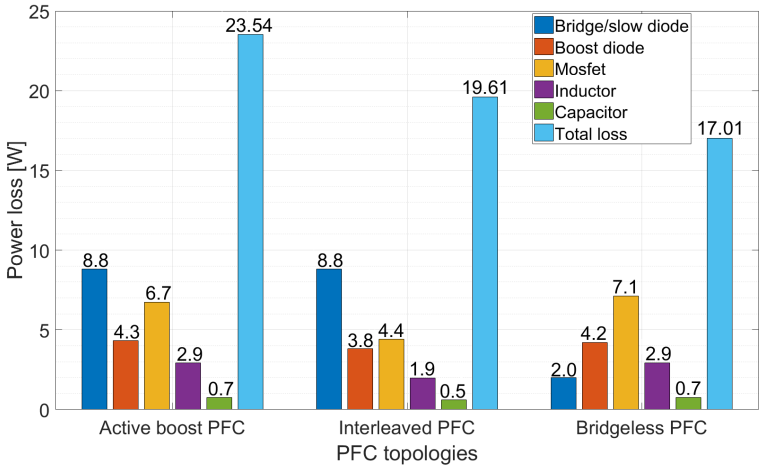


Figure 4.4: Power loss distribution at 1kW

As the power level increases the conduction losses become more evident and the losses in the active boost PFC becomes much higher as compared with the interleaved PFC as shown in Figure 4.5. This excessive power loss in the active boost PFC restricts the usage of this topology for higher power levels. The bridgeless PFC still shows less power losses due to the absence of the diode bridge. It has higher losses in the MOSFET as the body diode of the MOSFET carries nearly half of the reverse current.

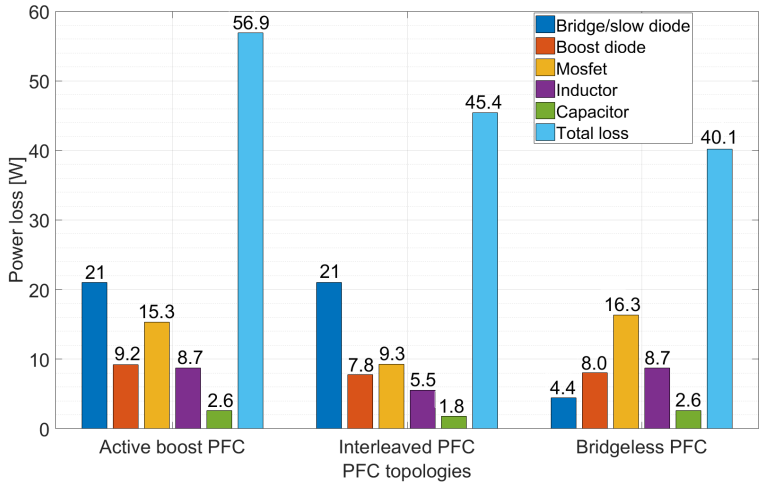


Figure 4.5: Power loss distribution at 2kW

Figure 4.6 shows the efficiency versus power plot of the three PFC topologies. The bridgeless PFC has better efficiency as compared to the other two. The efficiency for the active boost PFC starts to drop after 1kW since the conduction losses become more dominant. The result shows that there is a clear efficiency pattern for all three topologies and makes the topology comparison easier in terms of efficiency.

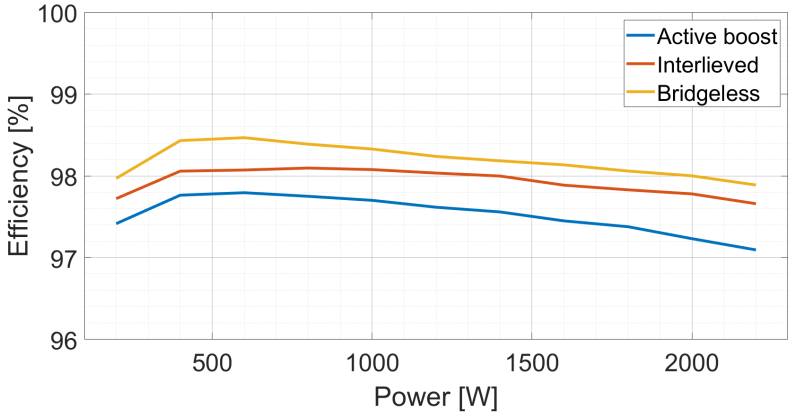


Figure 4.6: Efficiency versus power at 230V, RMS input

Another better way of comparing these PFC topologies is to keep the same power level and decreasing the supply voltage. This increases the current through the converters and helps to analyze the power losses more. This reveals the importance of using an interleaving approach, which became more advantageous if the input voltage level towards the low side i.e. 110V. At this voltage level the current through the converter becomes nearly double and the power losses became higher. In this scenario, using an interleaved PFC for power ranges between 1kW and 2kW becomes reasonable from efficiency perspective even if it has more number of components. Figure 4.7 shows the efficiency versus power plot of the three topologies at 110V input.

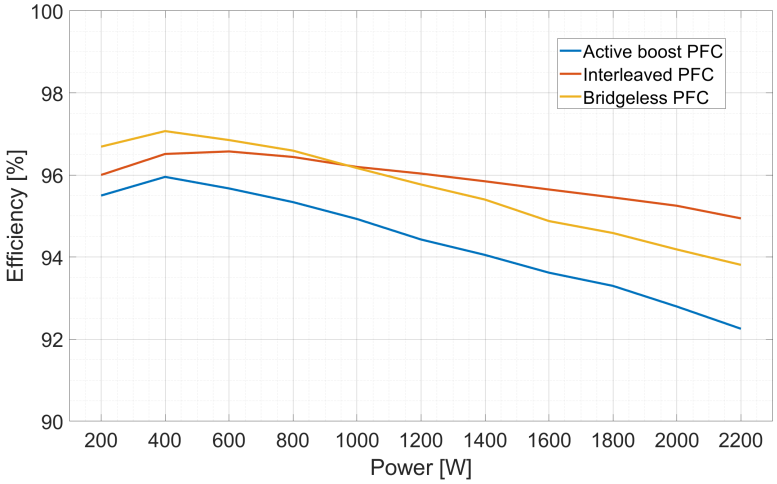


Figure 4.7: Efficiency versus power at 110V, RMS input

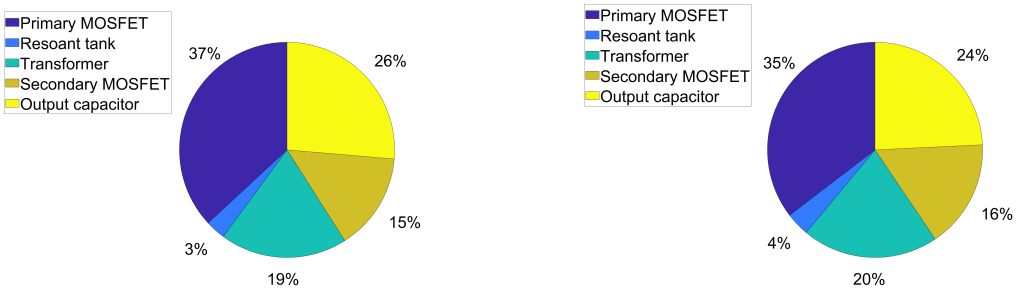
Table 4.1 summarizes the result of the three PFC topologies in terms of power factor and efficiency at 230V, RMS.

Table 4.1: Results of PFC converter topologies

PFC Topology	Power level (W)	PF	Efficiency (%)	Peak Eff. (%)
Active boost	500	0.9875	97.8	97.8@500W
	1000	0.9882	97.7	
	2000	0.9960	97.0	
Interleaved	500	0.9883	98.06	98.1@1000W
	1000	0.9946	98.1	
	2000	0.9954	97.8	
Bridgeless	500	0.9831	98.5	98.5@600W
	1000	0.9861	98.33	
	2000	0.9941	97.9	

4.2 Loss distribution of the LLC resonant converter

A small discrepancy can be observed between simulation and analytical results. Due to the non linear property of circuit components in the simulation, like MOSFETs and diodes, the same results cannot be achieved both in calculation and simulation. Figure 4.8a shows the analytical loss distribution and Figure 4.8b shows the simulation loss distribution of the full bridge LLC converter at 2kW.



(a) analytical loss distribution **(b)** simulation loss distribution

Figure 4.8: Loss distribution of Full bridge LLC converter at 2kW

The MOSFETs used are based on what is available in LT-spice. Due to their high output capacitance and turn on resistance it is observed that the MOSFET loss is dominant in all the topologies for all the three power levels. As can be seen from the power loss distribution at 500w shown in Figure 4.9, most of the power loss for all the three LLC resonant converters comes from the switching of the primary side MOSFETs.

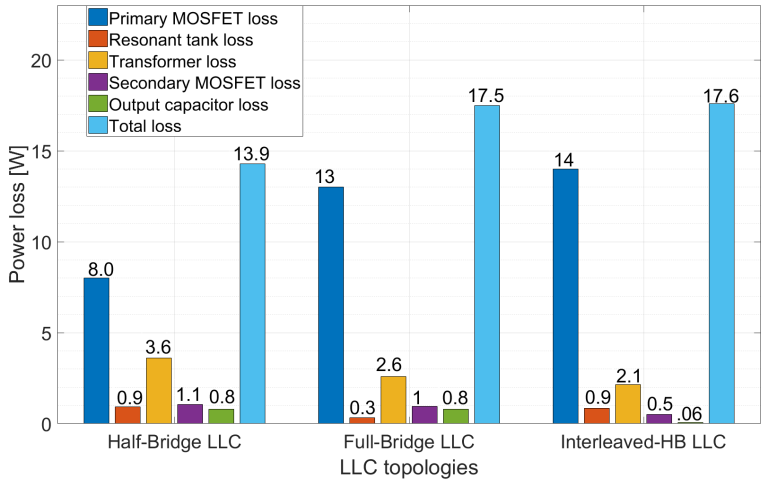


Figure 4.9: Power loss distribution of LLC resonant converter at 500W

As the load increases, the contribution from the conduction losses increases. The losses from the transformer winding and output capacitance gets higher. This is because of the reason that the resistance losses are directly related to the current. Figure 4.10 shows the power loss distribution at 1kW power level.

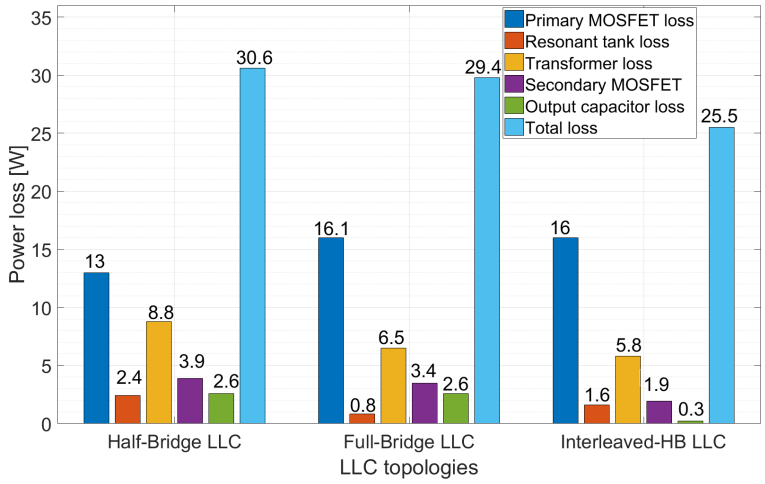


Figure 4.10: Power loss distribution LLC resonant converter at 1kW

Figure 4.11 The effect of conduction loss becomes more visible at 2kW. Especially, the loss reduction from the output capacitor with interleaved half bridge configuration as compared to the other two converter topologies becomes more visible. To improve the efficiency, it is of great importance to reduce the output capacitor losses with the parallel configuration of the half bridge LLC resonant converter.

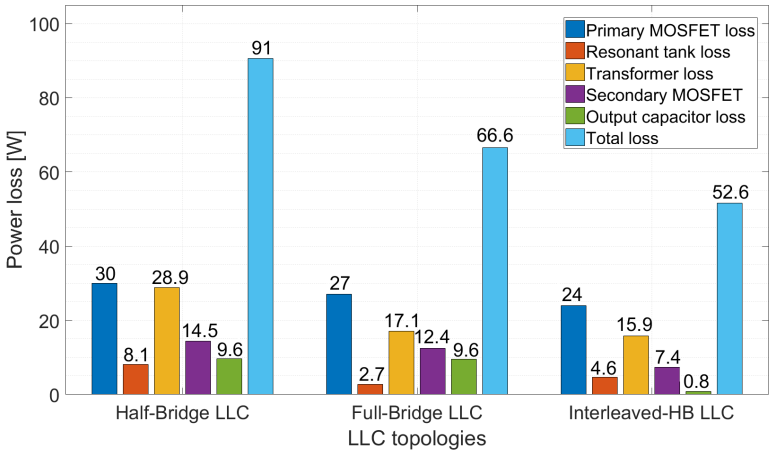


Figure 4.11: Power loss distribution of LLC resonant converter at 2kW

One way to compare the three LLC topologies for different power levels is the efficiency. Figure 4.12 shows the efficiency curves for the three LLC resonant converter topologies and the peak efficiency values of these topologies are summarized in Table 4.2 at the three power levels (500W, 1kW and 2kW). As can be seen from these curves, the half bridge LLC resonant converter has high efficiency at power levels below 800W and Interleaved has high efficiency at power levels above 1kW. The efficiency difference between full bridge and interleaved half bridge is more pronounced above 1.5kW power level.

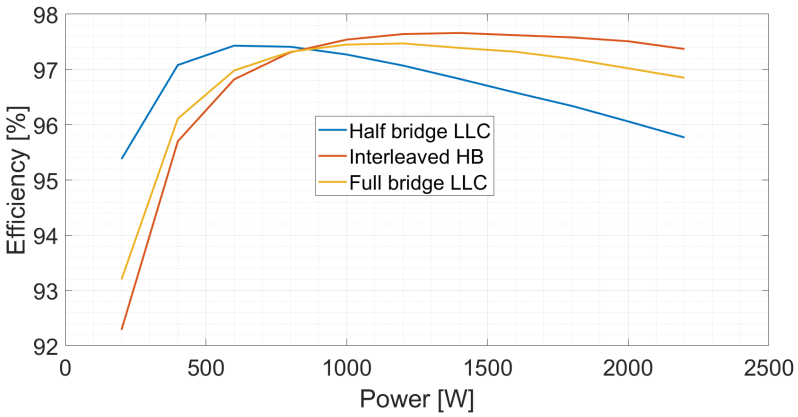


Figure 4.12: Efficiency versus power

Table 4.2: Results of LLC converter topologies

LLC Topology	Power level (W)	Efficiency (%)	Peak Eff. (%)
Half bridge	500	97.4	97.5@600W
	1000	97.3	
	2000	96	
Interleaved half bridge	500	96	97.7@1.4KW
	1000	97.55	
	2000	97.51	
Full Bridge	500	96.5	97.52@1.2KW
	1000	97.5	
	2000	97.1	

4.3 Cost

The cost of PFC and LLC stage can be compared by the count of components in each stage. For the PFC stage, active boost PFC has nine, the least, number of components but as compared with bridgeless PFC which has ten components. The interleaved PFC is not a cost effective PFC topology as compared with the other two as it has higher number of components.

For the LLC stage, half bridge LLC resonant converter is cheaper as compared with full bridge LLC resonant converter and interleaved half bridge is more expensive than the full bridge LLC resonant converter. But when it comes to efficiency, the half bridge, the full bridge and interleaved half bridge LLC resonant converters has better efficiency around 500W, 1kW and 2kW, respectively.

4.3.1 Investment cost

The bridgeless PFC has one more inductor, one more switch and two less diodes as compared with the active boost PFC. From electronics supplies like Digikey and Avent electronics accessed on date [23-05-2019] the critical circuit component price were found to be: diode 0.85$ MOSFET 2.35$ and for inductor 2.2$. These costs are per peace while purchasing 1000 of them at the same time. The total cost can then be estimated around 2.85$ higher than the active boost PFC.

4.3.2 Operating cost

The choice of PFC around 500W is a compromise between cost and efficiency. This thesis recommends the use of bridgeless PFC above 400W. The operating cost can determine how much money we can save by using this topology at 500W.

$$CF = \Delta\eta * P * Ep * Hrs \tag{4.1}$$

where P is the power level in kW, Ep is electric price in dollar per kWh and Hrs is the total number of hours per year. Then cash flow, CF becomes

$$= (0.985 - 0.978) * 0.5 * 0.12 * 24 * 365 = 3.68[\$/year]$$

this implies that using bridgeless PFC over active boost PFC at 500W saves nearly 35 Swedish Krona per year.

4.3.3 Net present worth

The net present worth, NPW, can be calculated using

$$NPW = \frac{CF}{(1+R)^i} - IC \tag{4.2}$$

where CF is cash flow, R is the discount rate assumed to be 20% and IC is investment cost. For 5 years, the NPW becomes

$$NPW = \frac{3.68}{(1+0.02)^5} - 2.85 = 0.48\$$$

If 100 converter printed circuit boards are produced per hour, assuming 8 hour shifts, for 46 production weeks per year and 5 working days per week gives

$$100[PCB/hr] * 8[hr] * 46[weeks/year] * 5[days/week] = 184,000[PCB/year]$$

With in one year of operation of this converter, the saving will be around 0.48*184,000= 88,320$. This cost can be divided to build additional converters and to be company's profit.

4.4 Power density

The power density of the selected topologies can be estimated by comparing the efficiency and size of the topologies. The bridgeless PFC is expected to have a high power density as compared with the other two. Its power density can be improved by implementing wide band gap switches.

The power density of resonant converters is relatively high as compared with other DC/DC converters since the switching frequency can be pushed higher as the switches achieve soft switching. Among the three LLC resonant converters, above 1200W the full bridge LLC resonant converter is expected to be higher than that of both half bridge and interleaved half bridge LLC resonant converters. Around 500W, the half bridge LLC resonance converter is expected to have high power density. The hardware should be developed for both PFC and LLC stages to determine the actual power density of this PFC.

4.5 Efficiency of the AC/DC converter

The efficiency of the selected topologies is cascaded together to give a two-stage AC/DC converter. Figure 4.13 shows a combined efficiency versus power plot for the combined converters. At power levels around 500W, 1kW and 2kW, the efficiency reaches 96.0%, 95.9% and 95.6% respectively.

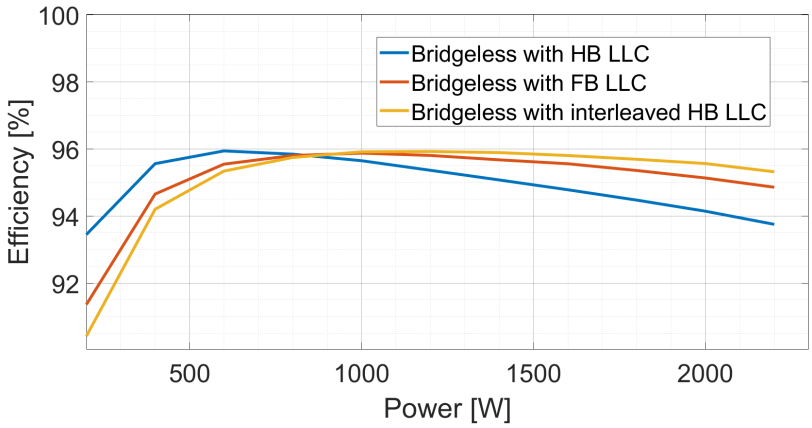


Figure 4.13: Efficiency versus power plot of the selected topology combinations

5
Conclusion

The main purpose of this study was to investigate promising, two stage AC/DC topologies. The six topologies selected from the literature study was further investigated in terms of efficiency, size and cost for power levels around 500W, 1kW and 2kW. From this study, it has been observed that, for the PFC stage, the bridgeless PFC is the most efficient as compared to the other two and is recommended for power levels $\geq$ 400W for high line input (230V) and the interleaved PFC is the most efficient with low line input (110V) for power levels $\geq$ 1kW. The active boost (classical boost) PFC was recommended for power levels $<$ 400W as a cost effective solution. For the DC/DC stage, the half bridge resonant converter was chosen to be efficient as well as cost effective for power levels around 500W. Similarly, the full bridge and interleaved half bridge LLC topologies are selected for power levels around 1kW and 2kW respectively. With the selected topologies, at 230V input, the two stage AC/DC converter has a peak efficiency of 96.0%, 95.9% and 95.6% for power levels around 500W, 1kW and 2kW respectively.

5.1 Future work

Analytical and simulation results are presented in this study. To verify these results further, a hardware should be developed to determine the actual efficiency and power density. The complete control method should also be developed for both PFC and LLC resonant converter stages. For power levels less than 400W, a critical or boundary conduction (BCM) and discontinues conduction modes can also be investigated since it's expected to have a higher efficiency, than continues conduction mode PFCs. The transformer design of the LLC stage is also something that should be given more attention since it's difficult to find a specific transformer from suppliers and custom design is usually needed.

Bibliography

[1] J. J. Lee, J. M. Kwon, E. H. Kim, W. Y. Choi, and B. H. Kwon, "Single-stage single-switch PFC flyback converter using a synchronous rectifier", *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1352–1365, 2008, ISSN: 02780046. DOI: 10.1109/TIE.2007.911908.

[2] A. Abramovitz, V. Yaskiv, and K. Smedley, "Power factor correction as the right step towards a safer environment", no. 3, pp. 244–246, 2013.

[3] P. Eve, F. R. Gomez, and E. Gao, "Trial of Super High Efficiency Rectifiers (98 %) in Telecom Networks", *2014 IEEE 36th International Telecommunications Energy Conference (INTELEC)*, pp. 1–5, 2014. DOI: 10.1109/INTLEC.2014.6972184. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=%7B%5C&%7Darnumber=6972184.

[4] "Guidelines to the standard EN 61000-3-2 Revision Date : 2010-04-06", no. April, pp. 1–9, 2010.

[5] N. M. O W, T. M. Undeland, W. P. Robbins, and J. Wiley, *POWER ELECTRONICS Converters, Applications, and Design THIRD EDITION*. 2003, ISBN: 9780471226932.

[6] O. semiconductor, "PFC Handbook", vol. 1, no. active power factor correction issues, 2011. [Online]. Available: https://www.onsemi.com/pub/Collateral/HBD853-D.PDF.

[7] T. Instruments, "1-kW , High Efficiency , Digital Power Factor Converter for Telecom and Server Power Supplies and Motor Drives Designed to Drive Wide Range of Downstream", no. November, 2015.

[8] L. Huber, Y. Jang, and M. M. Jovanovi, "Performance Evaluation of Bridgeless PFC Boost Rectifiers", no. February, 2013. DOI: 10.1109/TPEL.2008.921107.

[9] GaN Systems, "High Efficiency CCM Bridgeless Totem Pole PFC Design using GaN E-HEMT", *Reference design*, pp. 1–30, [Online]. Available: https://gansystems.com/wp-content/uploads/2018/01/GS665BTP-REF-rev170905.pdf.

[10] S. Sharifi, M. Babaei, and M. Monfared, "A High Gain Buck PFC Synchronous Rectifier", *26th Iranian Conference on Electrical Engineering, ICEE 2018*, pp. 1185–1190, 2018. DOI: 10.1109/ICEE.2018.8472575.

[11] T. Bang and J. W. Park, "Development of a ZVT-PWM buck cascaded buck-boost PFC converter of 2kW with the widest range of input voltage", *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2090–2099, 2018, ISSN: 02780046. DOI: 10.1109/TIE.2017.2739703.

[12] C. Shi, S. Member, H. Wang, S. Dusmez, and S. Member, "A SiC-Based High-Efficiency Isolated Onboard PEV Charger With Ultrawide DC-Link Voltage

Range", *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 501–511, 2017. DOI: 10.1109/TIA.2016.2605063.

[13] A. A. Fardoun, S. Member, E. H. Ismail, S. Member, A. J. Sabzali, and M. A. Al-saffar, "New Efficient Bridgeless Cuk Rectifiers for PFC Applications", *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3292–3301, 2012. DOI: 10.1109/TPEL.2011.2182662.

[14] M. Mahesh and A. K. Panda, "A High Performance Single-Phase AC-DC PFC Boost Converter with Passive Snubber Circuit", *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2888–2894, 2012. DOI: 10.1109/ECCE.2012.6342370.

[15] C.-e. Kim, D.-k. Yang, J.-b. Lee, and G.-w. Moon, "High-Efficiency Two-Inductor PFC Boost Converter Employing SPDT Relay", *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 2901–2904, 2015. DOI: 10.1109/TPEL.2014.2368567.

[16] F. Musavi, "A Phase Shifted Semi-Bridgeless Boost Power Factor Corrected Converter for Plug in Hybrid Electric Vehicle Battery Chargers",

[17] S. Ortmann, "Three-Level Single-Phase Bridgeless PFC Rectifiers", vol. 30, no. 6, pp. 2935–2949, 2015. DOI: 10.1109/TPEL.2014.2322314.

[18] J. Biela, J. W. Kolar, and I. Technologies, "Optimal Design of a Compact 99 . 3 % Efficient Single-Phase PFC Rectifier", *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1397–1404, 2010. DOI: 10.1109/APEC.2010.5433412.

[19] M.-h. Park, J.-i. Baek, J.-k. Han, C.-y. Lim, and G.-w. Moon, "ZVS Interleaved Totem-pole Bridgeless PFC Converter with Phase-shifting Control", *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pp. 3533–3537, 2018. DOI: 10.23919/IPEC.2018.8507373.

[20] J. Shao and E. Jianwenshaowolfspeedcom, "Analog Based High Efficiency 2KW Totem Pole PFC Converter Using Surface Mount SIC MOSFET ' s 2 . Totem Pole PFC Topology", no. June, pp. 5–7, 2018.

[21] J. C. Hernandez, L. P. Petersen, and M. A. E. Andersen, "A Comparison between Boundary and Continuous Conduction Modes in Single Phase PFC Using 600V Range Devices", *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, no. June, pp. 1019–1023, 2015. DOI: 10.1109/PEDS.2015.7203487.

[22] G. Koen De, V. de Sype, David M, and A. P., "Sample correction for digitally controlled boost pfc converters operating in both ccm and dcm", *IEEE Transactions on Power Electronics*, vol. 1, 203. [Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=%7B%5C&%7Darnumber=1179243.

[23] M. Shanthi and R. Seyezhai, "A Comparative Analysis of Bridgeless Power Factor Correction (Pfc) Ac-Dc Converter Topologies For Battery Charging Applications", vol. 3, no. 8, pp. 210–222, 2015.

[24] M. O. Loughlin, "UCC28070 300-W Interleaved PFC Pre-Regulator Design Review", no. August 2008, pp. 1–27, 2010. [Online]. Available: http://www.ti.com/lit/an/slua479b/slua479b.pdf.

[25] G. Rafael and Z. Florian, "Infineon Technologies - General description and Evaluation of 3kw bridgeless PFC", [Online]. Available: https://www.infineon.com/dgdl/Infineon-General%7B%5C_%7Ddescription%7B%5C_%7DEVAL%7B%5C_%7D3KW%7B%5C_%7DDB%7B%5C_%7DPFC%7B%5C_%7DC7-ATI-v01%7B%5C_%7D00-EN.pdf?fileId=.

[26] S. Abdel-rahman, "PFC boost converter design guide", 2016. [Online]. Available: https://www.infineon.com/dgdl/Infineon-ApplicationNote%7B%5C_%7DPFCCCMBoostConverterDesignGuide-AN-v02%7B%5C_%7D00-EN.pdf?fileId=.

[27] Magnetics Inc., *Magnetics - Inductor Cores: Material and Shape Choices*, 2019. [Online]. Available: https://www.mag-inc.com/Design/Design-Guides/Inductor-Cores-Material-and-Shape-Choices.

[28] A. Keith, "EMC Standards, EMC design of Switching Power Converters - Part 1", vol. 44, no. 0, [Online]. Available: https://www.emcstandards.co.uk/files/1%7B%5C_%7Demc%7B%5C_%7Ddesign%7B%5C_%7Dof%7B%5C_%7Dswitching%7B%5C_%7Dpower%7B%5C_%7Dconverters%7B%5C_%7Dintroduction.pdf.

[29] H. Raee, A. Rabiei, and T. Thirnger, "Analytical prediction of switching losses in MOSFETs for variable drain-source voltage and current applications", vol. 1, 2013.

[30] Illinoins Capacitors Inc, "Impedance , Dissipation Factor and ESR", no. 847, pp. 1–2,

[31] C. Basso, "Small-Signal Modeling of the Boost Converter Operated in CM Non-Linearity in a Switching Converter", *Energy efficient innoventions*, [Online]. Available: http://cbasso.pagesperso-orange.fr/Downloads/PPTs/Boost%20CCM%20DCM%20CM.pdf.

[32] Y. Ohta, K. Higuchi, and K. Chamnongthai, "Robust Digital Control for a PFC Boost Converter", vol. 10, no. 2, pp. 164–172, 2012.

[33] A. Villarruel-parra, A. J. Forsyth, and S. Member, "Enhanced Average-Value Modeling of Interleaved DC – DC Converters Using Sampler Decomposition", *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2290–2299, 2017. DOI: 10.1109/TPEL.2016.2559449.

[34] F. Semiconductor, "Average Current Mode Interleaved PFC Control", 2016. [Online]. Available: https://www.nxp.com/docs/en/application-note/AN5257.pdf.

[35] G. E. Mejía-ruiz, N. Muñoz-galeano, and J. M. López-lezama, "Modeling and development of a bridgeless PFC Boost rectifier", no. 82, 2017. DOI: 10.17533/udea.redin.n82a02. [Online]. Available: https://pdfs.semanticscholar.org/3a38/f619013185f0bdcfe12ab2e4ae371e8ad35b.pdf.

[36] M. Steve, "Power converter topology trends", *Fairchild*, 2014.

[37] H.-i. Hsieh, "Performance Study of High-Power Half-Bridge Interleaved LLC Converter", *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, vol. 1, pp. 123–129, 2018. DOI: 10.23919/IPEC.2018.8507942.

[38] D. Fu, "Topology Investigation and System Optimization of Resonant Converters", *Optimization*, 2010.

[39] Y.-k. Lo, C.-y. Lin, M.-t. Hsieh, and C.-y. Lin, "Converters for Wide Load Variations", *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2572–2575, 2011. DOI: 10.1109/TIE.2010.2058076.

[40] X. D. Gumera and I. Member, "Design and Implementation of a High Efficiency Cost Effective EV Charger Using LLC Resonant Converter", 2017.

[41] S. Alois, D. D. Francesco, C. Johnald, and S. Franz, "Infineone technologies, Half Bridge LLC Evaluation Board with 600V Cool MOS", [Online]. Available: https://www.infineon.com/dgdl/Infineon-ApplicationNote%7B%5C_%7DEVAL%7B%5C_%7D600W%7B%5C_%7D12V%7B%5C_%7DLLC%7B%5C_%7DC7%7B%5C_%7Dwith%7B%5C_%7D600V%7B%5C_%7DC7%7B%5C_%7DXMC-AN-v01%7B%5C_%7D00-EN.pdf?fileId=.

[42] R. Chen and S.-y. Yu, "A High-efficiency High-power-density 1MHz LLC Converter with GaN Devices and Integrated Transformer", *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 791–796, 2018. DOI: 10.1109/APEC.2018.8341102.

[43] J. Lu, S. Member, A. Khaligh, and S. Member, "Converter : Comparison between Phase-Shifted Full-Bridge and LLC Resonant Converters", *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, pp. 275–280, 2017. DOI: 10.1109/ITEC.2017.7993284.

[44] A. Amirahmadi, M. Domb, and E. Persson, "High Power Density High Efficiency Wide Input Voltage Range LLC Resonant Converter Utilizing E- Mode GaN Switches", *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 350–354, 2017. DOI: 10.1109/APEC.2017.7930716.

[45] H.-i. Hsieh, "Performance Study of High-Power Half-Bridge Interleaved LLC Converter", *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, vol. 1, pp. 123–129, 2018. DOI: 10.23919/IPEC.2018.8507942.

[46] C. Liu, S. Member, B. Gu, S. Member, and J.-s. Lai, "High-Efficiency Hybrid Full-Bridge – Half-Bridge Converter With Shared ZVS Lagging Leg and Dual Outputs in Series", *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 849–861, 2013. DOI: 10.1109/TPEL.2012.2205019.

[47] U. Kundu, K. Yenduri, and P. Sensarma, "Accurate ZVS analysis for magnetic design and efficiency improvement of full-bridge LLC resonant converter", *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1703–1706, 2017, ISSN: 08858993. DOI: 10.1109/TPEL.2016.2604118.

[48] C. H. Liang, T. J. Liang, K. H. Chen, and H. W. Liang, "Design and implementation of interleaved LLC half-bridge resonant converters", *Proceedings - 2014 International Power Electronics and Application Conference and Exposition, IEEE PEAC 2014*, pp. 1509–1512, 2014. DOI: 10.1109/PEAC.2014.7038089.

[49] C.-H. Yang, T.-J. Liang, K.-H. Chen, J.-S. Li, and J.-S. Lee, "Loss analysis of half-bridge LLC resonant converter", pp. 155–160, 2014. DOI: 10.1109/ifeec.2013.6687496.

[50] C. H. Chang, E. C. Chang, C. A. Cheng, H. L. Cheng, and S. C. Lin, "Small signal modeling of LLC resonant converters based on extended describing function", *Proceedings - 2012 International Symposium on Computer, Consumer and Control, IS3C 2012*, pp. 365–368, 2012. DOI: 10.1109/IS3C.2012.99.

[51] S. Tian, F. C. Lee, and Q. Li, "Equivalent circuit modeling of LLC resonant converter", *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2016-May, pp. 1608–1615, 2016. DOI: 10.1109/APEC.2016.7468082.

A

Appendix 1

For active boost PFC the voltage and current compensator are designed in MATLAB siso tool for power loss measurement purpose. The same can be developed for interleaved and bridgeless PFCs using similar method. The cross over frequency for current controller is one tenth of the switching frequency, 10kHz and the phase margin is 60° for fast response. The current to duty transfer function can is given as

$$G_i(s) = \frac{\hat{i_L}}{\hat{d}} = \frac{2V_o}{R_L(1-D)^2} \frac{1 + \frac{sCR_L}{2}}{1 + \frac{sL}{R_L(1-D)^2} + \frac{s^2LC}{(1-D)^2}} \tag{A.1}$$

with current compensator of the form

$$G_{cc} = k_{pi} + \frac{k_{ii}}{s} \tag{A.2}$$

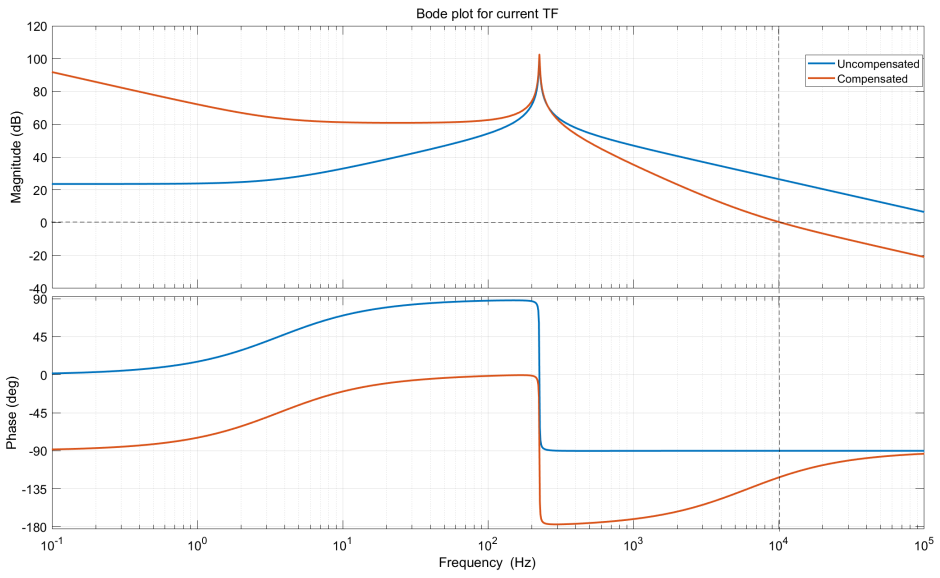


Figure A.1: current to duty transfer function bode plot

For voltage controller, as it should be slow, the cross over frequency is around 7Hx and its phase margin is 60°. The voltage transfer function is given as

$$G_v(s) = \frac{\hat{v_o}}{\hat{i_L}} = \frac{V_o(1-D) + sLI_L}{sCV_o + 2(1-D)I_L} \tag{A.3}$$

with voltage compenstor of the form

$$G_{cc} = k_{pv} + \frac{k_{iv}}{s} \tag{A.4}$$

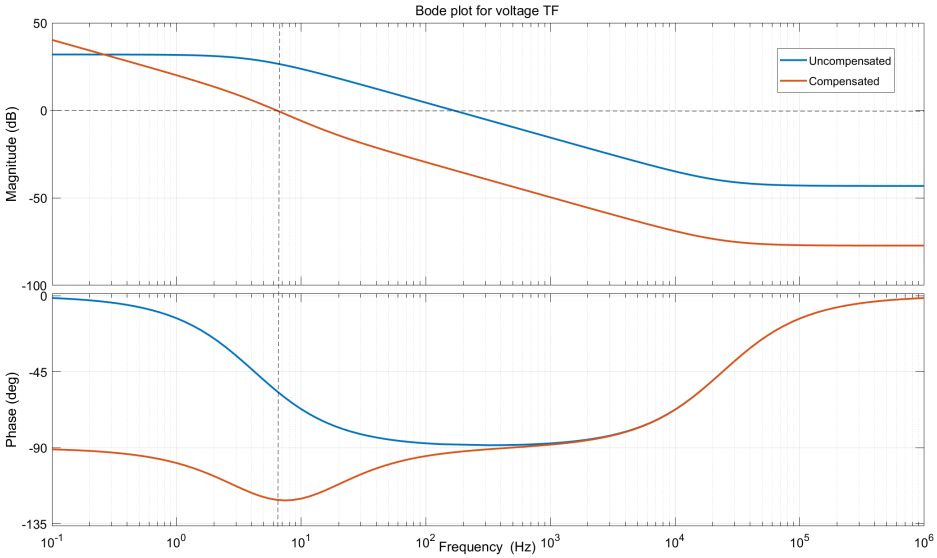


Figure A.2: current to voltage transfer function bode plot

Figure A.3 show the open loop and closed loop bode plots of the inner current controller and outer voltage controller.

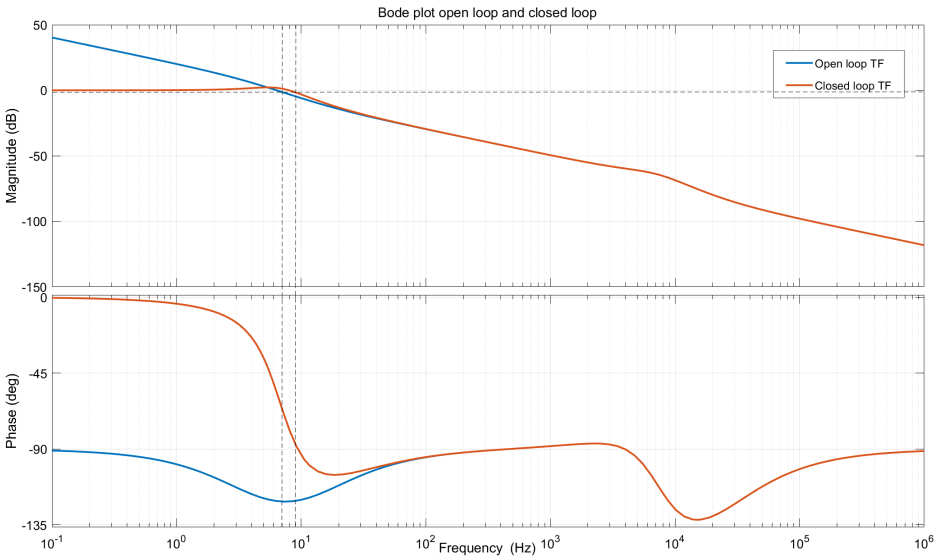


Figure A.3: Open loop and closed loop bode plots of active boost PFC

Figure A.4 shows current and voltage waveforms of interleaved PFC. The current ripple cancellation can be seen in the current waveforms four times in one period. This is when the duty cycle is 0.5.

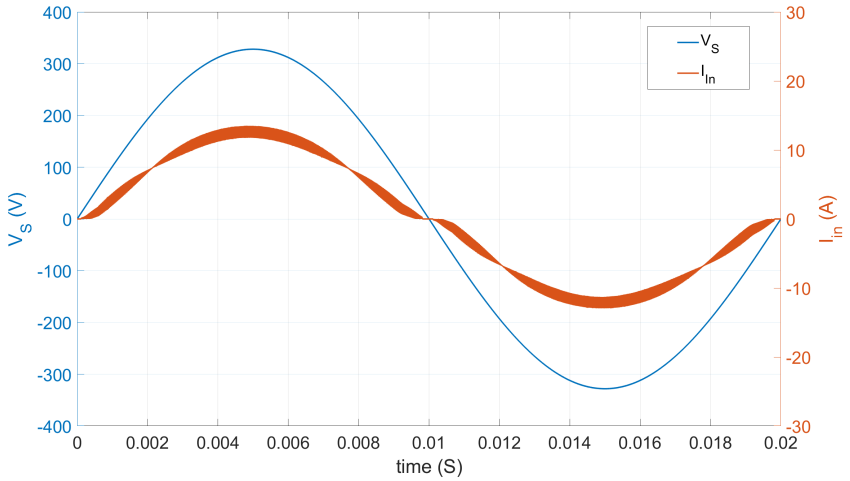


Figure A.4: Current and voltage waveforms of interleaved PFC at 2kW

Figure A.5 shows current and voltage waveforms of bridgeless PFC at 2kW. The simulation model uses two different controller for positive and negative AC cycles.

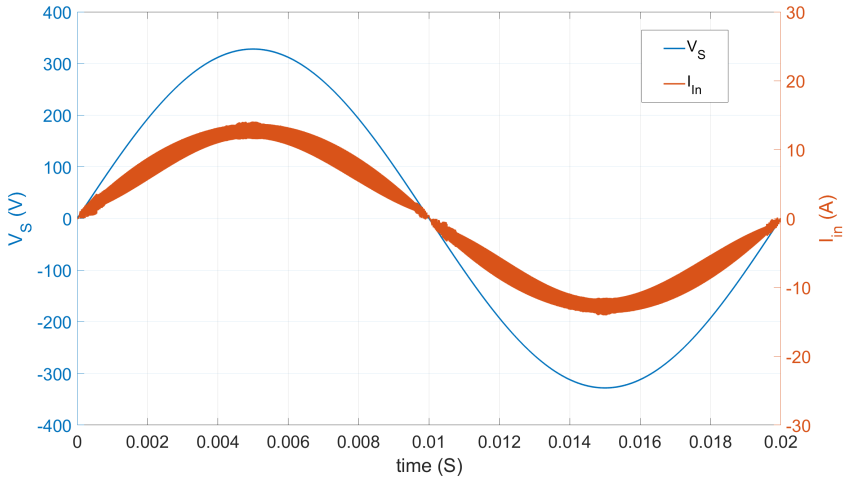


Figure A.5: Current and voltage waveforms of bridgeless PFC at 2kW