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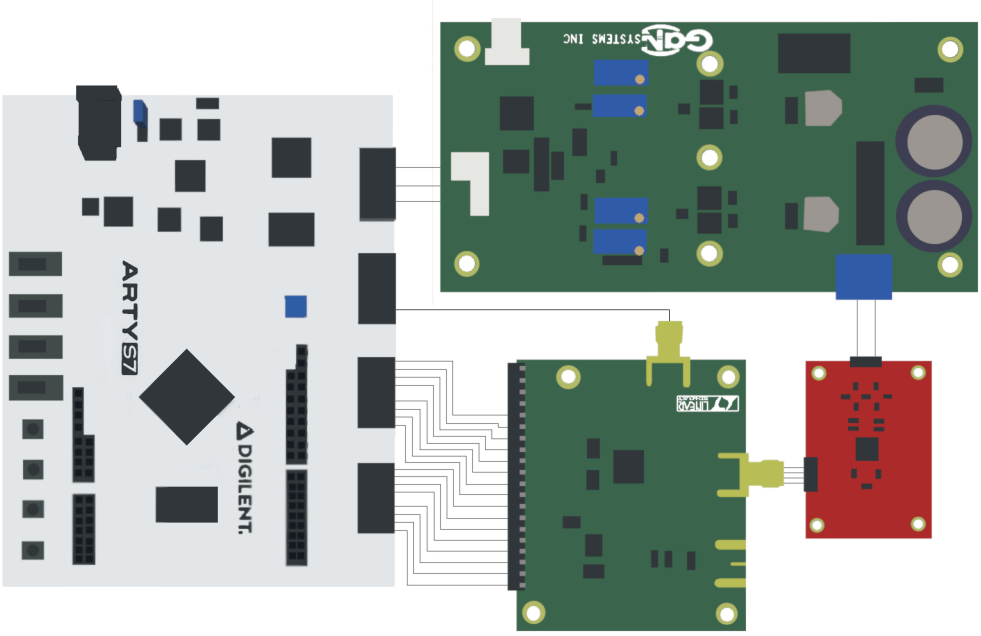

GaN Transistor Based Digital Class-D Amplifier with Global Feedback

Denis Hafizovic & Magnus Karlsson

Department of Electrical Engineering
Division of Electric Power Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2020

Master's thesis 2020

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Abstract

The class-D amplifier is a common type of amplifier in both low and high power applications, but they still most often use an analog signal path. A digital input class-D amplifier could reduce component count, increase flexibility, and possibly reduce noise and distortion. Furthermore, new GaN semiconductor technology has the potential of increasing the switching frequency in class-D amplifiers, thus allowing better noise performance. In this work, a fully digital class-D amplifier using gallium-nitride transistors with global feedback is designed and implemented. The system uses Sigma-Delta modulation to quantize the 24-bit input audio into a 5-bit signal that sets the pulse width of a three-level pulse width modulator with a switching frequency of 2 MHz. The proposed modulation technique offers very low noise and distortion in the audio band and keeps switching harmonics as low as possible. The high switching frequency allows for a higher cutoff frequency LC-filter, which is built using air-core inductors to eliminate distortion from core saturation. The high cutoff frequency yields a system frequency response, which has a phase distortion of less than 3 ° in the audio band. The output signal is fed back with a high-resolution analog to digital converter with a sample rate at least as high as the pulse width modulation switching frequency. The controller is designed to create a Chebychev noise transfer function, which ensures suppression of noise and distortion of at least 35 dB in the whole audio band. The proposed system has a THD of as low as 0.005 % and a THD+N of 0.02 %. Clock jitter in the design is believed to limit the noise performance of the system, which could be significantly improved with a redesign of the clock network.

Keywords: Class-D, Amplifier, PWM, Noise shaping, THD, GaN, Chebychev, ADC, digital

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This work has taken place at the Division of Power Engineering of the Department of Electrical Engineering at Chalmers University of Technology in collaboration with Lab Gruppen.

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Denis Hafizovic & Magnus Karlsson, Gothenburg, June 2020

Contents

1 Introduction **1**
- 1.1 Problem statement . . . 2
- 1.2 Scope . . . 2
- 1.3 Disposition . . . 3

2 Class-D amplifiers, signal modulation, and feedback **5**
- 2.1 Class-D Audio Amplifiers . . . 5
  - 2.1.1 Lowpass Filter . . . 6
  - 2.1.2 Core Saturation . . . 7
- 2.2 The GaN transistor . . . 9
  - 2.2.1 Two-Dimensional Electron gas (2DEG) . . . 10
  - 2.2.2 GaN Transistor Structure . . . 11
  - 2.2.3 Environmental Impacts of GaN . . . 12
- 2.3 Transistor switching behavior . . . 13
  - 2.3.1 Turn-on and turn-off . . . 13
  - 2.3.2 Power Losses . . . 15
- 2.4 Modulation technique . . . 16
  - 2.4.1 Interpolation . . . 16
  - 2.4.2 Quantization . . . 17
  - 2.4.3 Sigma-Delta Modulators . . . 21
  - 2.4.4 Higher Order Sigma-Delta Modulation . . . 22
  - 2.4.5 Pulse width modulation . . . 23
  - 2.4.6 Feedback system . . . 25
  - 2.4.7 Loop filter design . . . 26
  - 2.4.8 Higher order loop filters . . . 27
  - 2.4.9 Sampling of a PWM signal . . . 28
  - 2.4.10 Clock jitter in PWM signals . . . 29
  - 2.4.11 Blanking time distortion . . . 29

3 Design and implementation **31**
- 3.1 Power stage . . . 31
- 3.2 Sigma-Delta Modulator . . . 34
- 3.3 Pulse Width Modulator . . . 35
- 3.4 Linearization and discretization . . . 36
- 3.5 Loop filter design . . . 38
- 3.6 Voltage divider and anti-aliasing filter . . . 41

4 Digital hardware design **43**
4.1 Clock generation 44
4.2 Downsampling 44
4.3 Loop filter 45
4.4 Sigma-Delta modulator 46
4.5 Pulse width modulator 46
4.6 Pipeline 47
4.7 Upsampling 48
4.8 FPGA Resource utilization 48

5 Prototype Performance **51**
5.1 Frequency response 51
5.2 Noise and distortion performance 52
5.3 Efficiency 55

6 Conclusion and further development **57**
6.1 Further development 57

Bibliography **59**

List of Abbreviations

2DEG	Two-Dimensional Electron gas
ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
DAC	Digital to Analog Converter
DSP	Digital Signal Processing
E-HEMT	Enhancement Mode High Electron Mobility Transistor
FET	Field Effect Transistor
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
IIR	Infinite Impulse Response
MAC	Multiply Accumulate
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PCB	Printed Circuit Board
PCM	Pulse-Code Modulation
PWM	Pulse Width Modulation/Modulator
SDM	Sigma Delta Modulation/Modulator
SNR	Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion plus Noise
VHDL	Very High Speed Integrated Circuit Hardware Description Language

1

Introduction

For several decades, class-D amplifiers have been widespread throughout both industry and research. The inherently low efficiency in linear amplifiers [1] is not suitable for very low or high power applications, which is why many integrated amplifiers and high power touring amplifiers are now class-D.

When the class-D amplifier was invented, the audio input signal was analog [2]. The audio went through an analog modulation stage that converted the analog signal into a binary switching signal. Today, the audio in audio amplifiers often go through digital signal processing (DSP) stages before being amplified. After the DSP stages, the audio signal is conventionally converted into an analog signal via a digital to analog converter (DAC) before being sent to the power amplifier.

Since a binary switching signal is closely related to a digital signal, the modulation can efficiently be done in the digital domain instead of the analog domain. By performing the modulation in the digital domain, the need for a DAC in the signal path is removed, and it also reduces the noise and distortion inherent in analog circuitry.

Digital input class-D amplifiers have been studied carefully during the last couple of decades. Most, however, are of open-loop type, which means that there is no feedback. Feedback in audio amplifiers is most important [3] since distortion is unacceptable in professional audio equipment. Attempts have been made to introduce feedback in low power digital input amplifiers with promising results [3–6]. Common in most previous work is a switching frequency of far below 1 MHz.

The Gallium-Nitride (GaN) transistor has been used in radio-frequency (RF) applications since 2004, and the first GaN transistor which was designed to replace the Silicon MOSFET was launched in 2009 [7]. The GaN transistor has many benefits when compared to the Silicon MOSFET. First of all, it has a lower on-resistance when compared to a Silicon MOSFET of the same size, which makes the GaN transistor more efficient during on-state [8, 9]. Furthermore, the structure of the GaN-FET makes for a device with a low input capacitance, which allows for very high switching frequencies [7]. Higher switching frequencies can increase the Signal-to-Noise Ratio (SNR) of the system and provides the possibility of having a higher efficiency device compared to Si-transistor based devices. Because of the higher switching frequency of the system, the frequency response of the system can also be kept linear for a wider frequency range.

Little previous research has been done on digital input class-D amplifiers with global feedback for high power applications. In addition, with the help of new GaN technology, higher switching frequencies can help improve the audio performance of class-D amplifiers.

1.1 Problem statement

In this work, a prototype class-D amplifier is implemented that takes a digital audio input and drives a speaker load. The main target for the amplifier is medium to high power audio amplifiers for the installment and touring market. The following problems are investigated:

- Utilization of oversampling and noise shaping on FPGA to convert digital audio data into pulse signals with a noise level smaller than 0.04 % and less than 0.01 % harmonic distortion.
- Using a GaN drive stage to increase class-D system performance and finding a reasonable switching frequency to meet noise and distortion requirements while still providing at least 80 % efficiency.
- The design of output filters for minimum phase distortion in the audio frequency band and including an investigation on how the material of the passive elements affects the performance of the system.
- Implementation of a digital global feedback loop that keeps distortion within the accepted range.

Since the work is conducted at a company, the ethical requirement on reproducibility is naturally satisfied as the work would otherwise have no value for the company. If the work had not been reproducible, further development of the project would be difficult. Therefore, all important components are declared for with part numbers, and all system design aspects are presented, to make the work reproducible. Additionally, the measurement setups are stated in order to show that the system performance is presented in an honest manner.

1.2 Scope

Since the development of a full amplifier prototype is a very wide topic, some limitations must be made in order to enable focus on the important aspects.

Digital signal processing can be done on multiple platforms. Different solutions could include general-purpose processors, a digital signal processor, on FPGA, or a custom ASIC design. Since low delay and high-frequency precision is desired in this project, together with a need for fast configurability, an FPGA is used. Further comparison between different DSP topologies is not conducted throughout this report.

Since the noise and distortion requirements in this project are strict, the layout of the design can affect system performance. A carefully routed, integrated PCB solution could ensure good noise properties. However, due to the number of advanced components, such as an FPGA and a high-performance ADC, the risk of errors in the PCB design process is too large. Therefore, the prototype is built using a series of development boards.

1.3 Disposition

Chapter 2 provides a theoretical foundation necessary to motivate the design choices made in Chapter 3, Design and Implementation, and in Chapter 4, Digital Hardware Implementation. In addition to this, Chapter 2 helps with the understanding of each part of the system. In addition to presenting and motivating design choices. Chapter 3 also presents the performance of individual parts of the system.

Chapter 4, Digital Hardware Implementation, presents how the digital system was designed for FPGA implementation using VHDL. The performance of the finalized prototype is then presented in Chapter 5, together with a discussion about the results. Finally, the conclusion of the project, as well as possible further development, is presented in Chapter 6.

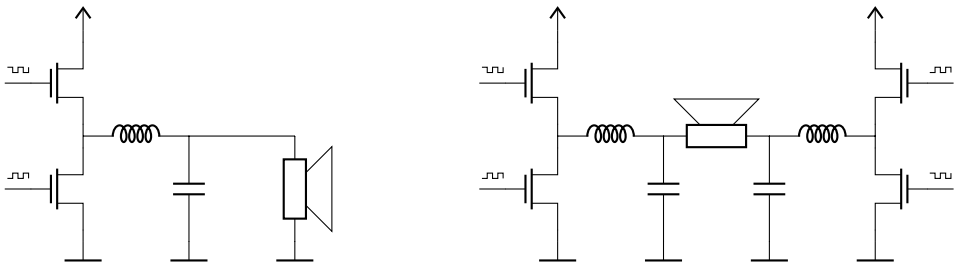
2

Class-D amplifiers, signal modulation, and feedback

In this chapter, the theoretical foundation needed for the upcoming chapters is presented. First, the basic operating principle of a class-D amplifier is presented, followed by a deeper dive into details of each system block. The focus lies on presenting sources of noise and distortion arising in each part of the system.

2.1 Class-D Audio Amplifiers

Audio amplifiers are used to amplify an input audio signal and drive a speaker. The goal is to reproduce the input signal efficiently and with low distortion [1]. There are different types of audio amplifiers, of which most use transistors in order to amplify the input signal. The class-D audio amplifier uses transistors as switches, which are either fully turned on or turned off. The transistors being either turned off or turned on leads to very low power dissipation compared to the other types of audio amplifiers [10]. The input signal is most commonly modulated by using a PWM modulator. The PWM signal is amplified in the output stage, which usually is either a half-bridge or a full-bridge topology, which is presented in Figure 2.1a and Figure 2.1b. A difference between the two topologies is that the full-bridge has twice as high output voltage as the half-bridge for the same supply voltage [11], which means that for the same output power, the supply voltage can be reduced by a factor of two.



(a) Half bridge **(b)** Full bridge

Figure 2.1: Typical class-D drive stages

The amplified PWM signal continues through a low-pass LC filter, which is implemented to remove the PWM carrier frequency. A block diagram of the class-D Amplifier is shown in Figure 2.2.

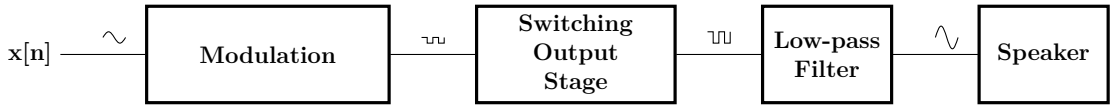


Figure 2.2: Working principle of a class-D amplifier. Reconstructed from [1]

2.1.1 Lowpass Filter

The amplified PWM-signal at the end of the switching stage contains high-frequency components which are removed by using a low-pass filter while passing through the audio frequency components between 20 Hz and 20 kHz. The Butterworth filter is often used due to that its frequency response has a smooth passband and a smooth increase in the attenuation of the stopband [12]. A second-order low-pass filter together with the load in a full bridge setting is shown in Figure 2.3.

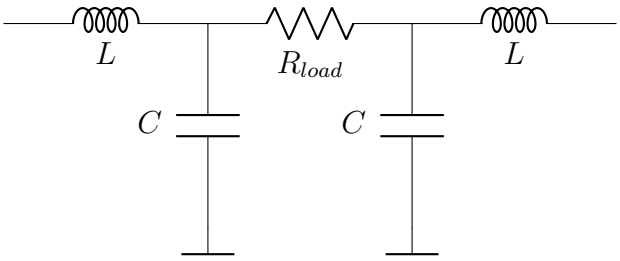


Figure 2.3: Schematic of lowpass filter in a full bridge setting.

In order to determine the values of L and C in the output filter, the schematic in Figure 2.3 can be simplified by assuming the potential in the middle of the resistor is 0 V. The simplified circuit is shown in Figure 2.4.

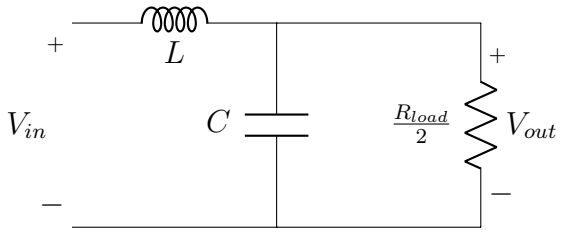


Figure 2.4: Schematic of lowpass filter in a full bridge setting.

By applying Kirchhoff's voltage and current laws to the circuit in Figure 2.4, the transfer function from V_{out} to V_{in} in the S-plane can be written as

$$\frac{V_{out}}{V_{in}} = T(s) = \frac{\frac{1}{LC}}{s^2 + \frac{1}{R_{LOAD}C}s + \frac{1}{LC}}. \tag{2.1}$$

This transfer function can be compared with the transfer function of a general second-order Butterworth filter, which is described by

$$T_B(s) = \frac{\omega_c^2}{s^2 + \sqrt{2}\omega_c s + \omega_c^2}, \tag{2.2}$$

which yields

$$CL = \frac{1}{\omega_c^2}, \tag{2.3}$$

and

$$\frac{L}{R_{LOAD}} = \frac{\sqrt{2}}{\omega_c}, \tag{2.4}$$

where the values for C and L can be obtained by setting a specific cut-off frequency ω_c. The stopband attenuation of a second-order low pass Butterworth filter is 20 dB each decade.

2.1.2 Core Saturation

The LC-filter does not only remove high-frequency components of the PWM signal but can also introduce distortion. Figure 2.5 shows a typical BH-curve of a magnetic material and a non-magnetic material, where the blue hysteresis curve shows the BH-curve of a common ferromagnetic material, and the red dashed curve is the BH-curve for air. The magnetic flux density, B, increases as the applied magnetic field, H, increases according to the constitutive relation

$$\vec{B} = \mu_0 \mu_r(H)\vec{H}, \tag{2.5}$$

where μ_0 is the vacuum permeability and μ_r is the relative permeability, which is a function of the magnitude of the applied magnetic field, and it also depends on magnetization history, in other words, previous values of H [13]. The flux density increases with the applied magnetic field until the point where there cannot be more B produced in the core. When this point is reached, the core is saturated.

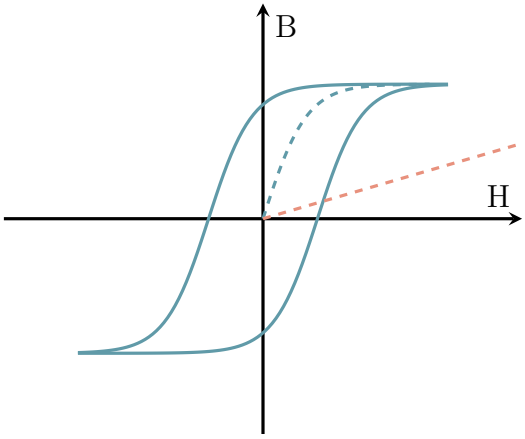


Figure 2.5: BH curve for a typical ferromagnetic material (blue) and air (red).

An inductor can be investigated by using magnetic circuit theory. The magnetic circuit for a simple inductor is shown in Figure 2.6.

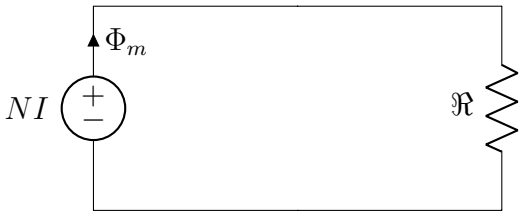


Figure 2.6: Simple inductor represented with a magnetic circuit.

The $\Re$ in Figure 2.6 is the magnetic reluctance which can be expressed as

$$\Re = \frac{l}{\mu_0 \mu_r A}, \tag{2.6}$$

where l is the length of the magnetic circuit, μ_0 is the vacuum permeability, μ_r is the relative permeability of the core material, and A is the cross-sectional area of the core. The NI in Figure 2.6 is the magnetomotive force, and Φ_m is the flux that flows in the core of the inductor. Φ_m can be calculated as

$$\Phi_m = \frac{NI}{R} \tag{2.7}$$

by using Ohm's law on the magnetic circuit in Figure 2.6. Moreover, the inductance of an inductor can be written as

$$L = \frac{\lambda}{I}, \tag{2.8}$$

where λ is the flux linkage, and I is the applied current through the inductor. The flux linkage can be described by

$$\lambda = N\Phi_m = \iint \vec{B} d\vec{s}, \tag{2.9}$$

where N is the number of conductors that are linked by the flux Φ_m and $\vec{B}$ is the flux density passing through a small area $d\vec{s}$. By substituting Φ_m in (2.8) with (2.7) the inductance can be expressed as

$$L = \frac{N^2}{\Re}, \tag{2.10}$$

which shows that the inductance is independent of the applied current I. However, when the current increases, the applied magnetic field, H, increases according to Ampere's Law,

$$\oint \vec{H} d\vec{l} = I, \tag{2.11}$$

which states that the current is equal to the integral of the magnetic field around a closed loop. As the applied current increases, the magnetic field increases until the core reaches saturation, which means that the inductance decreases accordingly because of the change μ_r when the core reaches saturation. Furthermore, the decrease in inductance causes harmonic distortion as well as intermodulation distortion [14]. The problem of magnetic saturation in the core of an inductor can be avoided by using an air-core inductor as the BH-curve for air is linear, and it does not saturate [15].

2.2 The GaN transistor

A MOSFET is a semiconductor device commonly used in applications where fast switching is required, such as power electronics, where it is used to control the power flow to the load. The device has a current-carrying capability in the on-state and a voltage blocking capability in the off state [11]. Since the late 1950s, Silicon has been a commonly used material for semiconductor devices in power electronic applications as it was more reliable than other materials, it enabled easier manufacturing of semiconductors, and it was cheap [7]. In this section, Silicon (Si) and Gallium Nitride (GaN) transistors are compared regarding essential characteristics such as on-resistance (R_{DS}), switching efficiency, breakdown-voltage, cost, and size. Material properties for Silicon and Gallium Nitride are presented in Table 2.1.

Table 2.1: Material Properties for Silicon and Gallium Nitride.

	Si	GaN
Maximum electric field strength, E_{BD}	0.23 MV/cm	3.3 MV/cm
Electron mobility, μ_n	1400 $cm^2/(V\,s)$	1500 $cm^2/(V\,s)$
Energy gap, E_g	1.12 eV	3.39 eV
Relative permettivity, ϵ_r	11.8	9

The strength in the chemical bonds of the atoms in the crystal lattice is related to the energy gap, E_g [7]. Wider energy gap means that a higher electric field needs to be applied in order to free an electron from a chemical bond in an atom. The process of freeing an electron from a chemical bond in an atom is called impact ionization [11]. The electron that was released could gain enough energy to break another bond, thus releasing more electrons. This process can continue, leading to the production of a large number of free electrons, which leads to high current flow. The power dissipation caused by this current destroys the device. The breakdown voltage of a semiconductor device can be approximated as

$$V_{BD} = \frac{1}{2} w_{drift} E_{BD}, \tag{2.12}$$

where w_{drift} is the width of the drift region, which means that the drift region of the semiconductor device approximately can be ten times smaller if GaN is used instead of Si. There need to be a number of carriers in the drift region that can be reduced when the electric field reaches the critical point, E_{BD}. In an N-type semiconductor, the charge carriers are electrons, and the number of electrons in the drift region can be calculated as

$$qN_D = \epsilon_0 \epsilon_r \frac{E_{BD}}{w_{drift}}, \tag{2.13}$$

where N_D is the total number of electrons in the volume, q is the electron charge, ϵ_0 is the permittivity of vacuum, and ϵ_r is the relative permittivity. By having a ten times smaller drift region, w_{drift}, and approximately ten times higher maximum electric field strength, E_{BD}, there can be 100 times more electrons in the drift region according to 2.13. The smaller drift region and higher maximum electric field strength mean that a GaN device can conduct more current than a Si-device of the same size. Another important characteristic is the on-resistance $R_{DS,on}$ (Ω) which can be calculated in the form of

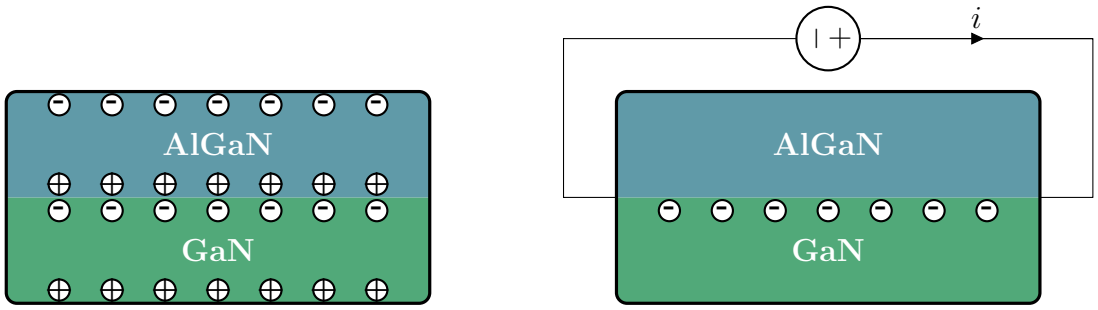
$$R_{DS,on} = \frac{w_{drift}}{q\mu_n N_D}, \tag{2.14}$$

where it is evident that the higher amount of charge carriers in the drift region and the size of the drift region gives GaN devices a lower on-resistance than Si devices.

2.2.1 Two-Dimensional Electron gas (2DEG)

GaN has a hexagonal crystalline structure, which is called wurtzite [7]. The structure is mechanically robust, and it can withstand a high temperature before decomposing because of the high chemical stability of the crystalline structure. As the crystal lattice is subjected to mechanical strain, a tiny shift of the atoms in the lattice occurs. This small shift produces an electric field, which results in a higher electrical conductivity compared to other semiconductor materials. Furthermore, this

phenomenon is made use of when growing a thin layer of AlGaN on a GaN crystal, which creates a strain in the interface between the two materials. The strain induces a two-dimensional electron gas (2DEG), as shown in Figure 2.7a. Electrons in the 2DEG are only free to move in parallel to the interface between the AlGaN and GaN [16]. The 2DEG becomes a conducting channel for electrons when an electric field is applied across it, as shown in Figure 2.7b. The mobility of the electrons is increased in the 2DEG, which is the basic principle of the High Electron Mobility Transistor (HEMT).



(a) Formation of the 2DEG due to strain induced polarization in the interface of the AlGaN/GaN structure.

(b) How the 2DEG becomes a conducting channel as a voltage is applied across it.

Figure 2.7: Simplified crossection of AlGaN grown upon a GaN crystal.

2.2.2 GaN Transistor Structure

The GaN transistor has gate, source, and drain electrodes just as the MOSFET. There are mainly two types of GaN transistors, the depletion mode HEMT and the enhancement mode HEMT. In the depletion mode HEMT, which is normally on, the electrons in the 2DEG are depleted away by applying a gate voltage that is negative relative to both drain and source that turns the transistor off. The depletion mode GaN HEMT has been used in radio-frequency applications since 2005, however the device has not been common in power switching applications due to the inconvenience of its operation [7]. An enhancement-mode HEMT (E-HEMT) is turned off when zero voltage is applied to the gate and on when a positive voltage is applied between the gate and source electrodes. The GaN E-HEMT is most commonly used in power electronic applications, and the basic structure of a GaN E-HEMT is presented in Figure 2.8.

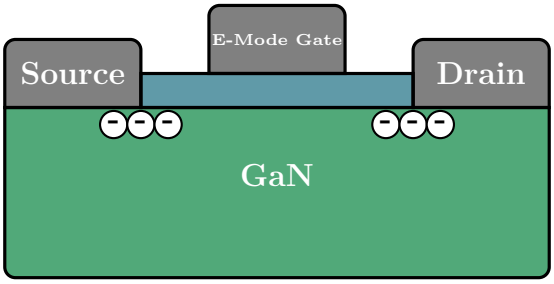


Figure 2.8: Simplified structure of a GaN E-HEMT. Three terminals Source, Drain and Gate. When a positive voltage is applied between Gate and Source the 2DEG will form a conducting channel from drain to source.

The GaN E-HEMT has a lower gate charge than the Si MOSFET with the same breakdown voltage and on resistance, as the GaN E-HEMT can be made smaller [17]. The lower gate charge means that less charge is required to change the state of the device from on to off and vice versa, this will, in turn, enable higher switching speeds. In Si-MOSFETs, a body diode is formed in the p-n junction from drain to the body of the channel. The body diode conducts current in the reverse direction [18]. A GaN E-HEMT does not have an intrinsic body diode. However, it can conduct current in the reverse direction by applying a positive voltage between the gate and drain, which turns on the 2DEG, which in turn conducts current from source to drain. As reverse conduction turns on the 2DEG, the forward voltage drop in the GaN E-HEMT will increase with temperature which is contrary to a Si-MOSFET where the forward voltage drop of the body diode which conducts in the reverse direction decreases with temperature [7]. The absence of a body diode means there is no reverse recovery charge in the GaN E-HEMT [18], which means that it does not have reverse recovery losses.

2.2.3 Environmental Impacts of GaN

Gallium occurs naturally in ores of other metals, especially in bauxite, which is the primary ore of aluminum [19]. Bauxite is found several meters beneath the surface in tropical or sub-tropical regions such as Australia and Guinea. When compared to the mining of other metals, bauxite mining has a more substantial effect on the surface land since bauxite deposits cover large surface areas, and only a small amount is produced from underground mines [20]. As the production of bauxite ore has a significant effect on the surface land, it could lead to the damage of ecosystems and farming land, which most likely would have a negative impact on people and animals living close to the mines. Moreover, China imports large amounts of bauxite from Malaysia, and from 2013 to 2014, there was an enormous surge in the production of bauxite. The rapid increase caused environmental- and health consequences for the residents of Kuantan, Malaysia, the town in which the bauxite was mined. The red dust, which came from the mines, covered trees, cars, and buildings and caused respiratory problems and skin problems for residents that came in contact with the red dust. Moreover, the high increase in bauxite mining also caused traffic congestions as there were a large number of trucks that transported the ores from

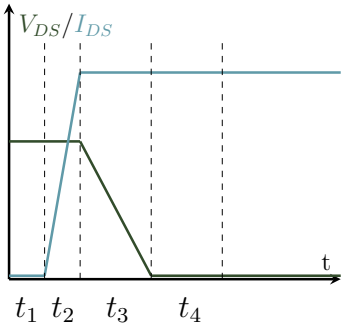
the mines to the harbor for shipping back to China [20]. As Gallium is a by-product of bauxite ore, it can be argued that the production of GaN transistors does not increase the negative impact on the environment as aluminum will still be mined.

2.3 Transistor switching behavior

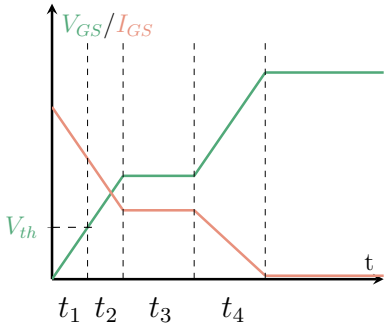
This section describes the turn-on and turn-off process of a transistor to help understand the types of losses that are present during the switching process. It also describes the main losses, which come from gate driver losses and switching losses, and how to estimate these losses using the transistor data sheet.

2.3.1 Turn-on and turn-off

A transistor is turned on by applying a positive voltage between the gate and source electrodes. Figure 2.9 and Figure 2.10 show the V_{GS}, V_{DS}, I_{GS} and I_{DS} during turn-on and turn-off of the device respectively. Figure 2.11 shows a simplified circuit that can be used to explain the turn-on and turn-off procedures.

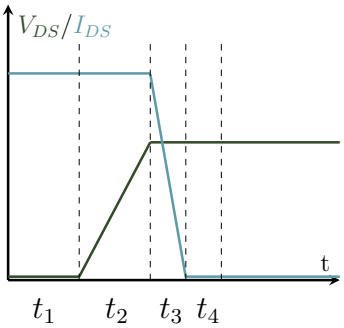


(a) Drain Current and Drain-Source Voltage during turn-on.

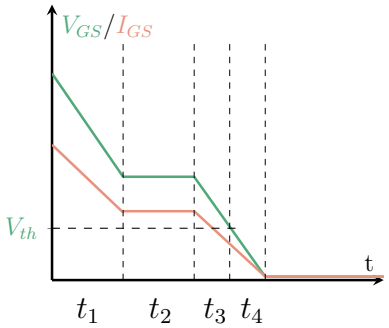


(b) Gate Current and Gate-Source Voltage during turn-on.

Figure 2.9: Turn-on



(a) Drain Current and Drain-Source Voltage during turn-off.



(b) Gate Current and Gate-Source Voltage during turn-off.

Figure 2.10: Turn-off

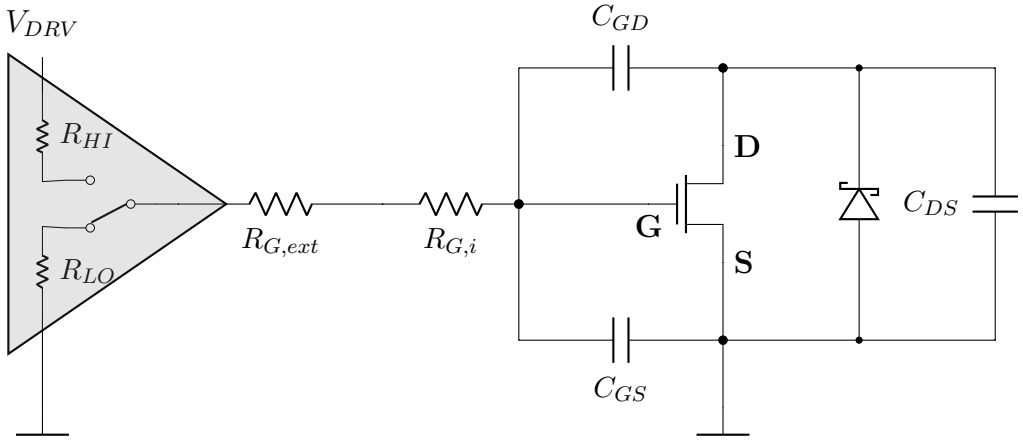


Figure 2.11: Schematic of the Transistor during turn-on and turn-off. The grey triangle is an simplified representation of the Gate Driver. During turn-on the switch is connected to the pull-up resistance R_{HI} and during turn-off the switch is connected to the pull-down resistance R_{LO}.

The turn-on procedure can be divided into several steps. In the first step, the input capacitance C_{iss} is charged to the threshold voltage V_{th}. In the second step, $C_{iss} = C_{GD} + C_{GS}$ is charged to the miller plateau, V_{pl}, and the drain-source current, I_{DS}, increases while the output voltage V_{DS} stays constant. In the third step, V_{DS} is reduced when the current from the gate drive, I_G, is used to discharge C_{GD}. The DC-source limits I_{DS} as it stays constant. During the last step, the 2DEG is fully enhanced by increasing V_{GS} to its final value, V_{DRV}.

2.3.2 Power Losses

There are two types of losses in a transistor, switching losses and conduction losses. Switching losses can be divided into two parts, gate drive losses and switching losses due to the on and off transitions where a high voltage and a high current are present at the same time [21].

The gate drive losses are dissipated in the gate drive circuitry as turning on or off the transistor involves charging or discharging the input capacitance C_{iss}. During each switching cycle, the charge has to pass through the driver output impedances, external gate resistance, and the internal gate resistance. The gate drive losses during turn-on and turn-off can be expressed as

$$P_{DRV,on} = \frac{1}{2}\frac{R_{HI}V_{DRV}Q_G f_{sw}}{R_{HI} + R_{GATE} + R_{G,i}}, \tag{2.15}$$

and

$$P_{DRV,off} = \frac{1}{2}\frac{R_{LO}V_{DRV}Q_G f_{sw}}{R_{LO} + R_{GATE} + R_{G,i}}, \tag{2.16}$$

where f_{sw} is the switching frequency, Q_G is the gate charge, $R_{G,i}$ is the internal gate resistance, R_{GATE} is the external gate resistance, and R_{LO} and R_{HI} are the pull-down and pull-up resistances of the gate driver. In addition, there are switching losses due to the on and off transitions of the transistor. The losses occur in the second and third steps during turn-on and turn-off where the current and voltage are changing. The steps are presented in Figures 2.9 and 2.10. To be able to approximate the switching losses, the gate current needs to be estimated in steps two and three. In step two, V_{GS} is changing from V_{th} to V_{pl}, and the gate current is changing as well. The average V_{GS} in step two can be expressed as

$$V_{GS,AV} = \frac{V_{pl} + V_{th}}{2}, \tag{2.17}$$

and in step three V_{GS} is constant at V_pl. The gate currents in the two timesteps can be written in the form of

$$I_{G2} = \frac{V_{drv} - V_{GS,AV}}{R_{HI} + R_G + R_{G,i}}, \tag{2.18}$$

and

$$I_{G3} = \frac{V_{drv} - V_{pl}}{R_{HI} + R_G + R_{G,i}}, \tag{2.19}$$

where I_{G2} is the current in time step two which charges the input capacitor, C_{iss}, and I_{G3} is the current in time step three which represents the discharging of the

$C_{rss} = C_{GD}$ capacitor while V_{ds} changes from $V_{d,max}$ to 0. The switching times can be approximated as

$$t_2 = C_{iss}\frac{V_{pl} - V_{th}}{I_{G2}}, \tag{2.20}$$

and

$$t_3 = C_{rss}\frac{V_{ds,max}}{I_{G3}}, \tag{2.21}$$

where t_2 is the time during which the current increases from zero to I_{load} and t_3 is the time during which the voltage decreases from $V_{ds,max}$ to zero. By approximating that the time steps two and three in both turn-on and turn-off of the transistor are the same, the switching power loss can be calculated in the form of

$$P_{sw} = 2\frac{V_{ds,max} \cdot I_{load}}{2} \cdot (t_2 + t_3)f_{sw}, \tag{2.22}$$

where f_{sw} is the switching frequency.

2.4 Modulation technique

The input audio is a 24-bit PCM signal with a sample rate of 96 kHz. This signal needs to be encoded into streams of pulses. The modulation has to be done in a way that keeps noise and distortion to a minimum to ensure that the correct information contained in the digital audio signal reaches the speaker. A quantization from 24 to 1 bit will, if not designed properly, ruin the audio signal. The relevant theory required to properly understand quantization noise in digital signals in order to later understand Sigma-Delta Modulation is presented in this section. Thereafter, different methods of PWM are described, followed by feedback system strategies and different loop filter structures.

2.4.1 Interpolation

If an input signal has a sample rate lower than the sample rate of a system, the input signal must be upsampled and interpolated, which means that extra samples must be added while keeping the signal spectrum intact.

By first adding zeros to the new samples, or holding the input signal constant during the extra sample times, images of the signal spectrum are created periodically at multiples of the Nyquist frequency [22], as shown in the first two rows of Figure 2.12. The spectral images, shown in red, can be removed through filtering in the new sampling domain. The last row shows how the signal looks after the filter, and its spectrum shows that the original spectrum is preserved in the new sampling rate.

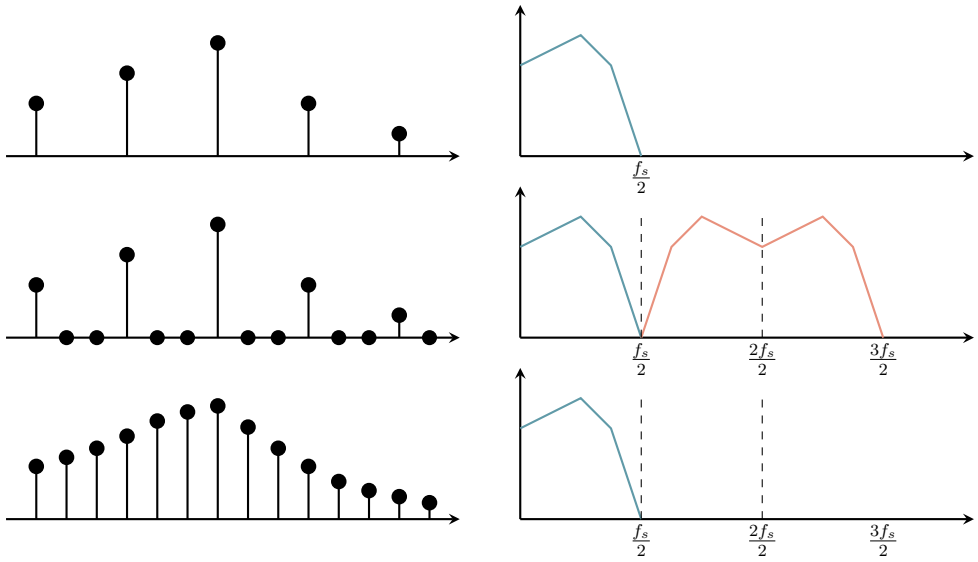


Figure 2.12: Interpolation process in time and frequency domain with an upsampling factor of 3.

2.4.2 Quantization

A continuous signal x which varies from $x_{min} - x_{max}$ has, by definition, an infinite resolution and the process of converting it into a signal with a finite set of discrete values, $q_i = q_1, q_2, ..., q_M$, is called quantization [23]. The quantizer type and its transfer function determines the number of discrete values M in q_i. If the range of the quantizer is

$$X_{FS} = x_{min} - x_{max}, \tag{2.23}$$

the quantization step is

$$\Delta = \frac{X_{FS}}{M}. \tag{2.24}$$

The mid-point of the n-th interval can represent all of the quantization interval amplitudes, described by

$$X_{m,n} = (n + \frac{1}{2})\Delta, \tag{2.25}$$

which means that quantizing anything other than $X_{m,n}$ results in a quantization error of

$$e = q_i(n) - x_i(n), \tag{2.26}$$

which is of the order of Δ. It can be quite small compared to the continuous-time signal, x, if a high number of quantization levels are used. It has a maximum absolute value of 0.5Δ. Moreover, the output y of a quantizer with an input of x_{in} is

$$y = x_{in} + e = (n + \frac{1}{2})\Delta, \quad \forall x_{in} \in (n\Delta, (n+1)\Delta). \tag{2.27}$$

The number of quantization levels that are available are

$$M = 2^k, \tag{2.28}$$

as the final signal is represented by a bitstream, consisting of k number of bits. Assume a signal x that ranges from 0-2 V, which means that the signal has $X_{FS} = 2$ and by quantizing the signal with a 3-bit quantizer the quantization step will be $\Delta = 0.25$ V according to 2.24. The large quantization step leads to a significant error and would not be acceptable in most applications. By increasing the number of bits of the quantizer, the quantization step can be reduced, and subsequently, the error as well. The use of a 16-bit quantizer would give a quantization step of $\Delta = 30\,\mu$V, which would lead to a much smaller error than the previous case.

The error signal e is called quantization noise. If the number of quantization levels is high, e has a white spectrum and a uniform probability density function in the range of $[\frac{-\Delta/}{2}, \frac{\Delta/}{2}]$ which means it is uncorrelated with the input. The signal-to-quantization noise ratio ($SQNR$) represents how much the quantization noise reduces the quality of the input signal. $SQNR$ can be expressed as

$$SQNR = 10\log(\frac{P_S}{P_Q}), \tag{2.29}$$

where P_S is the power of the input signal, and P_Q is the power of the quantization noise. Assume a signal that is large compared to the quantization step δ. The quantization error of this signal is uniformly distributed in the interval $[\frac{-\Delta/}{2}, \frac{\Delta/}{2}]$. Its power is the variance which is calculated as

$$\sigma^2 = Ee^2 = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 f(e) de = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}, \tag{2.30}$$

where E is the statistical expectation and $f()$ is the probability density function. Moreover, the quantization noise power, σ^2, is spread over the entire sample frequency range $[-\frac{f_s}{2}, \frac{f_s}{2}]$ [24]. The power spectral density of the noise power is therefore given by

$$N(f) = \frac{\Delta^2}{12 f_s}, \tag{2.31}$$

where f_s is the switching frequency. A sine wave input signal with an X_{FS} of $2A = (2^k)\Delta$ and thus a signal power of $\frac{A^2}{2}$ has an $SQNR$ of

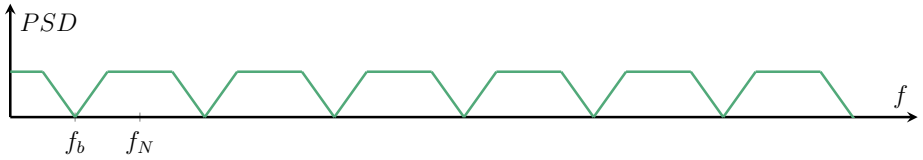
$$SQNR = 10\log\frac{\frac{A^2}{2}}{\frac{\Delta^2}{12}} = 10\log\frac{2^{2k}3}{2} = 6.02k + 1.72\,\text{dB}, \tag{2.32}$$

which means that for each increment of the number of bits, the signal quality increases by 6.02 dB.

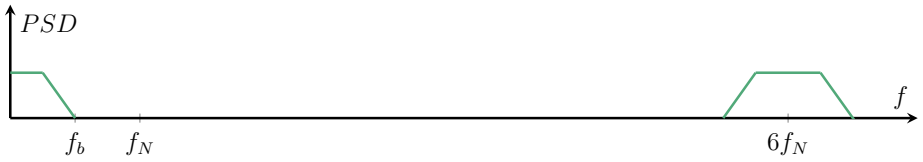
One way of improving the $SQNR$ of the quantizer is to use a sampling frequency higher than the Nyquist rate, which is two times the bandwidth. The oversampling is measured by the oversampling ratio OSR which is given by

$$OSR = \frac{f_s}{2f_b}, \tag{2.33}$$

where f_s is the sampling frequency, and f_b is the signal bandwidth. Figure 2.13a shows the PSD of a signal sampled at $2f_b$, and Figure 2.13b shows the same signal, but when the OSR is 6.



(a) PSD of a signal sampled with $f_s = f_N$



(b) PSD of a signal sampled at $f_s = 6f_N$

Figure 2.13: PSD of a signal which is sampled at different frequencies.

Figure 2.13b shows that the images of the signal are farther apart when the sampling frequency is higher than f_N. The space between the images relaxes the requirements of the anti-aliasing filter as oversampling spreads out the quantization noise power over a wider frequency range as illustrated in Figure 2.14. Moreover, this means that there is less noise in the signal band, which in turn has a positive effect on SQNR [23]. The out-of-band noise can be removed by using a digital filter. Consider the same sine wave as before, with $X_{FS} = (2^k)\Delta$. The signal has a power of $\frac{A^2}{2}$ and if an oversampling of OSR is used the $SQNR$ can be calculated as

$$SQNR_{OSR} = 10\log\left(\frac{\frac{A^2}{2}}{\frac{\Delta^2}{12(OSR)}}\right) = SQNR_{Nyquist} + 10\log(OSR), \tag{2.34}$$

which means that the $SQNR$ can be increased by 3 dB by doubling the OSR. Furthermore, additional improvements of the SQNR can be achieved by using noise shaping. It is a technique where the noise in the signal band, which was left after the oversampling, is pushed to higher frequencies [25].

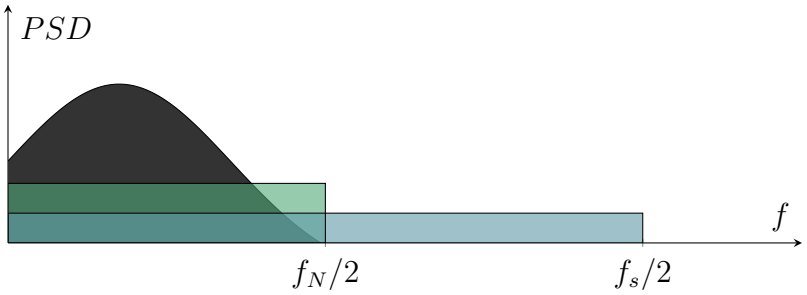
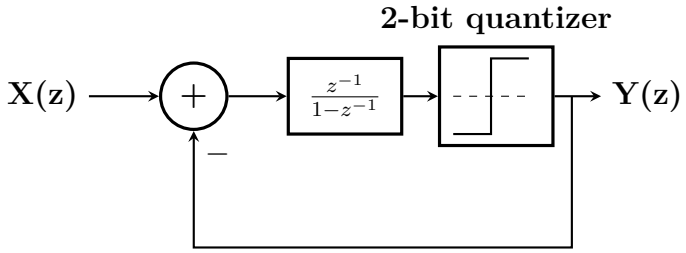


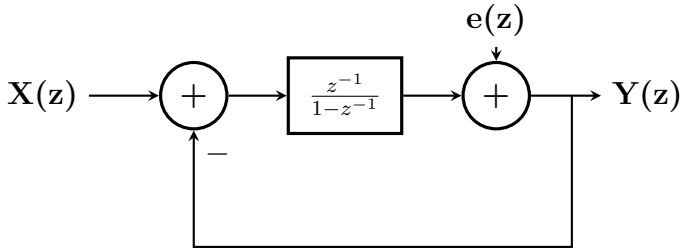
Figure 2.14: The green area represents the quantization noise when sampling at the Nyquist Frequency and the blue area represents the quantization noise when oversampling is used. The use of oversampling spreads out the quantization noise over a wider frequency range. Reconstructed from [25].

2.4.3 Sigma-Delta Modulators

A Sigma-Delta Modulator (SDM) uses oversampling to spread out the quantization noise over a wider frequency band as well as noise shaping to push the remaining noise in the signal band to higher frequencies [25]. A block diagram of an SDM is shown in Figure 2.15a, and its linear model is shown in Figure 2.15.



(a) Block Diagram of a First Order Sigma-Delta Modulator



(b) Linear Model of a first order Sigma-Delta Modulator.

Figure 2.15: Block diagram of a first order Sigma Delta Modulator and its Linear Model

The linear system in Figure 2.15 is analyzed in the Z-domain to obtain a relation between the input and output as

$$Y(z) = X(z)z^{-1} + (1 - z^{-1})E(z), \tag{2.35}$$

where the signal transfer function (STF) and the noise transfer function (NTF) are defined as

$$STF(z) = z^{-1}, \tag{2.36}$$

and

$$NTF(z) = 1 - z^{-1}, \tag{2.37}$$

where the STF does not alter the signal but delays it with one clock period, and the NTF acts as a high pass filter for the quantization error. Hence, it is suppressed at low frequencies and pushed to higher frequencies. In other words, the NTF is the

part of the SDM which applies noise shaping. By estimating the NTF on the unity circle, $z \rightarrow e^{j\omega T}$, it can be described as

$$NTF(\omega) = 1 - e^{-j\omega T} = 2je^{-j\omega\frac{T}{2}}\frac{e^{j\omega\frac{T}{2}} - e^{-j\omega\frac{T}{2}}}{2j} = 2je^{-j\omega\frac{T}{2}}\sin\left(\frac{\omega T}{2}\right), \tag{2.38}$$

which shows that the white spectrum noise power is amplified by 4 but shaped by $\sin^2(\frac{\omega T}{2})$ as shown in Figure 2.16. Furthermore, a first-order SDM is inherently stable [24].

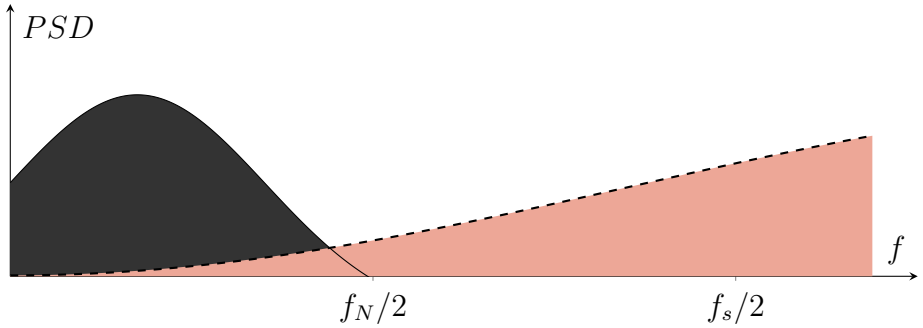


Figure 2.16: The red area represents the quantization noise after Noise Shaping has been applied. The quantization noise is pushed to higher frequencies.

2.4.4 Higher Order Sigma-Delta Modulation

A second-order SDM has an additional integrator in the loop, as shown in Figure 2.17.

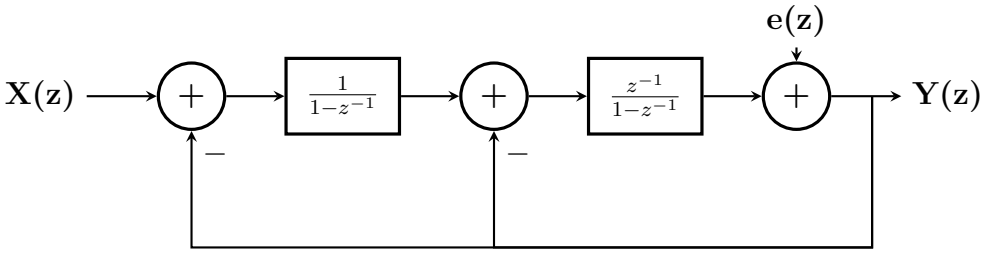


Figure 2.17: Block diagram of a second order Sigma Delta Modulator.

By analyzing the system, the relation between input and output can be described as

$$Y(z) = z^{-1}X(z) + e(z)(1 - z^{-1})^2 \tag{2.39}$$

this gives an STF that is a delay, which is the same as for the first order SDM, and a NTF the is $(1 - z^{-1})^2$. Moreover, the NTF calculated on the unity circle is given

by

$$NTF(\omega) = (1 - e^{-j\omega T})^2 = -4je^{-j\omega T} \sin^2\left(\frac{\omega T}{2}\right), \tag{2.40}$$

which gives further suppresses the noise in the signal band compared to the first order SDM. To further exploit this advantage, higher-order SDM can be used. However, higher-order SDMs are not inherently stable and can thus cause instability problems [25].

2.4.5 Pulse width modulation

A class-D amplifier, as previously stated, keeps the transistors fully on or off at all times, which means that the input audio signal must be encoded into a two-level signal. A common modulation technique in power converters is Pulse Width Modulation (PWM) [26], where the duty cycle of a high-frequency pulse signal is altered in relation to the input signal. Hence, the average of the PWM signal should be the same as the reference signal over a small time frame. A PWM signal is created by simply comparing the input audio signal with a high-frequency single ramp sawtooth or triangle wave [26]. Figure 2.18 shows the fundamental operation of a PWM modulator.

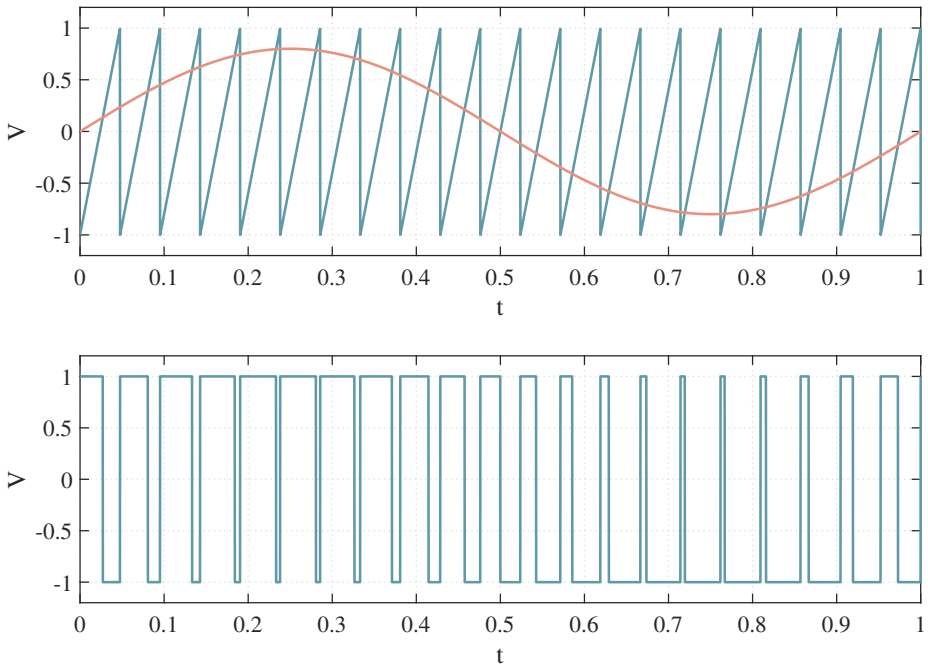


Figure 2.18: Pulse Width Modulation principle.

PWM is a nonlinear operation and generates both low and high-frequency harmonics. Figure 2.19 shows the harmonic content of a regularly sampled PWM signal that has an oversampling ratio of $m_f = 21$. It is clear that regularly sampled pulse

width modulators exhibit harmonics not only around the switching frequency but also at multiples of the fundamental signal [26].

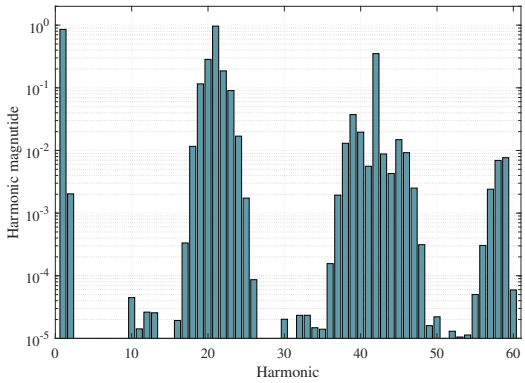


Figure 2.19: Harmonic content of a PWM signal with oversampling ratio $m_f = 21$ and modulation index $m_a = 0.7$. Reconstructed from [26].

The PWM generation is done in the digital domain by comparing a single ramp sawtooth or triangle wave to a regularly sampled input signal. Different modulation-schemes create different harmonic content, and a way to reduce harmonic distortion in the baseband is to use a three-level PWM-signal [11, 27]. The presented double ramp solution in [27] can effectively cancel out even-order harmonics, thus reducing distortion. The same principle can also be applied with a triangle wave. The triangle wave modulation does not only cancel even-order harmonics but also cancels the harmonics at odd multiples of the switching frequency [11]. The three-level PWM signal operation is also called unipolar switching, which means that each side of a full-bridge is switched individually.

Figure 2.20 shows a functional block diagram of the generation of a unipolar switching pattern. The triangle waveform could also be a sawtooth signal. As seen in Figure 2.21, The two created PWM signals are each other's complement and a subtraction of the two yields a three-level PWM signal.

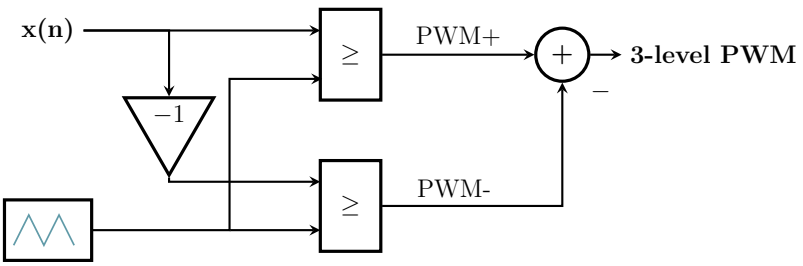


Figure 2.20: 3-level PWM generation.

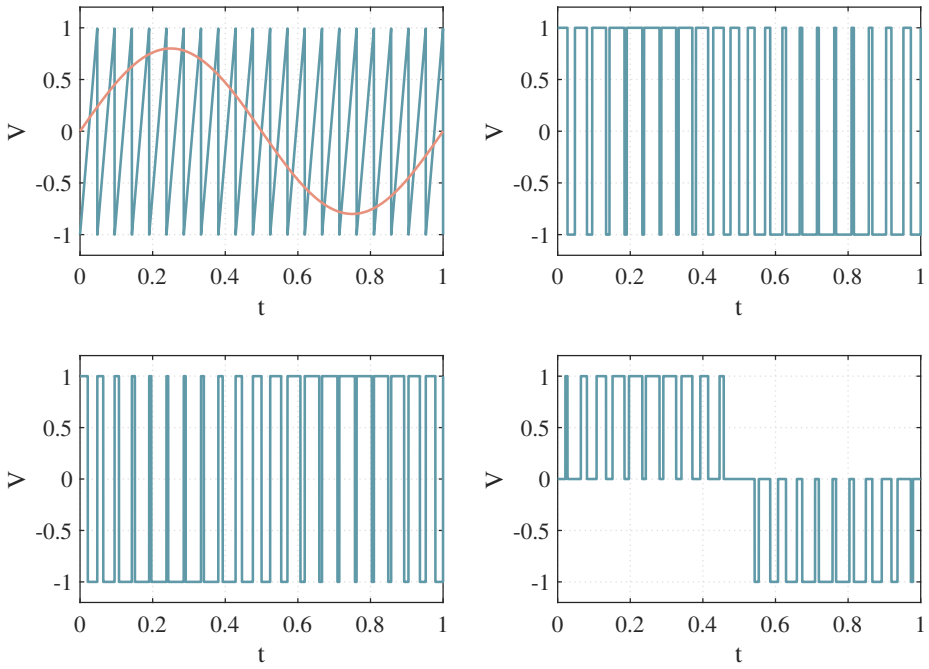


Figure 2.21: Three-level PWM signal principle. Two complementary two-level PWM signals are created and the subtraction of the two yields a three-level PWM signal.

2.4.6 Feedback system

Since the power amplifier switches high currents from the supply, voltage drops may occur and cause distortion in the audio band. The power rails on a high power amplifier can exhibit voltage fluctuations of up to 15 % or −17 dB. Voltage drops beating with the output signal causes harmonic distortion. The power amplifier also introduces distortion from the blanking time added to mitigate shoot-through [28]. Another possible source for distortion is core saturation in inductors mentioned in Chapter 2.1.2. An open-loop amplifier is unable to correct for these distortion sources. Hence, a closed-loop design is necessary.

Feedback in digital class-D amplifiers has been done before in different ways [3–6]. The feedback signal is often taken directly after the power stage, as in [4], which makes it possible to correct the duty cycle if it is not identical to the desired duty cycle. This method can, therefore, suppress blanking time distortion and power supply ripple. Since the output filter is not included in the feedback, it is not possible to correct for its distortion.

Global feedback is necessary to enable maximum distortion cancellation. Global feedback has also been done in a few ways, as demonstrated in [3, 5, 6]. [5] uses a control system clock that is significantly higher than the PWM switching frequency. Very low distortion can be achieved since the aliasing is mostly mitigated because of the high sampling frequency. The output filter ensures that the harmonic content

of the PWM signal is significantly suppressed above the high Nyquist frequency. A relatively low PWM switching frequency is used, which makes the sampling frequency modest. In a GaN amplifier with a higher switching frequency, the sampling frequency would have to be very high, which makes an off-the-shelf feedback ADC very difficult to find, and also very expensive.

[3] uses a control system clock that is the same as the PWM switching frequency, which relaxes the demands on the feedback ADC considerably, thus making the implementation more viable. This type of system can, however, suffer greatly from aliasing distortion. The harmonic at the switching frequency is folded down to DC, and harmonics around the switching frequency is folded down as multiples of the input signal. The size of the harmonic distortion is directly determined by the ratio between output filter cutoff frequency and PWM switching frequency and the order of the output filter.

All previously mentioned designs have all used PWM switching. By using pulse density modulation (PDM) instead, as in [6], the signal is never upsampled as high as in a PWM system. Hence, aliasing distortion can be mitigated. The downside of using PDM is that it is more prone to distortion from blanking time and rise- and fall times of the power stage, since the blanking time and rise- and fall times are not consistently placed in time for different signal magnitudes.

2.4.7 Loop filter design

Negative feedback can be employed to suppress distortion in the output stage. Figure 2.22 shows a traditional discrete feedback system where G(z) is a discretized linear model of a power amplifier, $F(z)$ represents the digital loop filter and $\beta(z)$ represents the discrete transfer function of dynamics in the feedback path. $X(z)$ and $Y(z)$ the input and output signal and $V(z)$ and $N(z)$ represents the noise and nonlinearities added by the power stage and sampling devices.

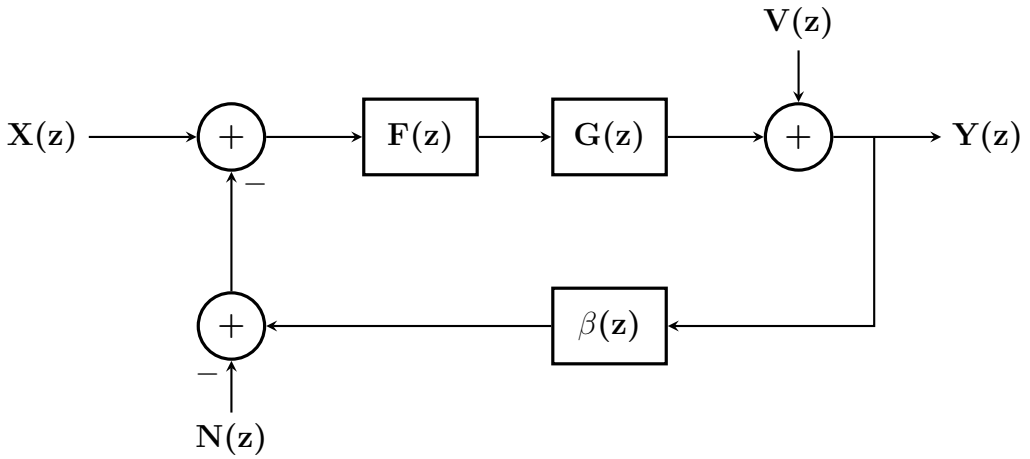


Figure 2.22: General control system.

The full system transfer function from the input to the output can be derived to

$$H_{xy}(z) = \frac{F(z)G(z)}{1 + \beta(z)F(z)G(z)}, \tag{2.41}$$

and the transfer function from the noise and distortion $V(s)$ to the output becomes

$$H_{vy}(z) = \frac{1}{1 + \beta(z)F(z)G(z)}. \tag{2.42}$$

Hence, to suppress distortion, the gain of loop filter $F(z)$ should be as large as possible.

The total loop gain can be described as

$$L(z) = F(z)G(z)\beta(z), \tag{2.43}$$

and in order for the system to be stable, the loop gain $|L(z)|$ has to be less than 1 when phase response is $arg(L(z)) = -180°$.

The transfer function from noise source $N(z)$ can be described as

$$H_{ny} = \frac{FG}{1 + FG\beta}, \tag{2.44}$$

which means that any noise added in the feedback path is not suppressed.

A conventional way to choose the loop filter is the PI-regulator. The proportional part is a flat gain all over the frequency spectrum. The integral part corresponds to an integration of the error. The frequency response of an integrator is a negative 20 dB slope with infinite DC gain. Since the integral part is a negative slope, the loop gain $L(z)$ crosses 0 dB at some frequency f_c. The phase $arg(L(z))$ at this frequency is called the phase margin. A simple method to design the loop filter is to increase the integral gain until the desired phase margin is achieved.

2.4.8 Higher order loop filters

The requirement for high gain in the audio band and low gain outside of the audio band creates a desire for a steep transition from high to low gain. By designing the noise transfer function as a Chebychev filter, a narrower transition band can be achieved [29], which also results in a more even gain than in the simple integrator case. By using a Chebychev filter, zeros can be placed in the NTF [29, 30], which means that the loop filter can have infinite gain.

A Chebychev NTF H_{vy} can be designed with requirements on passband frequency and minimum gain with filter design software. Thereafter, the open-loop gain of the system can be described as

$$L = \frac{1}{H_{vy}} - 1, \tag{2.45}$$

from which the loop filter can be extracted. The minimum gain in the audio band can then be increased until the desired phase margin is achieved.

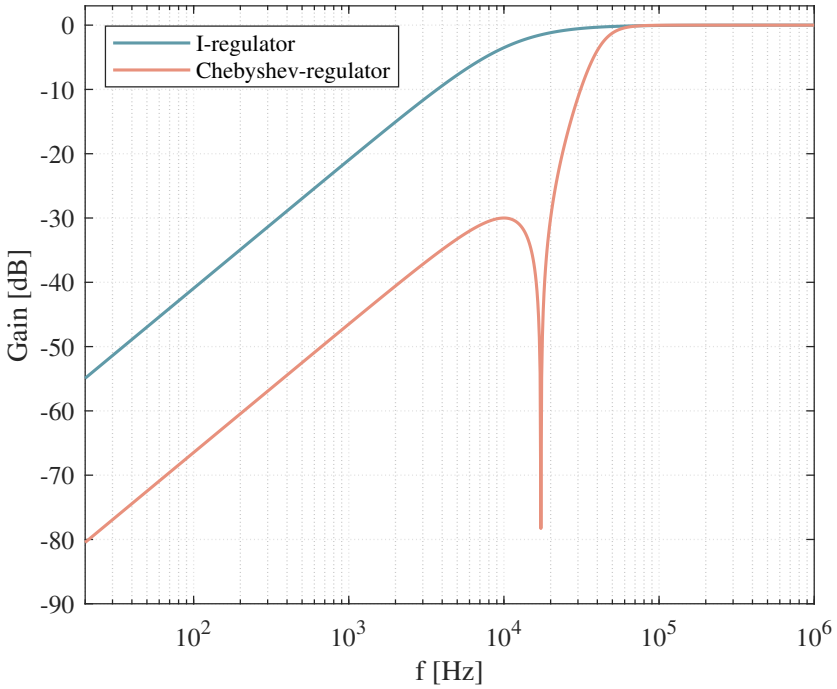


Figure 2.23: Comparison between integrating and a third order Chebyshev style loop filter

2.4.9 Sampling of a PWM signal

If a signal is band-limited and has a bandwidth f_B, it must be sampled with a frequency of at least $f_s = 2f_B$ to avoid aliasing [24]. The signal is then within what is called the Nyquist band, where the Nyquist frequency is $f_{Nyquist} = \frac{f_s}{2}$. Aliasing means that the signal frequency content outside of the Nyquist band is folded down into the baseband of the sampled signal. If a signal to be sampled is not band-limited, the frequency content above the Nyquist frequency must be removed to avoid aliasing, which can be done with an anti-aliasing filter.

A PWM signal, as mentioned earlier, contains harmonics at multiples of the switching frequency. Hence, to sample a PWM signal without aliasing, a sampling frequency that is at least twice the frequency of the PWM harmonics of significant magnitude is needed. Since the PWM signal has high-frequency components, a very high sampling frequency is needed, or a very good anti-aliasing filter.

2.4.10 Clock jitter in PWM signals

A synchronous digital system often operate with a master clock oscillator. All oscillators suffer from phase noise, which means that its frequency varies slightly and shift the clock in and out of phase. When the sinusoidal oscillator is converted to a digital clock signal, the phase noise results in clock jitter, which means that transitions of the clock are slightly misplaced in time, as shown in Figure 2.24.

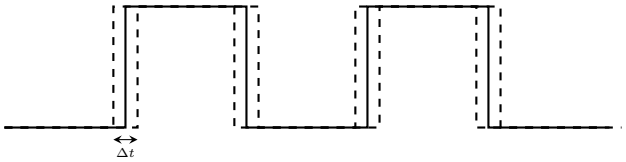


Figure 2.24: Clock signal with jitter

The clock jitter Δt can be considered a zero mean, uncorrelated, gaussian process [31]. The displacement of the clock transitions causes the PWM-signal transitions to be equally misplaced and induce noise in the output signal. The noise error ΔV can be described as

$$\Delta V = \frac{2V_{tri}}{T_{tri}/2}\Delta t, \tag{2.46}$$

where V_{tri} is the amplitude of the triangle wave, and T_{tri} is its period time [31]. Since there is a linear relationship between noise error and clock jitter, the noise error can also be considered a zero mean, uncorrelated, Gaussian process. Hence, the jitter noise will have a white noise spectrum in the interval $\frac{-f_{pwm}}{2} < f < \frac{f_{pwm}}{2}$.

With a sine wave input, the resulting THD+N can be described as

$$THD + N = 100\frac{4\sqrt{2}\Delta t}{m}\sqrt{f_{PWM}f_{BW}}, \tag{2.47}$$

where f_{BW} is the bandwidth of the noise calculation [31], and m is the modulation index of the PWM-signal.

2.4.11 Blanking time distortion

blanking time is the delay between the switching of transistors in an inverter leg. Ideally, transistors in an inverter can switch on and off simultaneously, but due to turn-on and turn-off times not being infinitely small, a blanking time needs to be implemented to avoid shoot-through [11, 28]. Figure 2.25 shows the gate voltage of each transistor, in the half-bridge shown in Figure 2.26, during one switching period with and without blanking time.

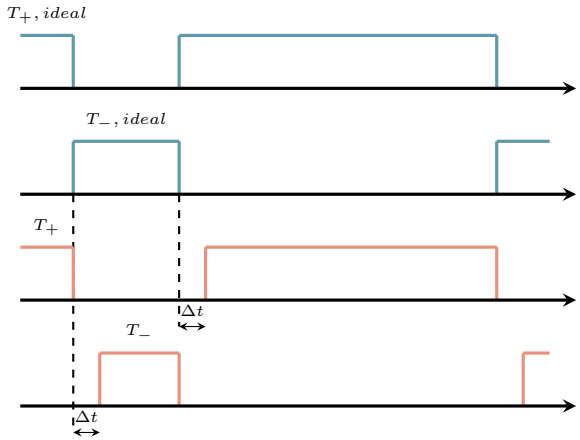


Figure 2.25: Figure which represents the gate voltage of transistors T_+ and T_-. Ideal switching without blanking time is represented by the blue graph and the red graph represents actual switching when a blanking time of Δt is implemented.

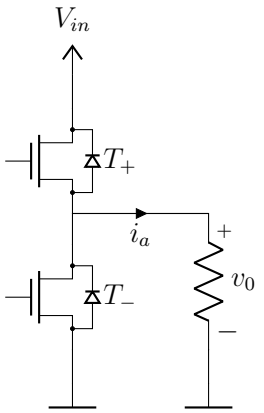


Figure 2.26: Half Bridge

The output voltage v_0 depends on the direction of the load current i_a during blanking time, Δt because both switches are off during this interval. Assume T_+ is conducting and $i_a < 0$. When the PWM signal that drives T_- goes from low to high the blanking time Δt delays the turn-on of T_-, forcing v_0 to be connected to V_{in} rather than ground. The blanking time leads to an increase in voltage area, causing the average output voltage to be higher than intended. Next, when $i_a < 0$ and T_- is on, the PWM signal that drives T_+ is delayed by Δt, i_a flows through the diode in parallel with T_+, which causes v_0 to be connected to V_{in} which means that Δt does not have an impact on v_0 in this case. Similarly, Δt does not affect v_0 at the moment when T_+ is on, and the PWM signal that turns on T_- is delayed. Furthermore, when T_- is on, $i_a > 0$ and the PWM signal that turns T_+ on is delayed by Δt, the load current i_a will flow through the diode in parallel with T_-. The current flowing through this diode causes v_0 to be connected to ground instead of V_{in}, which decreases the voltage area, thus causing a reduction in average output voltage. The misshaping of the output voltage pulses leads to harmonic distortion in the audio band [28].

3

Design and implementation

This chapter outlines the full design process of the system. It describes how the individual parts of the system are designed on a detailed level. Fig. 3.1 shows an overview of the proposed system. The input signal is a 24-bit 96 kHz audio signal, which is upsampled and interpolated to match the system frequency. The signal goes through a modulation stage within the feedback loop that uses an inner SDM to quantize the signal to the same resolution as the PWM signal. The PWM signal is then created and is fed to the GaN evaluation board, which in turn goes drives the LC-filter and speaker load. The voltage over the load is measured with an ADC and is fed back to the upsampled input signal. The following sections go through the design piece by piece and describe how each part of the system was designed.

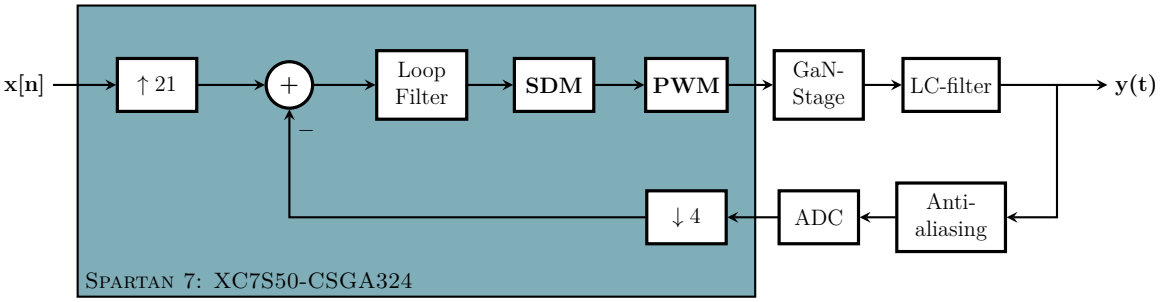


Figure 3.1: Proposed system block diagram.

3.1 Power stage

The Power Stage of the class-D Amplifier has a full bridge topology. The evaluation board GS61004B-EVBCD [32] was used, it consists of GS61004B GaN transistors and PE29102 High-Speed GaN FET drivers [33] as well as a second-order output filter. It is also possible to adjust the blanking time of the Gate drivers by using the onboard potentiometers. A simplified schematic of the power stage is shown in Figure 3.2.

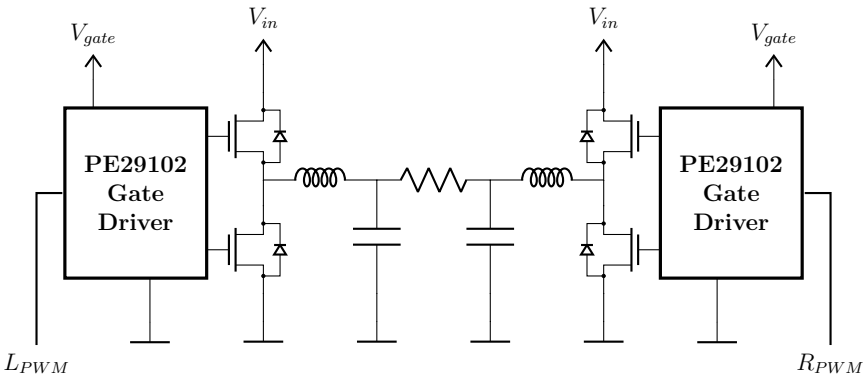


Figure 3.2: Simplified Power Stage schematics.

The losses of the Power Stage were estimated by using data provided in the datasheet of the GS61004B GaN HEMT and the datasheet of the PE29102 High-Speed GaN FET driver [33,34] to get a rough approximation of the efficiency of the Power Stage. The losses that were accounted for in the estimation were the switching losses of the GaN HEMT's and the gate driver losses. The losses were estimated according to the method presented in section 2.3, which show a linear relationship between the switching frequency and switching losses. A switching frequency of 2.016 MHz was chosen as it would yield a high OSR while still providing the possibility of achieving high efficiency in the power stage.

The output filter of the power stage was designed to be a second-order Butterworth filter with a cutoff frequency of 400 kHz in order to remove higher frequency components while still keeping the phase shift as low as possible. The proposed output filter had $L = 4.5016\,\mu H$ and $C = 35.168\,nF$. However, to simplify the filter implementation, it was decided to keep the capacitors that were on the GaN-board and replace the inductors. An air-core inductor was built and used to avoid core saturation as it can introduce harmonics and intermodulation distortion. Moreover, the use of an air-core inductor greatly reduces the resistive core losses as the induced eddy currents in the core significantly lower. The capacitors of the output filter have a capacitance of $0.22\,\mu F$, and the properties of the air core inductor are presented in Table 3.1.

Table 3.1: Air-core inductor properties.

	Value
Turns	21
Toroid diameter	50 mm
Cross-sectional area	31.41 mm^2
Wire type	Litz
Wire diameter	90 x 0.1 mm
L	760 nH

Figure 3.3 shows the real part of the impedance for different frequencies for the two custom-built air-core inductors as well as an inductor with a ferromagnetic core.

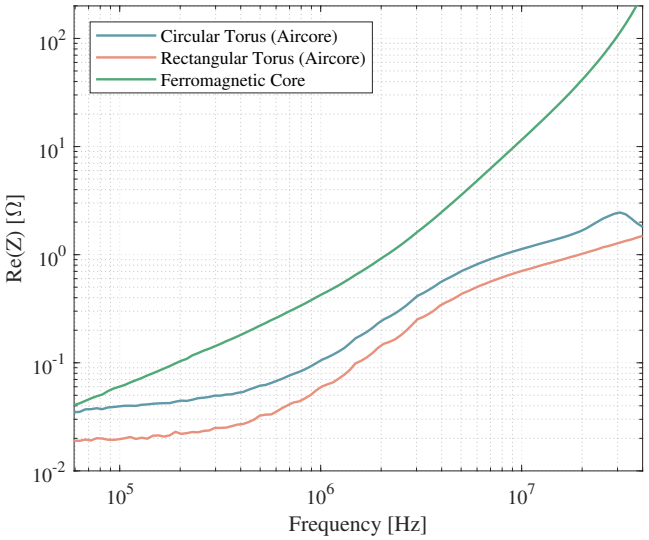


Figure 3.3: Re(Z) for custom built air-core inductors as well as an inductor with a ferromagnetic core.

It can be concluded from Figure 3.3 that the air-core inductors have lower resistive losses due to the reduced resistance. Furthermore, the rapid increase of the resistance of the ferromagnetic core inductor is due to the skin-effect where the resistance increases with higher frequencies [35]. The skin-effect was limited in the air-core inductors by using Litz wire, in which each conductor consists of a high number of strands where each strand has a small diameter, which means that the skin depth does not affect the resistance until the frequency exceeds 1 MHz. The frequency response of the output filter is shown in Figure 3.4.

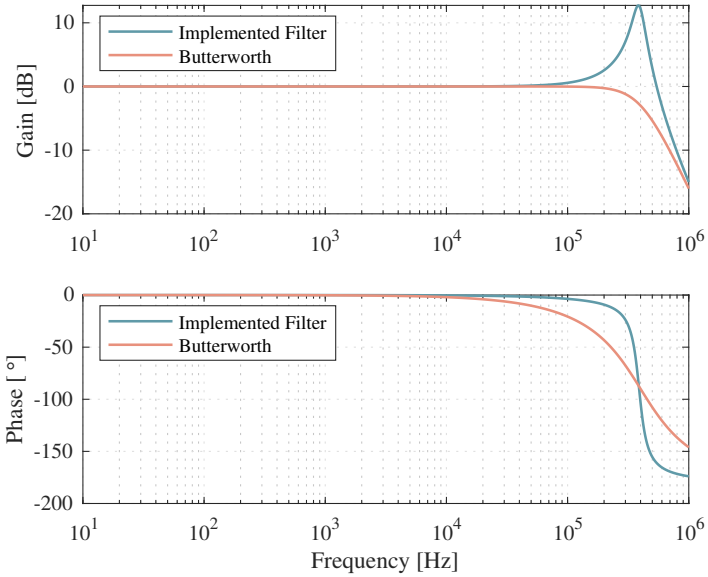


Figure 3.4: Bode plot of the implemented filter and a second order Butterworth filter.

It can be seen from Figure 3.4 that the filter which was implemented has a high resonance peak compared to the second-order Butterworth filter. The resonance peak is appears because of the component choices that were made. The capacitors were not changed from the original filter that was present on the GaN-board and air-core inductors were built to provide the correct cutoff-frequency together with the capacitors, other aspects of the filter were not considered during the design. The resonance peak could, combined with a high phase shift in the feedback loop, lead to instability when testing the implemented design.

3.2 Sigma-Delta Modulator

The OSR is a powerful tool to control the quantization noise. A higher OSR leads to lower noise. However, since the OSR directly corresponds to the PWM switching frequency, the OSR is fixed to 21 in order to get the PWM frequency of 2.016 MHz.

The order of the SDM decides the slope of the noise floor, as described in Chapter 2.4.3. The feedback ADC used in in the project has a noise floor around -120 dB [36]. Therefore, the noise floor at the SDM output should be lower than that over the whole audio band. Figure 3.5 shows the difference between a first- and second-order 6-bit modulator. The first-order modulator is not good enough with the chosen OSR and bit depth. A second-order modulator does not cost anything extra in terms of stability difficulties or hardware and is therefore preferable.

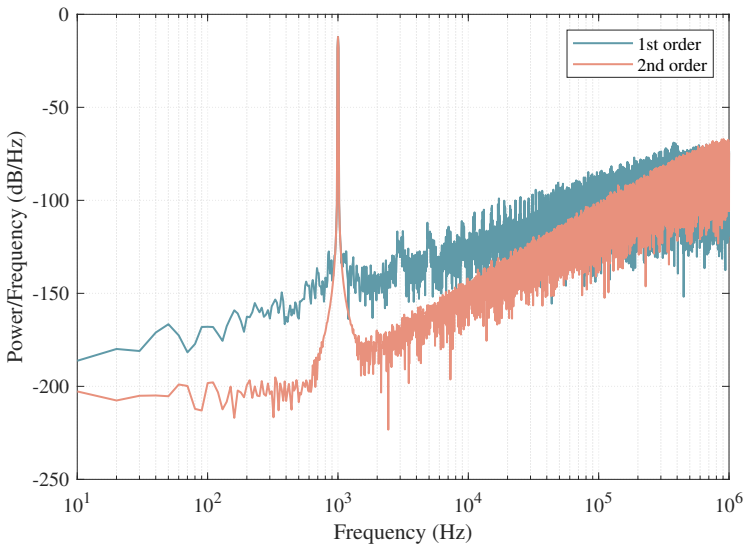


Figure 3.5: Comparison of first and second order 6 bit SDM, with a loop frequency of $f_s = 2.016$ MHz.

The number of bits in the modulator shifts the level of the noise floor, as shown in Figure 3.5. A larger number of bits means a lower noise floor. However, a larger number of bits also translates to a higher clock frequency, and every extra bit doubles the clock frequency of the PWM modulator. The number of quantization bits is set

to five, in order to keep the clock frequency reasonably low compared to the FPGA board specifications.

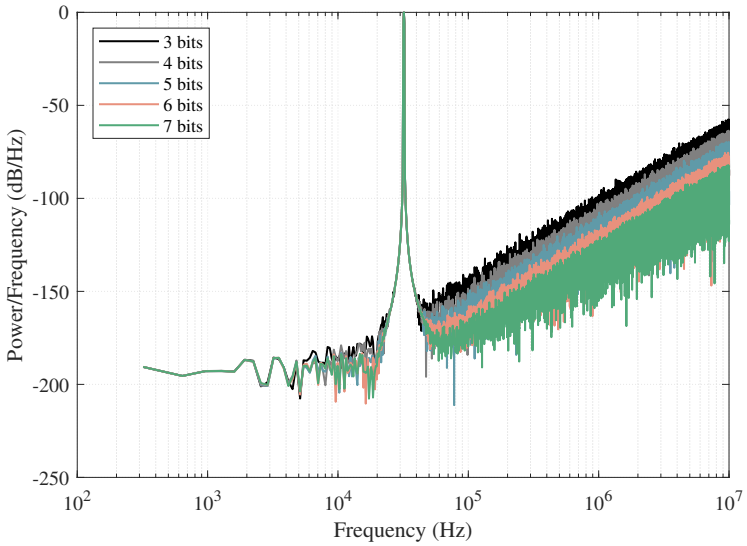


Figure 3.6: Comparison of number of quantizer bits in a second order SDM, with a loop frequency of $f_s = 2.016\,\text{MHz}$.

3.3 Pulse Width Modulator

The PWM modulator can essentially be done in four different ways, described in Chapter 2.4.5. The sawtooth style modulators have the benefit of operating at a lower clock frequency. For low power applications, a low clock frequency can be fundamental to reduce power dissipation. However, since the proposed system targets medium- to high power applications, dissipation from the FPGA circuit is very small in comparison. Hence, a triangular wave gives a higher performance without any noticeable cost.

If a half-bridge power stage is used, a two-level PWM signal must be used. A two-level PWM signal creates harmonics around the switching frequency, which causes aliasing into the audio band when sampled. Three-level PWM signal does, however, not create harmonics around the switching frequency but demands the use of a full-bridge power stage. Therefore, to keep aliasing distortion low, the three-level triangular method is used. Figure 3.7 shows the output spectrum of the SDM-output as well as the four different PWM techniques in an open-loop configuration. Notice that the two sawtooth techniques have severe second-order distortion, and the three-level triangle has very low distortion.

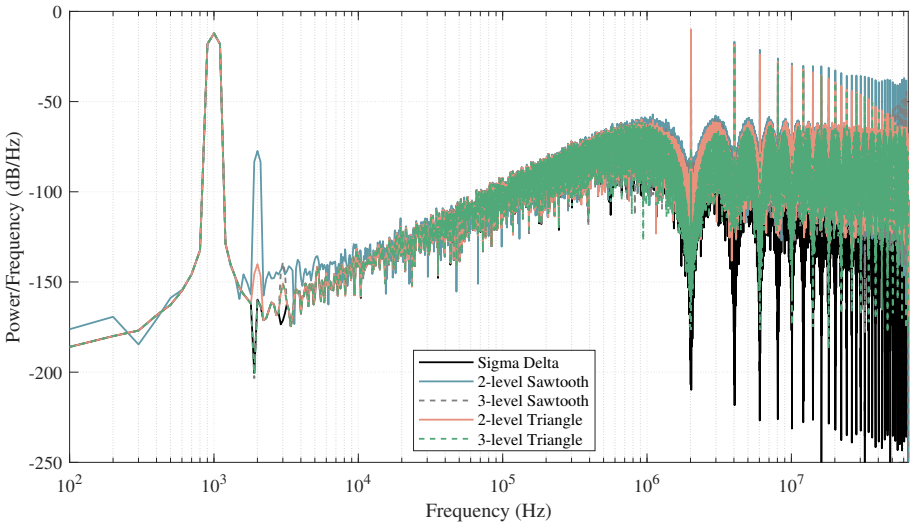


Figure 3.7: Comparison of four different PWM techniques with a switching frequency of $f_s = 2.016\,\text{MHz}$.

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Figure 3.8 shows the same graph zoomed in around the switching frequency. The three-level triangle PWM has virtually no harmonics around the switching frequency, compared to the other techniques which have peaks 80 dB larger in magnitude.

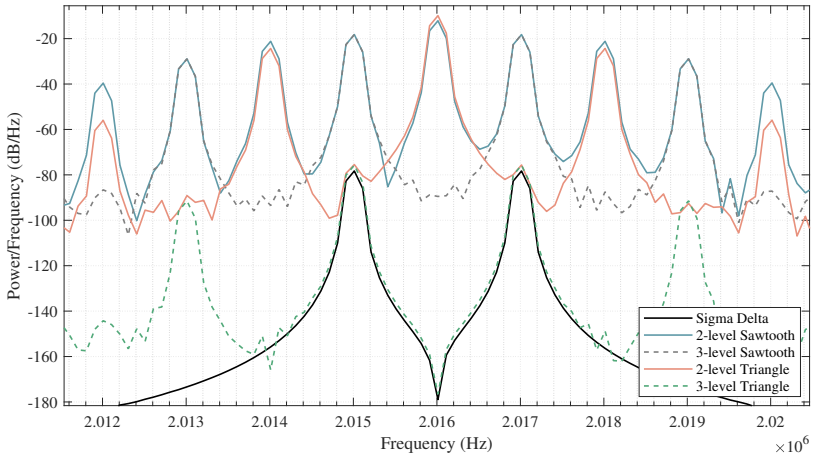


Figure 3.8: Comparison of four different PWM techniques, zoomed in around the switching frequency of $f_s = 2.016\,\text{MHz}$.

3.4 Linearization and discretization

The system diagram in Figure 3.1 contains several non-linear blocks. To be able to use linear control system design, all blocks must be linearized. The interpolation stage is not within the control loop and can, as such, be disregarded. The SDM and PWM introduce noise and harmonics as described in Chapter 2.4.5, which can be

modeled as a separate noise source $V(s)$, together with noise and harmonics created in the power stage and lc-filter. The power stage is therefore simply modeled as a gain block A and the LC-filter as the time-continuous transfer function $G(s)$.

The feedback path contains an analog anti-aliasing filter $B_f(s)$, which is already a linear filter. However, the ADC produces quantization noise of its own, distortion from INL and DNL [36], and creates an unavoidable sample delay. The ADC is modeled as a unit sample delay, and its noise and distortion are added as a separate noise source $N(z)$. The downsampling process is assumed to be perfect to avoid using multiple sample rates in the discrete system model.

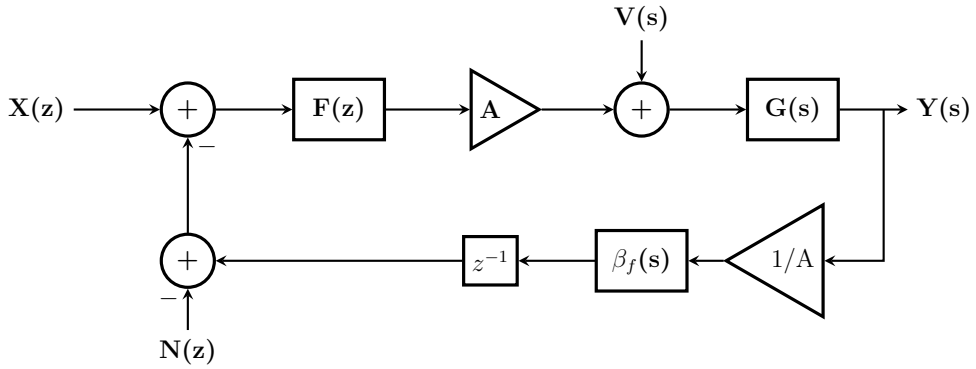


Figure 3.9: Linear mixed signal model of the system.

A discretized model of the ADC $B(z)$ can be constructed as

$$\beta(z) = z^{-1}\beta_f(z), \tag{3.1}$$

where β_f is a discrete model of the analog anti-aliasing filter. The unavoidable sample delay introduces phase shift that lowers the phase margin of the system. The chosen ADC is a LTC2202 [36] that is a 10 MSPS pipelined ADC with a 7 cycle pipeline latency. The ADC was used with a sample rate of 8 MSPS to achieve a factor of four from the PWM switching frequency. A 2 MSPS ADC evaluation board could not be found with an easy interface. The effect of this choice is that it slackens the demands on the anti-aliasing filter, but the phase shift is slightly larger than a regular 2 MSPS ADC without pipeline delay. Hence, the available loop gain is slightly smaller, but aliasing distortion is much lower. It also introduces a requirement of a decimation filter in the digital domain to adjust the feedback signal sample rate to the 2 MHz system. The small extra phase shift introduced by the pipeline was disregarded in the loop filter design.

The anti-aliasing filter introduces a noticeable phase shift, which creates a fundamental trade-off that limits the system performance. A high order anti-aliasing filter that has a low cutoff frequency worsens the phase margin and thereby limits the suppression of distortion. On the other hand, the distortion from the aliasing of the PWM harmonics becomes much lower. A low order anti-aliasing filter with a high cutoff frequency does not affect the phase margin as much and thereby increases the

headroom for more distortion suppression. This would, however, increase the effect of aliasing distortion. The anti-aliasing filter $\beta(s)$ was chosen to be a single-pole low pass filter with a cutoff frequency of 400 kHz in order to keep the aliasing distortion acceptably low.

The power amplifier A has a 10 ns propagation delay [32] which introduces additional phase delay. The delay is, however, small compared to the 2 MHz sample delay of 500 ns. Hence, the propagation delay of the power stage is disregarded during the loop filter design. Therefore, the simple delay-free gain model of the power amplifier holds.

Finally, a full discrete-time model can be described as in Figure 3.10.

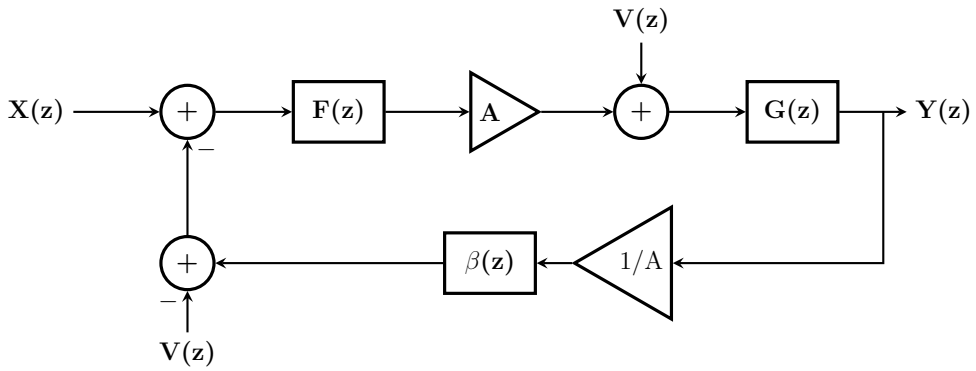


Figure 3.10: Linear discrete model of the system.

3.5 Loop filter design

The loop gain can be derived from Figure 3.10 to be

$$L(z) = \frac{F(z)AG(z)\beta(z)}{A} = F(z)G(z)\beta(z), \tag{3.2}$$

which is identical to the general control system loop gain in 2.43. Hence, the methods described in Chapter 2.4.7 is suitable for the proposed system.

$F(z)$ was at first chosen to be a simple delay-free integrator

$$F(z) = K_i \frac{T_s}{1 - z^{-1}}, \tag{3.3}$$

where K_i is the integrator gain, and T_s is the sample period. Since a large K_i increases the suppression of noise and distortion $v(t)$, K_i was increased until a desired minimum phase margin was achieved. However, due to the phase shift from the sampling and the analog filter, the gain could not be sufficiently high throughout the audio band using a simple integrating controller.

As described in Chapter 2.4.8, the noise transfer function can be designed as a Chebychev type II filter. Figure 3.11 shows the noise transfer function and system transfer function for different filter gains. The gain translates to the minimum noise suppression set throughout the whole audio band.

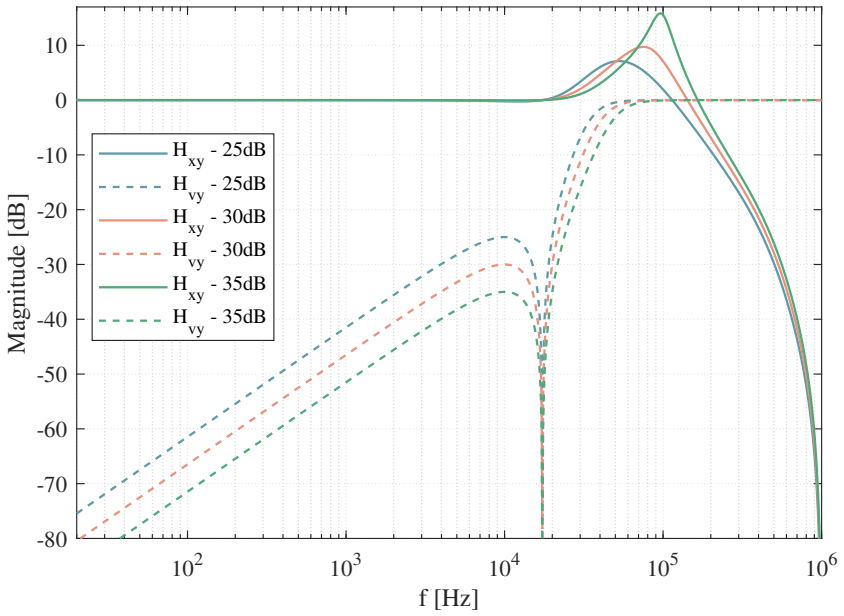


Figure 3.11: Transfer function from input x and noise source v.

The resulting loop filter is a simple delay-free integrator in series with a resonator circuit as described by

$$F(z) = K_i \frac{T_s}{1 - z^{-1}} \frac{1 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}. \tag{3.4}$$

Figure 3.12 shows the open-loop magnitude and phase response with the minimum noise suppression of 35 dB, which results in a phase margin of $\phi_m \approx 9°$.

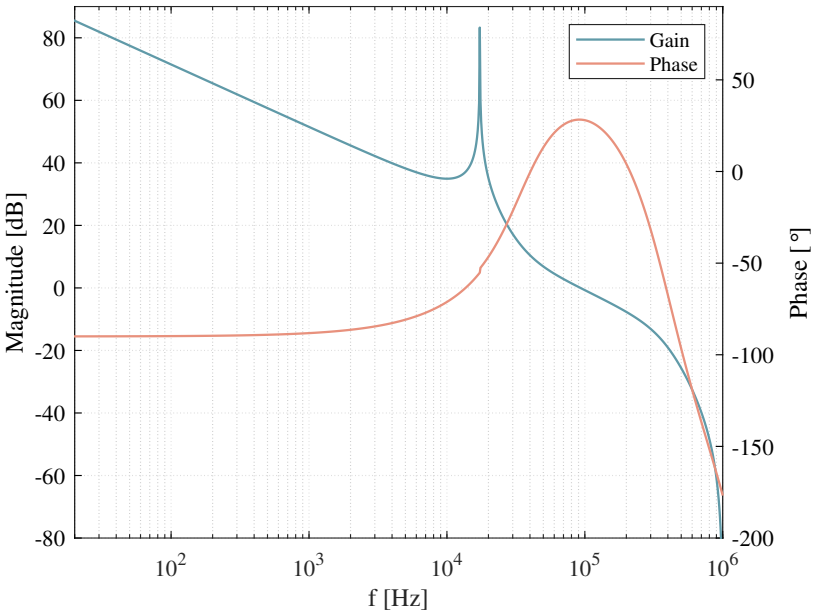


Figure 3.12: Loop gain of the control system with a resonator at $\sim 18\,\mathrm{kHz}$.

Figure 3.13 shows the step response of the design control loop both for the linear model and a mixed-signal system simulation including an SDM, a unipolar PWM block, and non-ideal ADC in the feedback path. The linear model seems to match the simulation reasonably well, except for the high-frequency oscillations present in the simulated signal. Notice that the simulation that contains extra phase delay in the feedback path from the ADC has a more significant overshoot, which is explained by the lower resulting phase margin.

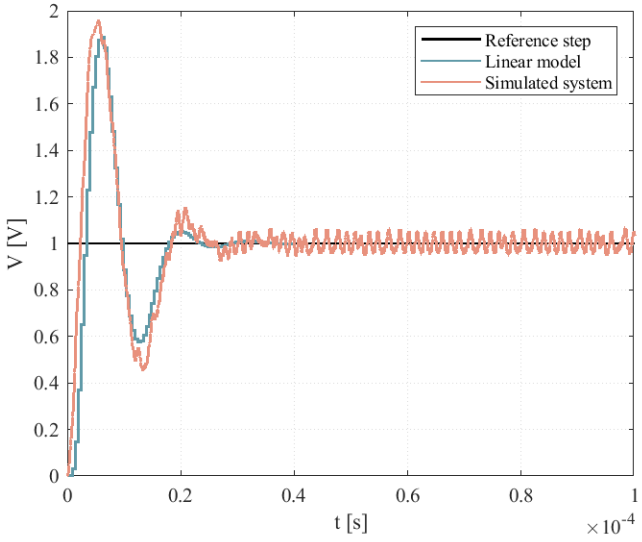


Figure 3.13: Step response of the linear system model and a full system simulation from input x.

Figure 3.14 shows an FFT of the output of the system when a 1 kHz sine wave is applied. The second-order slope of the SDM is visible, but the noise floor of the ADC converter at −150 dB limits the noise performance at low frequencies, which confirms that a third-order SDM is not necessary since the ADC noise dominates. Odd order harmonics are also visible. The harmonics originate from aliasing when sampling the PWM signal and from the nature of the PWM signal itself. Note that the distortion arising in the power stage and output filter is disregarded in this simulation. Thus, the real hardware system will most likely exhibit distortion larger than in Figure 3.14.

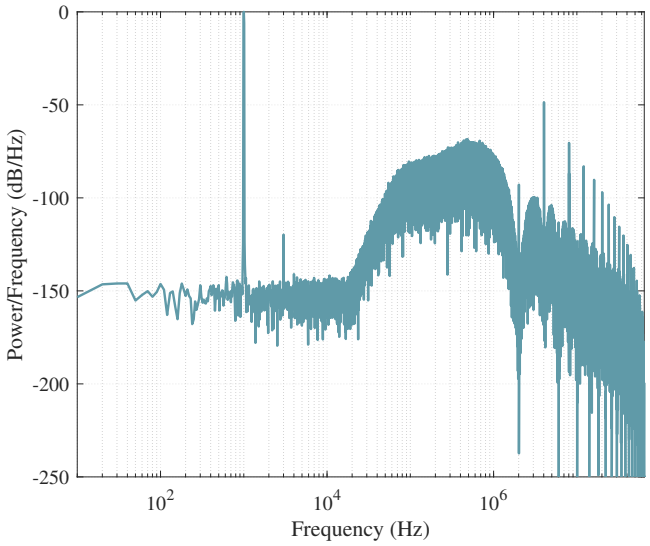


Figure 3.14: FFT of simulation of the full system

3.6 Voltage divider and anti-aliasing filter

The differential input voltage range to the ADC is 2.5 V, with a common-mode voltage of 1.25 V. Since the output of the amplifier has a much larger swing, depending on the supply voltage, this voltage must be divided down to fit the ADC input range. An OP-amp circuit is used to provide high input impedance, ensuring that the high power circuit is unaffected by the ADC measurement, while still being able to drive the ADC input. The OP-amp also has to be able to set the common-mode voltage to match the ADC.

Another analog component in the feedback path is the anti-aliasing filter, which is a first-order RC-filter. In order to reduce matching issues, a single capacitor is used. Figure 3.15 shows the schematic of the analog circuit. The Common mode reference is not shown in the circuit diagram but is fed to the OP-amp from a reference created internally in the ADC chip.

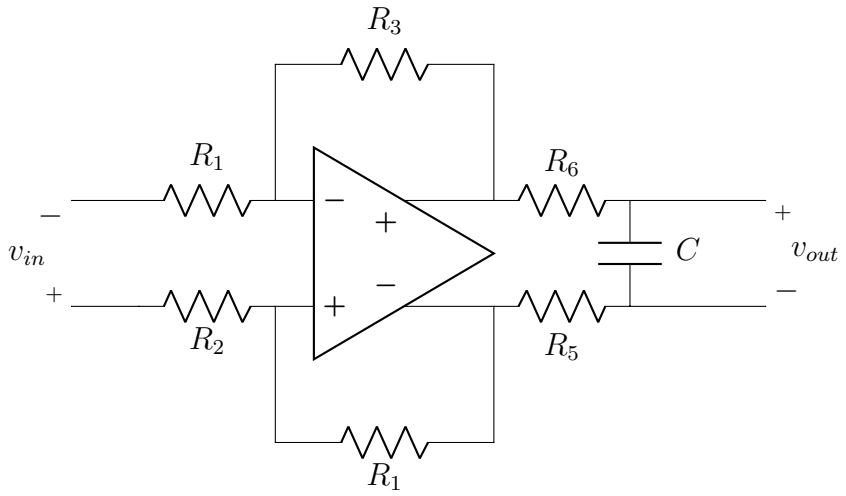


Figure 3.15: Schematic of analog feedback circuit

4

Digital hardware design

The digital part of the system is, as mentioned, implemented on a Spartan 7: XC7S50-CSGA324, which has a large number of resources compared to what is needed in similar digital design projects. Since there are no requirements on how large the implemented design can be, the focus lies on implementing hardware that has as low latency as possible. This section describes how the digital part of the system was implemented on the FPGA. A particular focus lies on architecture choices that affect the latency in the feedback path.

The theoretical system has no sample delay in its main feedback path, which means that a change in the sampled feedback signal can propagate all the way to the output within one clock cycle. The interpolation filter, however, is not inside the feedback loop and can, therefore, tolerate any latency. The longest path is, therefore, between the ADC and the PWM output, as seen in Figure 4.1.

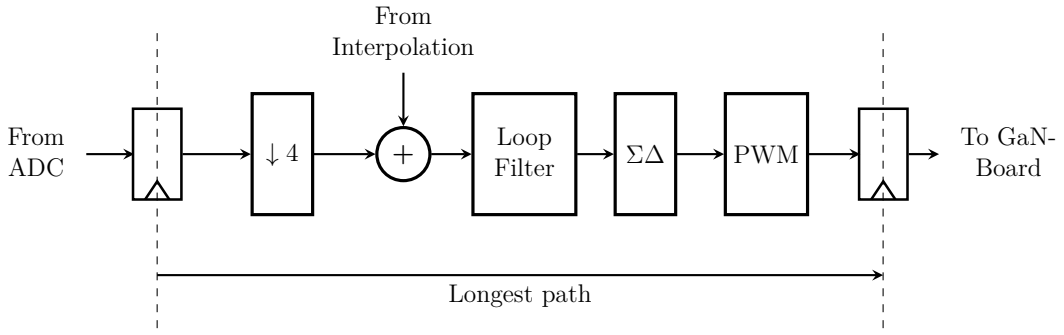


Figure 4.1: Longest path.

The following subsections go through how the latency of each block was minimized, and thereafter, how the design can be pipelined to meet the timing requirements of the digital system while also keeping feedback latency low. But first, the generation of clock signals is discussed to be able to relate the timing requirements of the design. Finally, the upsampling stage is presented together with an overview of the resource usage of the design.

4.1 Clock generation

The chosen FPGA board has a 100 MHz oscillator, which is used as a master clock on the design. This clock must be used to generate the four clocks needed in the design, which are presented in table 4.1. `clk_sys` is the highest clock frequency and is determined by the bit resolution of the PWM signal. The frequency of `clk_sys` is 129.024 MHz, which is 2^6 times the `clk_pwm` and comes from that the resolution is 5 bits and an extra doubling from that the PWM reference signal is triangular. `clk_pipeline` is used as a clock for the pipeline registers and as a local master clock for serialized blocks. `clk_adc` is the sampling frequency of the ADC.

Table 4.1: Different clocks generated in the system and their frequency in relation to each other

Clk	**frequency [MHz]**	**multiple**
clk_audio	0.096	-
clk_pwm	2.016	21
clk_adc	8.064	4
clk_pipeline	64.512	8
clk_sys	129.024	2

Spartan 7 FPGA:s has phase-locked loops (PLL:s) that can be used to generate frequencies down to 4 MHz. This means that `clk_sys`, `clk_pipeline`, and `clk_adc` can be generated using the built-in PLL:s. The other clock frequencies must be generated in other ways. One way is to use a synchronous counter to generate clock enable signals. Another way is to use dedicated clock division primitive blocks that are embedded on the FPGA chip. The second way is preferred since the generated signals then use the dedicated clock nets on the FPGA, and also generates clock constraints suitable for the generated clocks.

4.2 Downsampling

The downsampling consists of a decimation filter with a cutoff frequency of 1.008 MHz. The digital filter was implemented as an Infinite Impulse Response (IIR) Filter in which the current output value is based on both previous input values and previous output values [37]. The filter was designed using the FilterDesigner Tool in Matlab. It has an order of four, implemented as two second-order sections where each section is a biquad. A block diagram of the biquad is shown in Figure 4.2.

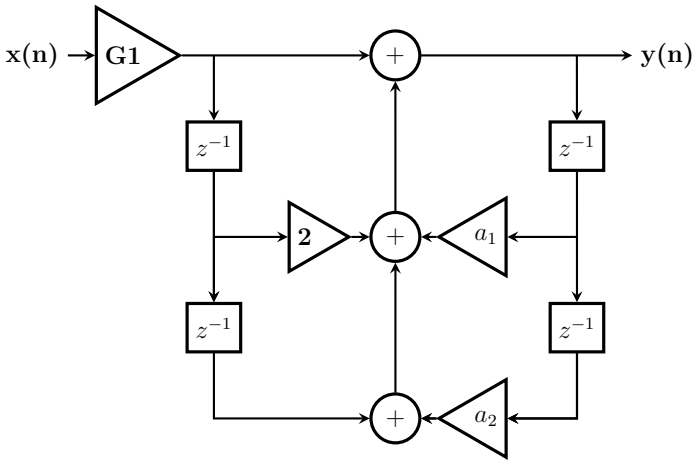


Figure 4.2: Second-order biquad. Two biquads are connected in cascade to form the 4th-order IIR filter.

When implementing high order IIR filters, the coefficients become increasingly more sensitive to quantization than for the low order IIR filters. The fourth-order IIR filter was therefore split into two second-order sections to avoid problems with quantization of the coefficients [38].

4.3 Loop filter

The loop filter consists of a simple integrator and a biquad, similar to the biquad described in the previous section, as shown in Figure 4.3. Hence, two adders and a multiplier are in the path from input to output. For an arbitrary gain K_i, the multiplier can be implemented with the DSP resources on the FPGA. If the gain is chosen to be a simple integer or integer division, the multiplier could be implemented with bit shifts and adders instead and possibly reduce propagation delay.

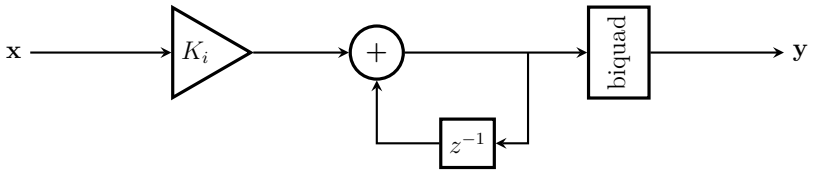


Figure 4.3: Implementation of loop filter.

4.4 Sigma-Delta modulator

The SDM is one of the components with the longest paths. Figure 4.5 shows how the algorithm can be implemented as a straight forward adaption of Figure 4.4. Notice that the path from input to output consists of four adders and possibly an adder in the quantization block.

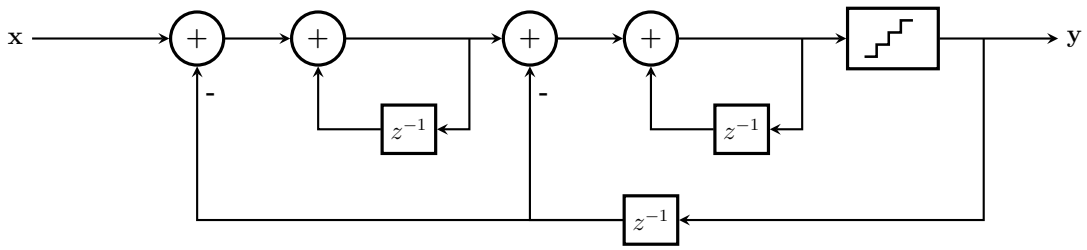


Figure 4.4: Straight forward implementation of second order sigma delta modulator.

With some simple transformations, the SDM can be implemented with only one adder in its path from input to output [39], as is shown in Figure 4.5. The multiplication block is a simple signed left shift, which means that no extra hardware is needed to build this implementation.

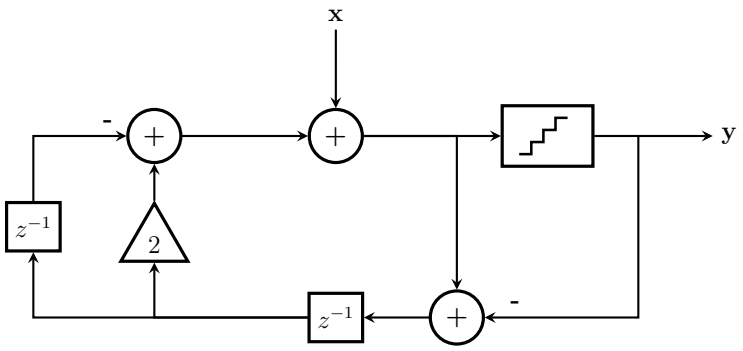
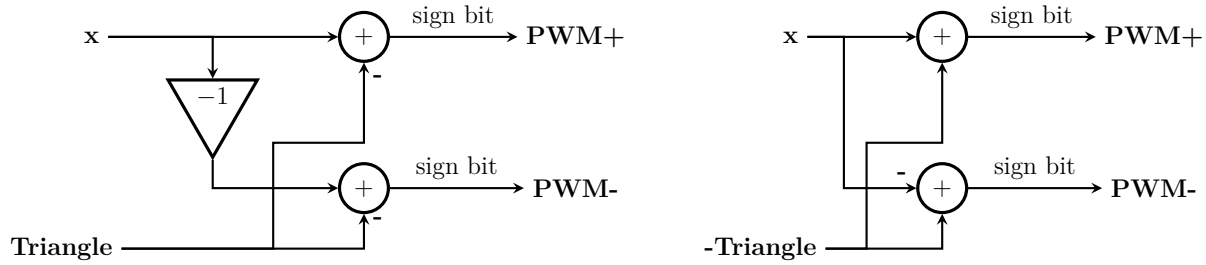


Figure 4.5: Lower propagation time implementation of second order sigma delta modulator.

4.5 Pulse width modulator

The longest path of the pulse width modulator is through the negation block followed by the adder used for comparison between the input signal and the triangle wave, as seen in Figure 4.6a. A negation block consists of a carry ripple circuit, which means that the longest path effectively consists of two adders. However, since negation of the triangle input signal can happen outside of the longest path, the negation of the input signal can be removed. The resulting design is shown in Figure 4.6b, and its longest path only consists of one adder.



(a) pwm **(b)** pwm2

Figure 4.6: Transformation of three level PWM block.

4.6 Pipeline

The previous sections have described the path between the ADC input and the PWM output signals. Even if the logic is designed carefully, the whole path consists of three multipliers and at least six adders. So much logic can not be put between the input and output registers since it would fail to meet setup timing requirements. Additionally, the latency of the path must be very low in order not to introduce phase shift, which would cause the phase margin to decline. Therefore, registers are placed in the design with a clock frequency of `clk_pipeline` = 64.512 MHz. A higher clock frequency introduces a lower latency but also sets a stricter setup timing requirement.

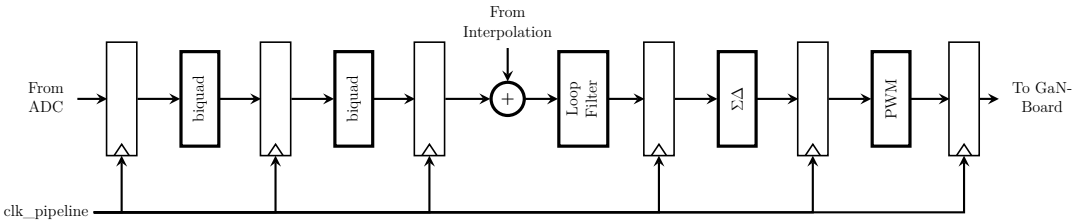


Figure 4.7: Pipelined design.

The registers are placed so that as few as possible are needed. Figure 4.7 shows the final pipelined design. The six registers set the latency of the digital system to

$$t_l = 6\frac{1}{\texttt{clk_pipeline}} \approx 93\,\text{ns}, \tag{4.1}$$

which reduces the phase margin with 3.3 °.

4.7 Upsampling

The upsampling block consists of oversampling and an interpolation filter. An oversampling ratio of 21 was used, and the cutoff frequency of the interpolation filter was 48 kHz. Since the interpolation filter can tolerate any latency, it was implemented as a high order Finite Impulse Response (FIR) filter, in which the current output is a function of previous inputs [37]. The filter was pipelined to meet the timing constraints during the implementation of the design, and it was also implemented as a serial Multiply-Accumulate operation (MAC) FIR filter. The reason a serial implementation was chosen was to minimize the size of the filter on the FPGA. A block diagram of a pipeline stage of the FIR-filter is presented in Figure 4.8.

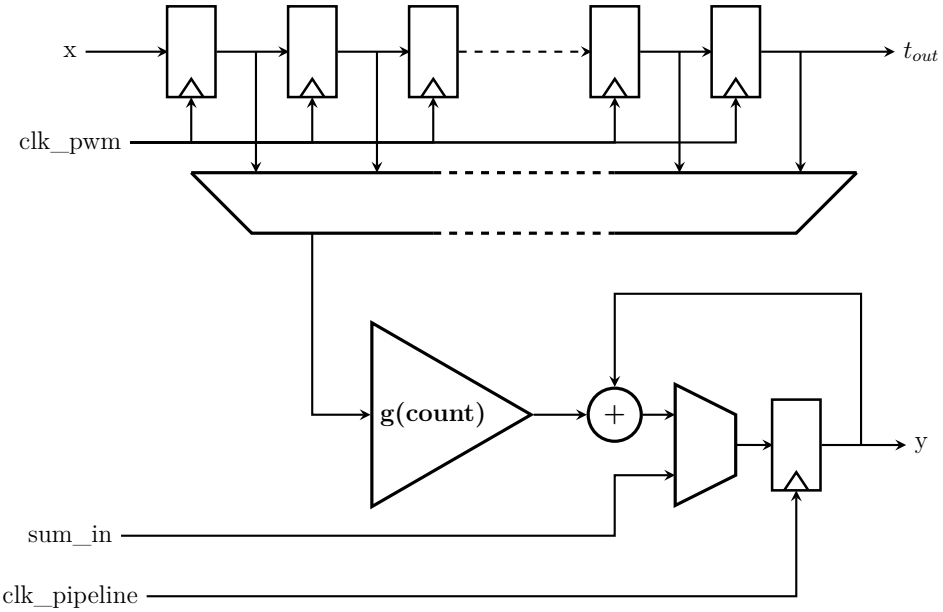


Figure 4.8: FIR filter pipeline stage with MAC operation.

4.8 FPGA Resource utilization

The total resource utilization of the system is presented in Table 4.2. The majority of the FPGA resources are used in the interpolation FIR filter with 186 taps. The filter could possibly be made more efficient with fewer taps, and with a more resource-scarce architecture. Another large portion of the design is the decimation IIR filter, which represents half of the remaining resources. The decimation filter might be omitted in a commercial product if the ADC sample rate is chosen to match the PWM switching frequency.

Table 4.2: FPGA resource utilization

Resource	Total Utilization	FIR filter	Rest of design	Available
LUT	2710	2058	652	32600
FF	5414	4941	473	65200
DSP	20	6	14	120
IO	25	0	25	210
BUFG	5	0	5	32
MMCM	1	0	1	5

5

Prototype Performance

This chapter shows the results of the finalized prototype as well as a discussion about each individual result. First, the frequency response of the system is analyzed. After that, the noise and distortion performance is presented, and finally, the effects of a higher switching supply voltage are analyzed both in regards to noise, distortion, and efficiency.

All audio performance data was gathered with the Audio Precision measurement instrument APx555 after going through an external anti-aliasing filter. The external filter was used since the sample rate of the APx555 is to low to avoid aliasing of large high frequency harmonic components from the output signal. The audio performance measurement setup is shown in Figure 5.1. The load R_{load} was purely resistive with a resistance of $8\,\Omega$.

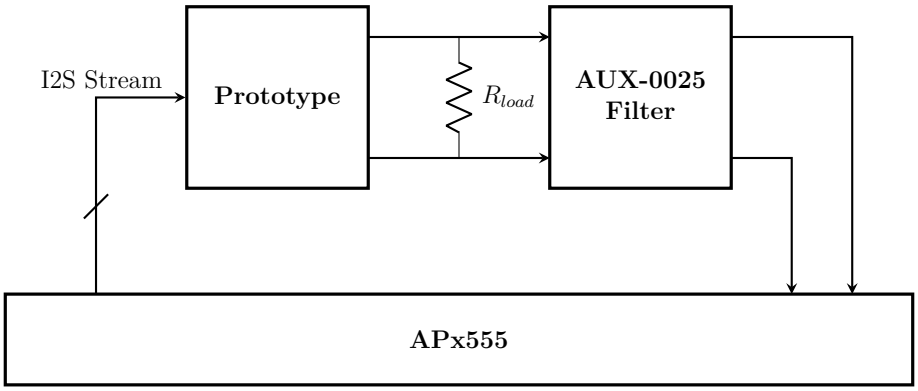


Figure 5.1: Audio performance measurement setup.

5.1 Frequency response

An audio power amplifier must not introduce any equalization of the input audio. Neither any substantial deviation in Gain or Phase may occur. Figure 5.2 shows the normalized frequency response of the system, excluding the linear phase shift of the interpolation FIR filter. The response has a dip in the gain of 0.4 dB and a phase shift of $-3\,^\circ$ at 20 kHz caused by analog filters in the system, which is considered acceptable.

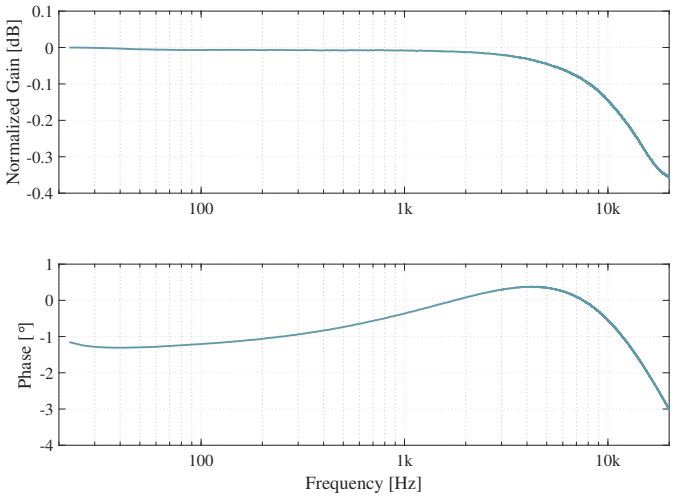


Figure 5.2: Measured frequency response of the proposed system.

The phase shift comes from the analog lc-filter, which has a cutoff frequency of 400 kHz. Silicon MOSFET class-D designs often have a filter cutoff frequency around 40 kHz [5, 30], which without pole cancellation results in a phase shift of over 40 degrees. Hence, in relation to conventional designs, the phase shift of the proposed design is an order of magnitude smaller.

5.2 Noise and distortion performance

In order to display the effect of the closed-loop system, a measurement of the open-loop spectrum with a supply voltage of 12.5 V, as seen in Figure 5.3, can be used as a comparison. There are large spikes of harmonic distortion at around −60 dB compared to the signal of interest.

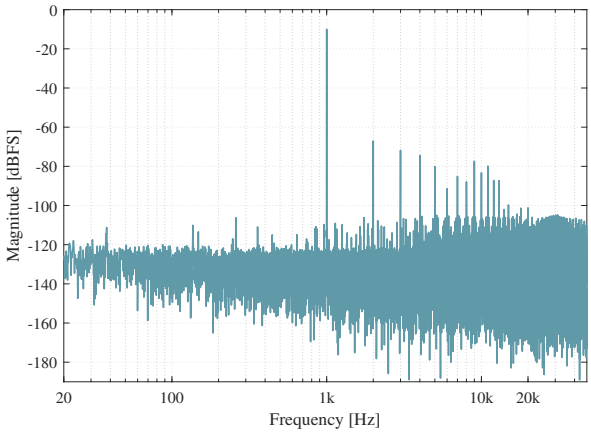


Figure 5.3: Amplifier output spectrum of the open loop system with a −10 dBFS 1 kHz sine wave input

Figure 5.4, 5.5, 5.6 and 5.7 show the closed-loop spectra of the system for different input frequencies and amplitudes. It can be seen that the distortion is proportional to the magnitude of the input signal, as it is not visible at an input power of −60 dBFS. It is clear that the apparent distortion from the open-loop system is greatly suppressed. The worst distortion spikes are now around −90 dB at an input power of −10 dBFS. The closed-loop spectra also show the zero in the NTF at 18 kHz, which shows up as a dip in the noise floor.

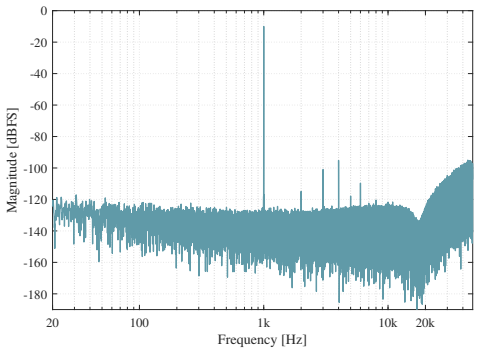


Figure 5.4: Amplifier output spectrum with a −10 dBFS 1 kHz sine wave input

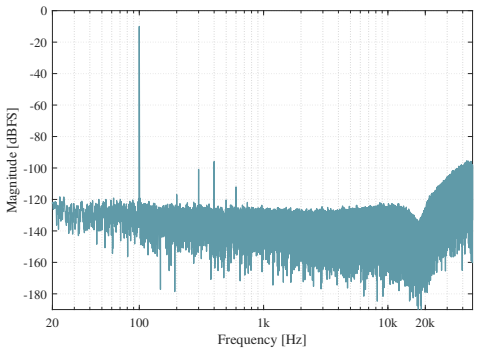


Figure 5.5: Amplifier output spectrum with a −10 dBFS 100 Hz sine wave input

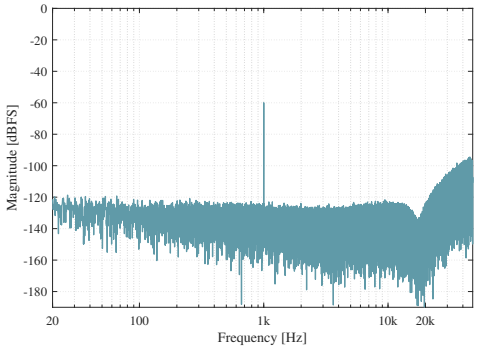


Figure 5.6: Amplifier output spectrum with a −60 dBFS 1 kHz sine wave input

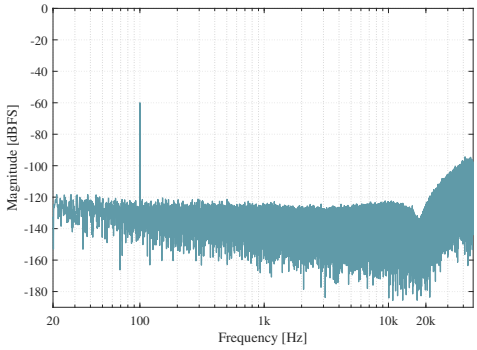


Figure 5.7: Amplifier output spectrum with a −60 dBFS 100 Hz sine wave input

The THD and THD+N were calculated at different frequencies, at 12.5 V and 50 V supply voltage, in order to show that system noise and distortion meets the specifications. Figure 5.8 shows that the THD is around 0.006 % over the whole audio band for the 12.5 V supply voltage, and almost 0.01 % at 50 V supply voltage. When testing the prototype with 50 V supply voltage, resistors in the transmission lines between the FPGA board and power stage were added to avoid spontaneous turn on due to problems with signal integrity between the two transmission lines. The increase in distortion has two potential reasons, partly due to increases voltage drop of the voltage supply and partly due to the extra rise and fall times added in the transmission lines. A custom made PCB could decrease the effects of the pulse shape distortion.

The THD+N is around 0.02 %, with a slight increase towards the highest frequencies for both the supply voltages. A conclusion can be drawn that the THD+N is only limited by noise and not distortion at these operating points.

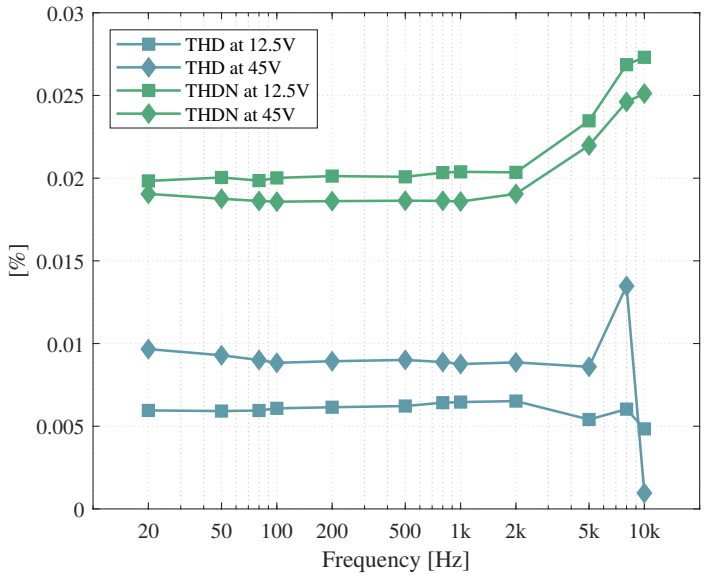


Figure 5.8: THD and THD+N at different frequencies with a sine wave input

The measurements concerning noise display the actual noise performance of the prototype. It does, however, not necessarily reflect the design choices made in Chapter 3. The measured noise is much higher than the anticipated noise from simulations. Noise measured varied markedly depending on how wires between the development boards were laying at the measurement instant. The angle of the inductors also significantly changed the noise level. The feedback loop had an effective length of almost half a meter, which could easily pick up electromagnetic interference from inductors and the power stage.

Another factor not taken into consideration during the design phase is clock jitter. In order to estimate the size of the clock jitter, an oscilloscope was used, and a peak-to-peak value of around 400 ps was obtained, which is in the order of magnitude expected on an FPGA board. Using (2.47) with an RMS clock jitter of $\Delta t = 100\,\text{ps}$, the calculated THD+N based on clock jitter becomes $\sim 0.02\,\%$, which is very close to what is measured on the prototype. Hence, the limiting factor of the system seems to be clock jitter. A means to reduce the clock jitter is to use another master clock oscillator, which has a lower phase noise, as well as being more careful when designing the clock tree on the FPGA.

5.3 Efficiency

The efficiency of the Power Stage was calculated by measuring the rail voltage, load current, and output voltage. During this measurement, the rail voltage was 50 V. The input sine wave had an input power of −5 dBFS, which gave an input power of 64.45 W and output power of 55.27 W. As a result of this, an efficiency of ≈ 85.8 % of the Power Stage was calculated. The main reason the efficiency did not reach 90 % and higher was due to the high power loss at idle state. The large idle state losses were probably due to that the GaN FETs that were used were rated at I_{DS} = 38 A and V_{DS} = 100 V, which means they were meant to be used in higher power application than the class-D amplifier that was designed. Figure 5.9 shows the idle power versus the supply voltage. The over-dimensioned transistors make the switching losses a larger part of the power dissipation in the power stage.

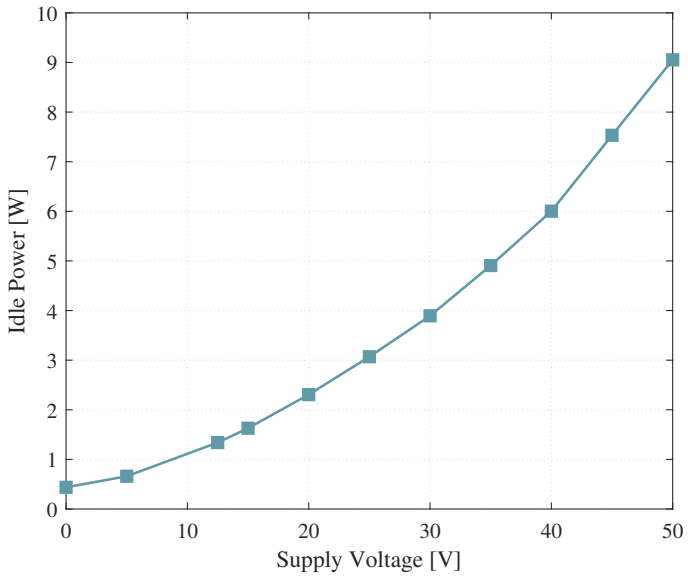


Figure 5.9: Idle power vs Supply voltage

6

Conclusion and further development

Oversampling and Noise Shaping was successfully implemented on an FPGA to convert digital audio data into pulse signals with a dynamic range and distortion far better that resulting noise and distortion from other sources.

The system frequency response resulted in a phase shift of $-3\,^\circ$ at 20 kHz, which is an order of magnitude smaller than the phase shift of conventional designs using Silicon MOSFETs. The output filter was a second-order low pass LC-filter with a cutoff-frequency of 400 kHz, as a result of a trade-off between aliasing distortion and loop filter gain. Air core inductors were used in the output filter, which resulted in lower resistive losses in the core and well as in the copper windings.

In addition, a THD+N of $\sim 0.02\,\%$ for both 12.5 V and 50 V supply voltage was measured, which is dominated by Gaussian noise. The resulting THD was $\sim 0.006\,\%$ for 12.5 V supply voltage and $\sim 0.01\,\%$ for 50 V supply voltage. Although the noise and distortion performance was acceptable, the noise could be greatly reduced by lowering the clock jitter of the system.

Furthermore, a GaN power stage was successfully used with a switching frequency of 2 MHz. An efficiency of $\sim 85.6\,\%$ was determined at 50 V supply voltage, which is considered a success as the used transistors have a higher current rating than utilized. A higher efficiency could have been reached if the GaN-FETs were chosen to suit the power levels of the prototype better.

6.1 Further development

Although the results are promising, there are many things to consider to further improve the results.

The maximum output power of the prototype is in the order of 100 W. Although the concept should work for any output power, a higher output power amplifier should be implemented to confirm the results. The next prototype iteration should also integrate a more substantial part of the system on the same PCB, which could reduce noise problems.

A large portion of the phase shift in the feedback loop comes from the poles from the LC-filter. These poles could be canceled in the digital domain [5], which could drastically increase the phase margin of the system. If the phase margin is increased, a larger gain can be used to further suppress distortion.

The most significant potential for improvement is the clock jitter. The SNR seems to be limited by the clock jitter, which has a linear relationship to the noise power, so if the clock jitter could be reduced with a factor of ten, the SNR might be increased by 20 dB.

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