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# Active Power Filters for Nonlinear Load Applications

Master's thesis in Electrical Power Engineering

Mernis Bajra  
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Master's Thesis in Electric Power Engineering

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### **Abstract**

This report is about the development of an active power filter used for filtering nonlinear current. The source of the nonlinear current is a fan system consisting of two parallel connected BLDC motors. A bi-directional power converter is designed analytically which is verified by simulations and a practical prototype. The outcome of the report is a simulation that is used to verify the performance of the active power filter and a cost and size analysis to compare a conventional passive filter used today with the active filter designed for this application. The final result was an active power filter that was 6.8 times more expensive in material cost and the same size as the conventional passive filter.

**Index Terms:** Active Power Filter, Shunt Active Power Filter, Bidirectional convert, Nonlinear load, LTspice simulation, Passive Filter, Power Electronics, PI-controller, circuit design, PCB.



## **Acknowledgements**

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<b>A</b>	<b>Schematic</b>	<b>A1</b>
<b>B</b>	<b>AVR code</b>	<b>B1</b>
<b>C</b>	<b>Simulation in LtSpice</b>	<b>C1</b>

# Abbreviations

- ADC Analog to Digital Converter, page 14
- APF Active Power Filter, page 2
- APF Passive Filter, page 4
- BLDC Brushless DC, page 15
- CCM Continuous Conduction Mode, page 10
- CSI Current Source Inverter, page 5
- DCM Discontinuous Conduction Mode, page 10
- FCCM Forced Continuous Conduction Mode, page 11
- MCU Microcontroller Unit, page 14
- PCB Printed circuit board, page 16
- PWM Pulse Width Modulated, page 6
- UPS Uninterrupted Power Supply, page 7
- VSI Voltage Source Inverter, page 5



# 1

## Introduction

### 1.1 Background

In the telecommunication industry the competition is high and there is continuously an ongoing race on who achieves the best solutions in the smallest package with the highest efficiency. One of the obstacles to achieve the goals are due to the fans used for cooling the equipment. Because of the power electronics used for controlling the fans and the nature of the motor driving them they draw a nonlinear current that impacts the surrounding systems by creating disturbances. Passive filters have traditionally been used for filtering the nonlinear current to prevent disturbances. The components of which the passive filters are based on are relatively big and have a narrow operation range, this has driven the pursuit for a better solution. One suitable replacement which has high potential is the Active Power Filter (APF) system. It basically uses switches and energy storage devices to perform the filtering. It is of interest for the power solutions department at Ericsson to develop such a system for future applications for fans because of the constant need for cooling among high power components in telecommunication equipment.

## 1.2 Aim

The aim of this project is to investigate the capability of an APF system used in a fan application motivated by simulation of the system in LTspice based on analytical calculations. To verify the calculations and the simulation model, a prototype shall be developed. The result will show the principles of an APF in operation.

## 1.3 Scope

The scope is to build an operational APF system that minimizes the current ripple at the source side. To do so, the component selection will be limited to Ericsson's preferred list of components and the main goal is to have an operational prototype on which measurements can be done. Based on results of the simulations and the prototype measurements, conclusions can be made on whether the APF-system is a better solution in comparison to a passive filter solution. What is out of scope is the modeling of the fan and its characteristics both analytically and in the simulations. The fan characteristics will be regarded as a constant current source in the simulations.

# 2

## Background Theory

### 2.1 Passive Filters

The use of nonlinear loads consuming currents with high harmonic content is causing power quality problems and traditionally Passive Filter (PF) have been applied for harmonic mitigation. The building blocks for PFs are capacitors, inductors and resistors. There are four groups of PFs that are based on the filters characteristics; low-pass, band-pass, high-pass and band-stop PFs. Low and high-pass filters cancel out the high and low order harmonics respectively, band-pass filters cancel out the harmonics that are outside a defined region and tuned filters cancel out a specific frequency. Their different characteristics has led to the usage of PFs in a wide range of areas such as:

- Elimination of signal contamination e.g. in communication systems
- Separation of relevant from irrelevant frequency components
- Improving the quality of audio equipment
- Equalization of transmission lines and cables
- Detecting signals in radios and TV's
- Harmonic mitigation

However, PFs have drawbacks which makes them less suitable in some applications. One major drawback of a PF is that the filtering characteristics is strongly affected by the system impedance which may create parallel or series resonances that causes amplification of harmonics voltages or currents at the resonance frequency. The operating condition of the non-linear load also affects the performance as well the aging of capacitors; consequently PFs need to be designed with high current rating because both the harmonics and the fundamental current is flowing through them. Furthermore, PFs are relatively

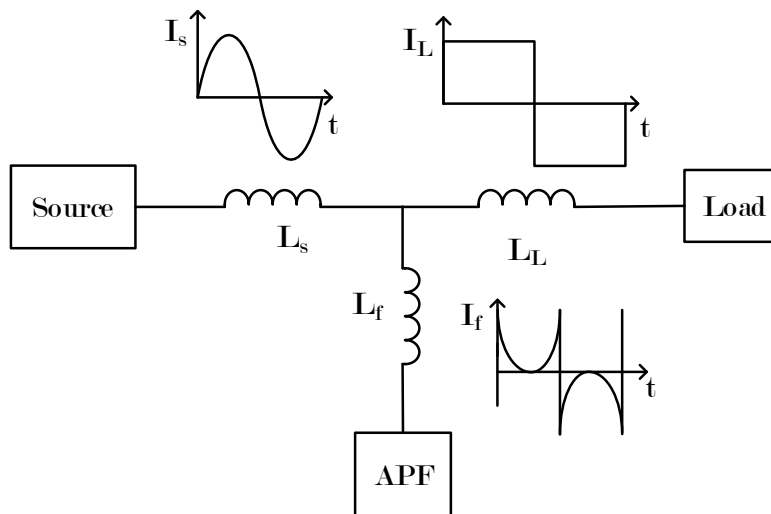
big, heavy and expensive. These drawbacks introduced by using PFs have contributed to the development of power electronic solutions based on converters [1] [2].

## 2.2 Active power filters

The development of the APF system was motivated by the undesired properties of the PFs presented in Section 2.1. The principle of an active filter is to monitor the current or voltage in the system and create an equal but opposite waveform of the harmonics so that from the source point of view, only the fundamental component is seen, see Figure 2.1. In Figure 2.1 it is demonstrated how the compensation is performed, the harmonic components that are present in the nonlinear load current ( $I_L$ ) are produced by the APF ( $I_f$ ) and according to kirchoff's current law the source current ( $I_s$ ) therefore becomes

$$I_s = I_f - I_L. \quad (2.1)$$

This results in the cancellation of the harmonic content in the source current  $I_s$ .



**Figure 2.1:** An APF connected to a system in need of filtration.

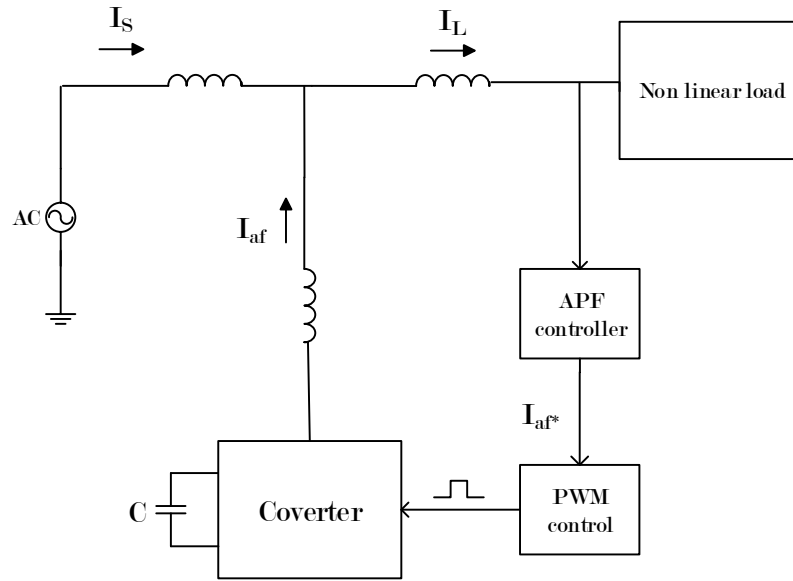
The APF system is a complex system that has to be configured in a suitable way so that it fulfills the purpose of the application. The configuration is done in three steps; selection of the converter, topology and controller. The first step is to choose the converter type, either Current Source Inverter (CSI) or Voltage Source Inverter (VSI), in a CSI, an inductor is used as the main energy storage device and a capacitor is used in the



VSI case. The VSI is the most dominant and frequently implemented because it is less expensive and easier to control in comparison to the CSI. The second step is to determine the topology which can either be series, a shunt or hybrid connection. The final step is to select a controller and switching mode suitable for the selected topology [3].

### 2.2.1 Shunt APF

The shunt APF was first introduced in [4] and has evolved to be used in commercial operation all over the world ever since. The shunt APF is one of the most popular topologies used for mitigating harmonics today [5]. The controller monitors the current consumed by the load ( $I_L$ ) and then creates a compensation current reference ( $I_{af}^*$ ) that generates the compensation current ( $I_{af}$ ) that goes back in to the system. The reference is used as an input to the power converter which then reproduces the inverse of the harmonics by switching in an certain pattern determined by the controller, see Figure 2.2.



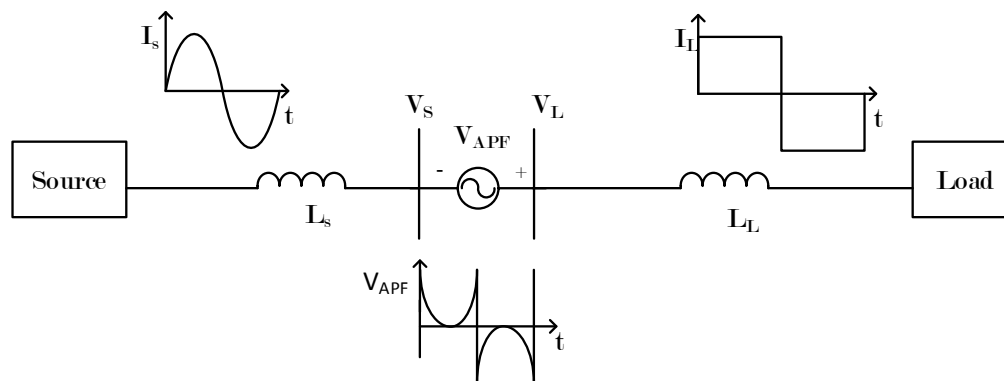
**Figure 2.2:** Shunt APF monitoring the load current and creating a compensation signal to the converter

In general, the shunt APF consists of three main blocks, the power stage circuit with a connected storage capacitor ( $C$ ), the pulse width modulated (PWM) controller and the APF controller. The compensation current ( $I_{af}$ ) that should be consumed by the system is determined instantaneously in real time by the controller and passed further to the PWM converter. The controller works in a closed-loop manner, continuously

sensing the load current ( $I_L$ ) and simultaneously calculating the compensation current reference ( $I_{af}^*$ ) for the PWM converter. The power stage is responsible of supplying the compensation current ( $I_{af}$ ) and to be able to reproduce the current in a proper way, a switching frequency ( $f_{PWM}$ ) should be selected which is at least 10 higher than the highest order of harmonic current that is to be compensated. The energy to supply the load with current is stored in the storage capacitor connected to the converter.

### 2.2.2 Series APF

In the late 1980s, the series APF was introduced with the purpose of voltage regulation and to act as an isolation barrier preventing the harmonics of the nonlinear load from propagating into the utility system, see Figure 2.3 for schematic overview. The basic operation principle is to inject a voltage component in series with the supply voltage that cancels the penetration of the harmonics into the power system. The APF can therefore be regarded as a controlled voltage source. This topology is preferable in applications where the consumer is sensitive to disturbances and has to be protected from insufficient supply voltage quality. Additional application areas are for counteracting voltage sags from the voltage source. From an economical point of view, the series APF is an attractive alternative in low power applications for uninterrupted power supply systems (UPS). The reason being that the series APF uses no energy storage device such as batteries and the rating of the series APF device is smaller in comparison to the UPS [4].



**Figure 2.3:** Series APF operating as an barrier, prohibiting the harmonics of the load from propagating into the source

### 2.2.3 Hybrid APF

A Hybrid APF is a combination of an shunt APF and a passive filter part and is shown in Figure 2.4. Despite the drawbacks of PFs as presented in chapter 2.1, they are still present in APF application where the combination of them both leads to rate, footprint size and cost reduction of the APF system. The rate reduction of the APF system is achieved by letting the passive filter cancel out the low order harmonics which have great contribution to the distortion [2][3].

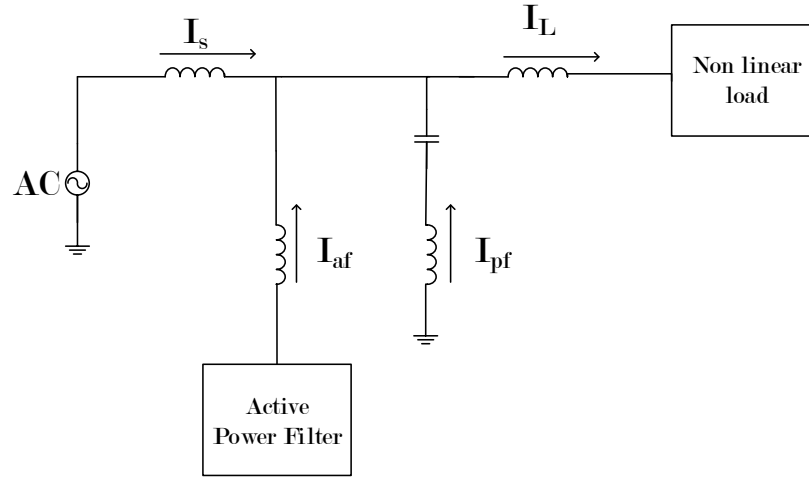
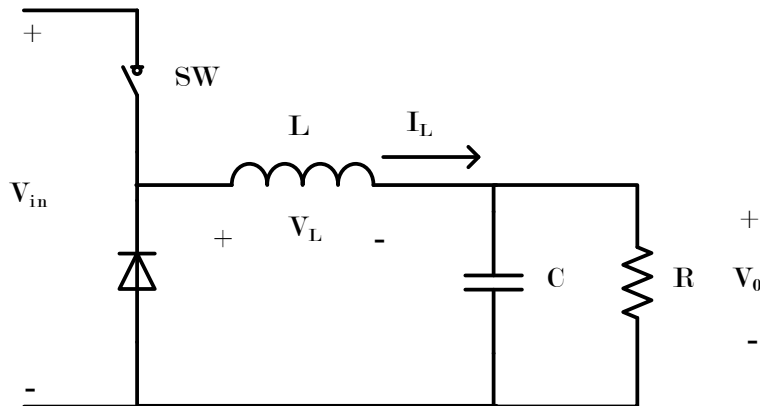


Figure 2.4: Hybrid APF, a combination of an shunt APF and an passive filter.

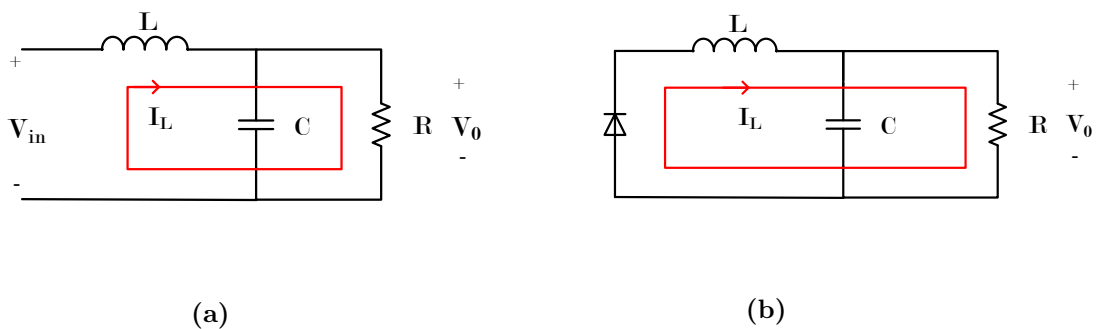
## 2.3 Buck converter

In the previous section, both series APF and shunt APF and their operation principle were presented and discussed. In both cases, switching devices are applied for the creation of the compensation quantity, therefore knowledge in the field of power converters is of great value. This section will cover the buck converter and the operating principles. The buck converter is illustrated in Figure 2.5 and it works in such a way that the voltage over the load is always lower in comparison to the input voltage. The voltage level is adjusted by changing the on ( $t_{on}$ ) and off ( $t_{off}$ ) times of the switches. The ratio between  $t_{on}$  and  $t_{off}$  is defined as the duty ratio  $D$ .



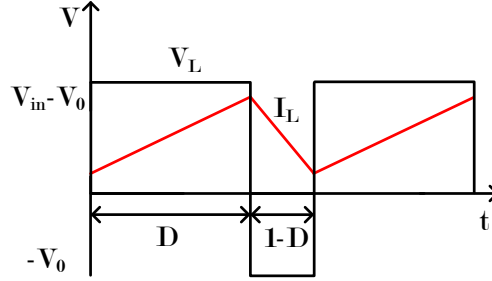
**Figure 2.5:** Buck converter.

There exists two switching states, one where the switch is conducting and the other one when the switch is not conducting. During the state when the switch is turned on, the inductor is energized in series with the load which results in a current flow that charges the capacitor and supplies the load, see Figure 2.6a. When the switch is turned off, the inductor is discharged through the load and the current flows through the diode as illustrated in Figure 2.6b.



**Figure 2.6:** Circuit states: (a) switch on (b) switch off.

The current flowing through the inductor and the voltage over the inductor during both switching states is illustrated in Figure 2.7. Because of the constant voltage applied over the inductor, the current is increased or decreased linearly under the circuit states.



**Figure 2.7:** The voltage over the inductor and its current.

The relation between  $D$ ,  $V_{in}$  and  $V_0$  of the buck converter can be explained by assuming that the the average voltage over the inductor is zero during one period as

$$V_L = \frac{1}{T_s} \int_0^{T_s} v_L dt = 0 \quad (2.2)$$

which expands to

$$V_L = \frac{1}{T_s} \left( \int_0^{DT_s} (V_{in} - V_0) dt + \int_{DT_s}^{T_s} -V_0 dt \right) = 0 \quad (2.3)$$

and results in

$$D = \frac{V_0}{V_{in}} \quad (2.4)$$

where  $V_{in}$  is the voltage on the source side and  $V_0$  is the voltage over the load. When the current in the inductor is continuously flowing, as in Figure 2.7 where the inductor current is greater than zero, the converter is operating in continuous conduction mode (CCM). In the case where the current does not flow continuously and reaches a state where it is zero, the converter is operating in a mode denoted discontinuous conduction mode (DCM).

## 2.4 Bidirectional converter

When the diode in the buck converter is replaced with a switch  $T2$ , demonstrated in Figure 2.8, the converter is able to conduct the current in both directions through the inductor. This ability is useful in situations when the load demand is varying and the converter can adjust the size and direction of the current. Because of this bi-directional current control, the converter is referred to as a bi-directional DC/DC converter [6].

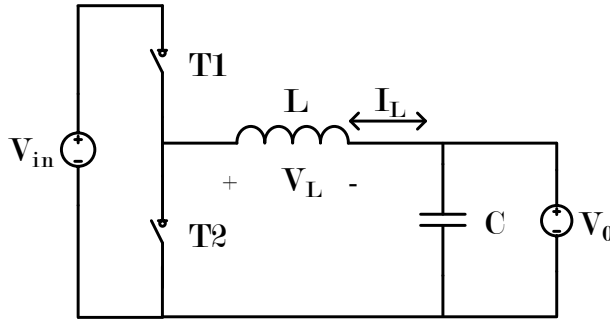


Figure 2.8: Bidirectional converter

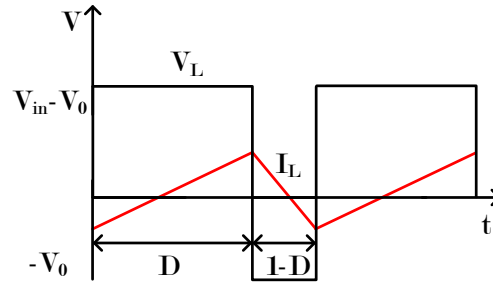
When two switches are used, the current can never enter the DCM state as would be possible if the switch  $T2$  were replaced by a diode. With the additional switch the converter is operating in forced continuous conduction mode (FCCM) and is forced to always have a current flowing in any direction in the inductor. The significance with FCCM is that the current through the inductor may change its polarity as illustrated in Figure 2.9. The advantage with FCCM is that the equations for CCM is valid to use because of the continuous conduction but the disadvantage is the negative impact on efficiency. If a converter with diode instead of switch  $T2$  would enter DCM mode, no power would be dissipated during the time interval  $t_{off}$ . But because the current in the inductor is always flowing during FCCM, the overall efficiency is impacted in a negative manner. The power loss equation for the diode is

$$P_{diode} = V_d(1 - D)I_0 \quad (2.5)$$

and for the switch

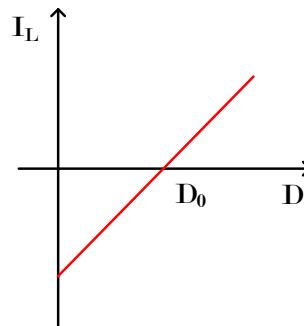
$$P_{T2} = I_0^2 R_{on}(1 - D). \quad (2.6)$$

By selecting a switch with low  $R_{DSon}$ , higher efficiency can be achieved in comparison with just using one diode. The drawback is the increased costs and complexity of the driver needed for both switches.



**Figure 2.9:** The current in the inductor when the converter enters FCCM

The current flow direction is adjusted by the duty cycle ( $D$ ) and in Figure 2.10 the average current as a function of the duty cycle is presented. At the point  $D_0$ , the average current through the inductor is equal to zero. This point is obtained by using the buck equation to calculate  $D$ , by varying  $D$  relatively to  $D_0$  the current can be controlled in the desired direction [6] [7].



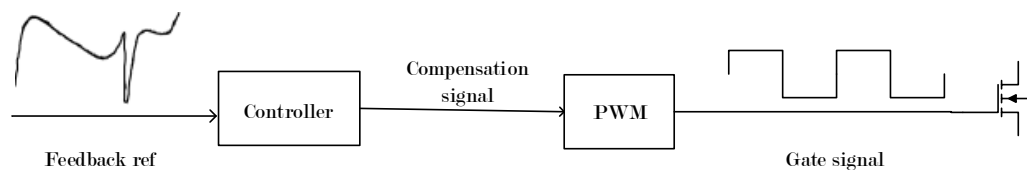
**Figure 2.10:** The average inductor current as an function of the duty cycle [6].

## 2.5 Control of active power filter

The strategy when designing a control for the APF is divided into three main blocks where the first one is to measure the current to the load. The second is to obtain a compensation signal from this current and the last step is to generate a signal to the switching devices.

There are different methods for sensing the current, for example with hall sensors, power transformers or by measuring the voltage drop over a resistor. In noisy conditions passive filters may be required to obtain a suitable signal as reference. The information of the current is then used as a feedback to the controller. The compensation signal is the signal processed by the controller to compensate for the ripple current to the load. The result of the calculated compensation signal is used to shape the outgoing switching signal from the PWM controller [2]. This compensation signal can be generated in both frequency and time domain. In frequency domain the signal is extracted using Fourier analysis and in time domain the compensation signal is derived using e.g. a P-I controller.

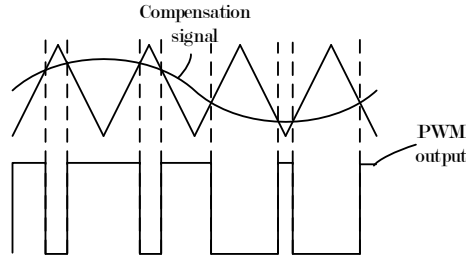
From the PWM controller the signal has the right square shape and duty cycle to switch the switches in the converter in the right way to obtain the desired current. Figure 2.11 visualizes the sequence from feedback reference to the generated gate-signal.



**Figure 2.11:** Control strategy

From the feedback signal, the shape of the current in the filter is calculated. To realize an opposite but equal current a switching signal is needed. To generate this signal to the switches, different methods can be used. The most common method is PWM where the switching pattern is generated by comparing the compensation signal with a triangle wave with fixed amplitude and frequency [2]. Figure 2.12 shows a visualization of the triangle wave compared with the compensation signal that is used to generate the PWM signal. Both triangle and sawtooth waveform can be used for generating PWM signals but in order to get a PWM that would not lag the analog signal a triangle wave is used for a better phase performance. The low-pass filtered value of the PWM signal is equal to the compensation signal voltage and that is the reason why this method can be used to control the switches [8].





**Figure 2.12:** PWM generation using an compensation signal.

## 2.6 Controllers

Regarding the implementation of a controller, a decision has to be made if a digital or an analog controller is to be used. Therefore it is crucial to know the advantages and disadvantages of both alternatives. The advantages with analog controllers are the high bandwidth, high resolution and simple simulation design. There are also component aging, temperature drift and the permanent design of selected components are hard to adjust. In comparison to the analog controller, the digital controller is not as sensitive to the environment, has a programmable solution and presents the possibility of implementing advanced algorithms. Drawbacks are present in the form of numerical problems and difficulties in design.

When using a digital solution to generate the compensation signal the reference current needs to be processed by a microcontroller unit (MCU). To generate the correct compensation signal from the MCU, the feedback signal first needs to be converted from an analog voltage to a digital value. This is done by using an Analog to Digital Converter (ADC). The ADC makes discrete values from an analog voltage with a finite resolution depending on the settings from the controller. The resolution of the conversion can be calculated as

$$\Delta V = \frac{V_r}{2^N - 1} \quad (2.7)$$

where  $\Delta V$  is the resolution of the voltage steps,  $V_r$  is the reference voltage range and  $N$  is the number of digital bits in the digital output. To obtain a high performance output signal, it is preferred to use the full voltage input range and use a controller with high amount of digital bits to make the step in the output values as small as possible.

This is important because digital controllers monitor the signals at discrete time steps and finite sampling rates, which gives that the sampling has to be done fast enough

so that important information is not lost. The signal processing has to be executed between two samples and too much delay in the calculation may lead to system instability. Processors that are not fast enough can use pre-calculated tables to compensate for their low processing speed.

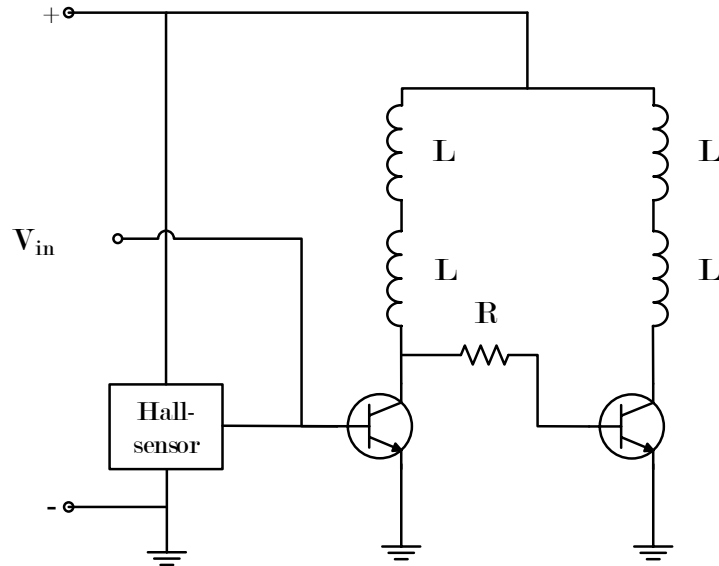
## 2.7 BLDC motor and its application

The source of the nonlinear current in this project is a pair of brushless DC (BLDC) motors implemented in a fan application. In the BLDC construction the rotor holds the permanent magnets and as a consequence causing trapezoidal magnetic flux, therefore electronics are required in order to shape the quasi-square current needed to achieve a torque ripple free performance. In Figure 2.13 a BLDC motor in a fan application is illustrated including the power electronics and hall-effect sensor. The BLDC from an electrical point of view is described using the following equation

$$V_{in} = Ri + L \frac{di}{dt} + k_m \omega_r \quad (2.8)$$

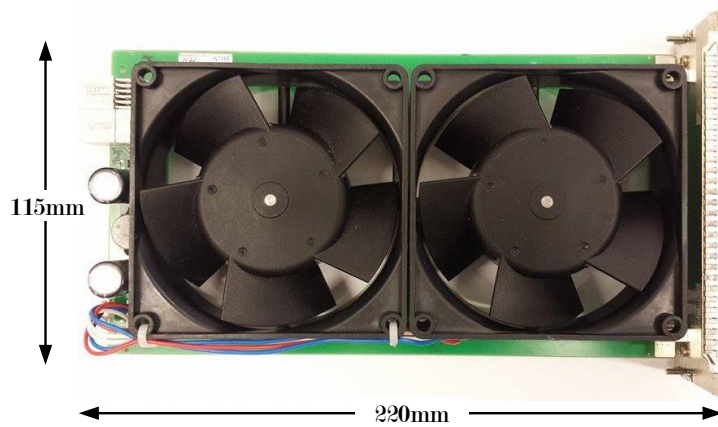
where  $V_{in}$  is the input voltage,  $R$  and  $L$  is the winding resistance and inductance respectively,  $k_m$  the back EMF and  $\omega_r$  the rotor speed.

The control of the BLDC motor is achieved by sensing the rotor position using a hall-effect sensor and further determines which stator coil that is to be energized. The commutation of the BLDC motor is carried out by applying a DC source over the stator coils in a predetermined sequential pattern. Because of the ability to use a DC-voltage as power source, the motor is referred to as a DC-motor. Because of the polarity change during each electrical cycle of the current in the coil it is effectively an AC motor [9][10]. In practical applications BLDC motors are more preferable in comparison to regular DC motors since they are more reliable. The reason is that no electrical connection is needed between the rotor and the stator. The need of a mechanical commutation is a disadvantage for the DC motor causing sparks, noise, interference and frequent need of service. The advantage that the BLDC motor gains in not needing a mechanical commutation is a large torque production capability which makes them suitable for direct drive applications. Even heat dissipation characteristics, operation speed, audible noise and power efficiency are improved by using a BLDC. The major drawbacks of the BLDC motor is the sensor costs and the complexity of the control technique. The control technique in combination with the needed power electronics to control the motor is the source of the nonlinear current shape generated by the motors.



**Figure 2.13:** General mechanical construction of a 4 pole BLDC motor including the power electronics and hall sensors

The fan system analysed in this report is schematically illustrated in Figure 2.14. The fan system consists of two separate BLDC motors equipped with fan blades and mounted next to each other on a printed circuit board (PCB) designed for a radio application. The motors are operating in parallel and connected to the bus voltage at 12V from the source and with a PF in between to attenuate the current ripple caused by the two BLDC motors.



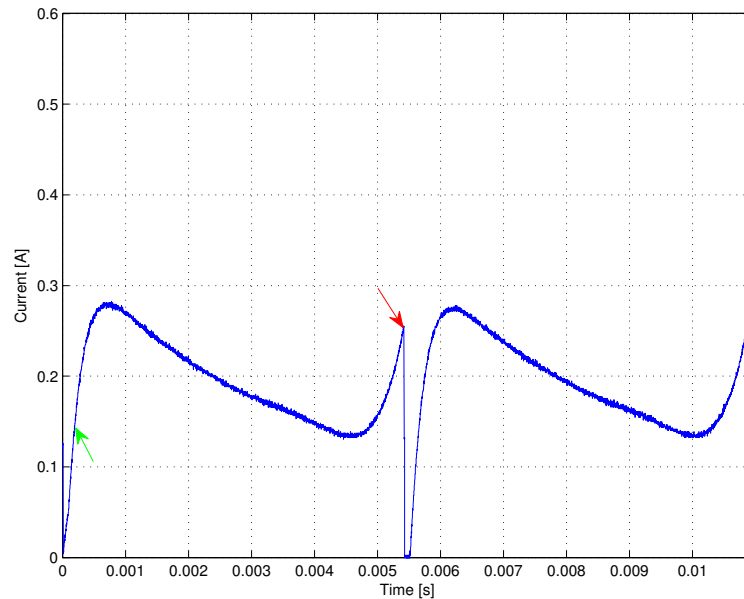
**Figure 2.14:** An illustration of the analysed fan system

In general, the datasheets of fans illustrate the airflow performances and similar but are lacking information regarding the current characteristics. The average current is presented but the shape of the current under one period is not described in detail. How the current may look like is presented in Figure 2.16 where the current drawn by two motors in parallel over two periods is illustrated which is measured from the particular fan used in this project. The shape but not amplitude of the current is the same for the whole operating range 7 – 15V. Technical and relevant information for the fan system used in this project is presented in Table 2.1 where the values originate both from the datasheet and from oscilloscope measurements.

**Table 2.1:** Fan system characteristics.

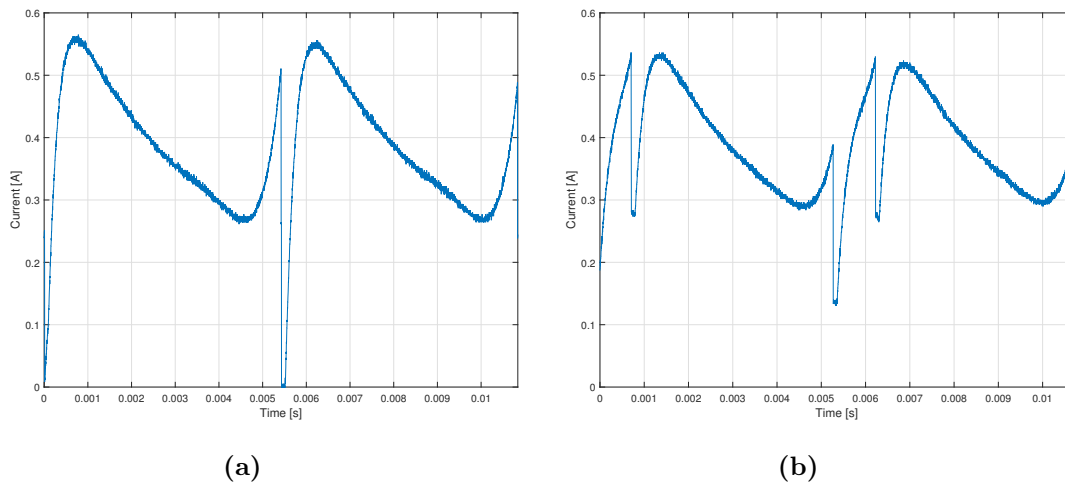
Nominal voltage	12 V
Voltage range	7 - 15 V
Average current	382 mA
Max current variation	570 mA
Peak current	600 mA
Fundamental frequency	180 Hz

The fan system is voltage controlled and works in such a manner that a constant voltage,  $V_{in}$ , is applied on the terminals of the motor which will lead to the dependence of the current being only on the term  $k_m$  in (2.8), where  $k_m$  is dependent on the speed of the rotor and the flux linkage. The positive derivative of the current in the first 0.5ms of the single fan in Figure 2.15, indicated with green arrow, is because of low  $k_m$  and later drops because of high  $k_m$ . The transient occurring at 5.5ms, indicated with red arrow, originates from the current commutation from one phase to the next phase.



**Figure 2.15:** Unfiltered current consumed by a single fan.

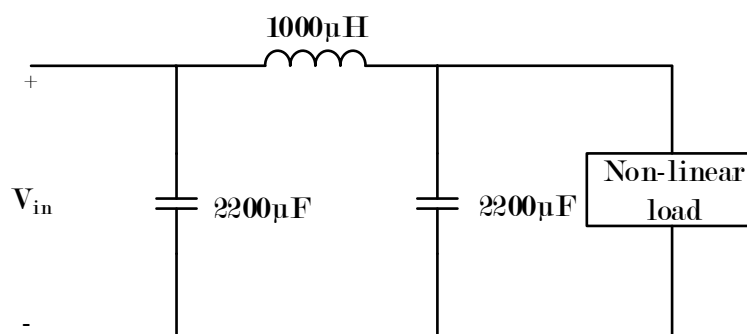
The reason why a system with two fans is analysed is because in an application of two parallel connected fans, the phase shift between them may not be constant but will rather vary with time. This is illustrated in Figure 2.16 where the unfiltered current from two parallel connected fans with slightly different speed is measured. Figure 2.16a illustrates the current drawn by the fans when they are in phase i.e. when the current is twice the amplitude of one single fan but with the same frequency as a single fan. This is the case when the peak current is the highest to the fans. When the current to the two fans is out of phase, the characteristics of the current from the source will be changed and can be seen in Figure 2.16b. The shape of the current to each fan will still be the same but the source will change continuously until they are 180 degrees out of phase again. At this moment the source current from the fans are with twice the frequency and different amplitude compared to when they are in phase to each other.



**Figure 2.16:** (a) two identical waves forms synchronized; (b) two identical waves unsynchronized.

## 2.8 Passive filter fan system

The filter used in the present design is a passive filter as shown in Figure 2.17 where the non-linear load is representing a fan system. The system consist of two capacitors of equal size and an inductor. All the components are fairly wide and a large footprint is used. The height of the electrolytic capacitors is a parameter that might be a problem if a small system is to be developed. The price of the components are low because of the simple manufacturing process and the common use of the components in other designs.



**Figure 2.17:** Schematic of passive filter connected to fan

# 3

## APF system

In Figure 3.1, an blockdiagram of the APF system is presented, including the fan system. The system consists of a converter, a storage device, a microcontroller, an analog controller and the measurement circuits.

For this application, the VSI shunt APF converter with a connected storage capacitor is concluded to be the most suitable. The voltage over the storage capacitor, that is included in the converter box in Figure 3.1, and the current drawn by the source are important quantities and are thus measured. The measured values ( $V_c$ ) and ( $i_m$ ) are used as the input for the microcontroller, where the output of the microcontroller is a compensation signal ( $e$ ) and operates as the input to the analog controller. The output of the microcontroller is a PWM type of signal and has to be filtered using an RC-filter so a smooth analog signal is supplied to the analog controller. The digital and analog controller combination is selected firstly because of its simplicity but also from the economical aspect where a cheap microcontroller can be selected. This combination results in a relatively easy calculation of the compensation signal and fast switching as a result of the analog controller. The converter switches are controlled with a gate driver which creates the desired switching pattern by creating two identical but opposite PWM signals to switch both MOSFETs. The converter delivers a compensation current ( $i_L$ ) into the fan system with the purpose of reducing the current ripple. In the analytical analysis of the APF system the state space average method is implemented to obtain the transfer function of the power stage. The derivation of the controller is limited to only suggest the type of controller that is suitable for this application.

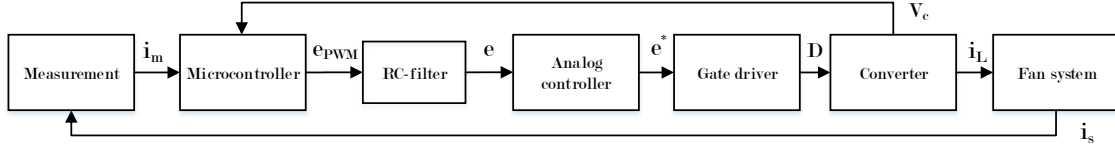


Figure 3.1: System overview

### 3.1 Measurement circuit

From a measurement point of view, the two quantities that are of great importance considering the functionality of the system are the nonlinear current and the voltage over the storage capacitor ( $V_c$ ). The nonlinear current is measured by the voltage drop over a small measurement resistor ( $R_m$ ) connected in series with the source. The small resistance results in a low voltage drop which has to be amplified. The *INA210* current-shunt monitor amplifier from Texas Instruments is used because of the simple and user friendly layout. Figure 3.2 presents how the current monitoring is performed and the structure of the device itself. The device has two inputs ( $-in$  and  $+in$ ) and one output pin (*OUT*). The input pins are connected over the measurement resistance and measures the voltage drop over the current resistor. The output is an amplification of the input by a factor of 200. Represented by an 0 – 5V signal which is connected to the input of the microcontroller.

The selection of the measurement resistor is done with respect to the current. The peak value through the resistor should represent the maximum output voltage of the amplifier for effective usage of the whole output range. Having a gain factor ( $G$ ) of 200 and peak fan current of almost 600mA (see Table 2.1) the output voltage becomes

$$V_{out} = GV_m = GI_{fan}R_m \quad (3.1)$$

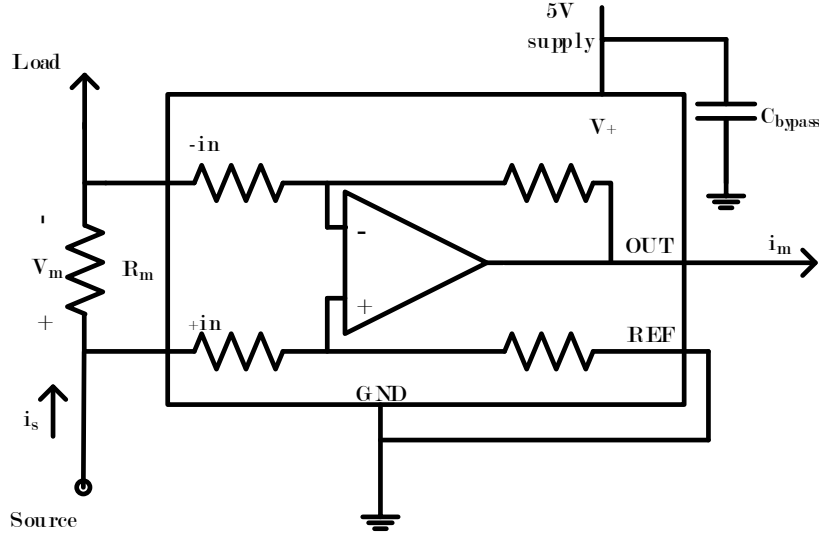
from which  $R_m$  is equal to

$$R_m = \frac{V_{out}}{GI_{fan}} = \frac{5V}{200 \cdot 0.6A} = 42m\Omega. \quad (3.2)$$

The resistance value will give an output of 5V when the current is at the peak value. The closest available value is 47m $\Omega$  and it is therefore selected for  $R_m$ . It is important to obtain a good resolution on the part around the average current rather than to the maximum peak value, thus an higher value is selected in comparison to the calculated one. Because critical information regarding the the charging and discharging of the storage device is obtained from the area around the average value. The voltage over



the storage capacitor ( $V_c$ ) is measured by directly measuring the voltage drop over the capacitor.

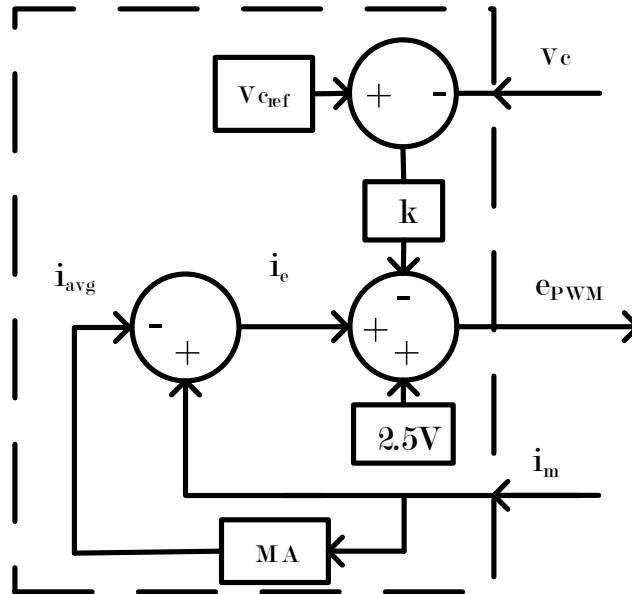


**Figure 3.2:** Operation of the amplifier INA210 and the performed current measurement.

## 3.2 Microcontroller

For gathering information regarding the state of the system in terms of current and voltages, a digital solution is preferred. The advantage is that a reduced size of electronic circuits for the measuring signals can be used, where measurement signals are filtered digitally leading to the overall size reduction of the filter [11]. The size reduction is achieved because of the lack of external PF needed to filter the noise and disturbances from the measurement signals which can be done digitally by implementing a filter in the software. To achieve a high frequency signal to the switches an analog controller is connected in series after the digital part and has the output of the digital solution as input. This improves the speed of the switching and simplifies the controller.

The purpose with the microcontroller is to create an error signal ( $e_{PWM}$ ) for the analog controller. This signal is calculated according to Figure 3.3 where the dashed line represents the microcontroller and  $i_m$  and  $V_c$  are the inputs and the output is the compensations signal  $e_{PWM}$ .



**Figure 3.3:** Calculations performed by the microcontroller

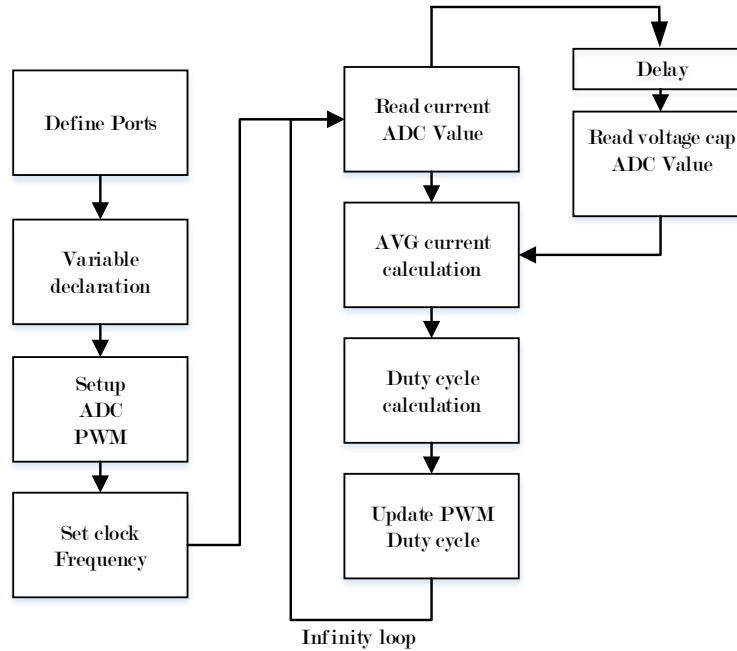
The in and outputs can also be seen in Figure 3.1 where the complete system is visualized. The first input is the measured current ( $i_m$ ) and from this signal an average value is created ( $i_{avg}$ ) by implementing an moving average algorithm. The moving average algorithm works in such a manner that a limited number of samples are continuously stored in an array. When a new measurement is performed, a new value is stored in the array and the oldest of the stored values is subtracted. The new sum is then divided by the total elements in the array and an average value of a finite time is used as an average value changing with time. This is an effective way of saving memory and to achieve a value that can be changed within a specific time period which will be useful in this application. An error signal ( $i_e$ ) is created by subtracting ( $i_{avg}$ ) from ( $i_m$ ).

The second input signal ( $V_c$ ) is an parameter used to modify the error signal ( $i_e$ ). The modification is necessary for the purpose of keeping the voltage variation of the storage capacitor in an range which is regarded as safe. The modification is performed by subtracting  $V_c$  from an desired reference ( $V_{c_{ref}}$ ). The result of the subtraction is multiplied with an sensitivity constant,  $k$ . The value of  $k$  is used as an tool for controlling the impact on the error signal ( $i_e$ ) and the result is the output ( $e$ ). The calculations needed

for the creation of ( $e$ ) are summarized as

$$e = (i_m - i_{avg}) - (V_{ref} - V_c)k \quad (3.3)$$

In Figure 3.4, the flowchart of the microcontroller is presented. When the infinity-loop is entered after the set of clock frequency, the value of the current is measured and an average value of the current is calculated. The voltage over the storage capacitor is also measured with an lower frequency. The reason why this measurement is not in series with the other events is because the rate of change of this value is much lower than the current change ratio and therefore only measured every 10th time. The slower update is illustrated by the delay box in the flowchart. When the information about the current and voltage is obtained the duty cycle is calculated and updated as an output signal to the analog controller. The ATtiny45 microcontroller from Atmel is found to be suitable because of its low cost and low complexity.



**Figure 3.4:** The microcontroller execution sequence

The output from the microcontroller ( $e_{PWM}$ ) is an PWM type signal with a amplitude of  $5V$ . The analog controller can not operate with an PWM type of signal and because

of this the signal has to be filtered. The filtering is performed using an RC-filter where the resulting signal  $e$  operates as the input to the analog controller.

### 3.3 Analog controller

The analog controller receives the compensation signal ( $e$ ) generated by the ATtiny microcontroller. The purpose with using the analog controller is to create a suitable control signal from the compensation signal which will control the switches properly. When selecting an analog controller, several aspects needs to be taken under consideration. The most important parameters are operation voltage, operation frequency, wide operation of duty cycle, PI- controlling opportunities and low amount of external components. The analog switch mode power supply controller *UC3843*, from the manufacturer Fairchild Semiconductor, was selected because it fulfills all the requirements. The controller has an output switching frequency of maximum  $1MHz$  which is more than needed for this application, a duty cycle of  $0-100\%$  and low amount of external components are needed. For this application, the controller switching frequency was set to  $450kHz$ . That is because a high switch frequency is necessary to keep the component sizes small and higher switching frequency presents higher switching losses. The structure and principal operation of the *UC3843* is presented in Figure 3.5 where the compensation signal  $e$  is the input,  $R_P$  and  $C_i$  are controller gain and integral parameters while ( $R_{sw}$ ) and  $C_{sw}$  are components used to set the switching frequency  $f_{sw}$ . The output is a single PWM signal with frequency  $f_{sw}$ .

Inside the controller in Figure 3.5 a basic visualisation of the operating principals are shown. The input error signal from the microcontroller is compared with an internal  $2.5V$  reference to determine if the actual value is above or below reference. The information is then compared with the oscillation signal to set the duty cycle of the output. The result is then compared in the logical OR gate to switch the transistors that is used to drive the output PWM signal.

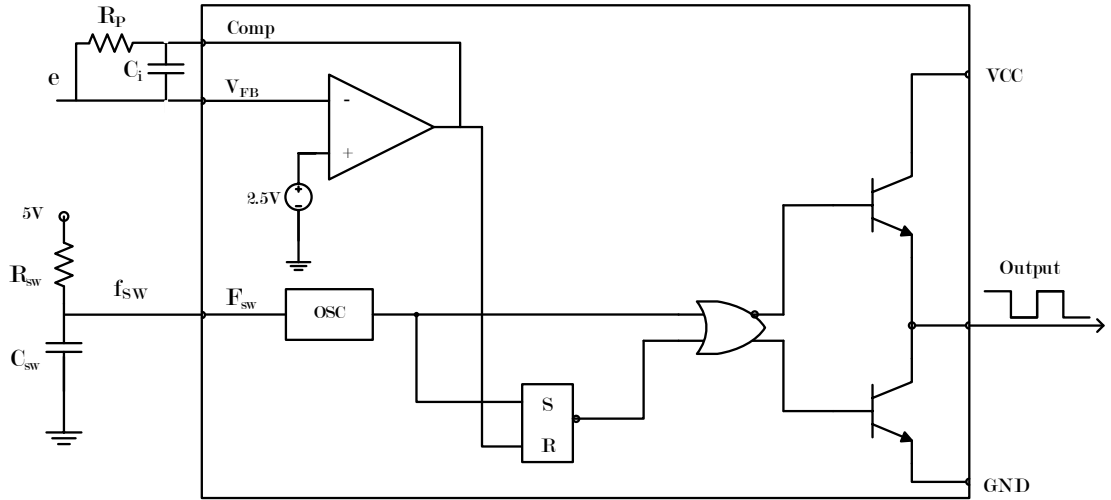


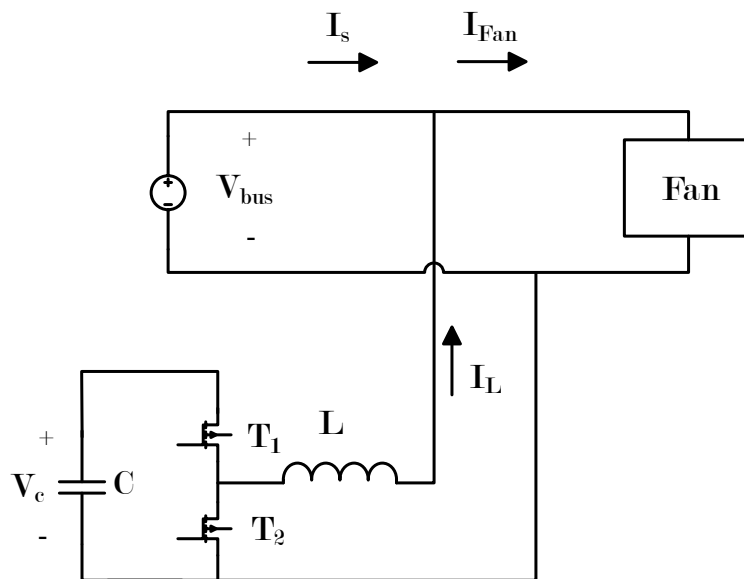
Figure 3.5: UC3843 operational structure

### 3.4 Switches and driver

The switches are important components in the converter and have a great effect on the performance. MOSFETs are selected as switching devices because they are the most suitable type of switching devices for low power application. When selecting MOSFETs it is important to analyze what voltage level that will be applied over them. For this application, it is important that the voltage rating is high enough because of the voltage variations that can occur in the storage capacitor. To be able to control the two MOSFETs in the converter, it is also a criteria to match a gate driver that is capable of delivering sufficient current. This is an additional restriction why the size of the MOSFET is of importance. The nature of the MOSFETs switching characteristics is that there will be losses during its switching, therefore it is of great importance to complete the switching sequence in minimum amount of time both during turn on and off. To achieve low switching losses large current pulses are needed for fast charging of the gate capacitor. Because of this and the fact that the the converter has a high- and low-side switch, a dual output driver circuit is needed. For this application, the requirements for the driver is the capability of delivering the necessary current to drive the MOSFETs synchronized and also a proper dead-time is needed. The dead-time function eliminates the possibility of a short circuit situation occurring during the switching transients of both MOSFETs. For this purpose a gate drive with single input signal and synchronized dual outputs including dead-time will be used. The TPS512604 gate driver from texas instruments is selected because it fulfils all the requirements.

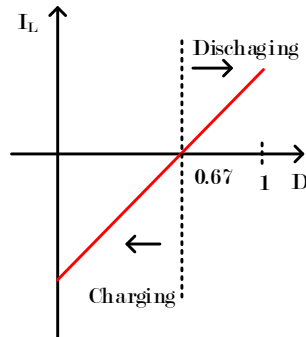
### 3.5 Converter

It is concluded that for this application, the VSI shunt APF converter is the most suitable topology. The shunt APF is fundamentally an bidirectional DC/DC converter with the only difference of the input voltage source being replaced by an storage capacitor, see Figure 3.6 where the converter and the fan system is presented.



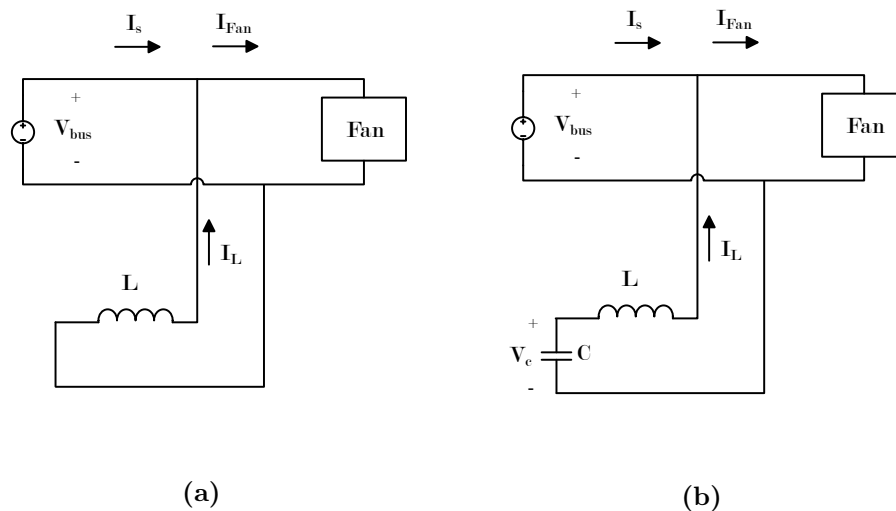
**Figure 3.6:** VSI shunt APF topology implemented in the fan system

The energy management in the capacitor is performed by varying the duty cycle according to Figure 2.10, resulting in the charging of the capacitor or discharging depending on the duty cycle ( $D$ ). With the duty cycle the average current flow is varied, the duty cycle is calculated using the buck equation (2.4). The output voltage in the equation is the fan systems operation voltage  $V_{bus}$ , 12V, and the input voltage is represented by the voltage over the storage capacitor  $V_c$ , 18V. The capacitor operational voltage of 18V is used because the voltage level over the capacitor should be 1.5 times greater than that of the output voltage of 12V, this to minimize the current ripple supplied from the converter [2]. This leads to the conclusion that the duty cycle  $D_0$  being equal to 0.67 will generate a current of 0A in average current. Values below  $D_0$  results in current being charged into the capacitor and the opposite yields for values above greater than  $D_0$  current is being discharged from the capacitor, see Figure 3.7.



**Figure 3.7:** Duty cycle relation to current direction

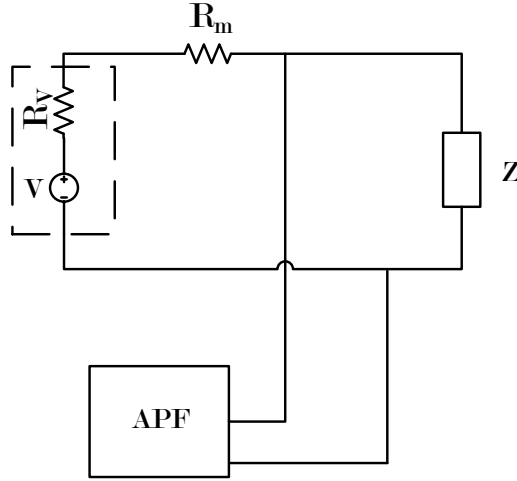
During the charging of the capacitor the switch  $T_2$  is conducting which results in the increase of the current through the inductor, see Figure 3.8a. This builds up a magnetic field in the inductor and when  $T_2$  turns off and  $T_1$  is conducting, the energy in the inductor is used to push the current into the capacitor  $C$ , see Figure 3.8b. The equivalent but opposite process occurs during the discharge of the capacitor.



**Figure 3.8:** Charging mode operation, (a) lower switch conducting (b) upper switch is conducting.

### 3.5.1 Analytical model

To extract an analytical model of the converter, some approximations have to be done. To start with, the load of the converter has to be determined which in this case is the system connected to the converter. What can be observed in Figure 3.9 is the voltage source on the left hand side illustrated as an ideal voltage source ( $V$ ) in series with an internal resistor ( $R_v$ ) and a measurement resistance ( $R_m$ ). The internal resistor is very small in comparison with the measurement resistor and can therefore be neglected. On the right hand side of converter is the load illustrated as an impedance because of the behaviour of the BLDC motor and to simplify the calculations.



**Figure 3.9:** A model of the loads connected to the filter

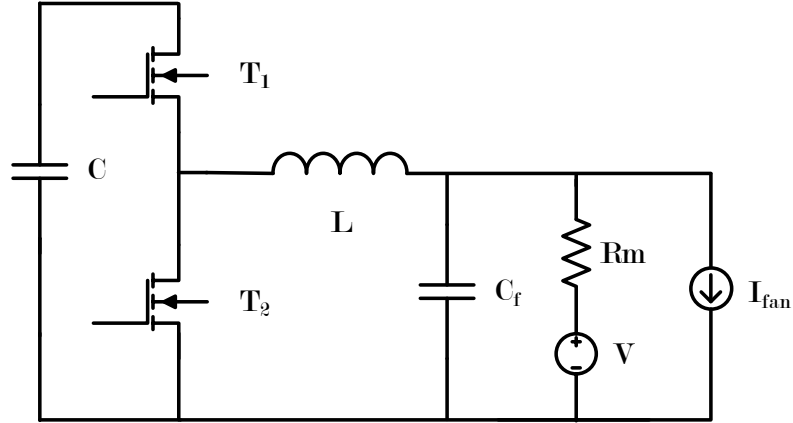
To approximate the fan impedance value, a calculation dependent on the voltage from the source ( $V$ ) and the current drawn by the fan can be performed as

$$Z = \frac{v_{bus}}{i} = \frac{\bar{V}_{bus} + \tilde{v}_{bus}}{\bar{I} + \tilde{i}} = \frac{\bar{V}_{bus}}{\bar{I}} = \frac{12V}{0.38A} = 31.6\Omega \quad (3.4)$$

where  $\bar{V}_{bus}$  is the DC voltage at the bus and  $\tilde{v}_{bus}$  is the AC ripple. The same nomenclature of AC and DC is for the current. In (3.4), the voltage ripple of the bus can be neglected in comparison with the substantially higher bus voltage and if the current is approximated to the average RMS fan current, the impedance will be significantly larger than the measurement resistance that is in the milli-ohm range. Because of the large difference in resistance between the fan impedance and the measurement resistance, the current from the APF can be approximated to only pass through the measurement resistance  $R_m$ .



in series with the voltage source. In Figure 3.10 the simplified system including the fans system is illustrated.



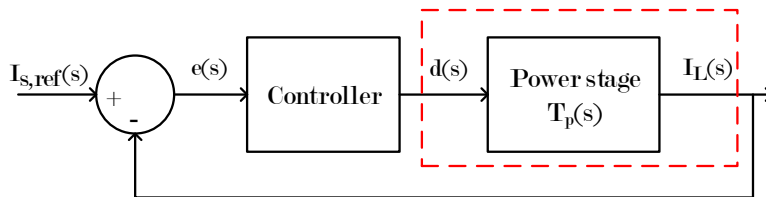
**Figure 3.10:** Schematic layout of the system where the fan is represented as an current source.

The fan system is assumed to draw a current shape that is independent of the output of the APF and is therefore implemented as a current source. On the output of the converter a voltage ripple will be present because of the voltage source in series with a resistor that will be affected by the regulation of the converter.

The goal of the analytical model is to extract a bode plot from the transfer function from which a suitable control type is obtained.

### 3.5.2 Transfer function

The construction of an analytical model is performed using the average state space method with the goal of obtaining the power stage transfer function ( $T_p(s)$ ) according to Figure 3.11. Once the  $T_p(s)$  is obtained a bode plot will be calculated from which a suitable type of controller will be selected. This information will be fundamental for the construction of the controller in the simulation environment in the next chapter.



**Figure 3.11:** Overview of the control block diagram

The procedure of the state space average method consists of four steps. The first is a state variable description of each circuit state according to

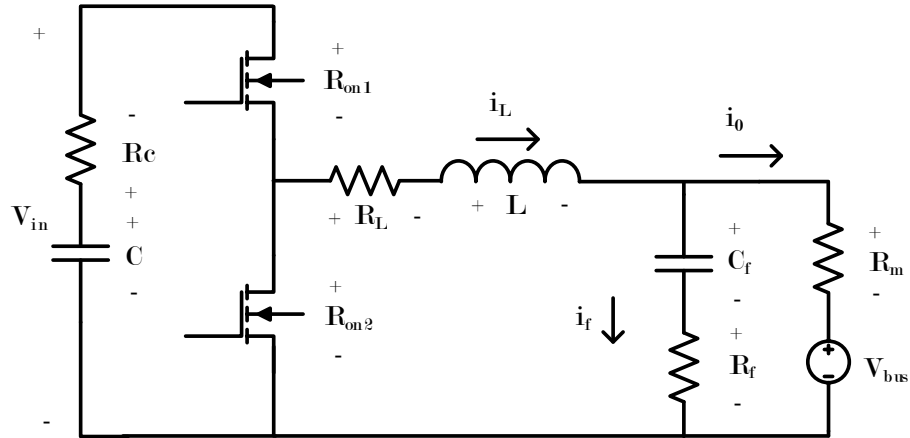
$$\dot{x} = \mathbf{A}x(t) + \mathbf{B}u(t) \quad (3.5)$$

and

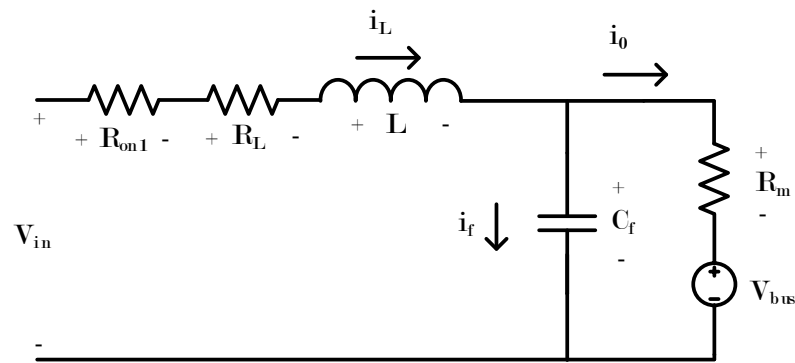
$$y = \mathbf{C}x(t) + \mathbf{D}u(t), \quad (3.6)$$

where  $\mathbf{x}$  are the selected states,  $\mathbf{u}$  and  $\mathbf{y}$  the input and output signals respectively and  $\mathbf{A}$  to  $\mathbf{D}$  are matrixes that define the state model. Secondly, the duty cycle is used as a tool to average the state space variables. Thirdly, implementation of small signal perturbation theory and finally the equations are transformed into the Laplace domain.

Figure 3.10 is the starting point for the analysis where capacitor internal resistances ( $R_c$  and  $R_f$ ) are added together with the inductor resistance ( $R_L$ ), see Figure 3.12. For the first state where the upper switch  $T1$  is conducting, the circuit is shaped according to Figure 3.13, where  $R_L$ ,  $R_f$ ,  $R_{on}$  and  $R_c$  are the inductor, output filter capacitor, MOSFET conductive resistance and the storage capacitor resistances. The output filter resistance  $R_f$  will be neglected in the calculations because of its low value. For reasons of simplicity, the voltage over  $C$  and  $R_c$  are also assumed to be constant. The assumption is made to limit the complexity of the analysis where otherwise three state variables needs to be taken account for. The validity of the assumption made will be verified in the simulations.



**Figure 3.12:** Model of bidirectional converter with component values



**Figure 3.13:** Model during state 1 where T1 is conducting

The first step is performed by describing each circuit state by applying basic circuit theory laws, where the inductor current and capacitor voltage are set as states, according to

$$\dot{x} = \mathbf{A}_1 \mathbf{x} + \mathbf{B}_1 \mathbf{u} \quad (3.7)$$

during period  $d$  and the remaining  $(1 - d)$  according to

$$\dot{x} = \mathbf{A}_2 \mathbf{x} + \mathbf{B}_2 \mathbf{u}. \quad (3.8)$$

Applying kirchoff's voltage law in Figure 3.13 the following equations are obtained

$$V_{in} - i_L R_{on1} - i_L R_L - \dot{i}_L L - i_0 R_m, -V_{bus} = 0 \quad (3.9)$$

$$i_0 = i_L - C_f \dot{V}_c, \quad (3.10)$$

and

$$V_c + R_m C_f \dot{V}_c - i_L R_m - V_{bus} = 0 \quad (3.11)$$

where the derivative of the inductor current is declared as  $\dot{i}_L$  and the derivative of the voltage over  $C_f$  is declared as  $\dot{V}_c$ . Equation (3.9) and (3.11), where (3.10) is inserted in both (3.9) and (3.11) for simplifying both expressions, are written in matrix form according to

$$\begin{bmatrix} \dot{i}_L \\ \dot{V}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_{on1}+R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_f} & -\frac{1}{R_m C_f} \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{R_m C_f} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{bus} \end{bmatrix}$$

where  $\mathbf{A}_1$ , which represents matrix  $\mathbf{A}$  for the first state, is identified as

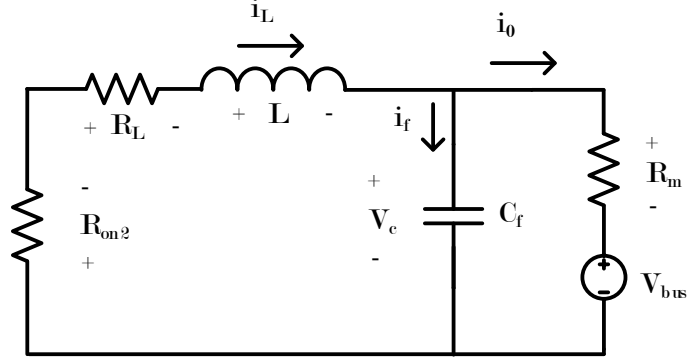
$$\mathbf{A}_1 = \begin{bmatrix} -\frac{R_{on1}+R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_f} & -\frac{1}{R_m C_f} \end{bmatrix}$$

and  $\mathbf{B}_1$  as

$$\mathbf{B}_1 = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{R_m C_f} \end{bmatrix}.$$

When comparing the circuit during the on and off state in Figure 3.13 and 3.14 it is observed that the only difference between them is the lack of voltage source ( $V_{in}$ ) during the second state  $(1 - d)$ . Resulting in the matrix  $\mathbf{A}_2$  equal to  $\mathbf{A}_1$  and  $\mathbf{B}_2$  equal to

$$\mathbf{B}_2 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{(R_m C_f)} \end{bmatrix}.$$



**Figure 3.14:** Model during state 2 where T2 is conducting

The inductor current is selected as the output because the goal is to obtain the transfer function from duty cycle ( $D$ ) to inductor current ( $i_L$ ) and is in matrix form equal to

$$i_L = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{bus} \end{bmatrix}$$

where

$$\begin{bmatrix} 1 & 0 \end{bmatrix}$$

is identified as both  $\mathbf{C}_1$  and  $\mathbf{C}_2$ .

To generate an average equation for the two different states of the model an average value is calculated by using the duty cycle as weight. By weighting the matrices  $\mathbf{A}_1$  to  $\mathbf{C}_2$  the new average states are

$$\dot{x} = [\mathbf{A}_1 d + \mathbf{A}_2(1 - d)]\mathbf{x} + [\mathbf{B}_1 d + \mathbf{B}_2(1 - d)]\mathbf{u} \quad (3.12)$$

and

$$i_L = [\mathbf{C}_1 d + \mathbf{C}_2(1 - d)]\mathbf{x}. \quad (3.13)$$

The next step is to divide the components into AC and DC component according to,

$$x = X + \tilde{x} \quad (3.14)$$

$$i_L = I_L + \tilde{i}_L \quad (3.15)$$

$$d = D + \tilde{d} \quad (3.16)$$

$$u = U. \quad (3.17)$$

In (3.17) the AC component is not included because of the assumption made of the voltage over the storage capacitor to be constant. Inserting (3.14) through (3.17) into (3.12) results in

$$\dot{\tilde{x}} = \mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{U} + \mathbf{A}\tilde{\mathbf{x}} + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (B_1 - B_2)\mathbf{U}]\tilde{d} \quad (3.18)$$

and additional terms such as products of  $\tilde{\mathbf{x}}$  and  $\tilde{d}$  are presented in (3.18) but are neglected.  $\mathbf{A}$  and  $\mathbf{B}$  in (3.18) are equal to

$$\mathbf{A} = \mathbf{A}_1 D + \mathbf{A}_2(1 - D) \quad (3.19)$$

$$\mathbf{B} = \mathbf{B}_1 D + \mathbf{B}_2(1 - D). \quad (3.20)$$

By setting the perturbation terms and their time derivatives to zero the steady state equation from (3.18) is obtained according to

$$\mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{U} = 0 \quad (3.21)$$

and applying (3.21) into (3.18) results in the following equation containing only the perturbations and time derivatives

$$\dot{\tilde{x}} = \mathbf{A}\tilde{\mathbf{x}} + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_{in}]\tilde{d} \quad (3.22)$$

Inserting (3.14) through (3.17) into (3.13) results in

$$I_L + \tilde{i}_L = \mathbf{C}\mathbf{X} + \mathbf{C}\tilde{\mathbf{x}} + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}]\tilde{d} \quad (3.23)$$

where

$$\mathbf{C} = \mathbf{C}_1 D + \mathbf{C}_2(1 - D). \quad (3.24)$$

Resulting in the small signal current equal to

$$\tilde{i}_L = \mathbf{C}\tilde{\mathbf{x}} + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}]\tilde{d}. \quad (3.25)$$

Transforming (3.25) and (3.22) into Laplace domain results in

$$\tilde{i}_L(s) = \mathbf{C}\tilde{x}(s) + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}]\tilde{d}(s) \quad (3.26)$$

$$s\tilde{x}(s) = \mathbf{A}\tilde{x}(s) + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)U]\tilde{d}(s) \quad (3.27)$$

which can be rearranged to the following form

$$\tilde{x}(s) = [s\mathbf{I} - A]^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)U]\tilde{d}(s). \quad (3.28)$$

where  $I$  is the identity matrix. After inserting (3.28) into (3.26) and dividing by  $\tilde{d}(s)$  one obtains

$$\frac{\tilde{I}_L(s)}{\tilde{d}(s)} = \mathbf{C}[s\mathbf{I} - A]^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)U] + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}]. \quad (3.29)$$

Applying  $\mathbf{A}_1$  and  $\mathbf{A}_2$  into (3.19) and  $\mathbf{C}_1$  and  $\mathbf{C}_2$  into (3.24) results in

$$\mathbf{A} = \mathbf{A}_1 \quad (3.30)$$

$$\mathbf{C} = \mathbf{C}_1 \quad (3.31)$$

which inserted in (3.29) result in the following transfer function from duty cycle to output current

$$\frac{\tilde{I}_L(s)}{\tilde{d}(s)} = \mathbf{C}[s\mathbf{I} - \mathbf{A}]^{-1}[(\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}]. \quad (3.32)$$

Calculating (3.32) using the software *mathematica* results in the power stage transfer function

$$\frac{\tilde{I}_L(s)}{\tilde{d}(s)} = \frac{(C_f R_m V_{in})s + V_{in}}{C_f L R_m s^2 + (L + C_f R_m (R_L + R_{on1}))s + R_L + R_m + R_{on1}}. \quad (3.33)$$

Equation (3.33) will later in the end of this chapter be used to generate a bode plot and further from the bode plot motivate a suitable controller. But first components and their values have to be selected.

### 3.6 Component calculation

When selecting components it is important to know the effect of each one of them. To get the desired performance from the converter, the components have to be matched together to obtain proper values. First of all the output current ripple needs to be determined. Because of the structure of the converter, the measurement signal can be seen as the voltage ripple source and the output ripple will directly affect the measurement performance. To minimize the impact of the switching in the filter, the current ripple from the filter is set to be 5% of the average fan current.

#### 3.6.1 Storage capacitor

The storage capacitor in the converter, see Figure 3.10, is an important component in the circuit and has great effect on the performance. To select a proper capacitor, several aspects have to be considered; the voltage level at which it operates, the voltage tolerance, the capability to store energy and discharge it with sufficient high frequency for the application and the voltage drop during the discharge period.

The voltage level is an important aspect, because of the varying load characteristic the charge and discharge current will vary and will affect the voltage over the capacitor. The storage capacity of the capacitor will have a great impact on the voltage variation during the charge and discharge period. In order to obtain a system that is not sensitive to slower regulation, a capacitor of fairly high storage capability will be used. To dimension the minimum required storage capacity needed to be able to operate correctly without a large voltage drop, the capacitance can be calculated as

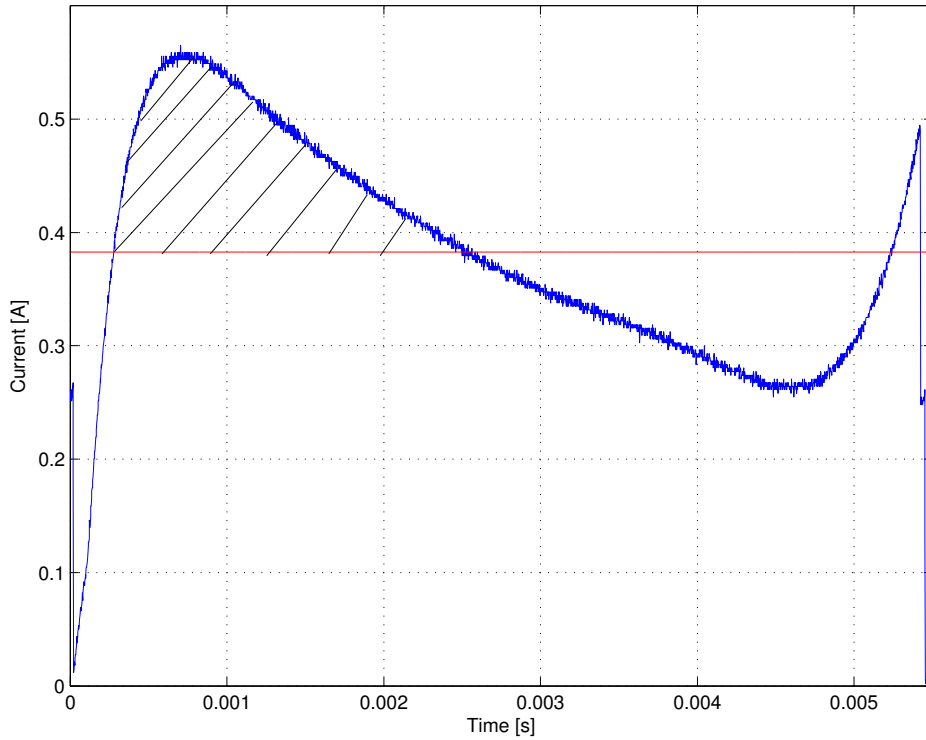
$$C = \frac{\Delta Q}{\Delta V} \quad (3.34)$$

where  $\Delta Q$  is the charges in one discharge period and  $\Delta V$  is the voltage drop during the discharge. The charge during a discharge period that the capacitor needs to be able to store is visualized in Figure 3.15. The figure illustrates the maximum current peak of current that occurs in the operation of the fan system and the area under the curve is equivalent with  $\Delta Q$  used in (3.34). The current presented in Figure 3.15 is the current that is supposed to be supplied from the filter to achieve a smooth current from the source. It is the current named  $I_L$  in Figure 3.6. This is a peak above average current and the curve shape is extracted by finding the highest peak value subtracted with the average current that is supplied from the source. The remaining current should be supplied from the storage capacitor calculated in (3.34) based on this assumption.

Too low energy storage capability will result in a complete discharge and the desired current can not be supplied to the system. Using (3.34), the minimum capacitor value is  $36\mu F$  if a voltage drop from  $18V$  to  $12V$  is considered and the calculated total charge under the current-time graph is  $216\mu C$ . The storage capacitor voltage level is of great



importance when the current ripple is to be kept as low as possible. The lower voltage difference between the storage capacitor and system voltage, the lower current ripple in the output of the converter. To get a voltage over the capacitor that does not fluctuate too rapidly, a capacitor value higher than the calculated minimum value is selected.



**Figure 3.15:** The current the storage capacitor should be capable of storing and supplying.

### 3.6.2 Inductor and output filter

The drawback by using switching devices is that they create harmonics with multiples of its switching frequency. These harmonics are present in the output current of the converter. To prevent the harmonics from propagating into the surrounding systems, a passive filter needs to be applied on the output of the converter to eliminate higher order harmonics. A capacitor is added after the inductor from the converter to form a low pass filter. This method is easy and stable but also capable of filtering higher order harmonics.

To calculate the values of the capacitor  $C_f$  and inductor  $L$  they have to be matched together. As mentioned before, the output current ripple from the converter is of great

importance and can not be too high. To set the ratings, the ripple current ( $\Delta I_m$ ) is set to be less than 5% of the average load current. The equation for determining the maximum current ripple in the converter inductor with a criteria of only 5% ripple in the load is calculated as

$$C_f = \frac{\Delta I_L}{8f_{sw}\Delta V_{buss}} = \frac{\Delta I_L}{8f_{sw}R_m\Delta I_m} \quad (3.35)$$

and rewritten to

$$\Delta I_L = 8C_f f_{sw} R_m \Delta I_m = 8 \cdot 22\mu F \cdot 450kHz \cdot 47m\Omega \cdot (380mA \cdot 5\%) = 70mA \quad (3.36)$$

where  $\Delta I_L$  is the peak to peak value of the inductor current,  $R_m$  is the measurement resistance and  $\Delta I_m$  is the maximum allowed peak to peak value of the ripple current through the measurement resistor. To match the capacitor  $C_f$  and  $L$  with each other, one of them has to be fixed while the other one can be calculated to achieved a good relation. The capacitor value of  $22\mu F$  is selected because of the reasonable size of both capacitor and inductor that is matched.

The minimum inductor value is calculated by using the inductor current ripple obtained in (3.36) according to

$$L = \frac{D(V_c - V_{buss})}{f_{sw}\Delta I_L} \quad (3.37)$$

which with inserted values becomes

$$L = \frac{\frac{12V}{18V} \cdot (18V - 12V)}{450kHz \cdot 70mA} = 127\mu H. \quad (3.38)$$

The inductance value is important because of the current stiffness in the inductor and to get a fast regulating system. This time is dependent on the derivative of the current ripple in the inductor which is the speed of change of the current during the switching phase. The speed of change of the current is dependent on the inductor value and needs to be considered during selection. Too small value will result is an inductor current that changes from one desired current level to another fast but with the side effect of high ripple current. An inductor of higher value will then give an inductor current with lower ripple amplitude but with longer regulation time.

### 3.6.3 Component selected

A summary of all component values calculated and extracted from datasheets are presented in Table 3.1. Based on these values, it is possible to use the transfer function previously derived to obtain its bode plot.

**Table 3.1:** Component values

Filter ceramic capacitor $C_f$	$22\mu F$
Filter capacitor resistance $R_{C_f}$	$1m\Omega$
Inductor $L$	$200\mu H$
Inductor resistance $R_L$	$1\Omega$
Measurement resistor $R_m$	$47m\Omega$
Storage electrolyte capacitor $C$	$100\mu F$
Storage capacitor resistance $R_c$	$1m\Omega$
Conduction resistance $R_{on1}$	$4m\Omega$

The integrated circuits that are selected to be used in the project are presented in Table 3.2 where the manufacturer for the used components also are stated.

**Table 3.2:** Selected hardware

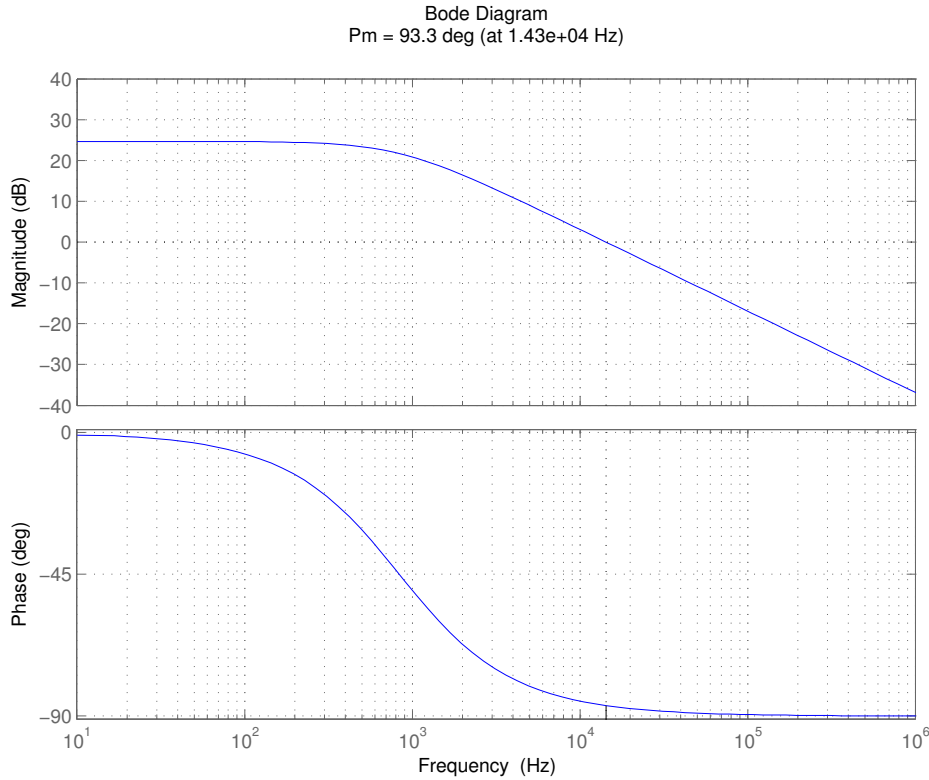
Component	Name	Manufacturer
Analog controller	UC3843	Texas Instruments
Digital controller	ATtiny 45	Atmel
Gate driver	TPS51604	Texas Instrument
Measurement amplifier	INA210	Texas Instruments
MOSFET T1, T2	SI4456DY	Vishay
Voltage regulator	KA7805	Fairchild Semiconductors
Converter inductor	A4223K	Epcos

### 3.7 Stability analysis

Applying the values from the different components of the system presented in Table 3.1 and inserted in (3.33) gives

$$T_p(s) = \frac{1.822 \cdot 10^{-5} \cdot s + 18}{2.024 \cdot 10^{-10} \cdot s^2 + 2.01 \cdot 10^{-3} \cdot s + 1.051}. \quad (3.39)$$

The bodeplot of (3.39) is extracted and presented in Figure 3.16, by analysing the behaviour of  $T_p(s)$  in the figure it is concluded that the transfer function behaves equal to an first order system despite being a second order system. The reason for this behavior is because the term  $s^2$  in (3.39) has negligible impact, the multiplication with  $2.024 \cdot 10^{-10}$  is the main reason. The impact of  $s^2$  is not noted until high frequencies, frequencies which are outside of the frequency range presented in Figure 3.16. From the same figure information of the phase margin is extracted, the phase margin of  $T_p(s)$  is  $93^\circ$  at the crossover frequency of  $143kHz$ .



**Figure 3.16:** Bode plot over the power stage in open-loop

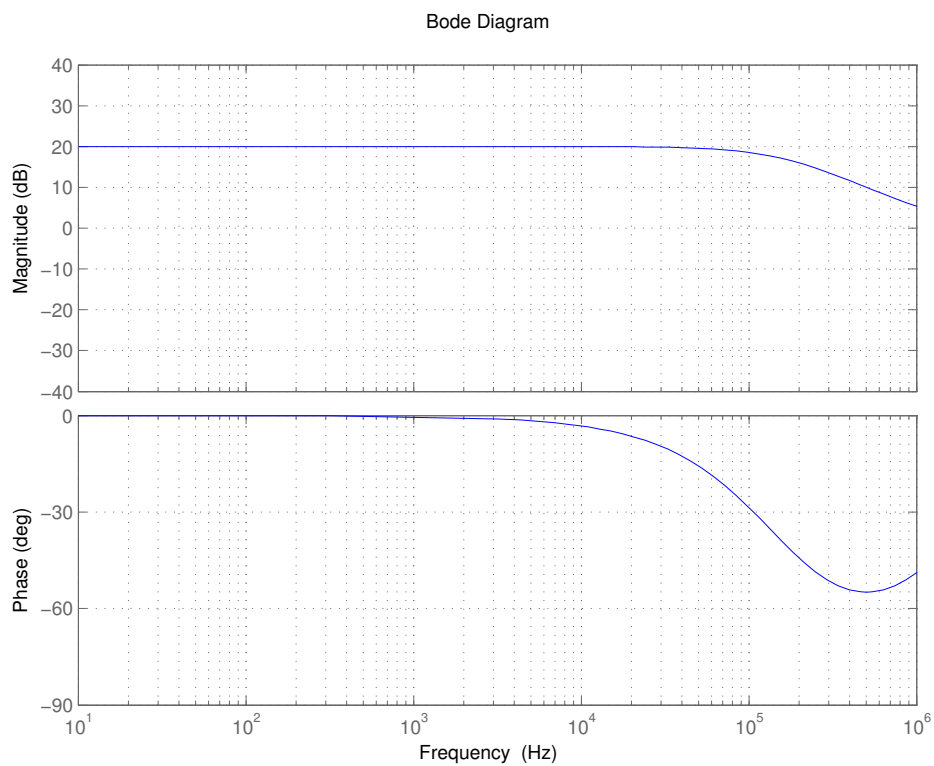
The open-loop transfer function of the powerstage with an compensated error amplifier should have high gain at low frequencies to minimize the steady state error in the output and an crossover frequency  $0.1f_{sw}$  of the switching frequency to allow the power supply to respond quickly to transients. Phase margin is the quantity which determines the transient response of the output voltage with respect to sudden changes in the load and the input voltage, a margin of  $45^\circ - 60^\circ$  is desired [8].

According to Figure 3.16 the phase margin is  $93^\circ$  which is outside the range of the desired phase margin. Too high phase margin results in a system with slow reaction to sudden changes and therefore the phase margin has to be lowered to the desired range of around  $45^\circ - 60^\circ$ . The desired phase margin is achieved by implementing a lag compensator, its transfer function is equal to

$$T_c(s) = \frac{\omega_p}{\omega_z} \left( \frac{s + \omega_z}{s + \omega_p} \right) \quad (3.40)$$

where  $\omega_p < \omega_z$  and represent the location of the pole and the zero respectively. The bode plot of the function  $T_c(s)$  is presented in Figure 3.17. Values of  $\omega_p$  and  $\omega_z$  are

selected so that an easy demonstration of its characteristics and its implementation with  $T_c(s)$  can be achieved. Its characteristic is that phase is subtracted from  $T_p(s)$  between the corner frequencies, in Figure 3.17 these frequencies are selected so they include the operational switching frequency of the powerstage  $T_p(s)$ . The amount of subtraction and the location of the corner frequencies is dependent on the location of the poles and zeros of the transfer function  $T_c(s)$ . This characteristic is suitable to be implemented on the transfer function  $T_p(s)$  of the power stage so that the phase margin of  $93^\circ$  degrees can be subtracted down to the desired range of  $45^\circ - 60^\circ$  degrees. The lag compensator is according to [12] a PI type of controller and is the reason for why a PI-controller should be implemented for this application.



**Figure 3.17:** Bode plot of the lag compensator



# 4

## Simulation

To predict the behaviour of the practical circuit a simulation model is developed. The purpose of the simulation is to give a deeper knowledge about the behaviour of the system and to simplify the practical construction by verifying components values. Two possible simulation programs for this application are Matlab/simulink from Mathworks and LTspice from Linear technology. An important part in this work is the control of the active power filter which is easiest implemented in Simulink. On the contrary, LTspice is the standard simulation software within Ericsson and it is selected as the main program for simulating the APF system even if the control is more complex to implement.

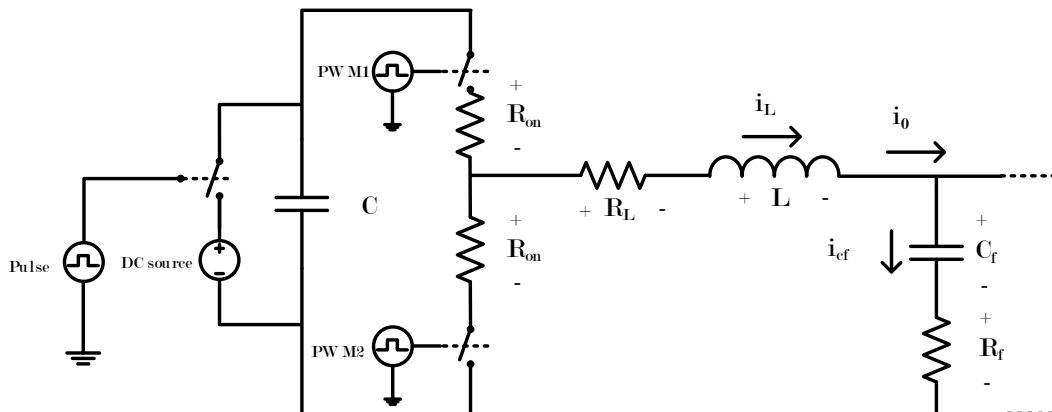
### 4.1 Implementation in LTspice

The implementation of the APF in a simulation is done to verify the theory in Chapter 3. The simulation is based on theoretically calculated values for the components that slightly have been modified to compensate for non-ideal operation. The system is developed to be as close as possible to reality where components are not ideal and where sampling frequency is limited. This is done by adding parasitical elements to the components used in the converter and by adding sample and hold circuits. By using these methods the simulations will more likely behave as it would in a practical environment and a more trust worth result is obtained. The final simulation schematic can be found in Appendix C.

The simulations are performed at the voltage level of 12V applied to the fan due to the fact that the behaviour of the fan current does not change with variations in operation voltage. The amplitude of the current is the only change when the operation voltage is varied. The shape and frequency of the current is remained the same during the voltage variation.

The simulation is divided into four main areas consisting of the converter, measurement,

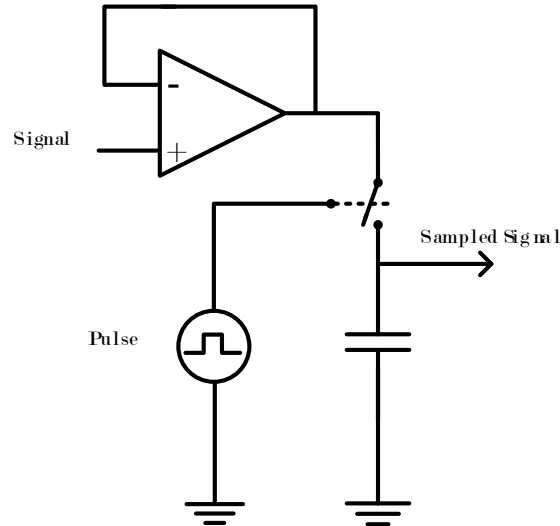
controller and load. In Figure 4.1 the power stage of the APF system is presented, where the output to the right is connected in parallel with the fan system and the left side is connected to the storage capacitor  $C$ . The storage capacitor in the simulation is connected to a separate voltage source and switch. The function of this setup is to simplify and speed up the simulation time by applying the operation voltage of the storage capacitor in the very first time period of the simulation. By doing this, the time for the system to stabilize will be much shorter without affecting the final simulation result. The simulation in this project will focus on a system during steady-state operation and excludes any start-up scenarios. In reality there will be very few startups during the lifetime of the system which is continuously operating for years.



**Figure 4.1:** Power stage simulation model

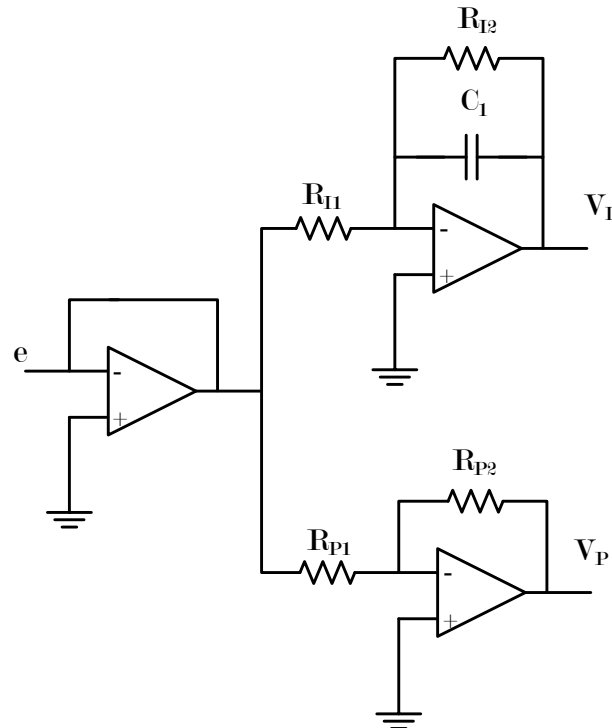
To control the converter the actual states in the circuit have to be analysed by first monitoring the system and then take necessary action to restore the preferred states. The monitoring of the system is implemented by measuring the current from the source and also the voltage over the storage capacitor. To mimic the practical environment as close as possible, sample and hold circuits are implemented. These circuits operate at the same sampling frequency as the selected microcontroller. In Figure 4.2 the sample and hold circuit is illustrated and the functionality of it is to take a sample and store that value, in this case a voltage, until the next sample is taken. To store a voltage level the switch is operated by a pulse generator and the capacitor is stored with the actual voltage that is applied when the switch is opened. When the switch is not conducting, the voltage level is kept constant over the capacitor. This value is then used as reference until next sample is taken. The criteria to use this application is that the connection point to this capacitor has high resistance value so the capacitor is stable at the specific voltage level during one cycle and not discharged.





**Figure 4.2:** Sample and hold circuit

The sampled voltages obtained from the sample and hold circuits are processed using arbitrary voltage sources since they are able to perform the desired mathematical operations, see Figure 3.3 that illustrates the calculations needed for obtaining the reference signal. The output of an arbitrary voltage source is the result of the mathematical formula expressed in a voltage level. The output signal  $e$  of the arbitrary function is in this case used as the error input signal for the controller. The usage of a lag compensator, a PI type of controller, is motivated in Chapter 3.7. The PI controller is implemented by using operational amplifiers and is illustrated in Figure 4.3. The operational amplifiers also operate as a substitute for the *UC3843* which is used in the practical implementation but not able to implement in the simulation program. By using the operational amplifiers in combination with the arbitrary voltage source, a duty cycle is calculated by using the voltages  $V_I$  and  $V_P$  in combination with the duty cycle obtained from the buck equation and then compared with a triangle wave as reference. This operation generates two PWM signals with opposite polarity which then are used for the two MOSFETs in the converter power stage.

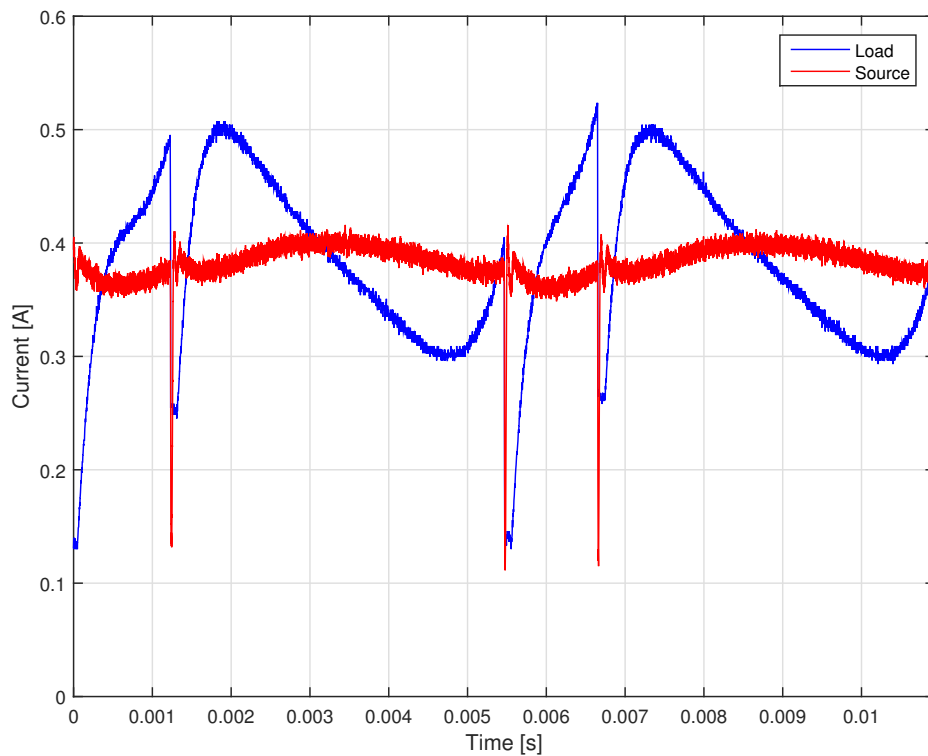


**Figure 4.3:** Operational amplifier PI-controller

The simulation of the load behaviour is performed in such a manner that practical measurement data from two BLDC driven fans is implemented as a data file and therefore a pre-determined current is used as load. This is preferred to make sure that the regulation system will be able to compensate for a similar load characteristic which is used in the practical environment. When the whole system is connected as one unit the PI-controller has to be tuned. There are several ways to tune a PI controller but a strategic and useful method is performed by using the Ziegler-Nichols method [13]. This is a common method used for tuning regulators connected to the system that should be controlled. The tuning is done by adjusting the values of the resistive and capacitive components in the OP-amp circuits in Figure 4.3 according to the criteria specified in [13]. A brief introduction to the parameter extraction method is to start by removing the integrating part of the controller and increase the gain until a constant oscillation is obtained in the loop. The period time of the obtained oscillation is measured and used to get the parameter value for the integrating part. The extracted information is then weighted to get the proper value to the gain and integration parameters. The result of the tuning is a gain factor of  $K_c = 14.5$  and a time constant of  $T_I = 48\mu s$ .

## 4.2 Results

The simulation result is presented in Figure 4.4 and it is clearly seen in the source current that the APF system fulfills its purpose by minimizing the nonlinear current seen by the source. This is so because the APF system manages to recreate almost the identical nonlinear current the load is drawing but phase shifted  $180^\circ$  degrees. As seen in Figure 4.4, spikes are present in the source current when the current to the fans makes a quick decrease in amplitude. This is partly a result of a regulation system that is not designed for compensating differences of this amplitude but also because of the size of the inductor in the filter where the current is not able to change instantaneously.



**Figure 4.4:** Comparison of the load current, in blue, and the source current, in red, during the operation of the APF.

The gain and time constant implemented in the PI regulator circuit gave a reasonable result for the simulated current step. The result of adjusting the integration part of the controller to the fast changes in the current waveform makes low frequency compensation limited. Because of this, the capability of keeping the current steady at one level is restricted and the current is varying with low frequency as can be seen in Figure 4.4.

To verify the calculations used for selecting the inductor ( $L$ ) and the capacitor ( $C_f$ ), the selected values of  $200\mu H$  and  $22\mu F$  are compared to the simulations. These values are used because they are closest to the standard values available for inductors and capacitors. The inductor current ripple should according to (3.37) be  $44mA$  which is also the result of the simulations. The capacitor  $C_f$  should dampen the inductor current ripple and as the simulation show, the calculated outgoing ripple ( $\Delta I_m$ ) when an inductor of  $200\mu H$  is used becomes ( $12mA$ ) as calculated with (3.35). These calculations indicates a validity of the simulation so that what is obtained from the simulations are reasonable results. Also, the simplifications made in the derivation of the transfer function regarding the voltage over the capacitor being constant and therefore setting it as  $V_{in}$  has shown to be an good assumption according to the simulation.

# 5

## Practical

The practical solution is realized on a PCB by first designing the circuit in a circuit design program. The final layout of the schematic can be seen in Appendix A1.

### 5.1 Printed circuit board and prototype

To compare the simulated results with reality, a prototype card was built. The design of the layout is of great importance because it has a great impact on the performance and functionality of the components in the layout. Aspects to consider during the design is the placement of components because of their effect on the surrounding components but also how the wires should be routed to avoid the creation of or picking up disturbances. To minimize the disturbances in the signal wires a separation from the power components is done by using two separated ground planes on the PCB, one for power components and one for sensitive signals. In the power ground-plane, the switches, gate driver and the analog controller are included. In the signal ground-plane the measurement circuit, micro controller and the voltage regulator are included. To make the analog controller (*UC3843*) more flexible it is equipped with a potentiometer between the *COMP* and  $V_{FB}$  pin, making the calibration of the gain constant easier. The final design is presented in Figure 5.1.

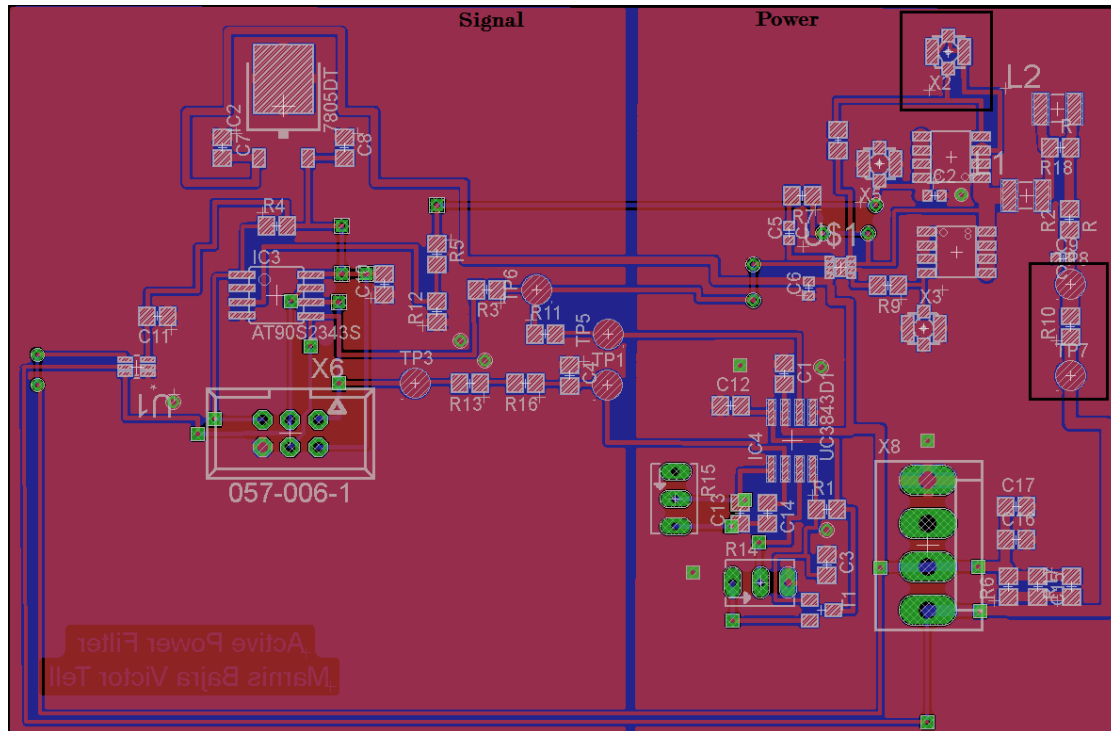


Figure 5.1: PCB design created in eagle

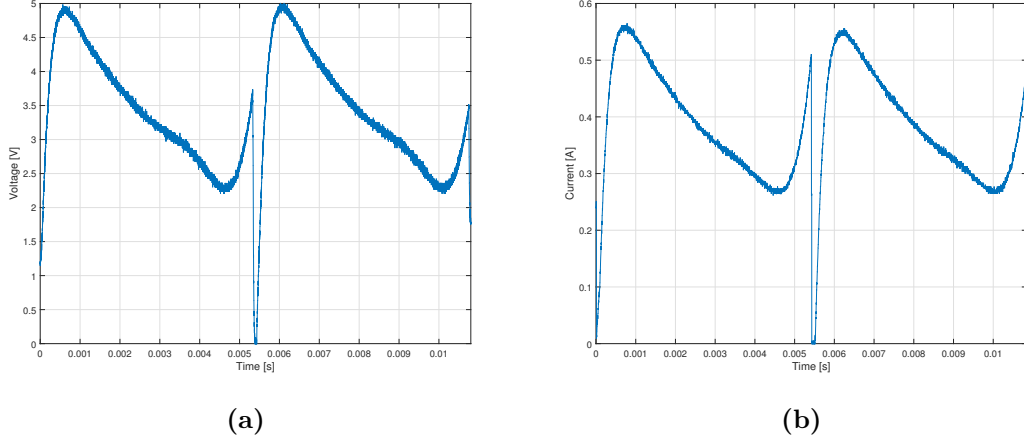
## 5.2 Practical implementation and result

The PCB was mounted with components according to the calculated values and components selected in table 3.1. Each subsystem is separately verified and tested before the entire system is connected together.

To obtain a disturbance free current sensing signal, the layout in Figure 5.1 had to be slightly modified. The modifications were necessary because the sense wire in the layout is connected through the input power pin, on component X8 in Figure 5.1. This resulted in a disturbed signal and the connection to the OP-Amp, (U1), was replaced by external cables. An easy fix which resulted in a vast improvement.

In Figure 5.2 a comparison between the measured load current signal to the left used in the practical implementation and the one used in the simulation to the right. Both are illustrations of an unfiltered current consumed by the fan. The one used in the simulation is measured with a current clamp meter and the one from the practical implementation is measured with the amplifier circuit *INA210* that amplifies the voltage drop over a resistor that is located in series with the load. The output from the amplifier is a voltage between 0 and 5 volts and as can be seen by observing the curves there are no disturbances by using the voltage drop over a resistor as current feedback to the microcontroller. This measurement result from the amplifier is of great quality and it

can be confirmed that the measurement circuit is operating well and the feedback to the controller circuit is correct.



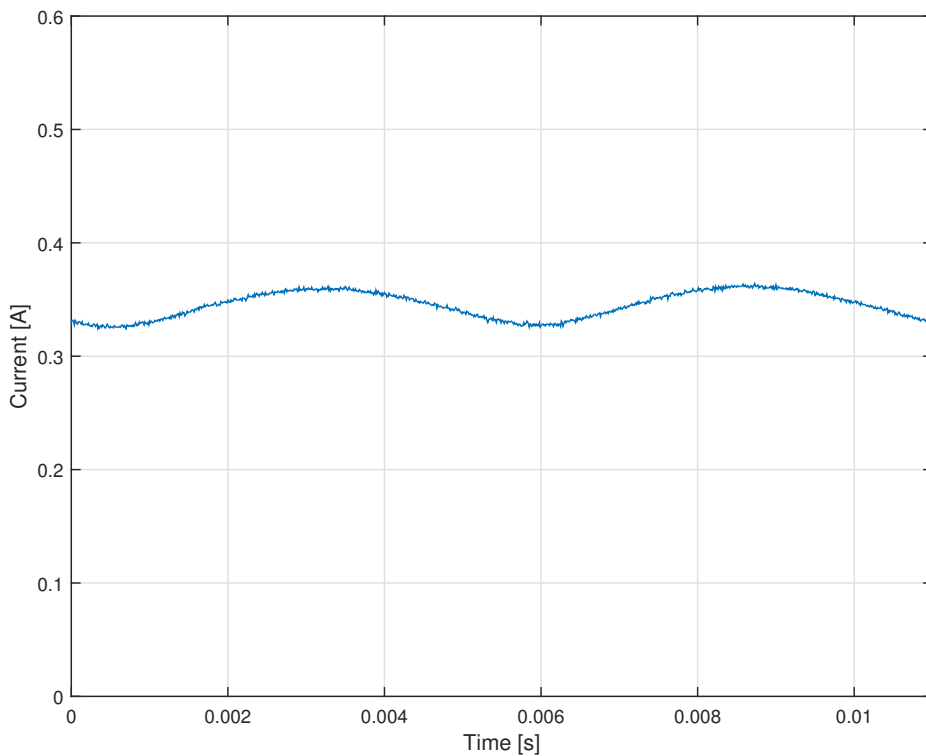
**Figure 5.2:** Unfiltered fan system current measured with (a) INA210 and (b) oscilloscope.

The microcontroller's logical functions including moving average and the calculation of the output reference signal operate as desired and was verified by observing a slower signal while the output was measured with an oscilloscope. Because the output of the microcontroller is a square wave signal that had to be smoothed out using an RC-filter, a weighting problem occurred between phase-shift and current wave-form. An RC-filter with lower crossover frequency contributes to higher phase-shift in the region above the crossover frequency, which includes the desired higher order harmonics. High crossover frequency result in low phase-shift but in turn a distorted waveform. The result of using this type of filter for filtering a square wave signal was not as accurate as needed for the application. The result of the filtering is a voltage in shape of a triangular wave that goes up during the high voltage period and down during the low voltage period. The ideal averaging filter would maintain a constant voltage during both on and off period at a level of the average voltage during one period of the square wave. The result of using this filter is that the fluctuating average feedback voltage from the RC-filter to the analog controller was too unstable to be able to operate as a decent power stage controller. The information about the actual average value was hence of too low quality to operate the converter at and the PWM signal from the controller was not representing the desired signal for a proper regulation.

The analog controller performed as desired where the output switch signal to the gate driver made both upper and lower switches perform in a synchronized manner including dead-time. The switching of the MOSFETs is executed very close to the simulated switching manners of the APF, further proving the simulation model equal to the practical environment. The switching frequency was verified to be similar to the theoretically calculated value.

The power circuit of the APF converter operates as expected and the verification was done by setting  $18V$  as the input over the storage capacitor and applying a switch signal with a duty cycle of  $0.66$  which according to (2.4) should deliver a  $12V$  output voltage. The result was satisfying with  $12V$  at the output and with only a small switch ripple present. The dead-time implementation in the switches was measured using the oscilloscope and found out to be working according to the datasheet specifications for the gate controller.

It was of interest to measure and obtain the performance of the present PF filter solution, presented in Chapter 2.8, so that a comparison of the proposed APF system and the PF solution could be possible. The performance of the PF in the present fan application, presented in Chapter 2.8, is illustrated in Figure 5.3. In the Figure the source current is illustrated and has a varying amplitude of  $40mA$ . Because of there are two fans connected in parallel, illustrated in Figure 2.14, the current consumed by them both consists of a varying amplitude because of the two fans are not rotating with the exactly same speed.



**Figure 5.3:** High frequency ripple of the PF current upon an low frequency ripple.



### 5.3 Cost and size comparison

To compare the PF in the present fan application with the proposed APF solution a cost and size comparison is also done. The comparison is based on the price of each component used in each filter based on the list price of 1000 pieces or as close as possible to make the comparison as similar as possible. The prices used for doing a fair comparison are found at Farnell which is a widely known electronic component dealer.

The size comparison is done by calculating the total footprint size of each component separately and then summarized together with all the component used in each layout to be presented as a total area. The size of the components can be seen in Table 5.1 where a comparison is made. In the calculation there has not been any consideration regarding connection between components and hence the wire routing area which increases with the amount of components.

**Table 5.1:** Size comparison

Passive filter Comp.	Quantity	à $cm^2$	Active power filter Comp.	Quantity	à $cm^2$
Capacitor	2	1,13	Microcontroller	1	0,425
Inductor	1	1,77	Voltage regulator	1	0,68
			Controller	1	0,36
			Gate driver	1	0,04
			Measurement AMP	1	0,06
			MOSFET	2	0,325
			Inductor	1	0,25
			Resistor	7	0,02
			Capacitor	11	0,02
			Measurement Resistor	1	0,18
			Transistor	1	0,09
Total area		4,03	Total area		3,095

The PF in the left column consists of a few but large components of common presence in electric circuits and as a result a large but cheap construction is achieved. As seen in Table 5.1, the PF is 30% larger in footprint size. The passive filter is large in footprint size but also in volume because of the large capacitors. In comparison with the APF the price of the APF is 6.8 times higher than the passive solution if the layout of this practical solution is used. The high cost of the APF is mainly due to the price of the microcontroller that is 27% of the total price of the APF. In comparison with the passive filter the microcontroller is twice as expensive as the whole passive filter solution which indicates that the microcontroller highly affects the price of the filter.



# 6

## Discussion

The topology proposed to be used as an APF seems to be a suitable choice. This is because of the flexible way of controlling the current in two directions with only one main PWM signal, from this PWM signal the gate driver controls both MOSFETs present in the APF converter. The few components needed for the design is also a contributing aspect if a small system is to be developed. The APF system presented in this report has the potential to decrease the implementation height compared to the passive filter used today. The main reason is because the bulky capacitors used in the present design could be replaced by smaller storage capacitors optimized to the energy storage needed during a full charge and discharge period of the current in the APF. Because of the smaller component size it is easier to adapt to the surrounding circuit board design and the components making the APF suitable for applications where installation is limited in height. To further decrease the footprint size the analog controller should be excluded from the system and a fully digital controller should be implemented in the microcontroller.

Simulations show that the constructed APF system is a good representation of theoretical values and the current is clearly more stable when the APF system is connected to the fan system in comparison to a system without any filtering. Because of the implementation of non-ideal components, a controller built with OP-amps and the implementation of sampling circuits the simulation model can be considered to be fairly representable of the practical circuit. The implementation of the ideal current source instead of a complete load representation of the fan could possibly have a minor effect on the simulated result. On the other hand, the estimation that the load of the fan is very large in relation to the measurement resistance and the assumption that all the current from the filter flows through the measurement resistor should still be reasonable.

To tune the PI-regulator and to achieve good control of the current the Ziegler-Nichols method was used. The values of the regulator parameters had to be tuned two times using the Ziegler-Nichols method. The tuning process was first optimized for a single

current step similar in step size to the step in the load current in Figure 5.2. A second adjustment had to be done to achieve a proper regulation for the overall current shape and not only the single step event. This was necessary because the current contains both high and low frequency variations. Because both these were present, the tuning of the filter was adjusted to dampen the highest frequencies and therefore the integration time of the controller is adjusted to a fast response for a single step event. This resulted in lack of integration time and the low frequency variations were still present. This might be compensated by implementing a second integration with a longer integration time to compensate for the low frequency variations in a future improved version.

The practical result that was achieved is that every subsystem did operate well but not as a complete system. A fully functional system was not able to be established because of limitations in the microprocessor and poor digital to analog filtering quality. To achieve a functional system, the relation between the frequency of the feedback signal from the microprocessor to the analog controller has to be matched with the digital to analog filter in between. Because of all the information to process in the microcontroller and to generate a PWM signal based on this a relatively low output frequency of  $31.7kHz$  was generated. Due to this low frequency, the time constant on the passive filter had to be large to keep the signal to the controller smooth without ripple from the PWM shape. Because of the large time constant, the filter response became insufficiently slow and the ability to control the system from this signal was not possible.

When the frequency of the PWM signal was increased to levels above  $31.7kHz$  a modification had to be done in the setting of timers in the microcontroller. This led to a conflict between the measurement sampling and PWM signal which resulted in a output signal being distorted. Because of this, the system was only able to work at low frequency resulting in improper regulation capability.

Due to time limitations; the soft start function of firstly charging the storage capacitor to a suitable voltage level prior to regular operation was not implemented. Because of the same reason an external voltage source was applied over the storage capacitor to keep the voltage at a steady level and to lower the complexity of the voltage regulation. With this solution, the voltage level was held in an safe range.

The ability of possibly applying an APF solution to other fan systems and expecting a good performance is high. The reason why the method is preferred is because very limited information about the current behaviour is needed. The information that is needed is only for the component size selection and switching frequency in the installation of the filter while the shape during operation is real time compensated by the regulator. This makes the system flexible and easy to be implemented for a wide range of applications.

The main difference is the fast current drops that occur in the APF because of slow regulation. This type of spike contains a higher order harmonics and can be hard to filter. This will result in a disturbance that propagates into the rest of the system. In comparison with the performance of the PF solution, presented in Figure 5.3, the

current has a smoother shape and will therefore not contribute with the same amount of disturbances.

Comparing the source current ripple of the PF system presented in Figure 5.3 and the source current of the simulated APF system, see Figure 4.4, only minor difference are observed. The differences are the present of spikes in the source current of the APF system. The comparison it not righteous because an practical value is compared with an simulated one but should be seen more as an indication of its performance. In the practical implementation of the APF system the current ripple is expected to be lightly higher because of phenomenas that the simulations does not account for.

When the decision is if an PF or APF solution should be used the importance of price and size has to be considered. The APF solution is 6.8 times more expensive and the size is smaller in comparison to the PF solution. But, including the routing area in the size comparison and the total area of both solutions becomes fairly equivalent. The reason being the higher amount of components present in the APF solution.



# 7

## Conclusion

The objective of this project was to investigate the concept and the possible implementation of an APF system for a fan application. During this project, different APF topologies have been investigated and it was concluded that the VSI shunt APF filter is the most suitable topology. Fundamentally it is a bidirectional converter with the possibility to control the current in both directions either from or to the storage capacitor.

To simulate the converter and the APF with sufficient accuracy, a model has been created with the aim of simulating the practical implementation as close as possible by using non ideal components and sample and hold functions. The results from the simulations are reasonable because of the regulating behaviour during different scenarios in the nonlinear current.

Problems occurred during the practical implementation of the APF system where the output frequency of the microcontroller was insufficiently low to meet a low pass RC filter with reasonable time constant. This resulted in a distorted feedback signal to the analog controller which made it impossible to regulate the APF system. Because of the RC filter between the microcontroller and analog controller did operate as expected the full system could not be tested as a functional filter unit. The overall functionality of the microcontroller such as current measurements, averaging and PWM calculations performed as expected. Every subsystem included on the PCB such as the measurement, gate switching, blanking time and power supply also performed as desired.

Comparing the results obtained from the simulations with the practical passive filter performance used in the present application, the results of the APF simulations are not satisfying in comparison. The reason is the spikes which occur in the APF system that contribute to a high amount of undesirable frequencies that will cause disturbances if they are not attenuated. The current in the PF solution has low frequency variations but any large current spikes are not present.

If price is an important aspect to consider during the development, the APF system is not the system to use because of the amount of expensive components needed in the design. The APF system is 6.8 times more expensive than the passive filter and only the microcontroller used is about twice the price of the passive filter. Because of this fact there will be hard to find a solution that is less expensive than the existing filter based on three components. The layout of the filter is on the other hand still the same size but more flexible and can easily be adapted to small volumes because of the smaller components that are implemented. The potential of using a APF system for this application is still relevant but a faster regulation system and cheaper microcontroller have to be implemented to make this solution useful.

## 7.1 Future work

For further development if an APF system for fan applications this topology is an alternative. The improvement that is needed to achieve good practical results is to change the microcontroller. A more powerful processor with higher switching frequency will make it possible to integrate the analog controller into the microcontroller and make the switching fast enough to compensate for the current shape to the fans. The integration of the controller also eliminates the problems of filtering the digital signal to an analog controller because of the driver circuit of the MOSFETs can be directly connected to the processor. This integration will also reduce the cost of the analog circuit which is about 20% of the actual price.

A higher switching frequency might be of interest if size is of great importance because it gives the possibility to use a smaller inductor, the largest component in the design, resulting in an even smaller design [6] [7].

The spikes presented in Figure 4.4 would be possible to eliminate by implementing an hybrid APF solution. The hybrid APF system would be more suitable because simultaneously as the APF handles the nonlinear current the PF takes care of the low energy spikes which the APF could not handle properly.



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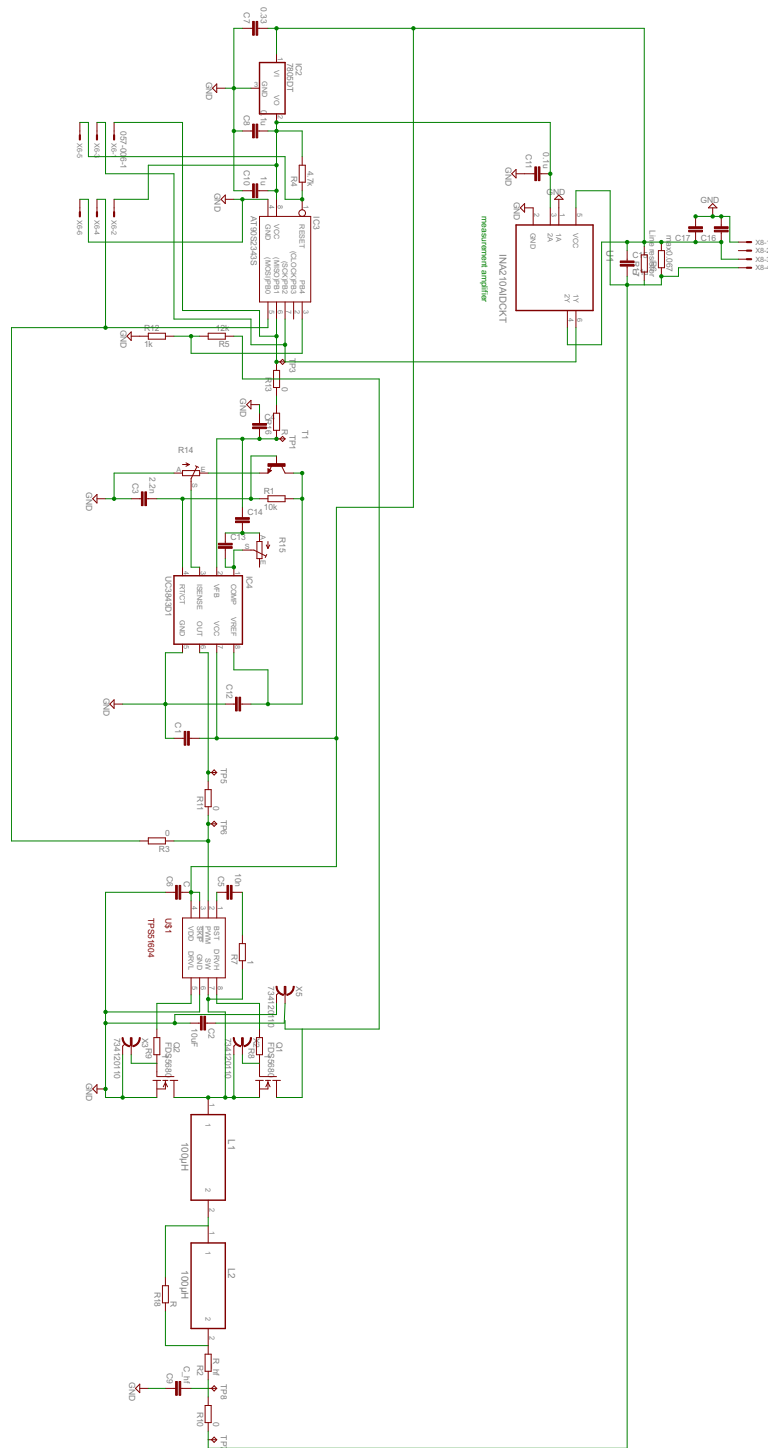
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A

Schematic



A2

Figure A1: Schematic drawn in Eagle

B

AVR code

```

#define F_CPU 8000000
#include <avr/io.h>
#include <util/delay.h>

void adc_init()
{
    ADCSRA = (1<<ADEN)|(1<<ADPS0); //enable ADC prescaler. division
factor 2

    ADCSRB |= (1<<ADLAR); //Left adjust 10 bits
}

uint8_t adc_read(uint8_t ch)
{
    ch &= 0b00000111; // AND operation with 7
    ADMUX = (ADMUX & 0xF8)|ch; // clears the bottom 3 bits before
ORing

    ADCSRA |= (1<<ADSC); // start single conversion

    while(ADCSRA & (1<<ADSC)); // wait for conversion to complete
    return (ADC); //Output ADC High nibble
}

void InitPWM(){
    DDRB|=(1<<DDB1); //Set output to PB5
    TCCR0A|=(1<<WGM01)|(1<<WGM00)|(1<<COM0B1); //WGM01 WGM00 sets
8-bit PWM. COM0B1 sets Oc0B low at match (1<<WGM01)|
    TCCR0B|=(1<<CS00); //No prescaler 4kHz
}

void timer1_init(){
    TCCR1 |= (1<<CS12);
    TCNT1 =0;
}

void SetPWMOutput(uint8_t duty)
{
    OCR0B = duty; //output at OC0B (ben nr6)
}

uint8_t add_sample(uint8_t val){
    static uint16_t total; //sum of 100 samples
    static uint8_t index; //buf index
    static uint8_t count;
    static uint8_t buf[100]; //store 100 samples

    total -= buf[index]; //sub 'earliest' value
    total += val; //add new value
    buf[index]=val; //store new value
    index++;

    if(index>99){ //if overflow

```

```

        index=0; //reset index
    }

    count = 100; //used because the array is 100 samples long

    return total/count; //return average
}
int main()
{
    uint8_t adc_result, adc_Vc; //Conversion values
    uint8_t VcSetPoint = 70; // Digital value for 18V after the
voltage division to 1.385V
    uint8_t Duty;
    uint8_t AVG = 0;

    DDRB |= (1<<PB1);          // to connect output to PIN6

    adc_init(); //Initialize analog to digital converter
    InitPWM(); //Setup of PWM
    timer1_init(); //setup of timer

    while(1)
    {
        adc_result = adc_read(1); // read adc value at PB2
        adc_Vc = adc_read(2); // read Vc voltage

        //When timer fullfills criteria take a new sample and add
in averaging value
        if(TCNT1>=79){
value
            AVG = add_sample(adc_result); //Update Average
            TCNT1 = 0; //Set timer to zero
        }

        VcDiff = VcSetPoint- adc_Vc; //Difference from Vc set-
point (18V)

        Duty = AVG - adc_result + 125; // - VcDiff; Calculate the
difference from the average value and add 125 (2.5V) so the analog
controller get the diff from 2.5V

        SetPWMOutput(Duty); //Update output duty cycle
    }
}

```



C

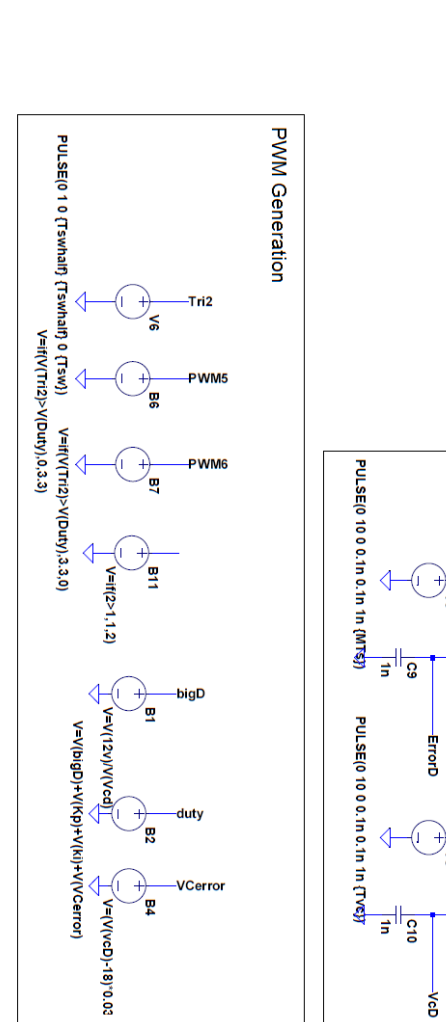
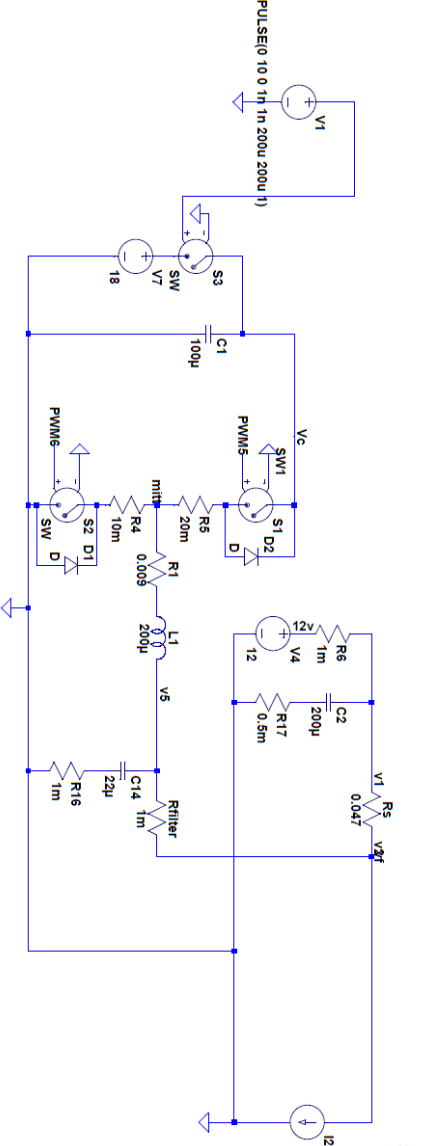
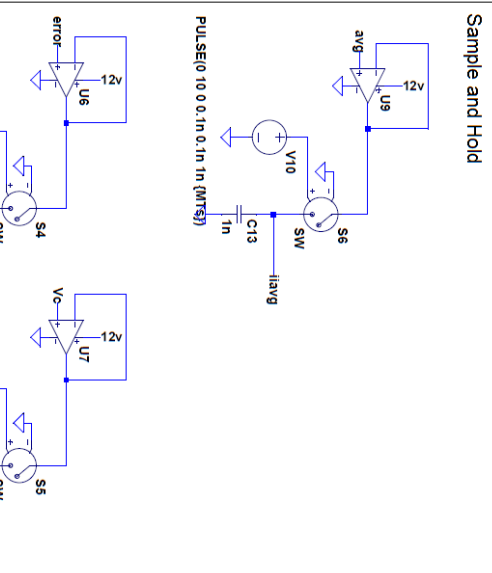
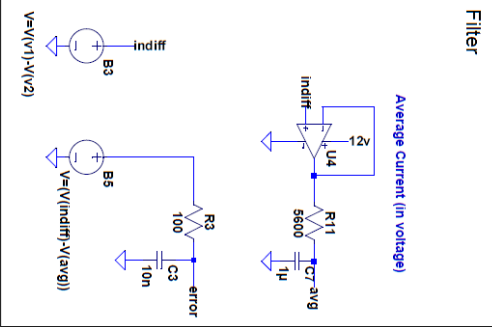
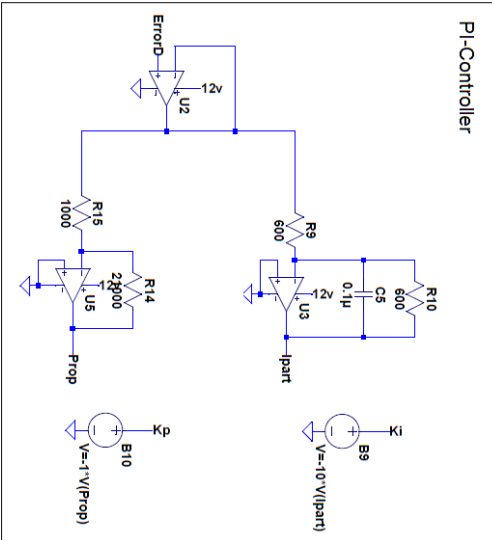
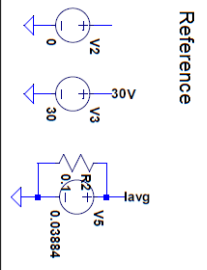
**Simulation in LtSpice**

```

Settings
.param Fmeasure = 0.6MEG
.param MTS = 1/Fmeasure
.param Fsw = 450k
.param Tsw = 1/Fsw
.param Tswhalf = Tsw/2
.param Tvc = MTS/10

.model SW1 SW/Ron=0.01 Roff=1G Von=2 Voff=0 Vh=0.5 Vh=1
.model SW2 SW/Ron=0.001 Roff=1G Von=2 Voff=0 Vh=0.5 Vh=1
.tran 0 60m 0 10u

```



```

PULSE0 10 0 1n 1n 200u 200u 1)
PULSE0 1 0 (Tswhalf) (Tswhalf) 0 (Tsw))
V=I/(Tri2)>V(Duty),0.3,3)
V=I/(Tri2)>V(Duty),3,3,0)
V=I/(2-1,1,2)
V=V/(12V)/V(Vcd)
V=V/(bigD)+V/(kp)+V/(ki)+V/(Verror)

```