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Wideband Inductor-less LNA with Resistive Feedback and Noise Cancelation

Master of Science Thesis in Integrated Electronic System Design

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Abstract

In this master thesis a wideband, inductorless LNA for GSM and WCDMA with noise canceling is examined and designed in 90-nm RF CMOS process. The goal was to design a wideband LNA that could work as a drop in solution in ST-Ericsson's receiver and have an input match below -12 dB for a bandwidth of 800 MHz to 2.5 GHz. The proposed LNA combines two techniques, resistive feedback and noise cancellation to provide both a wideband input match and good noise and linearity performance.

The result is a wideband, differential LNA without any need for external matching components. Furthermore, the solution is inductorless which saves valuable area on chip. The LNA covers frequency bands within 800 MHz – 2.5 GHz with S11 below -12.8 dBm and provides a voltage gain of 27 dB. The NF is below 2.1 dB and IIP3 is greater than -4 dBm with a power consumption of only 28 mW. In the receiver test bench the mixer is used as load which results in a conversion gain higher than 24 dB, S11 below -12.8 dBm, NF below 4 dB and IIP3 higher than -6.2 dB.

This solution has many features such as high bandwidth with a good input match, inductorless design saving area and costs and is fully differential.

Acknowledgments

First of all I would like to thank ST-Ericsson for providing me this master thesis. This project has been a big opportunity for me. To design a circuit and understand every aspect of it has been very educational and a perfect summary for my master studies in analogue- and radio-IC design. It has been a fun and enlightening project where I had to use a lot of knowledge from different courses to succeed.

I want to thank every person at ST-Ericsson who has helped me during these weeks, everything from small inputs on the work to computer service when I have been incompatible with Cadence. Especially a huge thanks to my supervisors at ST-Ericsson, Tobias Tired and Eric Westesson, for all the time you have put at my disposal, all the question you have answered and the enthusiasm you shown towards this project. Without your support the project had not been the success I believe it is.

Furthermore I would like to thank Lena Peterson, my supervisor from Chalmers, for being my supervisor during this project. As the project has been a collaboration between LTH and Chalmers, as well as ST-Ericsson, I would like to thank Martin Liliebladh from LTH, my colleague during this thesis, for putting up with me. It has been hard work and long days to get it done and it would never been possible without you.

This is the finale of my master studies and I would like to take the opportunity to thank my family and my friends on and off school for your tremendous support during these years, without you I would not succeeded as I have done and more importantly I would not had so much fun along the way.

Thank you all!

Tobias Ström, 2010-03-01

Contents

1 Introduction

Today everywhere around us radio signals and systems coexist and operate side by side such as GSM, 3G, WLAN, Bluetooth, FM-radio and many more. The demand for power efficient, accurate and small transmitters and receivers grows and is a big research field worldwide.

LNA stands for Low Noise Amplifier and is the first stage in a receiver after the antenna. Its purpose is to amplify the desired signal as much as possible without adding noise or consuming too much power. Another problem is to obtain a good impedance match between the antenna and the LNA input. The solution has been to use inductors off and on chip, the latter to resonate at the desired frequency to obtain real valued impedances. Because of the resonance circuits the bandwidth for this type of LNA is low and cellular phones must be able to receive signals at wide range of frequencies from 850 MHz to 2.5 GHz. In current handsets the solution is to implement a number of LNA:s to cover the whole bandwidth. A switch activates the appropriate LNA according to the frequency to be received. In this solution each LNA has its own inductors which gives good gain and low noise at the price of large chip. Inductors use a lot of area on chip and all the matching components off chip use valuable PCB area. To make matters even worse inductors on chip require expensive manufacturing steps to get a high Q.

In this thesis we present an inductorless, wideband LNA that will save both area and cost. The solution is also able to receive on all channels without compromising gain or noise figure. The LNA should also be a drop-in replacement of the existing LNA in the ST-Ericsson receiver.

2 Basic Radio Systems

The analog part of a basic radio system consists of an antenna with an impedance of 50 Ω, duplexer, receiver and a transmitter. This project has its focus on the receiver part of the system and to understand the basics of a radio system a brief description of each block is given below.

2.1 Receiver

When a signal is received at the input of the receiver the frequency is between 800 MHz and 2.5 GHz and have a maximum amplitude of -26 dBm ($\approx$ 2.5 μW). In the radio receivers today homodyne receivers are used. Looking from the input (figure 2.1) the incoming signal is first amplified with an LNA. The output of the amplifier is then down converted in a mixer which uses a local oscillator, synchronized in frequency to the carrier of the desired signal. Finally the baseband signal is amplified and can be used in the rest of the system.

To amplify such low signals it is crucial that the input stage (LNA) itself does not contribute with noise and distortion that could destroy the input signal. In today's solution the mixer is passive due to the linearity requirement. A passive mixer leads to a loss in signal amplitude and put an even higher requirement of the LNA gain.

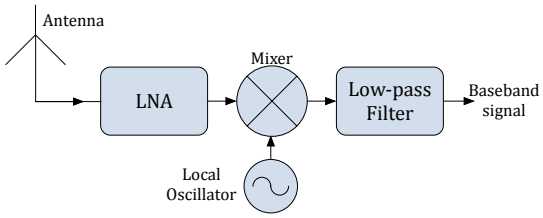

Figure 2.1: RF Receiver

2.2 Transmitter

This part is not considered in this project but is described for a deeper understanding of a radio system. The signal that is to be sent is first modulated to the correct carrier frequency. To retain the correct carrier a local oscillator is used. The oscillator frequency is then mixed with the desired signal where an oscillator chooses what frequency the signal will be transferred with between antennas. To be able to reach the next antenna the signal need to be strong and is therefore amplified with a power amplifier to 26 dBm.

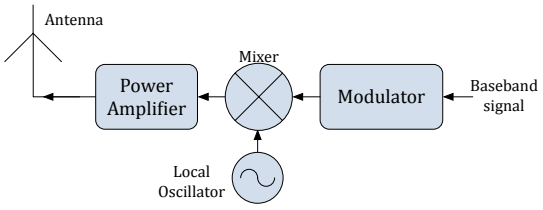

Figure 2.2: RF Transmitter

2.3 Duplexer

In some radio systems, e.g. WCDMA, the transmitter and receiver use the same antenna in a full duplex manner. To prevent the transmitter from damaging the receiver a duplexer is used between the antenna and the rest of the system. The duplexer is a filter that can be used when the transmitted and received signal uses different frequencies. A filter of this kind is designed to reduce the impact of the transmitted signal on the receiver antenna input,

leading to a higher sensitivity to small signals and a shield against high voltage peaks that can damage the receiver. In this project the duplexer has an internal voltage gain of 6 dB. Since it contributes with a gain, the gain requirements for the LNA can be lowered. The most common input impedance of a radio system is 50 Ω. In this project a duplexer with an output impedance of 200 Ω is used.

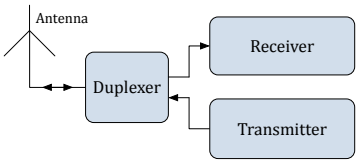

Figure 2.3: Radio System

3 Target Specifications

For an LNA to be usable in a radio system the LNA need to fulfill the system requirements. Different radio systems, such as WCDMA and GSM, have different requirements. The parameters of interest are input matching, gain, linearity and noise. For this project the specifications are listed in Table 3.1 and they are somewhat stricter than ones for the radio receiver used today. These specifications are therefore only a reference of a "perfect" LNA and are something to aim for.

All of the specifications are specified from the output of the antenna to the output of the mixer. This means that the requirements on the LNA itself are much stricter in terms of linearity and noise.

Table 3.1: Performance specifications of wideband LNA

Parameters	**Specifications**
Conversion Gain	30 dB
Noise Figure	$\leq$ 2.0 dB
IP3	$\geq$ -5 dBm
Current Consumption	$\leq$ 15 vmA
Operating frequency	800 MHz – 2.5 vGHz
Input Matching	$\leq$ -12 vdB
1dB Compression Point	$\leq$ -15 vdB
$Z_{antenna}$	50 vΩ

For a deeper understanding the requirements are described in more detail below.

3.1 Gain

Gain is a ratio between the output signal and input signal showing how much the signal can be amplified. It is often measured in voltage leading to the expression "voltage gain" and is often expressed in the logarithmic scale defined as

$$Gain = 20 \cdot \log\left(\frac{V_{out}}{V_{in}}\right) dB \tag{1}$$

Another gain definition is power gain, which is defined as the output power compared to the input power. There are three power-gain definitions that are used in RF applications [10]. Figure 3.1 illustrates the different powers coming in and out of an amplifier and the different gains.

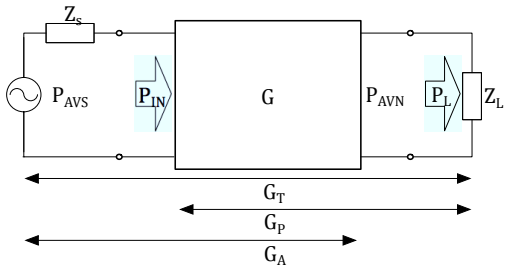

Figure 3.1: Power Gain Definitions

Power-gain definitions:

P_{AVS} - *Power available from source* P_{AVN} - *Power available from network*
P_{IN} - *Power delivered to the input* P_L - *Power delivered to the load*

$$Transducergain = G_T = \frac{P_L}{P_{IN}}, \tag{2}$$

$$Operatinggain = G_P = \frac{P_L}{P_{AVS}}, \tag{3}$$

$$Availablegain = G_A = \frac{P_{AVN}}{P_{AVS}}, \tag{4}$$

Conversion gain is another gain definition used in RF-receivers which is the ratio between the intermediate frequency(IF) power at the output of the mixer and the available power at the RF input of the receiver.

$$Conversiongain = G_C = \frac{P_{out\ mixer}}{P_{in\ receiver}}, \tag{5}$$

In this thesis voltage gain is always used if nothing else is stated.

3.2 Matching and S parameters

Matching is essential in a radio receivers and transmitters since good matching will lead to good power transfer between the blocks in Figure 2.1 and 2.2. S-parameter is a tool that is used to describe e.g. matching and gain for a circuit. This section is a summary from the book Radio Electronic [10].

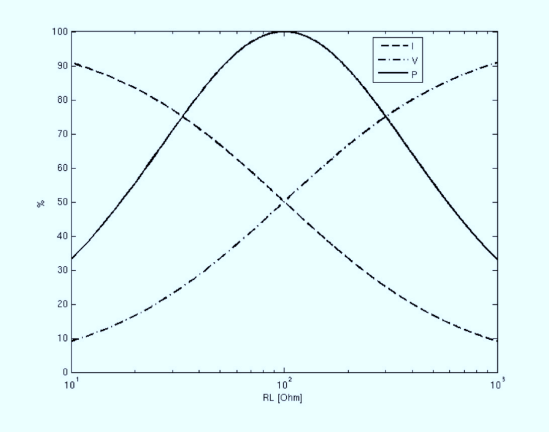

Figure 3.2: Transferred V, I or P in percent vs. the load resistance R_L. V_s=1V, R_s=100 Ω

3.2.1 Matching

When combining several stages it is essential to transfer as much of the signal between the stages as possible. Depending on the type of transfer that is to maximized (power, voltage or current) the load impedances have to chosen differently. Figure 3.2 shows how the transfer functions vary with the load when the impedances are purely resistive. Power transfer is often the desired option and that is the matching used in this thesis. The input impedance of the LNA should therefore be equal to the antenna impedance.

3.2.2 Reflection

Discontinuities in a propagation medium will cause a wave traveling through the medium to reflect some of the wave back towards the source. The wave in a transmission line will because of this consist of two waves, one original

traveling towards the load and one reflected in the opposite direction. The characteristic impedances of the transmission line becomes very important since the source and load impedance would cause discontinuities and reflection if not matched to it as shown in Figure 3.3 and equation (8) and (9). The ratio between the reflected and incident wave is called reflection coefficient and is a measure of how good the matching is between the transmission line and load and is defined according to equation (10).

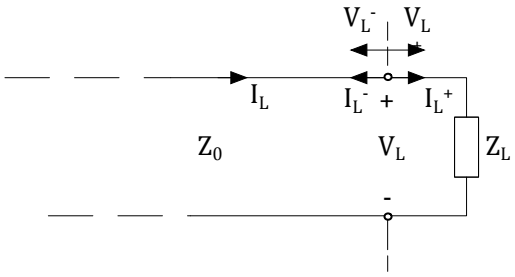

Figure 3.3: Reflection

$$V_L = V_L^+ + V_L^- \qquad (6) \qquad\qquad I_L = I_L^+ + I_L^- \qquad (7)$$

$$V_L^- = V_L^+ \cdot \frac{Z_L - Z_0}{Z_L + Z_0} \qquad (8) \qquad\qquad I_L^- = I_L^+ \cdot \frac{Z_L - Z_0}{Z_L + Z_0} \qquad (9)$$

$$\Gamma \equiv \frac{reflected\ voltage}{incident\ voltage} = \frac{reflected\ current}{incident\ current} = \frac{V^-}{V^+} = \frac{I^-}{I^+} \qquad (10)$$

Then it is easy to define the reflection coefficient for a load.

$$\Gamma_L = \frac{V^-}{V^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad (11)$$

It is obvious that when the load is perfectly matched, i.e. $Z_L = Z_0$, there will be no reflection. If a wire is short compared to the wavelength of a signal the wire can be neglected and no reflection will occur. To minimize the reflection in a system the characteristic impedance of wires needs to be designed to 50 Ω.

3.2.3 S-parameters

A commonly used way to describe a two-port network in RF systems is S-parameters. Instead of using open and closed circuit calculation, as in Y-,

Z- and ABCD-parameters, it is based on reflections at the in- and out-ports. This is very suitable for RF calculations but for lower frequencies, such as audio, the other methods are better.

In Figure 3.4 a_1 is the incident wave at each port and b_1 is the reflected but b_1 contains contribution from both incident waves as they scatter through the two-port. This is what gave the S-parameters its name, scattering parameters.

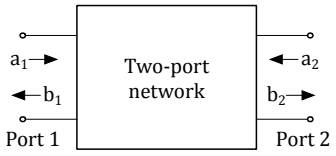

Figure 3.4: S-Parameters

The relation between the waves is described with the following equations

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \tag{12}$$

or in matrix form

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{13}$$

To understand the different S-parameters the easiest way is to look at the equations. S_{11} describes how much of a_1 that is reflected back to b_1 i.e. how good the input matching is and is a measure of the input impedance. S_{12} is a measure of how much of a_2 that scatters through the system i.e. how good the isolation is from output to the input. S_{22} is the same as S_{11} but at the output i.e. the output impedance but S_{21} is a bit different. It is a measure of how much the incident wave at the input affects the reflected wave at the output or in other words how the input signal affects the output signal. For many networks this is a much wanted effect as it is the gain of the two-port.

A good amplifier would have a S_{11} and S_{22} low, S_{21} high and S_{12} equal to zero.

In this thesis S_{11} is used to measure the input match of the LNA.

3.3 Noise

Every component and wire contributes with noise which lowers the overall performance. In a signal spectrum noise is visible as a "floor" where the signal and distortion peaks above the noise floor. If a circuit adds with more noise the noise floor will rise and the signal will eventually drown in the noise.

The ratio between the signal and the noise floor is called the Signal-to-Noise Ratio (SNR). Here follows a brief review of the main noise sources present in this project, the devoted reader can find a more detailed description in The Design of CMOS Radio-Frequency Integrated Circuits [6].

3.3.1 Resistors

All resistors generate thermal and flicker noise. Wires are resistive and can be modeled as lumped resistors. The mean-square open-circuit noise voltage can be modeled according to:

$$\overline{e_n^2} = 4kTR\Delta f, \tag{14}$$

where T is the absolute temperature in Kelvin, k is Boltzmann's constant, R is the resistor value and Δf is the noise-bandwidth. Δf is the bandwidth where the circuit operates and is not the same as the -3 dB bandwidth because even noise with lower gain will affect the circuit. The noise bandwidth is about 1.57 times the -3 dB bandwidth.

The flicker noise, or 1/f-noise as it is also called, dominates the thermal noise for lower frequencies and disappears under the noise floor for higher frequencies. The equation for the flicker noise is

$$\overline{e_n^2} = \frac{K}{f} \cdot \frac{R_\square^2}{A} \cdot V^2 \Delta f, \tag{15}$$

where A is the area of the resistor, $R_\square$ is the sheet resistance, V is the voltage across the resistor, f is the frequency and K is a material-specific parameter.

3.3.2 Transistors

A transistor contributes two thermal noise sources and flicker noise. The latter can be modeled as a current source between source and drain and is expressed as:

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f, \tag{16}$$

and is dependent on the width, the length, the transconductance, the gate-oxide capacitance, K – a device specific constant and f, the frequency at interest. The two thermal noise sources are the gate noise and the drain current noise and the equations are shown in (17) and (18), respectively.

$$\overline{i_{ng}^2} = 4kT\delta \cdot \frac{\omega^2 C_{gs}^2}{5g_{d0}} \cdot \Delta f \tag{17}$$

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \Delta f \tag{18}$$

g_{d0} is the drain-source conductance at zero V_{DS}, γ is one when V_{DS} is zero and then goes towards 2/3 in saturation, δ is 2 times γ (4/3) and C_{gs} is the gate-to-source capacitance. As the flicker noise equation (16), the drain current noise equation (18) can be modeled as a current source between the source and drain of a transistor but the gate noise will act as a current source between the gate and source. Equation (17) can be rewritten as equation (19) [6] and then be modeled as a voltage source at the gate which will give rise to a drain current just as a normal small signal voltage at the gate.

$$\overline{v_{ng}^2} = 4kT\delta \cdot \frac{1}{5g_{d0}} \cdot \Delta f \tag{19}$$

3.3.3 Noise Factor and Noise Figure

As described, all devices contribute with noise but what is important is how much noise a circuit adds to the signal i.e. how much the SNR is deteriorated. This is called the noise factor (F) or noise figure (NF), where the noise figure is the noise factor expressed in dB. The noise factor of a circuit is the ratio between the SNR_{out} and SNR_{in} and expression as:

$$\begin{aligned} F = \frac{SNR_{in}}{SNR_{out}} = \left[SNR_n = \frac{S_n}{N_n}\right] = \frac{S_{in}}{N_{in}} \cdot \frac{N_{out}}{S_{out}} = \\ = \frac{S_{in}}{N_{in}} \cdot \frac{G \cdot N_{in} + N_{amp}}{G \cdot S_{in}} = \frac{G \cdot N_{in} + N_{amp}}{G \cdot N_{in}} = 1 + \frac{N_{amp}}{G \cdot N_{in}} \end{aligned} \tag{20}$$

where S_n is the signal-to-noise ratio for input and output, G is the gain and N_n is the noise for input and output. The noise factor is

$$F = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} \tag{21}$$

For a noiseless amplifier $N_{out} = N_{in} \cdot G$ and $F = 1$ or 0 dB which is the lowest theoretical value of noise factor. The more noise the source contributes with, the less sensitive will F be to the noise generated in the circuit, according to equation (20) and the higher the source impedance is the more noise will be generated at the source. It is extremely important to design an LNA with high gain and low noise factor as Friis' formula illustrates very well. Friis's formula is used to calculate the total noise factor (F_{tot}) of a cascaded system. Every stage in the system contributes with a noise factor (F_i) and available power gain (G_i). F_{tot} can be calculated according to equation (22) where both the noise factor and the gain should be represented in linear scale and not in decibels.

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \frac{F_4 - 1}{G_1 \cdot G_2 \cdot G_3} + \ldots = F_1 + \sum \frac{F_i - 1}{\Pi G_j} \tag{22}$$

The importance of the first stage is obvious and it is dominating Friis's formula. Equation (22) can be simplified to (23) and still give a good approximation.

$$F_{tot} = F_1 + \frac{F_{rest} - 1}{G_1} \quad \Rightarrow \quad F_{reciever} = F_{LNA} + \frac{F_{rest} - 1}{G_{LNA}} \tag{23}$$

The noise from the LNA is dominating and the gain suppresses the impact of the rest of the noise.

3.4 Linearity

Nonlinearities in electronic circuits are due to distortion in active components like transistors. Third order intercept point (IP3) is a very important measure since it shows how third orders distortions influence the signal. To understand IP3 the concept of distortion will first be explained.

A nonlinear system can be approximated as:

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + ... \tag{24}$$

Given a sinusoid input signal

$$x = A \sin(2\pi f_t) \tag{25}$$

If the expression is extended and the constant A is assumed small the output of the polynomial will be

$$y \approx a_0 + a_1 A \sin(2\pi f_t) + \frac{a_2 A^2}{2} \sin(4\pi f_t) + \frac{a_3 A^3}{4} \sin(6\pi f_t) \tag{26}$$

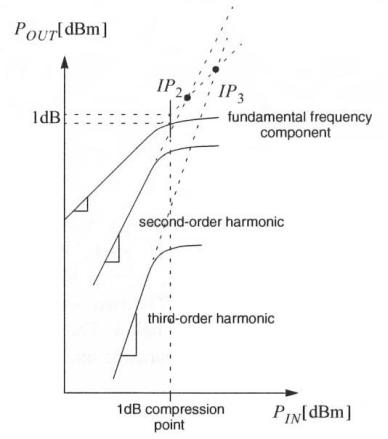

Figure 3.5: Intercept points for harmonic distortion [10]

The expression shows harmonics distortion as multiples of the input frequency *f*. Harmonic products expressed as function of input and output

power can be displayed as Figure 3.5. The fundamental frequency has a slope ratio of one, the second order harmonic has a slope equal to two and the third order harmonic has a slope equal to three. In a linear system the second and third order harmonics lead to intersections between the fundamental component and the two harmonics. In a real system, losses and nonlinearities make the slopes to saturate before the intersections but the extrapolated slopes are still important characteristics of a system and are called Intercept point two (IP2) and three (IP3). Harmonic distortion can often be reduced by filtering the output, but with today's wideband circuits it is difficult to reduce the harmonics without filter the signal bandwidth.

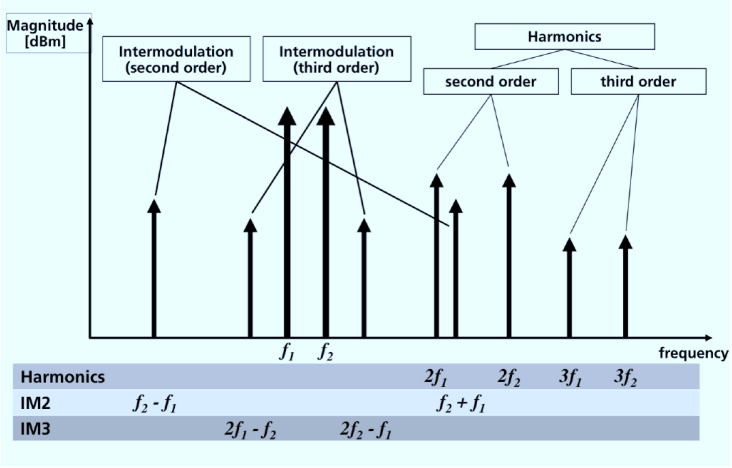

Figure 3.6: IM_2 and IM_3 products in frequency domain [10]

Another problem is the intermodulation distortion (IMD), which can be described with an input signal with two different frequencies close to each other with the same amplitude, also called a two-tone test. As seen in Figure 3.6, if a signal with two frequencies f_1 and f_2 is received at the input of a nonlinear amplifier these will produce second-order harmonics at $2 \cdot f_1$ and $2 \cdot f_2$ and third-order harmonics at $3 \cdot f_1$ and $3 \cdot f_2$. The input frequencies also create second-order intermodulation products (IM_2) $f_2 - f_1$ and $f_2 + f_1$. The most critical distortion is the third-order intermodulation product (IM_3) at $2 \cdot f_1 - f_2$ and $2 \cdot f_2 - f_1$. These frequencies are close to the fundamental tone and therefore hard to reduce with filters.

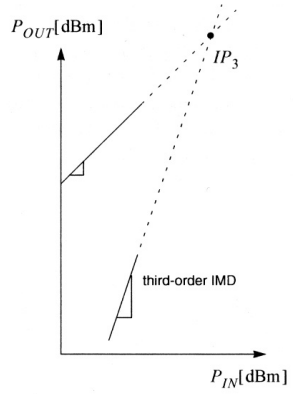

Figure 3.7: Intercept point for IMD [11]

As with the harmonics, intercept points can be defined also for the IMD products. The intercept point for the third-order IMD product can be seen in Figure 3.7.

3.5 Compression Point

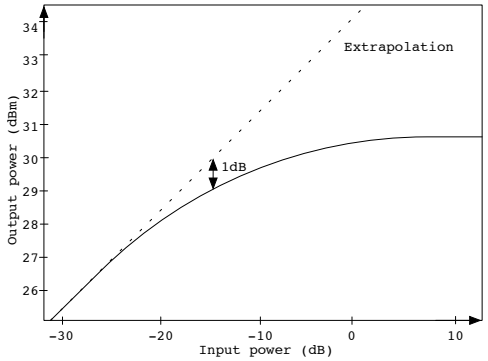

Figure 3.8: Gain Compression Point

An ideal amplifier maintains its gain for all input signal levels. When nonlinearities are introduced the amplifier will eventually go into saturation and the output gain will decrease. A common measurement is the 1dB Gain Compression point, which defines the input power when the gain has dropped 1dB from the extrapolated signal level.

4 LNA design considerations

4.1 Present Solutions (Narrowband)

The most common solution used today for on-chip LNAs is a common source coupled transistor with inductive source degeneration. The inductor at the source will create a real part to the input impedance without adding a resistor, thus makes it easier to match it against the output impedance of the 50 Ω antenna.

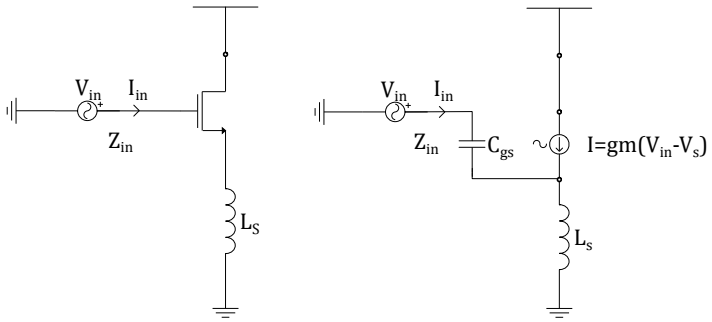

Figure 4.1: Common-source stage with source-inductive degeneration

The input impedance, Z_{in} is given by

$$Z_{in} = \frac{V_{in}}{I_{in}} \tag{27}$$

and with the following currents and voltages from Figure 4.1

$$I_{inductor} = I_{in} + g_m V_{gs} = I_{in} + g_m I_{in} \frac{1}{sC_{gs}} \tag{28}$$

$$\begin{aligned} V_{inductor} &= sL_s \cdot I_{inductor} = \\ &= sL_s \left(I_{in} + g_m I_{in} \tfrac{1}{sC_{gs}} \right) = I_{in} \left(sL_s + g_m \tfrac{L_s}{C_{gs}} \right) \end{aligned} \tag{29}$$

Z_{in} can be calculated to

$$\begin{aligned} Z_{in} &= \tfrac{V_{in}}{I_{in}} = \tfrac{V_{inductor}+V_{gs}}{I_{in}} = \left(I_{in} \left(sL_s + g_m \tfrac{L_s}{C_{gs}} \right) + I_{in} \tfrac{1}{sC_{gs}} \right) \Big/ I_{in} = \\ &= L_s \tfrac{g_m}{C_{gs}} + s \left(L_s - \tfrac{1}{C_{gs}} \right) = [s = j\omega] \Rightarrow \\ Z_{in} &= L_s \tfrac{g_m}{C_{gs}} + j \left(\omega L_s - \tfrac{1}{\omega C_{gs}} \right) \end{aligned} \tag{30}$$

L_s is the source inductor and it lowers the gain from the CS stage working as negative feedback and thus improving the linearity. Furthermore it introduces the real part of Z_{in}. The real part of Z_{in} is then set by carefully choosing L_s, C_{gs} and g_m. C_{gs} is the parasitic capacitance between the gate and source of a transistor with the transconductance g_m.

Besides the components in Figure 4.1 there are capacitances from wires, ESD diodes and pad connected between the gate and ground, which will complicate the matching. To obtain good matching two inductors are added off chip, one shunted, L_{in}, and one in series with the gate, L_g. L_g is selected to remove the imaginary part of Z_{in}, i.e.

$$\omega \left(L_s + L_g \right) - \frac{1}{\omega C_{gs}} \tag{31}$$

and L_{in} is chosen to cancel the effect of the parasitic capacitances from the pad, wire and others.

To increase the gain of the LNA a cascoded transistor is used in the input stage. The gain can also be increased with an inductor connected to the drain of the cascoded transistor. When the capacitance at the output node is at resonance with the inductor the gain will peak.

Because the input impedance is 50 Ω only at resonance frequency and the gain also peaks at resonance this solution gives a narrowband LNA. To work around this problem a number of LNA:s have been implemented in the present solution, one for each band to be received which all have their own pad on the chip. A switch at the bias current then turns on and off the entire LNA determine which LNA to conduct depending on the desired frequency. This solution has the disadvantage that it uses many matching components that needs a lot of area both on and off chip. To reduce the number of inductors on chip all the low band LNA:s share the same balun and L_S. Another balun and inductor are used for the high band LNA:s. To tune the resonance frequency a capacitance bank is connected to the input of the balun and the capacitance is switched on with control logic depending on desired resonance frequency. This reduces the number of components implemented on chip but still consumes a lot of area.

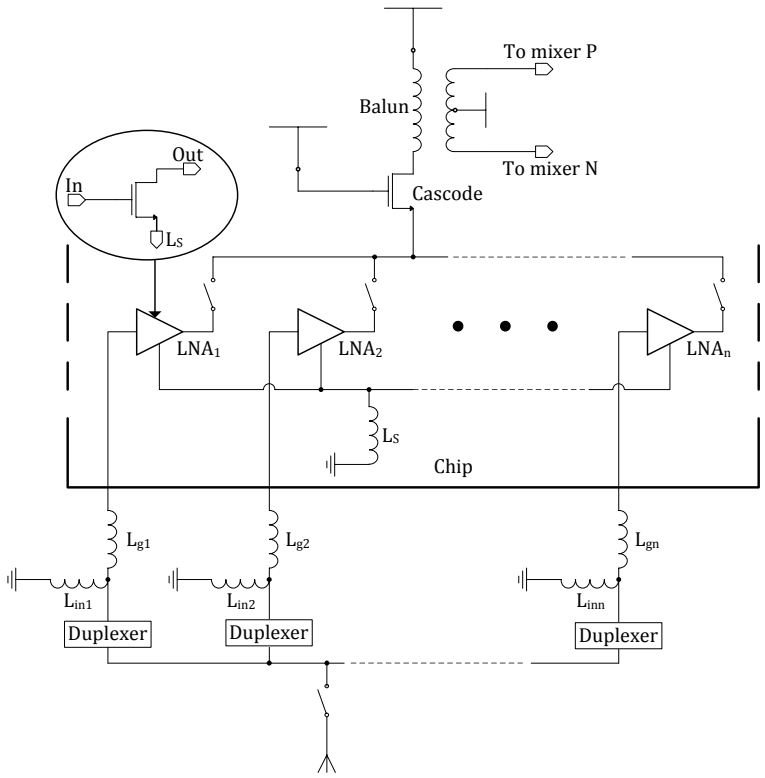

Figure 4.2: Present LNA system

This solution is simple and well known and has good gain, noise figure and linearity but the drawback is its narrowband characteristics and the matching components and inductors needed.

4.2 Input Stage

4.2.1 CS Stage with Resistive Feedback

A Common Source(CS) stage standalone need matching components on the input to be able to match an antenna impedance of 50 Ω. If feedback is used with the CS stage the transconductance of the transistor can be used to match the input.

Figure 4.3 shows a simple sketch of a common source LNA with resistive feedback. The input current can only go through R_f and then M_1 to reach ground and by applying Kirschoffńs current law (KCL) at the output node it is obvious that $I_{in} = I_d$. I_d and the current through R_f can also be expressed as

$$I_f = -I_d = \frac{V_{out} - V_{in}}{R_f} \tag{32}$$

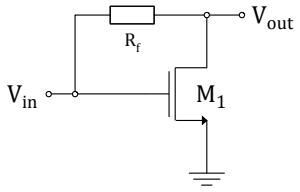

Figure 4.3: CS stage with resistive feedback

$$I_d = g_m \cdot V_{in} \tag{33}$$

and from this the gain and input impedance can be calculated:

$$\begin{aligned} &I_f + I_d = 0 \;\Leftrightarrow\; \tfrac{V_{out}-V_{in}}{R_f} + g_m V_{in} = 0 \;\Leftrightarrow \\ &\Leftrightarrow \tfrac{V_{out}}{R_f} - V_{in}\left(\tfrac{1}{R_f} - g_m\right) = 0 \;\Leftrightarrow\; \tfrac{V_{out}}{V_{in}} = 1 - g_m R_f \end{aligned} \tag{34}$$

$$A_v = \frac{V_{out}}{V_{in}} = 1 - g_m R_f \tag{35}$$

$$I_{in} = -I_f = -\frac{V_{out} - V_{in}}{R_f} = -\frac{(1 - g_m R_f - 1)}{R_f} V_{in} = g_m V_{in} \tag{36}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{g_m V_{in}} = \frac{1}{g_m} \tag{37}$$

Since no inductors are used to match the input it is possible to reach a wider signal bandwidth.

4.2.2 Cascode

The advantages of a cascode is the increased output impedance and reduced input capacitance. The gain from input node to node V_x is lowered due to that the load will be

$$Z_X = \frac{1}{g_{m2} + g_{mb2}} \tag{38}$$

instead of R_f as in section 4.2.1 which will lead to a gain of

$$A_v = g_{m1} \cdot Z_X = \frac{g_{m1}}{g_{m2} + g_{mb2}} \tag{39}$$

If the devices have roughly the same dimensions the gain will be one. This will reduce the Miller capacitance, the capacitance from gate to source due to C_{GD}, at the input of M_1, which will lead to a higher bandwidth.

$$C_{Miller} = (1 + A_{v,CS})\ C_{GD} = (1 + (1 - g_{m,CS}R_f))\ C_{GD} \tag{40}$$

$$C_{Miller} = (1 + A_{v,cascode})\ C_{GD} \approx (1 + 1)\ C_{GD} = 2 \cdot C_{GD} \tag{41}$$

As an example would a $g_{m,CS}$ of 20 mS and R_f of 500 Ω give a C_{Miller} of $8 \cdot C_{GD}$.

The gain from the input node to the output node will increase as the output resistance increases. The drawback is a lower voltage swing due to the overdrive voltage needed for the cascoded transistors.

Consider the small-signal characteristics, it is shown that the cascode transistor has little effect on the total transconductance [8]. The transconductance is expressed as:

$$g_{m,tot} = \frac{i_0}{v_i} = g_{m1}\left(1 - \frac{1}{1 + (g_{m2} + g_{mb2})r_{o1} + \frac{r_{o1}}{r_{o2}}}\right) \approx g_{m1} \tag{42}$$

As discussed earlier the output impedance is higher for a cascode stage. calculations of the output impedance is expressed as

$$R_0 = r_{o1} + r_{o2} + (g_{m2} + g_{mb2})r_{o1}r_{o2} \approx (g_{m2} + g_{mb2})r_{o1}r_{o2} \tag{43}$$

showing that the output impedance is increased by a factor of $(g_{m2}+g_{mb2})r_{02}$ compared to a common CS stage where the output impedance is r_0. The voltage gain of a cascode stage is expressed as

$$A_{v,cascodedCS} = (g_{m2} + g_{mb2})r_{o1}r_{o2}g_{m1}A_{v,CSonly} = g_{m1}r_{o1} \tag{44}$$

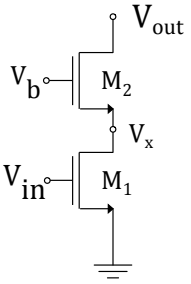

Figure 4.4: Cascode stage

The gain and input impedance in Figure 4.5 will not change from the CS stage with resistive feedback. The currents and node voltages of interest will remain the same but the internal gain of the amplifying stage will increase as shown earlier.

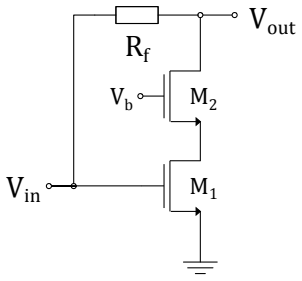

Figure 4.5: Cascode stage with resistive feedback

4.2.3 Inverter

An inverter is a basic gain stage based on the CS stage. There are different types of inverters but the one considered in this project is the push-pull inverter.

Compared to a CS stage an inverter has a lower NF with the same amount of current. This is due to the current reuse technique or gm-enhance as it is called.

$$\frac{g_m}{I} = \frac{g_{m,n}}{I_D}\left(1 + \frac{g_{m,p}}{g_{m,n}}\right) \approx \frac{g_{m,n}}{I_D}\left(1 + \sqrt{\frac{K_P W_P}{K_N W_N}}\right) = \frac{g_{m,n}}{I_D}\xi \tag{45}$$

From equation (45) where ξ is the inverter efficiency factor it can be seen that for fixed $g_{m,n}/I_D$ and W_n the efficiency is larger than one. When $W_p = W_n K_n/K_p$ the efficiency factor ξ is equal to 2 meaning that the g_m is 2 times higher for an inverter than for a CS stage.

A drawback with the inverter is the increase in input capacitance. For a typical inverter the W_p is 2-3 times larger than W_n leading to an input capacitance of

$$C_{IN} = C_{gs,n} + C_{gs,p} = C_{gs,n}\left(1 + \frac{W_p}{W_n}\right) \tag{46}$$

Compared to the input capacitance of a CS stage of

$$C_{IN} = C_{gs,n} \tag{47}$$

The inverter performance depends on what operating region the transistors are biased to. If both transistors are saturated the maximum gain can be received. The small signal voltage gain can be expressed as:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{ds\,1} + g_{ds\,2}} \tag{48}$$

If a simplified model of an inverter with resistive feedback is considered, the gain and input impedance can be calculated with the same principles as the CS stage and cascode earlier. The results are expressed as

$$A_v = \frac{V_{out}}{V_{in}} = 1 - (g_{m1} + g_{m2})R_f \tag{49}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_{m1} + g_{m2}} \tag{50}$$

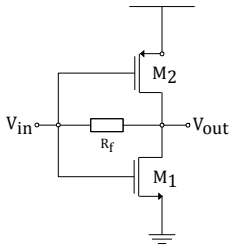

Figure 4.6: Inverter with resistive feedback

4.2.4 Summary

Table 4.1 compares the different input stages with resistive feedback.

Table 4.1: Performance comparison of input stages

Input-stage	A_v	Z_{in}
CS-stage	$1 - g_m R_f$	$1/g_{m1}$
Cascode	$1 - g_m R_f$	$1/g_{m1}$
Inverter	$1-(g_{m1}+g_{m2})\cdot R_f$	$1/(g_{m1} + g_{m2})$

4.3 Source Follower

A source follower, also called a common-drain stage, is often used as an adder or a buffer stage. When the source follower works as a buffer the transistor senses the gate voltage and drives the same voltage at the source. As an adder, it operates in the same manner but simply adds the signal, V_{in}, to an already existing drain signal, provided from e.g. a CS stage.

The small-signal gain is

$$A_v = \frac{g_m R_s}{1 + (g_m + g_{mb})R_s} \tag{51}$$

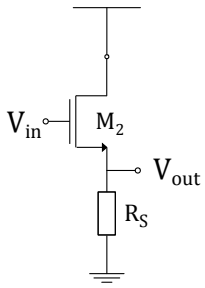

Figure 4.7: Source follower

The problem with a source follower is that it does not have unity gain, i.e. it is not a perfect adder. The gain A_v approaches a gain equal to unity when g_m increases.

$$A_V \approx \frac{g_m}{(g_m + g_{mb})} \rightarrow 1 \tag{52}$$

4.4 Noise Cancellation Techniques

As explained earlier all circuit elements contribute with noise and when noise is added it is not possible to remove it. The designer's goal has been to minimize the amount of noise generated within each element and thus get a low NF. However, lately there have been articles discussing and proving noise cancellation techniques [1, 2, 4, 9].

4.4.1 The Main Idea

If two signals are added together they will cancel each other out when they have opposite phase and add if they have the same phase. Referring to figure 4.8, we see that if the high frequency signals are noise and the others is the desired signal then the output would only contain the desired signal while the noise is eliminated. If it is possible to create two nodes where the signal has the same phase and the noise has the opposite then noise canceling would be possible. Note that if the signal had opposite sign and the noise the same it would just be to invert one of the nodes before adding them to achieve noise cancellation.

4.4.2 Noise Canceling Circuit with CS Input Stage

Consider the circuit in Figure 4.9, assume that the two-port is noiseless and all the noise created by the two-port is modeled as a current source between the output pins. The rest of the noise in the circuit is ignored for now. The only way for the current is through R_f and the source towards ground. Then

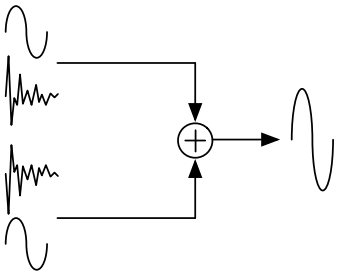

Figure 4.8: Basic noise canceling theory

the noise current instantaneously creates two noise voltages with the same phase but different amplitude in nodes X and Y. The signal voltage at the two nodes on the other hand will have opposite phase due to the inverting amplifier coupled two-port but it will also have different amplitude. Now the criterion for noise cancellation is fulfilled. All that is needed is an inverting amplifier from node X and then an adder.

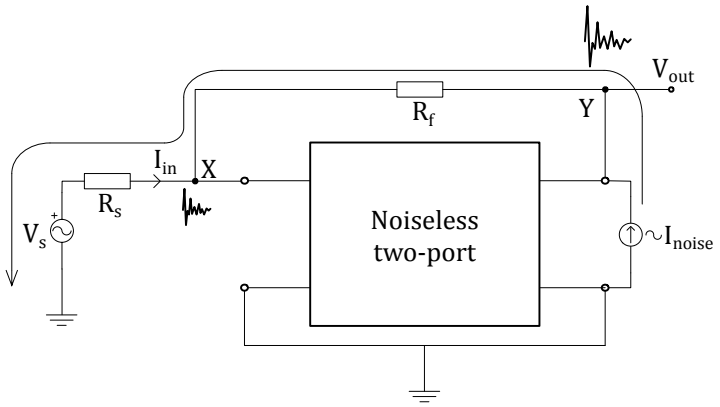

Figure 4.9: Noiseless two-port with feedback

Figure 4.10 illustrates the full solution and both the signal and the noise can be followed through the circuit. By carefully choosing the gain of the inverting amplifier, -A_v, one can make sure that the noise in node Y and Z will have the same amplitude and the total noise cancellation will occur. The noise voltages in nodes X and Y will now be

$$V_{nx} = \alpha \cdot i_n R_S(53) V_{ny} = \alpha \cdot i_n \left(R_S + R_f\right) \tag{53}$$

where α is a constant depending on the relation between Z_{in} and R_s and $0 < \alpha < 1$. The noise output voltage will then be

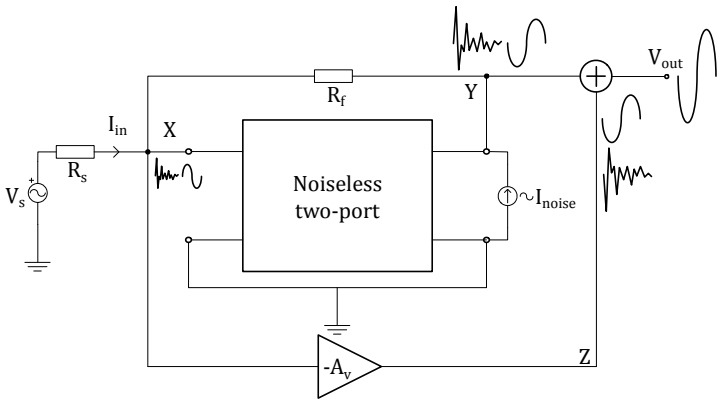

Figure 4.10: Ideal noise canceling circuit

$$V_{n,out} = V_{ny} - A_v \cdot V_{nx} = \alpha \cdot i_n \left(R_S + R_f - A_v \cdot R_S\right) \tag{54}$$

For total noise cancellation $V_{n,out}$ should be zero and that happens when

$$\left(R_S + R_f - A_v \cdot R_S\right) = 0 \;\Rightarrow\; A_v = 1 + \frac{R_f}{R_S} \tag{55}$$

In Figure 4.11 implementation of the circuit with transistors is shown where both the two port and the negative amplifier have been realized with a CS stage and a source follower. The input impedance and gain for the input CS stage has been presented in section 4.2.1 and the gain of the second stage will be $A_v = g_{m,CS}/g_{m,adder}$ which gives the relation between $g_{m,CS}$ and $g_{m,adder}$ (and by so also between M_{CS} and M_{adder}) because

$$A_v = 1 + \frac{R_f}{R_S} = \frac{g_{m,CS}}{g_{m,adder}} \;\Leftrightarrow g_{m,CS} = \left(1 + \frac{R_f}{R_S}\right)\, g_{m,adder} \tag{56}$$

The total gain for the signal from X to output will then be

$$A_{v,tot} = 1 - g_{m,input} R_f - \frac{g_{m,CS}}{g_{m,adder}} \tag{57}$$

All noise sources that can be modeled as a current source between source and drain of the input device will be canceled e.g. flicker noise, gate induced noise and channel noise. The noise from R_f will not be canceled nor that from M_{CS} and M_{adder}.

4.4.3 Noise Canceling Circuit with CG Input Stage

In Figure 4.12 a simple Common Gate(CG) LNA is shown. The small-signal current i_{in} has no signal path to ground except through the CMOS and then

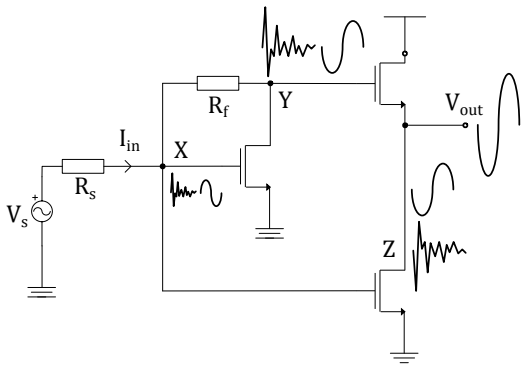

Figure 4.11: Basic noise canceling circuit with CMOS devices

i_{in} must be equal to i_{CG} and i_{CG} is also equal to $g_{m,CG}v_{in}$. Combining those expressions we get input impedance, Z_{in}, of

$$i_{in} = i_{CG} = g_{m,CG}v_{in} \;\Rightarrow\; Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{g_{m,CG}}. \tag{58}$$

Furthermore

$$\begin{array}{l} i_{CG} = \frac{v_{out}}{R_{CG}} = \frac{v_{in}\cdot A_{V,CG}}{R_{CG}} \;\Rightarrow\; i_{in} = \frac{v_{in}\cdot A_{V,CG}}{R_{CG}} \;\Rightarrow \\ \frac{1}{Z_{in}} = g_m = \frac{A_{V,CG}}{R_{CG}} \Rightarrow A_{V,CG} = g_{m,CG}R_{CG} \end{array} \tag{59}$$

and for impedance match at the input Z_{in} should be equal to R_s which finally gives

$$A_{V,CG} = \frac{R_{CG}}{R_S}. \tag{60}$$

The noise generated by the CG transistor can, as in the CS case, be modeled as a current source between the source and the drain and it will create two noise voltages, one at the input and one at the output. These voltages are fully correlated but have opposite phase and now there are two nodes where the signal have the same sign but the noise have different sign thus noise canceling would be achieved by adding the two nodes. The noise voltages are expressed as

$$v_{n,in} = \alpha \cdot i_n R_s(62) v_{n,CG} = -\alpha \cdot i_n R_{CG} \tag{61}$$

$$v_{n,CG} = -\alpha \cdot i_n R_{CG} \tag{62}$$

$$\alpha = \frac{Z_{in}}{Z_{in} + R_s} \tag{63}$$

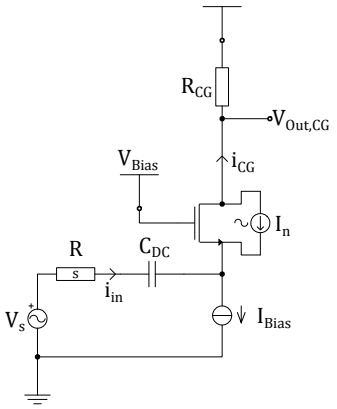

Figure 4.12: Common gate (CG) LNA

and because $R_{CG} > R_S$ the noise at the input must be amplified before they are added to the output. If a CS stage is used and the nodes are not added but subtracted through differential outputs the noise would be canceled while the desired signal would add up. Figure 4.13 illustrates the circuit with differential outputs and noise canceling. For total noise canceling $A_{v,CS}$ must be equal to $-A_{v,CG}$ which gives the g_m of the CS transistor.

$$A_{v,CS} = -A_{v,CG} = -\frac{R_{CG}}{R_S}(65)A_{v,CS} = g_{m,CS}R_{CS}(66)g_{m,CS} = -\frac{R_{CG}}{R_S \cdot R_{CS}} \tag{64}$$

The CG and CS transistor can be designed to have equal g_m and then $R_{CS} = R_{CG}$ or $g_{m,CS} = kg_{m,CG}$ and $R_{CS} = (k-1)R_{CG}$. Either way $A_{v,CS} = -A_{v,CG}$ and that makes the differential output signal balanced and ready for the mixer input.

4.5 Distortion Cancellation

In the article where noise canceling is discussed it is also discussed that the technique for noise canceling also can be used for cancellation of distortion [2]. Using a Taylor approximation the drain current of the matching device will be $I_{NL} = g_{mi} \cdot V_X + I_{NL}$ where N_L stands for nonlinearity high order terms. From Figure 4.14 the node voltages X and Y can be written as

$$V_X = V_S - R_S(g_{mi}V_X + I_{NL}) \tag{65}$$

$$V_Y = V_S - (R_S + R)(g_{mi}V_X + I_{NL}) \tag{66}$$

Equation (65) and (66) show that the relation between node X and Y is same as for the noise cancellation where the node Y voltage has $1 + R/R_S$

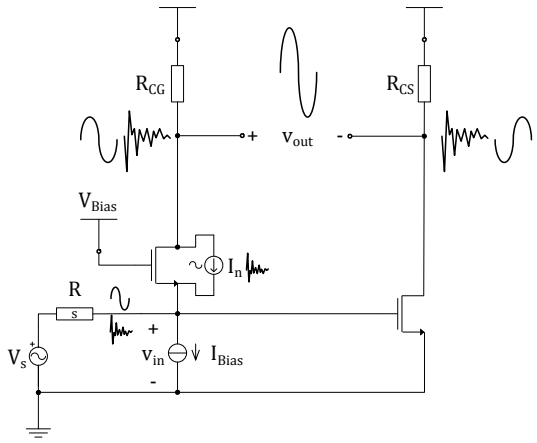

Figure 4.13: LNA with integrated balun and noise canceling

times higher amplitude than node X. Same as for the noise cancellation a gain of the feed-forward path of $A_V = 1 + R/R_S$ will cancel all nonlinear terms from the matching stage. As for the noise cancellation the distortion from the distortion cancellation stage itself is not cancelled.

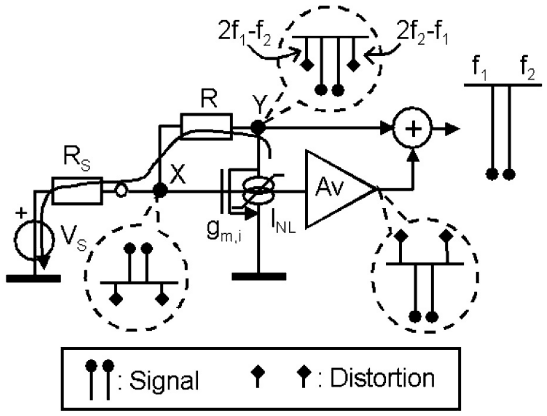

Figure 4.14: LNA with distortion canceling [9, figure 4.33]

Figure 4.14 shows the distortion cancellation principle for a CS stage with noise and distortion cancellation output. Two frequencies f_1 and f_2 with the same amplitude on the input are producing two 3rd intermediate distortions (IM) at frequency $2f_1 \cdot f_2$ and $2 \cdot f_2 - f_1$. In node X and Y the wanted signals are in anti phase while the distortion products are in phase. This difference between phases is used to cancel the distortion at the output where a feed-forward path with a gain A_v amplifies the signal and shift the phases of the signal and distortion products. Node Y and the feed-forward

path now have same signal phases leading to a higher signal output and different distortion phases leading to cancellation of distortion products.

4.6 Mixer

The mixer used in the test bench is a four-phase passive mixer. Here follows a quick description of the mixer as well as a small comparison with an active mixer.

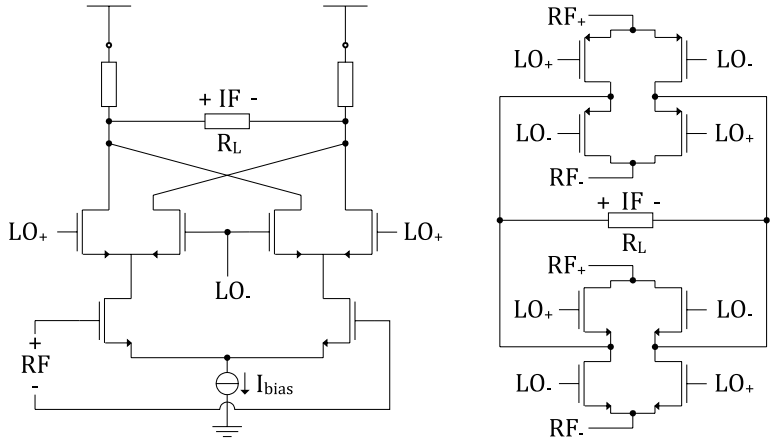

Figure 4.15: Left: Active Mixer Right: Passive Mixer

Figure 4.15 illustrates both an active Gilbert type mixer and a passive mixer. The RF input of the Gilbert mixer is a differential cascode CS stage and the LO signal is applied at the gate of the cascoded transistors. A benefit of the active mixer is the gain provided by the CS stage which lowers the gain requirement for the preceding LNA.

In the passive mixer the RF signal is connected to the drain or source respectively and works as the "voltage supply" for the transistors. RF+ and RF- both have the same bias level and therefore there is no DC drop over the transistors in the mixer, i.e. there is no DC current consumption. A great advantage with the zero drain current is that the flicker noise in a CMOS device is proportional to the drain current and this mode of operation greatly improves the noise figure of the mixer. To improve the noise figure even further the LO signal has a duty-cycle of 25%.

The architecture of the mixer is complementary, i.e. the mixer core contains both NMOS and PMOS devices. The switch conductance of the mixer is modulated by the RF voltage at the mixer input and this creates second-order intermodulation. This will still occur with NMOS and PMOS devices but in opposite direction for different devices and ideally will the modulation be canceled when summed together, if the devices are balanced.

The major drawback with the passive mixer is the lack of gain which puts higher demands on the LNA.

Both mixers in Figure 4.15 have a balanced structure which suppresses the noise injected from LO signal.

4.7 Differential Solution

As the LNA in this project is to be a drop-in replacement for the current LNA solution, consideration needs to be taken to match the surrounding components. As described in section 4.6 the mixer uses differential inputs and the LNA therefore needs a differential output. Since the simplest LNA stage in this project is a single-ended design the signal need to be converted to a differential output. The first design that was considered was with a balun as in the current architecture today. The problem was the conversion between voltage and current since the balun needed a current to drive it and the LNA had a voltage-to-voltage gain. To use the LNA in a differential model two LNA blocks were therefore used in parallel. This makes this LNA solution fully differential which is very good while it cancels common-mode distortion, something that can be devastating in mixed-signal chips.

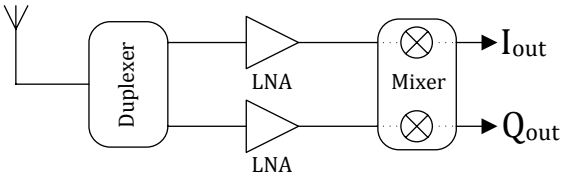

Figure 4.16: Differential solution

4.8 Discussion of Articles

At the start of this project a large amount of articles were considered. Some of the most interesting articles are investigated in more detail. This project has its main base from two articles "*Wide-band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling*" [2] and "*A 5 GHz, 21dBm Output-IP3 Resistive Feedback LNA in 90-nm CMOS* [3]. "The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology" [4] was also studied.

4.8.1 Wide-band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling

This articlewas written by Federico Bruccoleri, Eric A. M. Klumperink and Bram Nauta and discusses the tradeoff between nose figure (NF) and source-impedance matching. This fundamental tradeoff is often limiting the noise

figure to values above 3 dB. In this paper the tradeoff is broken with a feed-forward technique to apply noise canceling on the output. The technique that is used for noise cancellation is discussed in section 4.4 and can be seen in Figure 4.11.

The circuit that is designed is using an inverter as input stage which provides the input impedance and gain according to equation (49) and (50).

$$Z_{in} \approx \frac{1}{g_m} = \frac{1}{(g_{m1} + g_{m2})} \tag{67}$$

The main advantage of this design is the ability to cancel noise and distortion produced by the input stage. For optimal noise cancellation the CS stage M_1 have the gain according to equation (55).

To isolate the output from the input and decrease the effect of miller capacitances a cascode transistor M_{2b} is used. To use the supply voltage of 2.4 V only a small part of the current in M_2 are used in M_3. This is possible with a current bias on the output.

The design in this paper is a good base for a low-noise wideband amplifier due to its many advantages as

1. Simultaneous noise and distortion canceling due to matching device
2. Simultaneous noise and power matching for frequencies where the effects of parasitic capacitances can be neglected.
3. Robustness to variations in device parameters

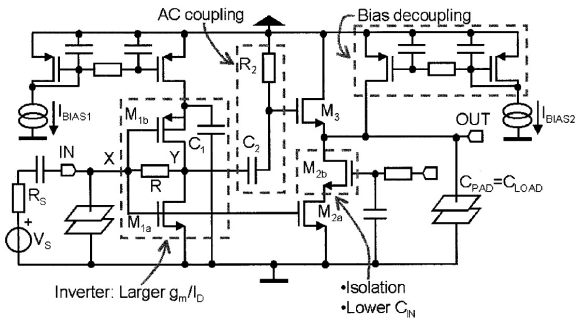

Figure 4.17: LNA solution from paper [2]

4.8.2 A 5 GHz, 21 dBm Output-IP3 Resistive Feedback LNA in 90-nm CMOS

This paper is written by Bevin G. Perumana, Jing-Hong C. Zhan and Stewart S [3]. Taylor and was made to investigate an inductor-less LNA with non-linearity cancellation. The main goal was to design a high linearity amplifier and at the same time be able to provide high gain. The solution is

an amplifier with two modes, high-linearity mode and low-noise mode. The LNA architecture that is used is the common CS stage with resistive feedback where cascoded transistors are used as input stage. When a cascode transistor is used in the matching stage a higher bandwidth is achieved due to lower W/L ratio. A lower current is used in the cascode to reduce the voltage drop over the load resistance. This is achieved by a gm-enhance technique using a bias resistor R_1 to bias current directly to transistor M_1. Still with a low g_m for the cascode stage the nonlinearity limits the overall circuit linearity. Resistive feedback is used to reduce the nonlinearity from the input stage by a factor ($IP3_{closedloop}/IP3_{openloop}$) of:

$$\frac{IP3|_{CL}}{IP3|_{OL}} = (1 + a_1 f)^2 \sqrt{\frac{a_3}{a_3(1 + a_1 f) - 2 f a_2^2}} \approx (1 + a_1 f)^{3/2} \qquad (68)$$

Measurements from this paper show a good performance with a high gain, good linearity and low current consumption. The drawback is the noise figure, which is 2- 3 dB

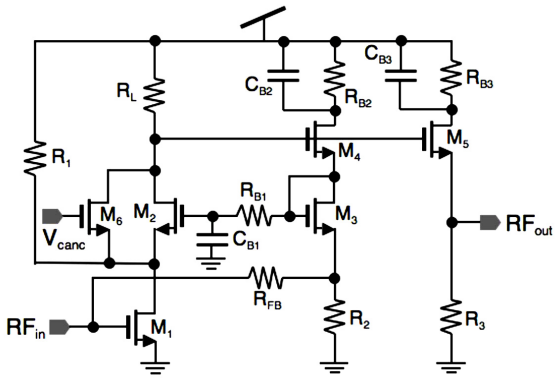

Figure 4.18: LNA solution from paper [3]

4.8.3 The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology

The article is written by S.C. Blaakmer, E.A.M. Klumperink, D.M.W. Leenaerts, B [4]. Nauta and introduces the simultaneous output balancing and noise canceling with CG stage at the input and a CS feed-forward shown in Figure 4.13 but not the circuit itself. According to the articles the circuit was first introduced 15-20 years ago but they all used CG and CS devices with the same size and bias and then the circuit cannot take advantages of simultaneous output balancing, noise canceling and distortion canceling. Instead the authors show that a larger $g_{m,CS}$ (wider M_{CS}) than $g_{m,CG}$ and a smaller R_{CS} than R_{CG}, so that $A_{v,CS} = -A_{v,CG}$ still applies, gives an optimal performance. Scaling M_{CS} with a factor of about four is said to give the best result and it is used for the circuit in [4].

$$g_{m,CS} = 4 \cdot g_{m,CG} \tag{69}$$

$$R_{CS} = R_{CG}/4 \tag{70}$$

$$R_S = 50\Omega g_{m,CG} = 20mS$$

$$g_{m,CS} = 80mSR_{CG} = 400\Omega R_{CS} = 100\Omega$$

The first article [1] introduces the balun-LNA and confirms the noise- and distortion canceling and in the second [4] the balun-LNA is combined with an active I/Q-mixer in such ways that the mixer works as the load for the LNA and call this approach a BLIXER, Balun-LNA-I/Q-Mixer, see Figure 4.19. The advantages in the later is that there are only three RF nodes in the circuit that can lower the RF bandwidth, the bias current is reused in the active mixer and LNA and the compact and area efficient design.

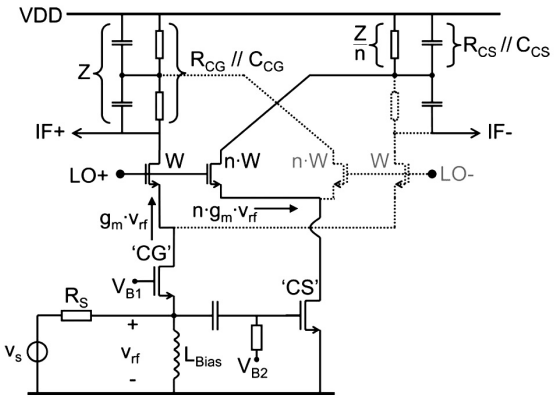

Figure 4.19: Blixer circuit

The results for the balun-LNA alone is much improved in the second article and it is those results that will be discussed and compared but there are some details in e.g. biasing from the first article that need some attention. The IIP2 demand for an Ultra Wideband (UWB, 3.1-10.6 GHz) receiver is above +20 dBm and IIP3 above −9 dBm and the goal with [1] was to investigate whether this is possible to achieve or not. The noise and distortion from the CG device is canceled and that makes the CS device the bottleneck of the circuit and the linearity of a resistively loaded CS stage has been carefully investigated. Section IV B in [1] is dedicated to "Distortion of the CS stage" and especially Fig. 6 in [1] is of interest and shown here in Figure 4.20. A V_{GS} of around 0.5 V would meet the linearity demands and the gain also peaks around this voltage but as seen in the graph IIP2 peaks

quite narrow around 0.5 V. This could be an issue when manufacturing the chip, process corners, or because of temperature variations. If the V_{GS} would shift, the IIP2 of the LNA could decrease below +20 dBm and the question is if it is stable enough.

In [4] the authors present results for the balun-LNA alone as well for the whole BLIXER. Because this thesis is about an LNA the results presented here from [4] will be taken from the graphs for the balun-LNA for a better comparison with the other LNA solutions. The balun-LNA in [4] is loaded with C_L=100fF

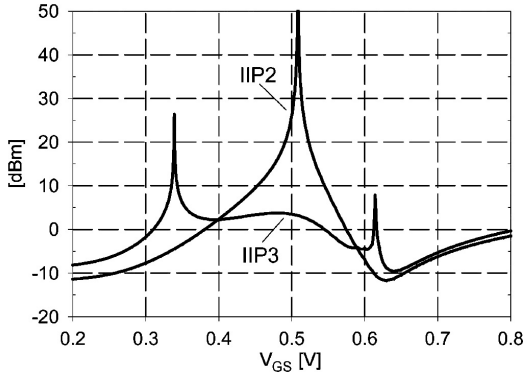

Figure 4.20: IIP2 and IIP3 due to V_{GD} is a CS-stage

4.8.4 Article Comparison

The results in Table 3 deviate a bit from those presented in the articles. This is due to that most of them have a higher bandwidth than the goal for this thesis and many of the values decrease at higher frequencies. For a more interesting comparison the result has been read from graphs in the articles to match the bandwidth of 800 MHz-2.5 GHz.

By comparing the measurements from these papers by the specifications from *table.1* several results are in line with our requirements. A wide signal bandwidth, good input matching, high linearity and a low current consumption are achieved. Still, big enhancements need to be done to reach the specifications of this project.

Table 4.2: Performance Comparison

Specifications	**[2]**	**[3]**	**[4]**	**Table.1**
Gain(dB)	13.7	25.2	21dB	30
S11 (dB)	<-8	<-15	< -12dB	<-12dB
IIP3 (dBm)	0	-6	0	-5
NF (dB)	2 - 2.6	≤2.5	< 2dB	<2dB
Power	35mW	42mW	21mW	27mW

5 Wideband LNA Design

In this project a Cadence design kit for a 90-nm RF-CMOS process is used and the LNA is simulated in a test bench containing pad models, duplexer and mixer provided by ST-Ericsson. The transistors that are used in this process has a breakdown voltage of 1.2 V there is also a transistor with thicker gate-oxide, which has a breakdown of 1.8 V. The voltage supply used in this design is 1.8 V, to give large voltage headroom, but the transistors are still implemented with the normal transistor. As long as the devices are cascoded or in series with a resistor breakdown can be avoided and the faster and less noisy transistor can be used with the higher supply voltage.

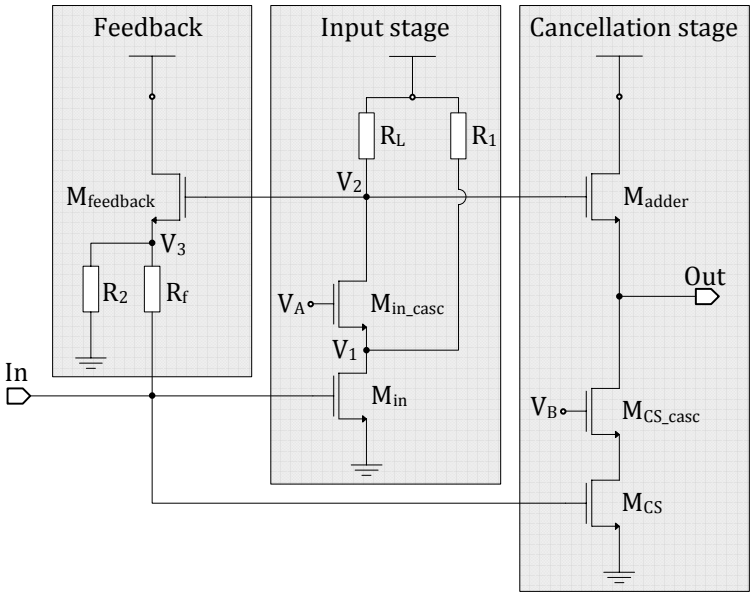

Figure 5.1: Circuit Overview

5.1 Input Stage

As discussed earlier different types of input stages have been considered such as common gate stage, common source and an inverter. The different solutions differs in terms of noise contribution, gain and distortion. Many papers [2] [3] [4] have more or less reached good performance with all of the different techniques. The decision fell on a CS stage with a cascode transistor as the input stage. This technique is chosen due to its simplicity and relatively good performance in terms of noise and gain, [9 section 4 fig 4.16f], and is complemented with a cascode transistor [3] for increased gain and input isolation and lower input capacitance, as discussed in section 4.2.2. The input is biased through R_L, which also serves as the load for the

cascode. To ease the requirements on M_{in_casc} and to lower the voltage drop over the transistor, a resistor R_1 was added as a current source to lead some of the drain current from M_{in} past M_{in_casc} and R_L. This makes it easier to find good bias levels for the input stage but it lowers the gain as some of the ac current will go through R_1 instead of R_L.

The main reasons for not choosing the LNA architecture from the "BLIXER" [4] is that it works best integrated with an active mixer and there are fewer devices that influence the gain and input match. It seems harder to adjust to this project specifications.

5.2 Negative Feedback

In amplifiers negative feedback is an efficient way to improve stability and linearity. In this project the feedback is employed to obtain a wideband input match. Instead of inductors as matching components the transconductance of the input stage has a big effect on the input match. At the start of this project a resistive feedback was used, which is a simple and effective way to control the input matching. The resistive feedback is described in section 4.2.1 and, as seen in equation (37), the feedback resistor itself does not contribute to the input match for lower frequencies. Instead the input match is set by $1/g_m$ of the input device. Considering the gain in a feedback circuit it is known that the closed loop gain will decrease due to the extra load on the output.

$$Open\ loop\ gain = -g_m R_L \tag{71}$$

$$Closed\ loop\ gain = \frac{R_L}{R_L + R_f} - g_m(R_L//R_f) \tag{72}$$

From [3] a solution with an active feedback is presented and by using this technique, one can isolate the input from node V2 and improve the input match. This approach will be discussed further in section 5.4.

We decided to implement an active feedback network using a source follower. This feedback has the drawback that it has gain below unity compared with a CS stage which contribute to more noise. The main advantage is a more stable circuit. The active feedback also increases the gain since it relaxes the load contributed by the feedback.

With the gate of a transistor as a load instead of a resistor, equation (72) would go towards infinity and the gain towards the open loop gain. However, this result holds only as long as $M_{feedback}$ is kept small and the frequency is relatively low. In this design the capacitance at the gate of $M_{feedback}$ is 5.67 fF and at a frequency of 2.5 GHz this gives an impedance of

$$\frac{1}{j\omega C_{gg,feedback}} = -j\frac{1}{2\pi \cdot 2.5 \cdot 10^9 \cdot 5.67 \cdot 10^{-15}} \approx -j11.2k\Omega \tag{73}$$

which can be considered large compared to $R_L = 3\ k\Omega$.

Even though $M_{feedback}$ is introduced R_f is kept in the feedback loop for two reasons. First of all it gives one more variable to set for making the input match and second the feedback loop contributes less noise with a resistor. A resistor is the least noisy element and by adding R_f, $M_{feedback}$ can be kept smaller, thus there is less noise introduced in the feedback. To prevent DC current from going through R_f, which will lead only to higher current consumption in the source, a DC bias is placed between the source of the transistor and the resistor R_f.

5.2.1 Noise Considerations in Feedback

We have investigated two solutions of feedback. The noise contribution in the first alternative with a resistive feedback is discussed in section 3.3. Since the feedback is designed with a source follower in the final solution the noise need to be investigated further.

Output noise due to the resistor R_f is

$$\overline{V_{n,out|R_f}^2} = 4kTR_f \tag{74}$$

The total input referred noise is

$$\overline{V_{n,in}^2} = \overline{V_{n,in}^2} + \frac{\overline{V_{n,out|R_f}^2}}{A_{v,VoltageFollower}} \tag{75}$$

Gain for the source follower is expressed as in equation (51).

As discussed in section 4.3 it is difficult to achieve a gain equal to one. To increase the gain the width of the feedback transistor can be increased leading to higher noise from the transistor but at the same time the total input noise will be suppressed by the increased gain.

5.2.2 Schematic Design

To lower its noise contribution the width of the transistor $M_{feedback}$ is chosen such that the transistor drives a relative low current due to noise consideration. At first a width of $W_{feedback}$=1.23 μm was chosen for the transistor and a resistance of 300 Ω. Simulations was showing that the design produce much noise. This leads to a new design where the width of the transistor is increased to 10 μm and R_f to 722 Ω. This results in a higher gain of the source follower and therefore lower noise in the feedback path.

5.3 Cancellation Stage

In accordance to the discussion in section 4.4 a cancellation stage is designed. First the theory was investigated by a test bench with an ideal cancellation stage according to Figure 5.2.

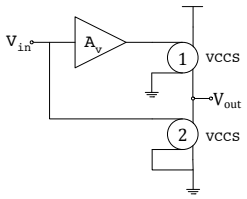

Figure 5.2: Cancellation-stage test bench

The cancellation stage is designed with two different blocks, one gain stage to amplify the feed-forward signal and one adder to add the feed-forward signal with the main stage signal.

To verify the function of the cancellation stage an ideal test bench is first designed. The input stage is designed as a CS stage with a cascode transistor and the cancellation stage with two voltage controlled current sources (VCCS). A VCCS works as a transistor thus it drives a current dependent on the voltage at the input. The VCCS is ideal and depends only on the transconductance, g_m, and is a good way to verify a system.

The VCCS 1 is working as a source follower explained in section 4.3. The second VCCS is working as a CS stage. For total cancellation the gain in the cancellation stage should match the gain in the input stage as in equation (55). To verify the theory a quick estimation was made and the noise figure is measured with and without cancellation stage. The result can be seen in Figure 5.3. The results show that the cancellation stage suppresses the noise by at least 10 dB compared with the signal without cancellation output.

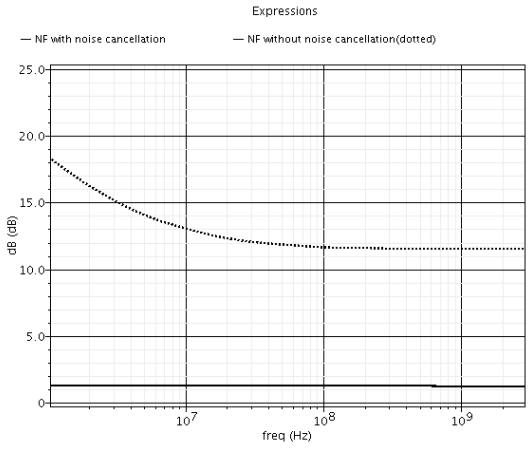

Figure 5.3: NF with and without cancellation-stage

For values $R_f = 300\ \Omega$ and $R_S = 100\ \Omega$ it can be seen from equation (55) that total noise cancellation occurs when

$$A_v = 1 + \frac{R_f}{R_s} = \frac{g_{m,CS}}{g_{m,adder}} \Leftrightarrow g_{m,CS} = \left(1 + \frac{R_f}{R_s}\right) g_{m,adder} = \left(1 + \frac{300}{100}\right) g_{m,adder} = 4 \cdot g_{m,adder} \tag{76}$$

$$g_{m,CS} = x \cdot g_{m,adder} = 4 \cdot g_{m,adder} \tag{77}$$

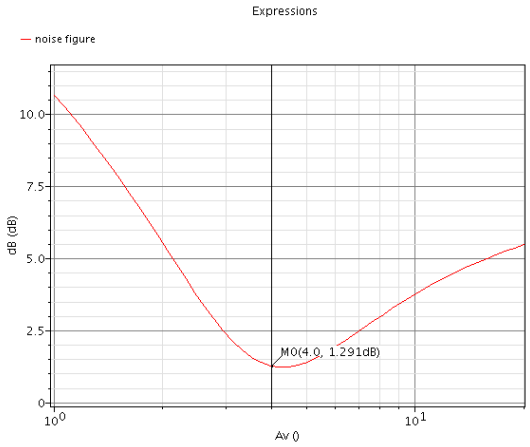

Figure 5.4: Gain optimum for NF

According to the theory in section 4.4 the cancellation technique should work for distortion as well as for noise.

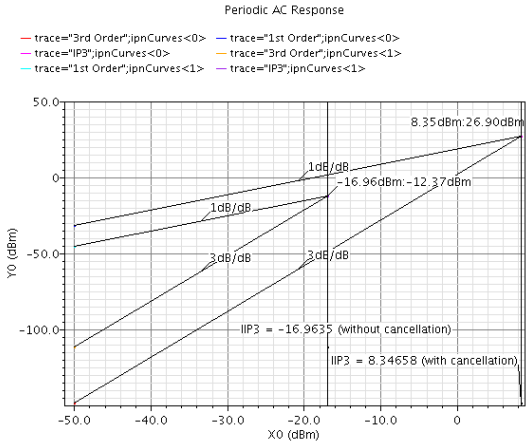

Figure 5.5: IP3 with and without cancellation-stage

Using the same test bench as for the noise cancellation simulations, we simulated the distortion for the two cases. From Figure 5.5 it can be seen that there is an improvement in linearity between the two cases. It is hard

to compare the result of these different simulations since they have different gain due to the extra output stage. One conclusion can still be made since there are more components introduced in the circuit and both a higher gain and a better linearity are achieved at the same time. In a typical circuit the nonlinearity increases if the gain increases. Figure 5.6 shown that the IP3 depends on the gain A_v for the cancellation stage. The figure clearly shows that the optimum for noise cancellation from equation (55) is also the optimum for distortion canceling.

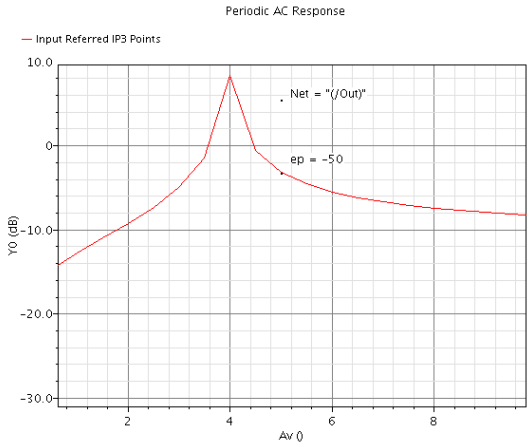

Figure 5.6: Gain optimum for IP3

5.3.1 Circuit Design

The ideal VCCS are changed to transistors. The gain of the cancellation stage is defined by the gain from the input stage as equation (56). For a gain of 24 dB from the input stage, the output stage is designed as

$$A_{V,inputstage} = 24dB = 15.8$$
$$A_{V,inputstage} = A_{V,\text{cancellation}} = \frac{g_{m,CS}}{g_{m,adder}} = 15.8$$

For a $g_m = 5mS$ for the adder the g_m of the CS-stage is defined as

$$g_{m,CS} = A_{V,inputstage} \cdot g_{m,adder} = 15.8 \cdot 5mS = 79mS$$

Figure 5.7 shows how the noise figure is affected by the noise cancellation-stage when transistors are used in the design.

To improve the cancellation stage a cascode is used to increase the gain of the common source stage in the feed-forward path.

If the gain, $A_{v,input}$ from the input to the output of the adder is measured with the feed-forward path disconnected a gain of 16 dB is measured. When the adder is disconnected and only the feed-forward path is used, a gain of

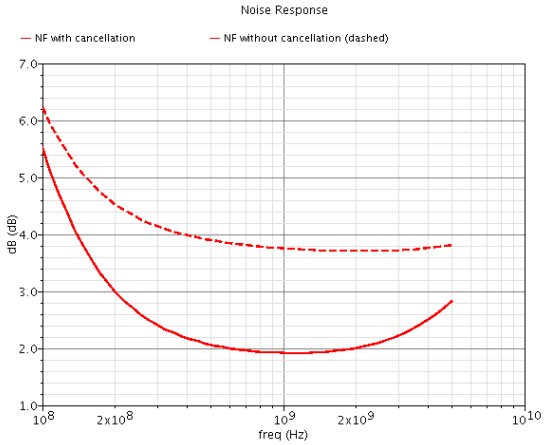

Figure 5.7: NF with and without cancellation-stage (Transistor model)

17 dB ($A_{v,cancellation}$) is measured. $A_{v,input}$ and $A_{v,cancellation}$ are relatively good matched according to the theory for optimal noise cancellation equation where $A_{v,input} = A_{v,cancellation}$.

5.3.2 Drawbacks in Cancellation Stage

A reduction by 5 dB is measured over the LNA compared with the gain over only the first gain stage, without adder and feed forward. This shows that the gain is decreased significantly over the adder which is a major drawback.

By investigating this more we found that by increasing the load of the CS stage by decreasing g_m of the adder the adder will have less gain. The adder needs a high g_m to provide a gain close to unity. The source follower is described in more detail in section 4.3.

Another drawback is the complex load of the mixer. Since the mixer is switched it is hard to design an equivalent load that can be used in the test bench. The equivalent load that was used is a resistor of 600 Ω and a capacitance of 100 f connected in parallel between the output nodes. For the first design ($A_v = 21\ dB$) the load worked well as an equivalent load, but when a second design was tested, which had higher gain ($A_v = 23\ dB$) in the test bench, the result was a smaller conversion gain than the first design when feeding the mixer.

Contrasting the two different designs we find that they differ in output impedance, which in the use with the mixer has large influence on the performance. As seen in Figure 5.8 the output impedance of the first design is around 550 Ω up to 1GHz while the second design, Figure 5.9, has only an impedance of 470 Ω. The equivalent mixer load has an impedance of 300 Ω. 61 % of the current goes through the load in the second design while the first design has 65 % of the current through the load.

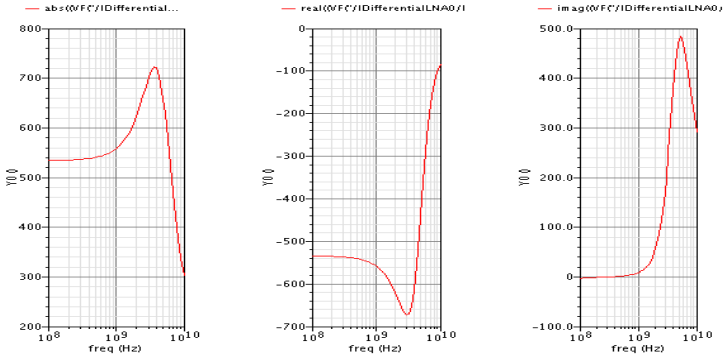

Figure 5.8: LNA output load (design1)

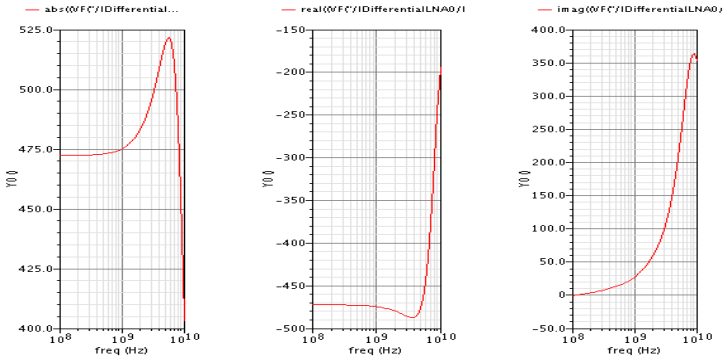

Figure 5.9: LNA output load (design2)

5.4 Input Matching

In LNA solutions it is essential that the input impedance is matched with the antenna impedance to achieve efficient power transfer. As discussed in section 2.3 a duplexer is used at the input, leading to new source impedance depending on the output of the duplexer (normally 50 Ω). In this project the duplexer has a differential output, which adds both a voltage gain and the opportunity to change the output impedance of the duplexer. The duplexer in this project has a differential output impedance of 200 Ω leading to an impedance of 100 Ω for each input. A higher input impedance results in a lower *NF*, section 3.3.3, for the circuit and a wider range for the input impedance. From equation (11) in section 3.2.2 it is obvious that a larger Z_0 can tolerate a larger variation in Z_L without causing larger reflection. For a S11=-12 dB is sufficient if 60 Ω $< Z_{in} <$ 167 Ω when matched against 100 Ω. From the beginning we used a resistive feedback to match the LNA input to a 100 Ω input load. This is a good and simple way to match the input and the absence of inductances makes it possible to use in a wideband solution. Quick pole estimation at the input is expressed as:

$$f_{-3dB} \approx \frac{1}{\pi R_S C_{IN}} \tag{78}$$

and it indicates that the input impedances should be constant up to *f-3dB*.

From simple impedance calculations, section 4.2.1, the input impedance can be expressed as:

$$Z_{in} = \frac{1}{g_m} = 100\Omega \quad \Rightarrow \quad g_m = 10mS \tag{79}$$

showing an input match when g_m of the main transistor is equal to 10 mS. The reality is somewhat different from these simple calculations. Input impedance calculation when the load is considered is expressed as

$$Z_{in} = \frac{Z_L + R_f}{1 + Z_L} \tag{80}$$

and it shows that the output has big influence on the input match. Z_L is not completely resistive and has a frequency dependence, which will make it harder to get a good wideband match.

5.4.1 Isolation

The circuit in Figure 4.11 has two weaknesses related to input reflections. One is the resistive feedback, which is not isolated from node *Y*. The second weakness is the CS stage in the noise cancellation which creates a direct connection with its C_{gd} to the output node. The influence of C_{gd} is increased due to the Miller effect. To improve the isolation to the input of the LNA we made two enhancements in the circuit. In the feedback an active transistor

is added and in the feed-forward path a cascode transistor is placed at the drain of M_{CS} to isolate the output (V_{out}) from the input. The active feedback consists of a common-source connected transistor, $M_{feedback}$, and a resistor, R_f, connected between the source of $M_{feedback}$ and the input of the LNA.

5.4.2 Active Feedback

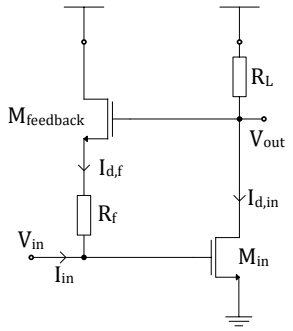

Figure 5.10: Active feedback

Figure 5.10 shows a simplified schematic of the input stage with the active feedback. By applying KCL at V_{out} and V_{in} the expression for the input impedance is obtained.

$$
\begin{aligned}
&V_{out} = I_{d,in}R_L = -g_{m,in}R_L V_{in} \quad \Leftrightarrow \quad A_v = \tfrac{V_{out}}{V_{in}} = -g_{m,in}R_L \\
&I_{d,f} = g_{m,feedback}\left(V_{out} - (V_{in} + I_{d,f}R_f)\right) = \\
&= -g_{m,feedback}\left((1 + g_{m,in}R_L)\, V_{in} + I_{d,f}R_f\right) \quad \Leftrightarrow \\
&I_{d,f}\left(1 + g_{m,feedback}R_f\right) = -g_{m,feedback}\left(1 - A_v\right) V_{in} \quad \Leftrightarrow \\
&I_{d,f} = -\tfrac{g_{m,feedback}(1-A_v)}{1+g_{m,feedback}R_f} V_{in} \\
&I_{in} = -I_{d,f} = \tfrac{g_{m,feedback}(1-A_v)}{1+g_{m,feedback}R_f} V_{in} \quad \Leftrightarrow \\
&Z_{in} = \tfrac{V_{in}}{I_{in}} = \tfrac{1+g_{m,feedback}R_f}{g_{m,feedback}(1-A_v)} \approx \tfrac{R_f}{-A_v}
\end{aligned}
\tag{81}
$$

As with a purey resistive feedback g_m of the input device sets the input impedance but now the impedance is scaled by R_f and R_L. When the cascode transistor M_{in_casc} and resistor R_1 are added to the circuit the gain of the input stage is changed to

$$A_v = -\frac{g_{m,in} g_{m,in\_casc} R_1 R_L}{1 + g_{m,in\_casc} R_1} \tag{82}$$

according to calculations in Design of analog CMOS integrated circuit [5]. R_1 and g_{m,in_casc} will effect the gain and then also the input match, especially R_1. The system is of course even more complex, transistors add capacitances in the signal path and the cancellations stage add capacitance to the load of the input stage and to the input of the LNA.

5.5 Biasing

In the design two bias circuits are used, current mirror and resistive voltage division. The first circit is used for M_{in} and M_{CS} which both should drive a current. The other transistors are biased via the resistive voltage division which has a lower current consumption but is not as stable as the current mirror. Since the transistors biased through the resistive voltage division are less sensitive to voltage deviations and do not have to drive a current this method works fine. Figure 5.11 shows the two current mirrors used in the bias circuit with their sizes and Figure 5.12 shows the two types of resistive feedback circuits used. The one with a DC capacitor is used for the cascode transistors as they need an AC ground on their gates in order to work.

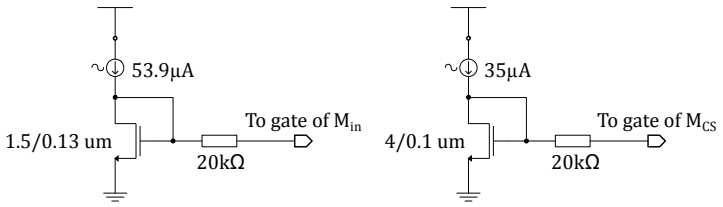

Figure 5.11: Bias current mirrors

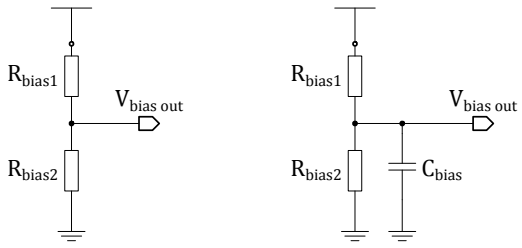

Figure 5.12: Resistive voltage division biascircuit

5.6 Considered Architectures

A few other architectures were considered during the project but for different reasons they where abandoned. This section will present these architectures.

5.6.1 Balun

The signal to the mixer has to be differential and as discussed in section 4.1 the solution today has been to use a balun. Early in the project the idea was to use the same balun together with the new LNA. The problem was that the balun has a current input whereas the LNA with the cancellation stage has a voltage output. Various attempts were made: to put the balun above the M_{adder}, between the M_{adder} and $M_{CS_{casc}}$ or to use a CS stage as a buffer between the LNA and the balun. In the two first attempts it was obvious that the LNA could not drive the balun because all the gain from the LNA was lost at the outputs of the balun. The CS buffer stage had a large current consumption and there were also degradation in noise figure from below 2 dB at the output of the LNA to above 3 dB after the balun.

The idea to use a balun was consequesntly abandoned. Besides, the goal from the beginning was to make a wideband, inductorless LNA. A balun is neither wideband nor is it inductorless.

5.6.2 Inverter Input Stage

Our first designs used an inverter as the input stage as described in section 4.2.3. Inspired by article [2] and motivated by the increased gain due to current reuse this seemed to be the best approach. In this early stage of the project the simple resistive feedback with only one resistor was used. This architecture showed promising results, especially in noise figure and linearity, but the gain was too low. One reason for this was that at the time it was thought that the balun used after the LNA which would add gain. Another reason was that the design was focused to have good results in noise figure and linearity at the cost of gain.

When the balun was dropped from the solution and the differential duplex with two LNAss was introduced instead the design was remade to meet the current consumption specification. The circuit was simulated in the same test bench as the final architecture later used and duplexer was not included in the test bench. The results are shown in Table 4.

Table 5.1: Result from differential LNA with inverter input stage

Parameters	**Results**
Differential output gain	15.8 dB
Noise Figure	$\leq$ 1.95 dB
IIP3	4.6 dBm
Current Consumption	15 mA
Input Matching	$\leq$ -12.5 dB
Bandwidth	800 MHz - 2.5 GHz

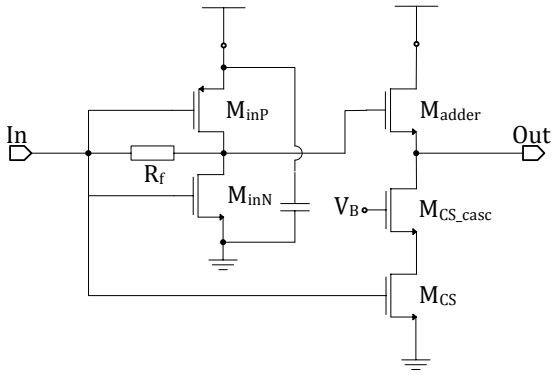

Figure 5.13: LNA with inverter input stage

Table 5.2 shows widths used towards the end before the design was dropped and as seen there were huge variations. Especially M_{CS_casc} raises some questions. It is huge which lowers M_{adder} efficiency as an adder and as a cascode it should be smaller or at least the same size as M_{CS} to be useful in the sense of increase the output impedance of the cascode configuration. It will still improve the isolation from the output to the input but not increase the gain as much as a cascode usually do. The simulations showed better results with this large cascode but when the cancellation stage of the cascode input stage architecture was designed, this huge transistor was not needed. The simulations were correct and it was good with a huge cascode but it would probably have worked better with a smaller transistor.

This architecture was never tested with the mixer and as the architecture presented in this chapter showed a higher gain this solution was set aside.

6 Simulations

All the results found in this chapter are from simulations using Cadence Virtuoso Analog design Environment. Two different test benches are used,

Table 5.2: Widths of the devices in the inverter input design

Device	Width (μm)
M_{inN}	30 - 50
M_{inP}	84 - 140
M_{CS}	80 - 100
M_{CS_casc}	350 - 510
M_{adder}	10 - 25

one with only the LNA stage using an equivalent mixer load and one with the mixer included. Below a short description of some of the simulations are included.

IP3 for LNA only

To measure IP3 of the circuit both a PSS and a PAC simulation is used. This is a two-tone test where two adjacent signals, one small signal (PAC) and one large signal (PSS) with equal amplitude drive the LNA simultaneously. The result is a cross section between the first order tones f_1, f_2 and the third order harmonics $f_1 \cdot 2 - f_2$, $f_1 \cdot 2 - f_2$.

PSS Stands for periodic steady state and is performed in the time domain. A PSS analysis consists of two phases: one transient phase and one shooting phase. In the shooting phase the circuit is repeatedly simulated over one period to find a steady state solution while the simulation changes the initial condition. In short the shooting phase tries to find two matching periods which can be seen as a steady state.

PAC Stands for periodic small-signal analysis but the simulations can be seen as non-periodic simulations presuming that a PSS simulation has been done. The PAC analysis translates the frequency period from the PSS when it affects the circuit with a small stimulus.

IP3 for LNA with Mixer

To simulate the IP3 for both the LNA and the mixer a QPSS and a QPAC simulation have to be done. The difference from the IP3 of the LNA only and with the mixer is that the mixer has an LO frequency that affects the system. The LO frequency acts like a large signal which results in two large signals on the input, something that the regular PSS and PAC simulation can not handle.

QPSS stands for Quasi periodic steady state analysis and is a series of PSS like simulations for all the input signals. A QPSS simulation starts by suppressing all moderate input signals and then performs a PSS on the large signal only. Moderate signals are large signals that are not used as references in the simulation. A PAC simulation is then made and the initial conditions

from the PAC simulation are used for the QPSS. This simulation technique is used when several large input signals are used at the input.

QPAC stands for quasi periodic small signal analysis. This simulation must follow a QPSS and computes transfer functions for multi tone frequency translation from QPSS simulations. This simulation is used when mixers are used in the circuit.

Conversion Gain for LNA with Mixer

To simulate a compression point when the LNA is used with a mixer a PSS and a PXF simulation iare needed. The periodic transfer function analysis, PXF, computes the transfer function from the input to the output of the circuit. The simulator can measure from any source at any frequency to a single output at a single frequency. The simulation also includes frequency conversion effects. First a PSS simulation is executed which computes the periodically time varying operating point. The PXF analysis then predicts the input to the circuit with the help of small sinusoidal signals. This tool is often used when conversion gain is to be calculated in circuits with oscillators.

Noise Figure for LNA with Mixer

To measure the noise figure when a mixer is used a PNOISE simulation must be used. PNOISE stands for periodic noise analysis and is similar to the regular noise simulation. The difference is that it can compute the frequency conversion effects in a mixer. A PNOISE simulation computes the total output noise where both input noise and mixer load noise are included. When a noisy input source is identified the noise figure can be calculated.

Compression Point for LNA with Mixer

To simulate the compression point for the full system with mixer the simulation can be made as a regular compression point simulation. In a regular simulation for the LNA only PSS and PAC simulations are used. When using a mixer the QPSS and QPAC need to be used instead due to the LO frequency that have to be considered in the simulation. The simulations are carried out by fixing the small signal amplitude from the source and then sweep the amplitude of the large input signal. By plotting the voltage of the small signal, QPAC, the 1 dB compression point can be found.

6.1 Differential LNA

First the LNA is simulated separately using a test bench with an equivalent mixer load. The differential load is a 600 Ω resistance and a 100 fF capacitance in parallel. In the simulations an ideal duplexer is used at the input to transform the single input to a differential output. The duplexer is specified

with an input impedance of 50 Ω and a differential output impedance of 200 Ω. Simulations of interest for the LNA standalone are

1. Gain
2. Input matching ($S11$)
3. Noise figure (NF)
4. Input referred third order intercept point ($IP3$)

It is hard to optimize the circuit for all the specifications since they are correlated in one way or another. A high gain is always desired since a high gain suppresses the noise in the circuit and is needed for the passive mixer. The drawback with high gain is that it increases the distortion, which can be devastating when many different frequencies are affecting the wideband LNA. During the project two versions of the LNA was designed. The first design was shown to have low IIP3 performance and the transistors were not designed with minimum length. A second design was made with the same architecture but with minimum length of the transistors and tuning for better distortion performance. Below the test bench used for the differential LNA can be seen.

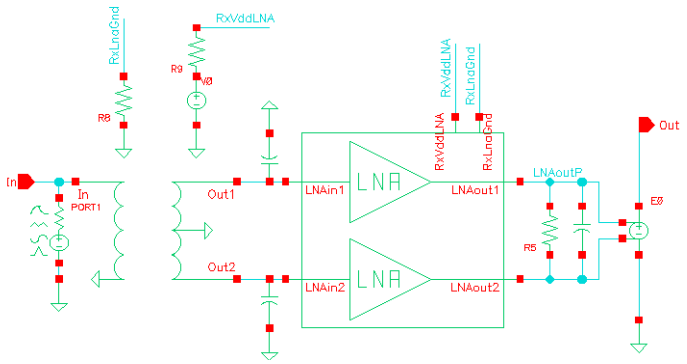

Figure 6.1: Test bench for differential LNA

6.1.1 Design 1

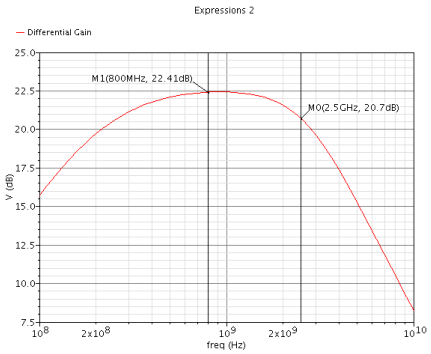

Figure 6.2: Differential gain

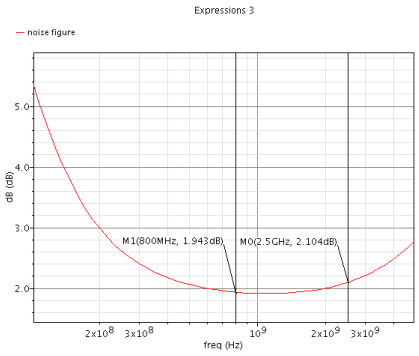

Figure 6.3: Noise figure

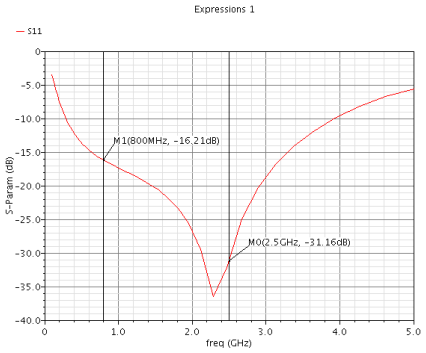

Figure 6.4: Input Match - S11

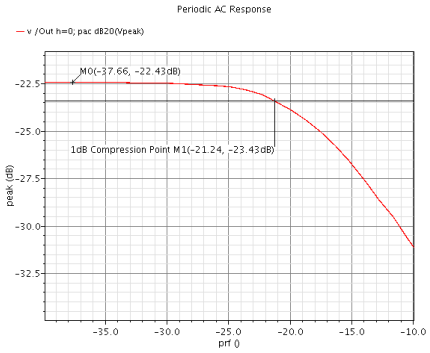

Figure 6.5: 1dB Compression Point

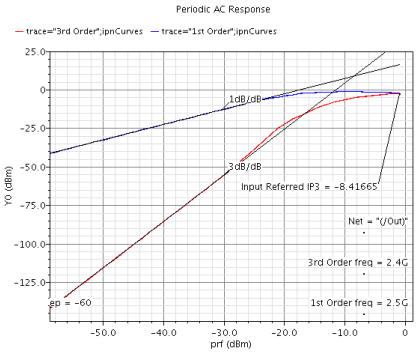

Figure 6.6: IIP3

To simulate how the circuit is affected by pad and wire capacitances the two inputs are swept with an extra capacitance. The results are shown below.

Sweep of Input Capacitance

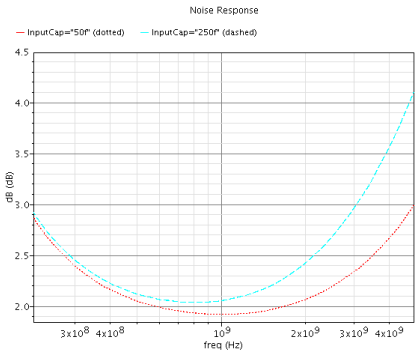

Figure 6.7: NF vs Input Cap (50 fF - 250 fF)

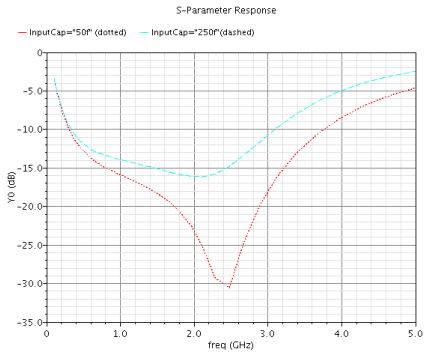

Figure 6.8: S11 vs Input Cap (50 fF - 250 fF)

To investigate the performance in different temperature a sweep between -30° and 90° Celsius is made. The result is shown below.

Sweep of Temperature

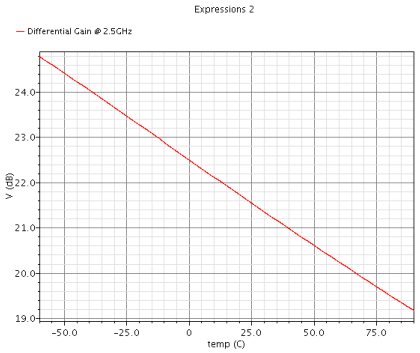

Figure 6.9: Gain vs. Temperature (2.5 GHz)

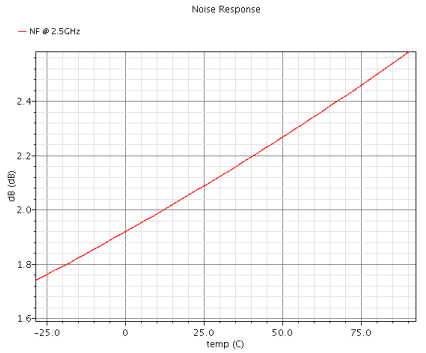

Figure 6.10: NF vs. Temperature (2.5 GHz)

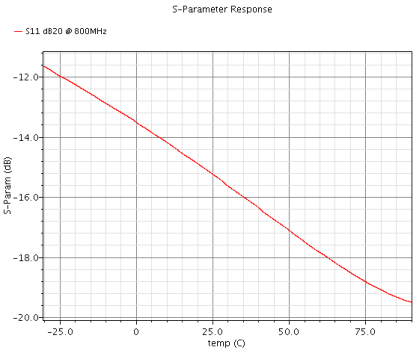

Figure 6.11: S11 vs. Temperature (800 MHz)

6.1.2 Design 2

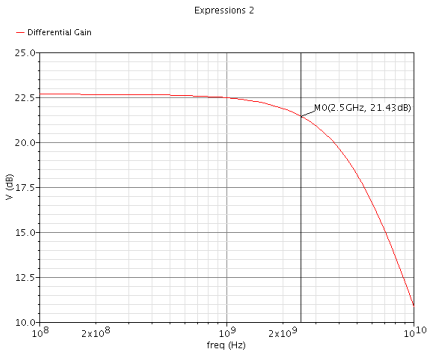

Figure 6.12: Differential gain

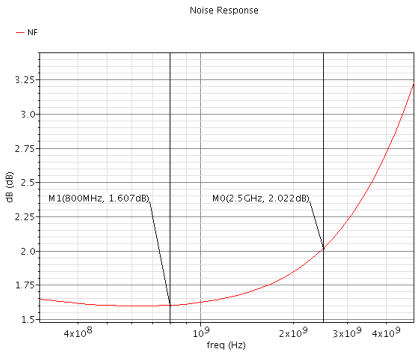

Figure 6.13: Noise figure

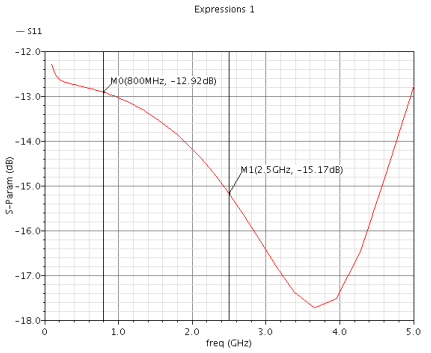

Figure 6.14: Input Match - S11

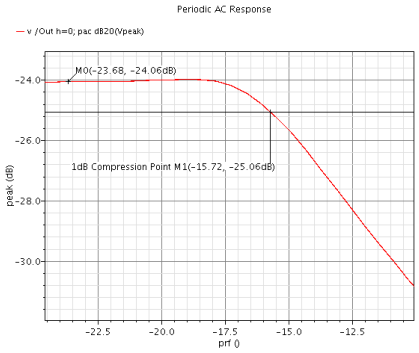

Figure 6.15: 1dB Compression Point

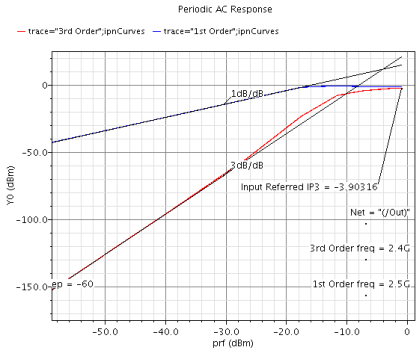

Figure 6.16: IIP3

6.2 Full System

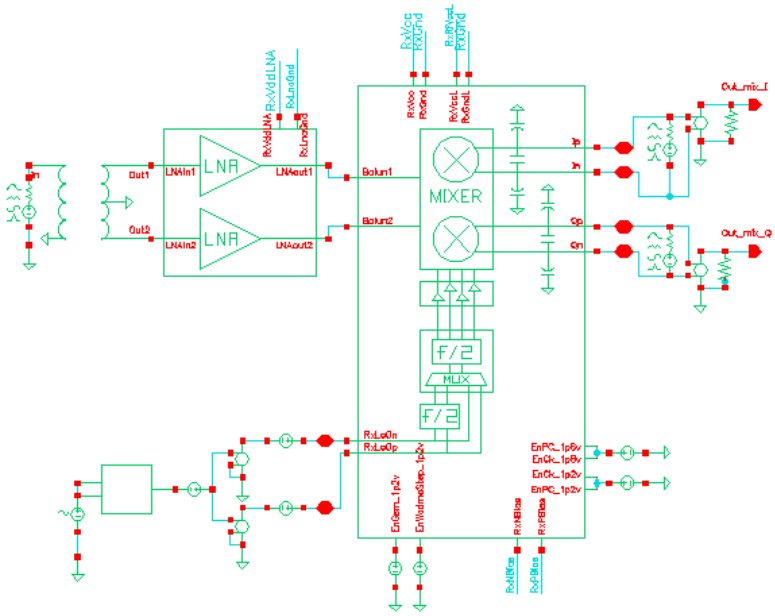

Figure 6.17: Test bench with Mixer

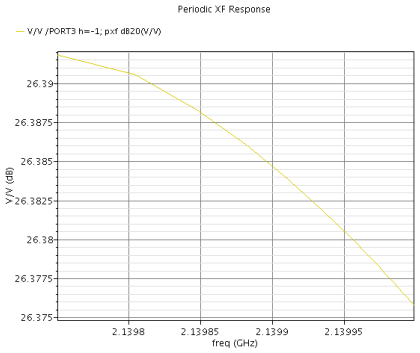

Figure 6.18: Conversion Gain Design 1

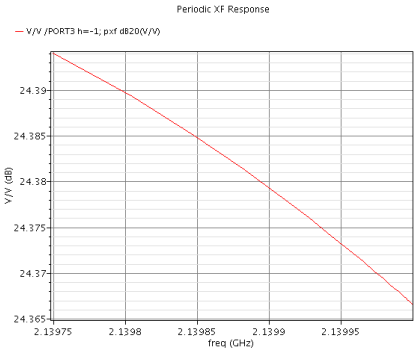

Figure 6.19: Conversion Gain Design 2

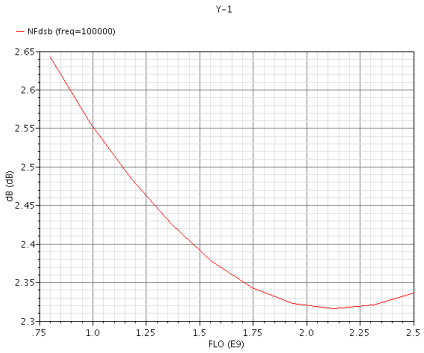

Figure 6.20: Noise figure, Design 1

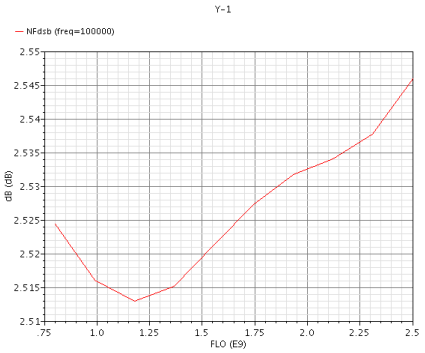

Figure 6.21: Noise figure, Design 2

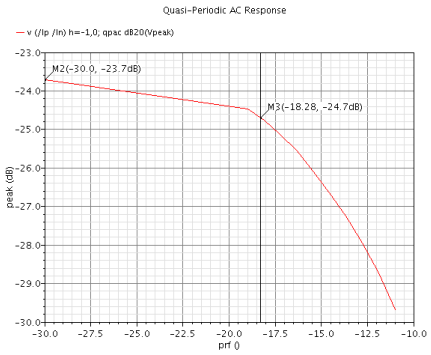

Figure 6.22: Compression point -1 dB, Design 1

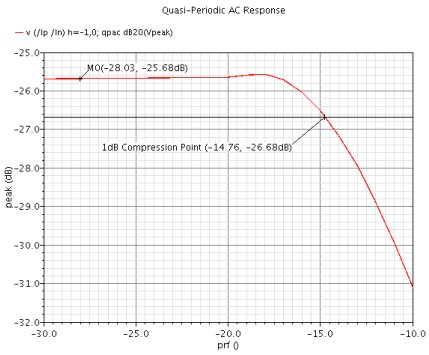

Figure 6.23: Compression point -1 dB, Design 2

By comparing the simulated values by the requirements from Table 1 we can see that the parameters do not have the performance that is required for a drop-in replacement in today's platform. A drawback in a wideband solution is that more sidebands introduce noise at the output leading to a higher noise

Table 6.1: Performance comparison of design 1 (D1) and design 2 (D2) Differential standalone

Parameters (Differential)	**D1**	**D2**	**Specifications**
Differential Gain (dB)	27.5	27.5	30.0
Noise Figure (dB)	2.1	2.0	≤ 2.0
IIP3 (dBm)	-8.4	-3.9	-5.0
Current Consumption (mA)	15.0	15.6	15.0
Input Matching (dB)	-15.4	-12.9	≤ 12.0
1dB Compression Point	-21.2	-15.7	-15
Operating frequency (GHz)	0.8 - 2.5	0.8 - 2.5	0.8-2.5

Table 6.2: Performance comparison of design 1 (D1) and design 2 (D2) with Mixer

Parameters (With Mixer)	**D1**	**D2**	**Specifications**
Conversion Gain Mixer (dB)	25.8	24.4	30.0
NFdsb (dB) @ 2 GHz	3.1	2.6	2.5
NFdsb (1st harmonic only)	2.9	2.8	n/a
IIP3 (dBm) @2.14 GHz	-8.4	-6.2	-7.0
Current Consumption (mA)	15.0	15.6	15.0
1dB Compression Point (dBm)	-18.3	-14.8	-15
Operating frequency (GHz)	0.8 - 2.5	0.8 - 2.5	0.8-2.5

figure when simulating the circuit with the mixer. One simulation was made to test this theory and if only the fundamental signal was considered during the simulation NF dropped 0.4 dB.

7 Conclusion and Future Work

The goal of this project was to implement a wideband LNA that would work as a drop-in solution in a test bench provided by ST-Ericsson. The wideband LNA should replace the narrowband LNA used today without compromising the performance of the receiver. The narrowband LNA needs matching components off chip and inductors on chip which both occupy valuable area whereas the wideband LNA needs none of these. The main idea was to design a resistive feedback to match the input over the whole bandwidth and to improve the noise figure and linearity by adding a cancellation stage.

7.1 Conclusion

A common-source input stage with a cascoded transistor is chosen to provide high gain in the LNA. To improve the input match an active resistive feedback is used since investigations showed that the output node of the

first stage had a big negative influence on the input match. Furthermore a cancellation stage is implemented to improve NF and linearity.

The input stage together with the feedback provides a good gain in the first stage, 23.9 dB, and with the source-follower in the feedback the input device is no longer locked to set the input match. This gives the designer more freedom to optimize the input stage for gain and noise figure. The input match can thereafter be adjusted with R_L and R_f. An S_{11} of -18 dB is easily obtained but to improve the gain and noise figure S_{11} is set to -13 dB as its lowest value inside the bandwidth of interest.

As discussed and shown in section 5.3 the cancellation stage greatly improves the noise figure and IIP3. One of the objectives was to investigate the effect of this stage and the result is clear. It works well and can be used to reduce the noise figure. and improve the linearity which is very useful in the LNA design. Unfortunately there are some drawbacks in the design that affects the gain of the LNA.

During the work transistors sizes were swept to find a good design and many simulations showed promising results. In an early stage, even if the results looked good, the gain from the input of the LNA to after the input stage was higher than the total gain of the LNA. This effect is due to the losses over the adder. The source-follower is not a perfect adder and the loss in gain over M_{adder} was simulated to 6dB when the RF signal was disconnected from the gate of M_{CS}.

Design 2 was made with the objectives to only use minimum lengths for the devices and one of the main reasons to try this approach was to improve the adder. As the devices becomes wider and shorter the losses over M_{adder} decreases but a wider transistor has however lower output resistance which turned out to be just as bad for the gain. The gain did not increase in the second design even though the loss in gain over M_{adder} decreased. That depends on the amplifier in the feed-forward path.

M_{CS} and M_{CS_casc} constitute an ordinary cascoded common-source amplifier and the gain of such an amplifier depends on its load. In this case the output impedance of M_{adder} is also the load of that amplifier. When the width of M_{adder} is increased to improve the addition, the output impedance, and the gain of the cascoded amplifier with it, is decreased. The total gain of the LNA is the gain from input stage over the adder plus the gain from the feed-forward path and therefore the total gain is not improved.

The noise-cancellation theory states that the gain of the CS amplifier in the feed-forward path should be the same as over the input stage and adder for total noise cancellation. The gain of M_{CS} and M_{CS_casc} is dependent on the output impedance of M_{adder} and the gain of the adder is dependent on the output impedance of the CS amplifier. Increasing the width of the transistors is not a solution to the gain problem. There is an optimum between the devices in the cancellation stage where good cancellation and gain is obtained.

Another problem faced with design 2 was that when it was simulated with the equivalent mixer load design 2 had a better gain than design 1 but when simulated in the test bench the result was the opposite. Our conclusion is that the equivalent mixer load does not represent the mixer well enough but the reason for this discrepancy is more difficult to understand. Design 2 has a lower current in the cancellation stage than design 1 and it is possible that as the mixer switches the current in design 2 is too low to drive the mixer without losses. One solution would be to design a new mixer with higher input impedance to improve the gain.

Another advantage with this topology is that its differential structure suppresses common-mode distortion which is not the case for the solution today.

The results show that it is possible to design an inductorless wideband LNA for GSM and WCDMA (800MHz-2.5GHz) and that the cancellation stage works. As for now the LNA connot be considered a drop-in solution to the existing test bench at ST-Ericsson, but the results are promising in that it is possible to achieve a wideband inductorless LNA that can meet the specifications.

7.2 Future Work and Improvements

As in all projects the major problem in this thesis was the time. Some ideas were not fully investigated and some approaches could have be improved if the time had allowed it. Here are the two main considerations for improvements and future work for this circuit.

7.2.1 Cascoded Input Stage

In table 5 and 6 the results from two designs of LNA architecture from chapter 5 are presented. The major differences between the designs are the sizes of the devices and resistors values, see appendix A for the parameter values in the designs. The device sizis differ much between the designs whereas the results are alike, especially in the test bench with the mixer. This result that there are more combinations of parameter values that will give good results and probably better ones than the ones presented here.

Because of the complexity of the input match and the correlation between input match, gain, noise figure and linearity a lot of simulations were made to find optimal parameter values. This is very time consuming and design 2, with the goal to have all devices at minimum length, was not investigated until the very end of the project and could therefore not be investigate thoroughly enough. With the experience from the first design the work was more structured and good results could be obtained in a short period of time. It is likely that this architecture can give better results if designed from the beginning once more with a more structured approach, i.e. set all the length

to minimum, start with small widths in all transistors and then start to get as good gain as possible disregarding, more or less, other results.

7.2.2 Inverter Input Stage

The design of the inverter input stage was the first design made and the procedure was unorganized. To get good results, parameters were swept and altered without reflections of a real implementation. The result was a huge variation in size between the transistors which probably made the design stiffer, i.e. it was harder to tune and alter the design with the transistor widths as the relative variation between the transistors was locked. The reason the inverter approach was abandoned was that the gain never got high enough while the LNA with cascoded input stage showed a higher gain that continued to climb. The cascode input stage was more aggressively designed, when it comes to the gain. All devices were swept to obtain a good gain and the other requirements were more and less ignored until the gain was good enough. Then it was easier to adjust the component values to improve NF, S11 and IIP3. This design method was never used for the inverter and active feedback was never studied together with the inverter either. Therefore it is likely that this solution can achieve a higher gain and still meet the other specifications. The inverter input stage LNA should be redesigned from the beginning with the same approach described in section 7.2.1. There was not time enough left in the project to test these improvements.

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A Design 1

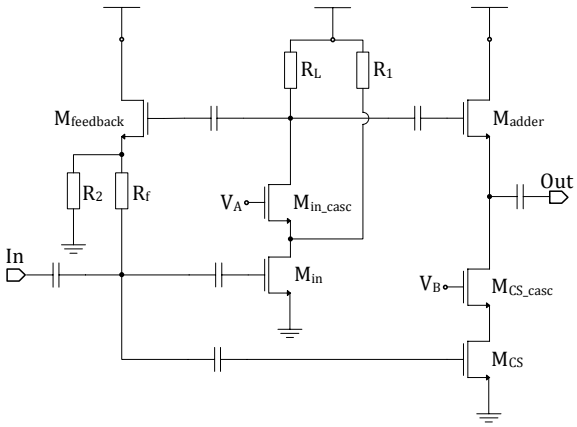

Figure A.1: Schematic design 1

M_in	50/0.13 μm
Min_casc	10/0.145 μm
Mfeedback	1.23/0.1 μm
Madder	13.5/0.4 μm
MCS	200/0.19 μm
MCS_casc	72/0.19 μm
RL	3 kΩ
Rf	300 Ω
R1	970 Ω
R2	1.7 kΩ

B Design 2

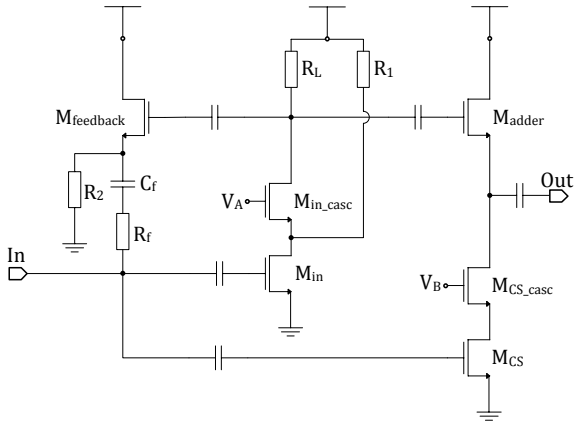

Figure B.1: Schematic design 2

Min	70/0.13 μm
Min_casc	10/0.1 μm
Mfeedback	10/0.1 μm
Madder	10/0.1 μm
MCS	200/0.19 μm
MCS_casc	72/0.1 μm
RL	3 kΩ
Rf	722 Ω
R1	700 Ω
R2	1.7 kΩ
Cf	10 pF

All the DC block capacitors are 10 pF in booth designs.