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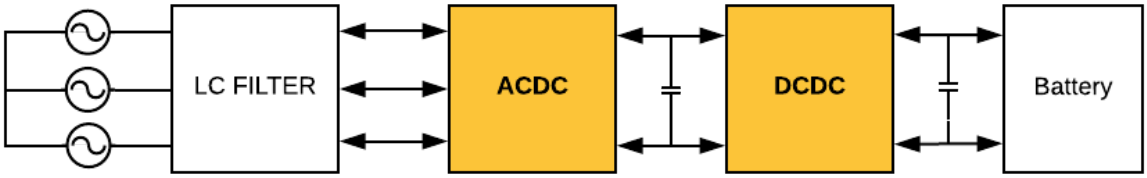

Loss and Thermal Analysis of a 300 kW Fast Charging Station

Master's thesis in Electric Power Engineering

MOHAMMAD JALAL UDDIN

Division of Electric Power Engineering
Department of Electrical Engineering
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2018

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A step by step description of 'Loss and thermal analysis of a 300 kW fast charging station' is presented in this report.
The software used was MATLAB Simulink and COMSOL Multiphysics.
MOHAMMAD JALAL UDDIN

Supervisor: Saeid Haghbin, Elbind Elektronik AB
Examiner: Ola Carlson, Professor of Electric Power Engineering

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Cover: Block diagram of a fast charging station (FCS).

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Abstract

This report presents the thermal modelling of a 300kW fast charging station. It includes details of steady-state loss calculation of single phase dual active bridge (DAB) converter and estimations of steady-state loss of three-phase ACDC boost converter, selection of cold plate, and finite element method (FEM) analysis of the system based on the calculated loss.
The thermal performance analysis of the system based on the FEM simulation shows that having 8 liter per minute (LPM) liquid flow with maximum 50 ^oC inlet temperature can maintain the maximum junction temperature of the MOSFET chip below 110 ^oC throughout the normal operating range with maximum of 314 $mbar$ pressure drop.

Keywords: fast charging, converter loss modelling, thermal design of converter.

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As a part of the thesis, I have stayed, as a research visitor, at Aalborg University, Denmark for one month. My special thanks to my supervisor Amir Sajjad Bahman, Assistant Professor of Energy Technology (ET) department of Aalborg University (AAU), for his support and precise supervision of how to learn something valuable in shortest possible time. Besides this, I want to remember in this particular time, Mohsen Ali, a visiting PhD fellow at ET department of AAU, for his time during my stay at AAU.
I would like to thanks all of my colleagues in the Department of Electric Power Engineering, Chalmers for their support and time, and having the useful discussion during the project period.
Here is my special thank belongs to my wife for her loving company, sincere patience, and sacrifice during the time of my thesis work. My parents, especially my mother, because of your endless prayer, I am here today. All praise and thanks belong to the Almighty, the one and only creator of this universe, for everything bestowed upon me.

Mohammad Jalal Uddin, Gothenburg, September 2018

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1
Introduction

1.1 Introduction

The conventional vehicles comply the fossil fuel to drive it. It leads to contamination of the atmosphere. However, the transport division has a significant contribution to greenhouse gases emission in the environment. Shortage of oil, environmental effects make thinking of alternative vehicles technology. Introduction of Hybrid and later Electric vehicles considered as the solution [1][2]. Nowadays the global electric automobiles have taken a right amount of percentage of the transportation sector [26]. The challenge in electric vehicles is to recharge its batteries as fast as possible. The implementation of the active power control is solely to control the charging rate for the EV charging operation while the reactive power control can be utilized to improve the overall power factor, provide the reactive power support to the power utility and reduce the power grid losses [3]. Increasing the power level of EV charger for fast charging the batteries produces a large amount of heat across the converter circuit as well on the components. Due to the thermal limitations of the device's components, keeping the temperature at a permissible level for having a longer lifetime of the components used and getting the reliability in the converter operations. This can be done by choosing the components or by having a properly designed heat sink. In this thesis, a heat sink, simple in layout, compact in design, is proposed for the investigated fast charging station (FCS) for keeping the maximum junction temperature within the allowable limit.

1.2 Project Background

The general trend in power electronic systems is towards a higher frequency operation. However, increasing the switching frequency leading to increased semiconductor and magnetic losses. Using SiC high-power modules and nano-crystalline magnetic materials provide the possibility to increase the switching frequency while improving the efficiency. A 50 kW charger is designed and constructed in Chalmers to demonstrate the concept. The idea is to continue that work for a power level of 300 kW. This charger has two converter units and mounted water cooling sink on it. The converter units provide the desired output power to charge the batteries. A liquid cooling system is implemented as the heat sink for cooling the system. It is the system on which the ongoing study is done. The converter that rectifies the AC power and maintains a constant dc link voltage is a VSC (Voltage Source Converter) type of converter. The semiconductor loss in it is well described in [4]-[8]. The other

converter that is used to charge the batteries is well known single-phase Dual Active Bridge (DAB) converter. The estimation of loss in it is explicitly demonstrated in detail in [9]-[15]. The analytical loss calculation is done in details for the DAB converter for the specific operating points, and a simplified approach is used to estimate the loss in VSC converter. Finite Element Method (FEM) simulator, in this case, COMSOL Multiphysics, is used to investigate the thermal performance analysis of the modelled system of FCS. Some of the useful techniques for thermal analysis are described in [16]-[19].

1.3 Main objective and contributions

The main objective of the thesis is to calculate and analyze steady state thermal losses of a 300 kW fast charger station (FCS) for designing a thermal system based on the analysis to ensure the maximum junction temperature of the switches within the permissible limit. So, the steady-state loss is evaluated for the FCS, a thermal system is modelled, verified, and thermal performance is done of the system. Hence, the main contribution of the thesis could be summarized as below:

- Modelling of losses of a single phase DAB converter in details considering two models of DAB, that are DAB lossless model (DAB-LL model) and DAB conduction loss model (DAB-CL model), and two switching technique known as soft switching (SS) and hard switching (HS).
- The estimation of loss in VSC converter in a simplified way with some assumptions.
- Modelling and verification of a power module (PM) with datasheet value in FEM simulator.
- Modelling of the thermal system of FCS in FEM simulator and its performance analysis.

1.4 Thesis outline

After the brief introduction, chapter two introduced the objectives and the design procedure of the FCS whereas chapter three described the mathematical model for semiconductor loss calculation in DAB and VSC converter of FCS. Chapter four presented the result of losses and efficiency of the system. In chapter five, details procedures of modelling and verifying PM, designing of the thermal system for FCS, and the thermal performance analysis of the FCS is demonstrated. Conclusion and future suggestions are texted in the last chapter, chapter six.

2

Design of fast charging station

2.1 Aims of the design

To reach the main objective, this thesis decided the aims of the design mentioned below.

- Finding the power loss across each of the semiconductor switches
- Thermal resistance between junction to ambient will be calculated to keep the case temperature around 90 ^oC.
- A suitable cold plate will be selected based on the thermal resistance and water flow speed of around 6 to 8 LPM.
- Modelling the system for the thermal analysis.
- The thermal performance will be analyzed on the designed system

2.2 Block description of FCS

The block diagram of a FCS is shown in Figure 2.1. The grid frequency three-phase AC power is getting into the ACDC rectifier through a low-frequency LC filter. The ACDC block includes three power module also known as half bridge leg, each of the modules includes two semiconductor switches depicted in Figure 2.2. This block rectifies the AC power to DC power at the switching frequency of 25 kHz. It also regulates the DC link voltage at around 700 V.

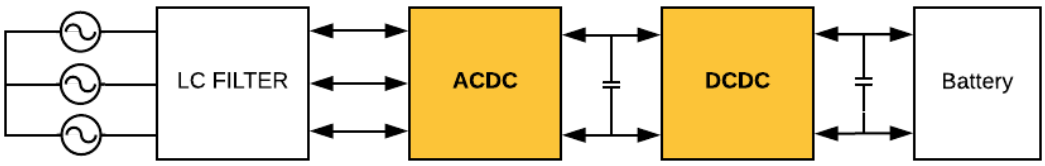


Figure 2.1: Block diagram of fast charging station

The last block is the high-frequency DCDC converter named single phase dual active bridge (DAB) converter. It provides the isolation between the power circuit and the charging circuit. It also provides the demanded current or power for fast charging of the batteries. Furthermore, it has an inductor that makes the bridge between the input bridge and the output bridge of the DAB converter. Input bridge and output

bridge of the DAB have two modules each that are switched at switching frequency of 25 kHz.

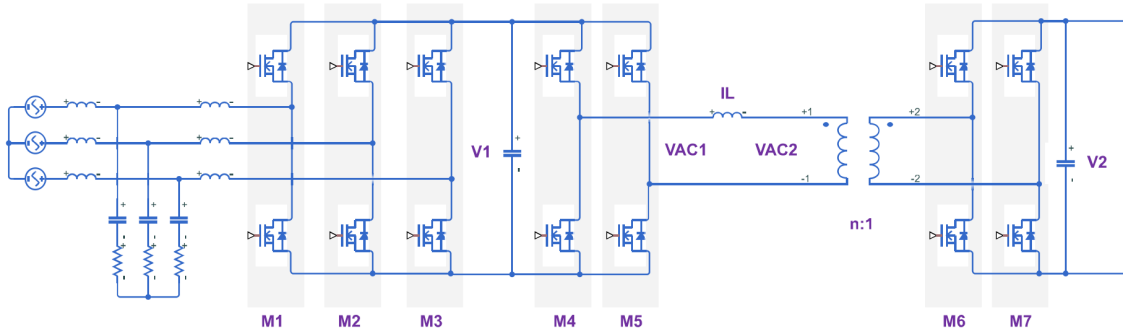


Figure 2.2: Electrical diagram of fast charging station

2.3 Steps of designing fast charging station (FCS)

The main focus of the design is to model the proper heat sink or cold plate to cool down the power module of the system. Because of these, estimation of power loss in active three phase VSC, and details losses in the single phase dual active bridge (DAB) converter are to be determined as described in [4]-[15]. The voltage and current at the semiconductor switches are two essential parameters to calculate the power semiconductor losses. The following steps are followed to find the losses in the DAB. The first steps of designing the FCS is to decide the nominal charging current and the charging voltage along with switching frequency. Based on the nominal charging current the phase shift between the two bridge of the DAB is to be determined. After that, the transformer turn ratio and the inductance value of the bridge inductor are to be determined. Then the stress values of the system are calculated based on the loss less model to identify the rating of the switch and to select the switches. After that, the on state resistance of the MOSFET and the diode are determined from the data sheets. Once the switches are selected, the switching and conduction losses are calculated for different operating points to find the worst-case switching and conduction loss per switch and module. Based on the assumption of constant dc-link voltage shown in Figure 2.2 as $V1$, and the unity power factor, the power loss of each module of VSC converter is estimated. After that, the thermal resistance calculation and selection of cold plate are done based on the worst-case loss. The system is built in COMSOL to see the thermal performance and to find the required velocity of the inlet liquid temperature and the pressure drop of the liquid. Based on the temperature and pressure drop, a suitable heat pump can be selected to take away the heat from the fluid. Finally, the thermal performance of the system is analyzed to see the temperature of the system.

2.4 Selection of phase shift

Selection of phase shift between two terminal voltages VAC1 and VAC2 of inductor defines the amount of power transfer to the load or batteries. Considering the

constant output current, primarily the operating points decided to analysis the DAB are tabulated in table 2.1. Two output voltages around the nominal output voltage are selected to include the effect of voltage changes during the charging period and to observe the impact on power semiconductor loss.

Table 2.1: Phase selection for constant output current and different output voltages

Operating points	DC Link voltage	Output voltage	Output current	Output Power	Phase shift
1	700 V	700 V	140 A	98 kW	49.7538^o
2		840 V		117.6 kW	
3		560 V		78.4 kW	

The phase shift between the terminal voltages of the inductor is found 49.7538^o. The maximum output current considers 140 A. Equation 2.1 is used to evaluate the phase shift and described in [14]. The maximum power and maximum output current can be achieved at the phase shift of 90^o. The maximum current, in that case, is about 315 A for three different operating points. Changing phase difference changes the output current as well as output power and vice verse as long as inductance, frequency, and turns ratio is fixed.

$$Pout = \frac{nV1V2\phi(1-\phi)}{2\phi^2 f_s L} \tag{2.1}$$

$$\begin{aligned} &where, \\ &\phi = \frac{\pi - \sqrt{\pi^2 - 4K}}{2} \\ &K = \frac{2\pi^2 f_s L P_{out} d}{nV1V2} \\ &d = \frac{V2}{V2_{nominal}}. \end{aligned}$$

2.5 Stress Value

The selection of semiconductor switches depends on the maximum stress of voltage and peak current in the system. So, it is important to find out the stress value of the system for selecting the power semiconductor switches or to validate the selected power semiconductor switches or module. The zero loss DAB model detailed in Chapter 3 is used to calculated the stress value for selecting the switches and estimated the losses in each component [13] [9]. The stress values evaluated are as below:

- RMS current flowing through the inductor, switches and transformer.
- Peak current at certain time points or at switching instant.
- Voltage across the switches during the turn on and turn off of the switches

Equations 2.2 to 2.5 are derived based on the single phase DAB lossless model (BAB-LL model) to determine the current at different time points of a switching cycle mentioned in [13]. $I_{L,T0}$, $I_{L,Tphi}$, and $I_{L,Thalf}$ are the current respectively when $t = 0$, $t = T_\phi$, and $t = \frac{T_s}{2}$. Based on the parameters values and different output voltages, the stress values are calculated for two different phase shift values where one is to supply nominal output current and others is to supply possible maximum output current. The result are tabulated in 2.2 and 2.3.

$$I_{L,T0} = \frac{\pi\left(nV2 - V1\right) - 2\phi nV2}{4\pi f_s L} \tag{2.2}$$

$$I_{L,Tphi} = I_{L,T0} + \frac{V1 + nV2}{L} T_\phi \tag{2.3}$$

$$I_{L,Thalf} = I_{L,Tphi} + \frac{V1 - nV2}{L}\left(T_{\frac{1}{2}} - T_\phi\right) \tag{2.4}$$

$$T_{IL=0} = -\frac{I_{L,T0} L}{V1 + nV2} \tag{2.5}$$

Table 2.2: Calculated stress current for $\phi = 49.7538^o$

Output Voltage	$I_{L,T0}$	$I_{L,Tphi}$	$I_{L,Thalf}$	$I_{L,RMS}$
700	-193.49	193.49	193.49	174.75
840	-162.18	263.49	162.18	195.65
560	-224.79	123.49	224.79	161.44

Table 2.3: Calculated stress current for $\phi = 90^o$

Output Voltage	$I_{L,T0}$	$I_{L,Tphi}$	$I_{L,Thalf}$	$I_{L,RMS}$
700	-350	350	350	285.77
840	-350	420	350	315.65
560	-350	280	350	258.78

The maximum peak and RMS value of currents are 420 A and 315.65 A respectively for the phase shift of 90^o. The same quantities are 193.49 A and 195.65 A respectively for the phase shift of 49.75^o. Hence, there is a 30^o of phase margin available for higher load power demand or higher load current. A power module (PM) of CAS300M17BM2 is available with maximum instantaneous current of 900 A and continuous current rating of 300 A detailed in [25] [15]. This device is selected and used for the project implementation.

2.6 Components selection

The selection of components for the DAB converter based on the optimized efficiency is described in details in [13]. It also explained the procedure of the choice of switches and their stress values explicitly.

2.6.1 Selection of n and L

The turns ratio of the transformer known as n is selected as one in this study and the value of the bridge inductance is selected in a way to be able to produce the required output current of the system as an RMS value. The value of inductance needed is selected using equation

$$I_o = \frac{nV1\phi(1-\phi)}{2\phi^2 f_s L} \tag{2.6}$$

where I_o is the output current plotted against inductance, L, in Figure 2.3 for phase shift (PS) of 49.75^o. Hence the inductance of 20 uH is considered throughout the study. Figure 2.3 depicts that to generate any current higher than 140 A, the mentioned inductance value is sufficient for the system.

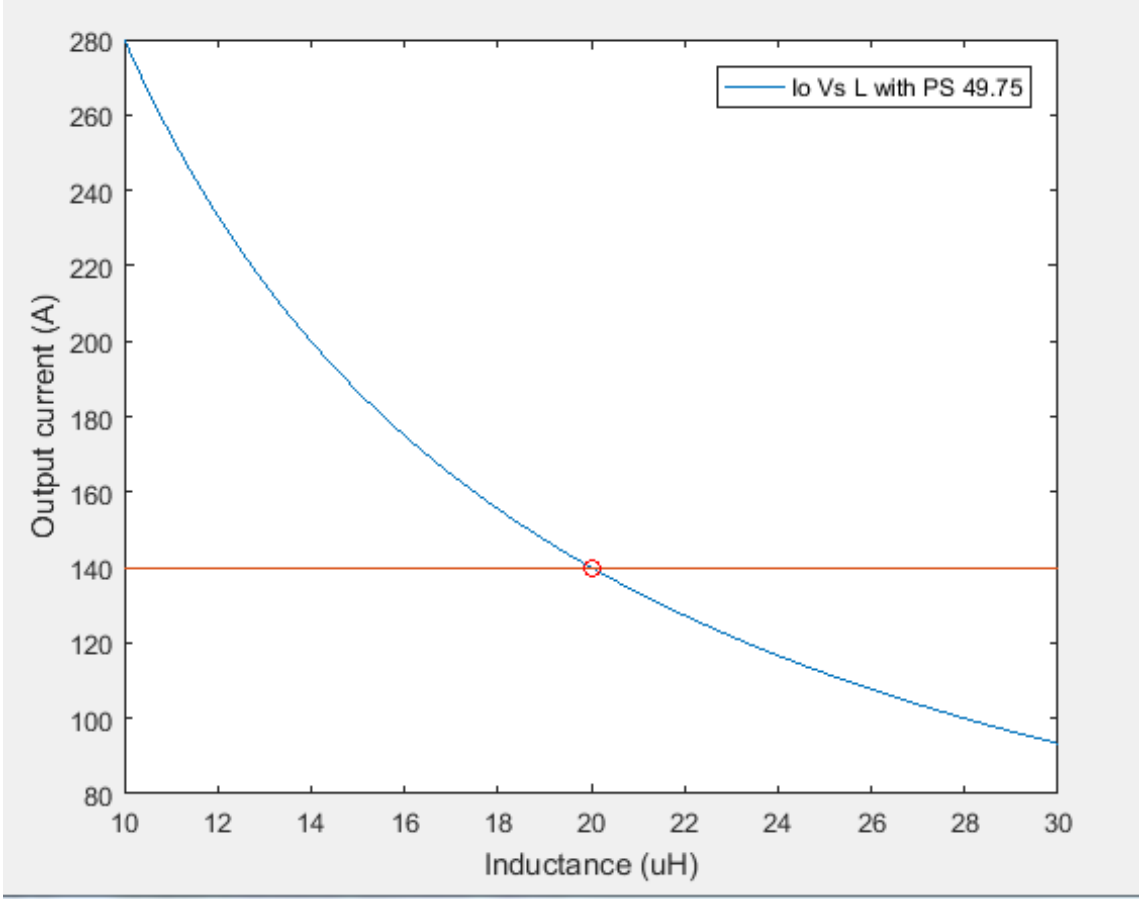


Figure 2.3: Block diagram of fast charging station

2.6.2 Selection of switch

The power module selected in section 2.5 has the capability to carry the required RMS output current. It is a half-bridge power module (PM) having two MOSFET switches with corresponding anti-parallel DIODEs. The main features of this module are that it has very low on-state resistance and there is no reverse recovery current flowing through the DIODEs.

2.6.2.1 Selection of on-state resistance

The selection of the on-state resistance for the MOSFET and the DIODE has been made using the datasheet value [25]. The nominal value of the datasheet can be used if the temperature variation does not take into account. For the high power application, it is good to take the temperature variation into account for selection of the on-state resistance. The temperature versus the on-state resistance graph can be used along with the equation 2.7 to estimate the on-state resistance of the MOSFET or the DIODE [24].

$$R_{ds,on}(Tj) = R_{ds,on}(25^oC)(1 + \frac{\alpha}{100})^{(T_j - 25)} \tag{2.7}$$

where $R_{ds,on}$ is the on-state resistance at mentioned junction temperature, α is the coefficient of the temperature variation, T_j is the junction temperature, and the nominal temperature is 25^oC. The value of α could be determined by selecting two points from the datasheet temperature-resistance graph and using the nominal value of the datasheet along with the equation stated.

2.7 Conclusion

After a brief description of the system, the stress values of the switches of the system are calculated based on the required amount of output current and output voltage. After that, the switches, transformer turn ratio, and the inductance have been selected for the operating point. The procedure of calculation of the on-state resistance of the MOSFET and the DIODE is presented at the end of the chapter. Based on the selection made on this chapter, the steady state loss of the system and the thermal system design based on the steady-state loss will be made in the upcoming chapter.

3

Steady state loss calculation

3.1 Introduction

This chapter introduces the basic of semiconductor loss classified as switching loss and the conduction loss. Then it selects the essential parameters which need for semiconductor loss calculation.
It also presents a details loss calculation method for the single phase dual active bridge (DAB) converter based on two different models and two different switching techniques. Those models are DAB lossless model (DAB-LL model), and DAB conduction loss model (DAB-CL model). The switching techniques used are soft switching (SS), and the hard switching (HS). The switching current, average current, and the RMS current are extracted for four cases such as 'DAB-LL model with SS,' 'DAB-LL model will HS,' 'DAB-CL model with SS,' and 'DAB-CL model with HS.' Based on these current, semiconductor losses across the DAB will be calculated in the next chapter.
Finally, the chapter ends with the estimation of the power losses across the ACDC rectifier.

3.2 Semiconductor loss

Switches in each half-bridge module cause the semiconductor losses commonly known as switching loss and conduction loss. These are the principal losses contribute to the heating of the power module as well as the power switches. Accurate modelling of these losses is essential for designing the thermal system for cooling down the system and keeping the junction temperature below the permissible limit. The basis of calculating those losses are described in the following sections.

3.2.1 Conduction loss

The first equation used to evaluate semiconductor conduction loss is described in Equation 3.1. The parameters used in the equations, some of them can be extracted from the datasheets of PM such as R_{on}, V_F, etc., and some of them must be calculated from the physical circuit using circuit analysis such as I_{AVG}, I_{RMS}. R_{on} is the on state resistance of the MOSFET known as $R_{ds,on}$ or on-state resistance of the Diode know as $R_{diode,on}$. V_F is the forward voltage drop of the semiconductor device which is 0V for MOSFET in the chosen PM and 0.7V for the DIODE of the selected PM. Average and RMS current needed for evaluating conduction loss for

ACDC boost converter will be estimated for steady-state loss calculation. These currents are assessed for single phase DAB using details loss calculation method of the DAB.

$$P_{COND} = V_F I_{AVG} + R_{on} I_{RMS}^2 \tag{3.1}$$

3.2.2 Switching loss

The general equation uses to evaluate the switching loss are in equation 3.2 described in [14]. The parameters which are estimated from the datasheets of the PM are shown in table 3.1 according to [14]. Switching current and switching voltage are two parameters depend on the types of converter topology, switching technique, and circuit conditions. These parameters calculations are detailed in the respective section.

$$P_s = f_s \left(E_{on} + E_{off} \right) \tag{3.2}$$

$$E_{on} = E'_{on} \left(\frac{I_s}{I'_s} \right)^{K_{I,on}} \left(\frac{V_s}{V'_s} \right)^{K_{V,on}} \tag{3.2a}$$

$$E_{off} = E'_{off} \left(\frac{I_s}{I'_s} \right)^{K_{I,off}} \left(\frac{V_s}{V'_s} \right)^{K_{V,off}} \tag{3.2b}$$

Table 3.1: Parameters of switching loss calculation

Parmeters	Explanation	CREE (CAS300M17BM2)
E'_{on}	Data sheet Turn-on Switching Energy (mJ)	13
E'_{off}	Data sheet Turn-off Switching Energy (mJ)	10
V'_s	Data sheet value of switching voltage (V)	900
I'_s	Data sheet value of switching current (A)	300
$K_{V,on}$	Turn-on voltage coefficient	1.83
$K_{I,on}$	Turn-on current coefficient	0.647
$K_{V,off}$	Turn-off voltage coefficient	1.17
$K_{I,off}$	Turn-off current coefficient	1.26
E_{on}	Calculated turn-on energy at I_s and V_s	–
E_{off}	Calculated turn-off energy at I_s and V_s	–

3.3 Details loss calculation of DAB

The thesis has investigated the details loss in single phase DAB converter shown in figure 3.1 as it is one of the most critical parts in the FCS circuit.

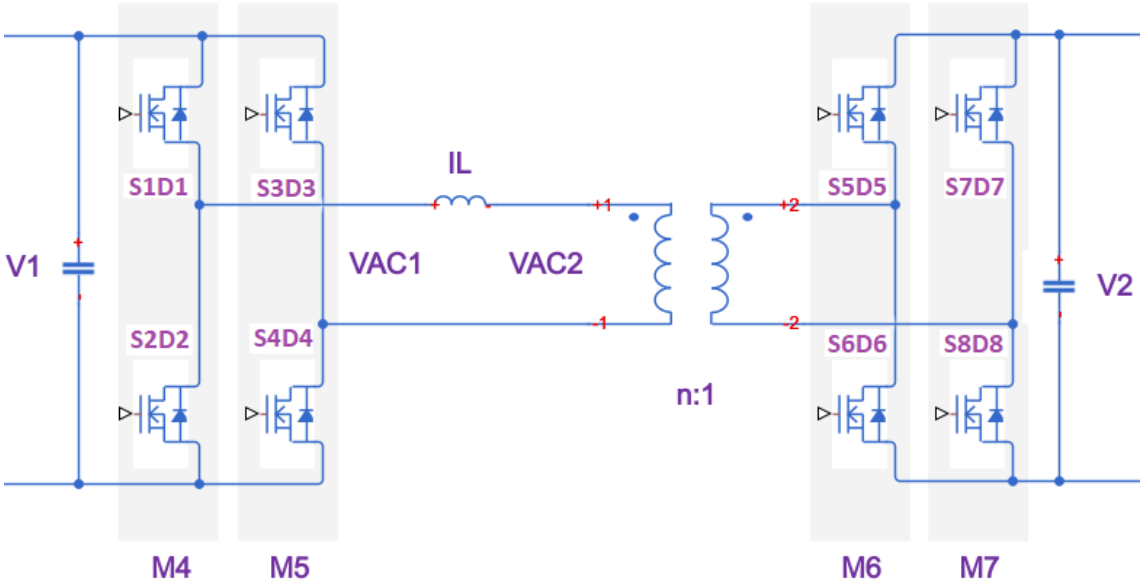


Figure 3.1: Block diagram of the single phase DAB

It has four power modules (PMs), one isolation transformer, and one bridge inductor as the main components of it. It has been modelled in two different way detailed in [13]. These two models are named as

- DAB lossless model (DAB-LL model)
- DAB conduction loss model (DAB-CL model)

The calculation of switching and conduction loss of the semiconductor switches require the average and RMS current of the inductor for different time intervals. Figure 3.2 depicts the six different section of the induction current for one period of switching frequency. The time points $T_0, T_1, T_\phi, T_{\frac{1}{2}}$ and T_s label in the figure are representing following meaning.

- T_s represents the one switching period
- $T_{\frac{1}{2}}$ represents the half switching period
- T_ϕ represents the time equivalent phase difference and $T_\phi = \phi/(2 * \Phi * f_s)$
- T_1 represents the time when current is equal to zero.
- T_0 represents the time when current begins
- f_s represents the switching frequency
- ϕ represents the phase difference between two ac voltages of the DAB

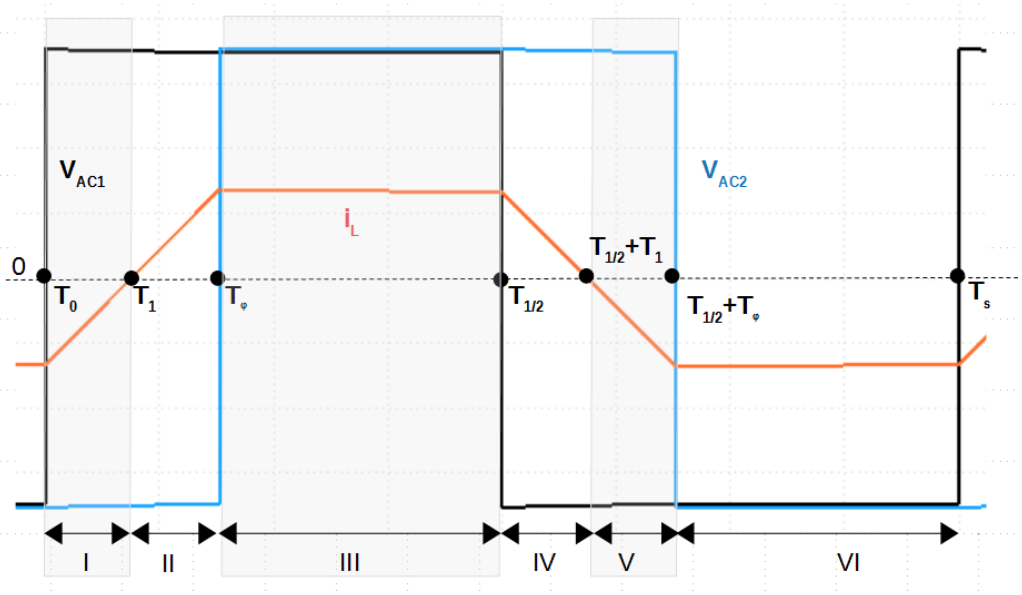


Figure 3.2: The time interval of the inductor current are labelled in six different segments

Here $V_{AC1} = V1$ and $V_{AC2} = nV2$ and $V1, V2$ are the input and output voltage of the DAB and n is the turn ratio of the transformer.

The phase shift modulation technique creates the phase shift between two terminal voltages of the inductor, which are VAC1 and VAC2, with 50% duty cycle of the switching frequency to control the amount of power flow and its direction.
In Figure 3.2, section IV, V and VI are the complements of section I, II and III as because of the half-wave symmetry of the inductor current. The voltage difference for the different section is as follow.

- Section I and II have the voltage difference of $V_{AC1} + V_{AC2}$
- Section III has the voltage difference of $V_{AC1} - V_{AC2}$
- Section IV and V have the same voltage difference of section I and II but opposite in direction, i.e., $-(V_{AC1} + V_{AC2})$
- Similarly for the section VI as $-(V_{AC1} - V_{AC2})$

The switching current and the conduction current comprise the inductor current of the DAB. Hence, the accurate estimation of the inductor current (i_L) is fundamental to correctly estimate the conduction and switching current of all the switches in the four PMs of the DAB.
Moreover, these two models are used to determine the flow through the inductor (i_L). Besides, there are two switching technique, known as soft switching (SS) and hard switching (HS), happened during the switching of the MOSFETs of the PMs. The estimated inductor current by the proposed models along with the switching technique has selectively been used for calculating switching and conduction loss of the DAB in four different categories stated below and detailed in the respective section [9]-[13].

- Switching and conduction loss for DAB-LL model and SS
- Switching and conduction loss for DAB-LL model and HS

- Switching and conduction loss for DAB-CL model and SS
- Switching and conduction loss for DAB-CL model and HS

3.3.1 DAB lossless (DAB-LL) model

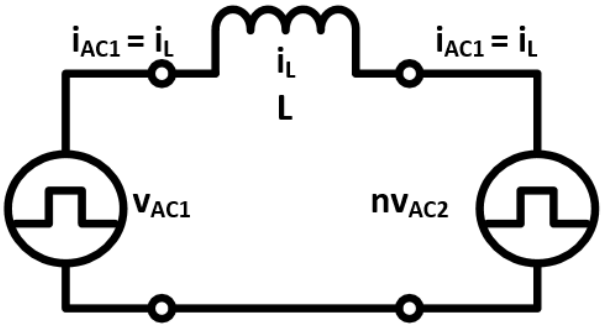


Figure 3.3: DAB lossless (DAB-LL) model

DAB-LL model is an ideal lossless model of the DAB. It ignores any resistive effect for deriving the inductor current. Hence, the resistance from the switches, inductor, transformer, any parasitic elements, and PBC boards have been neglected building the model. Because of this, there is only one inductor showing in the figure 3.3. The sources on both sides of the inductor are the voltage across the inductor from the two full-bridge networks of the DAB, the left side full-bridge voltage is VAC1, and the right side full-bridge voltage is nVCA2. The parameter, n is the transformer turn ratio which is equal one in this study.

3.3.2 DAB conduction loss (DAB-CL) model

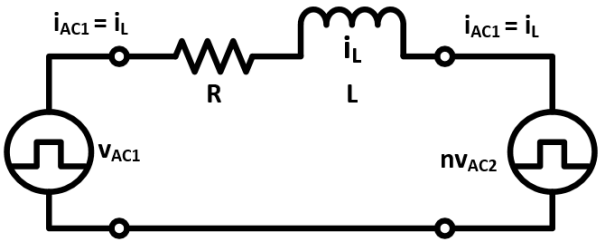


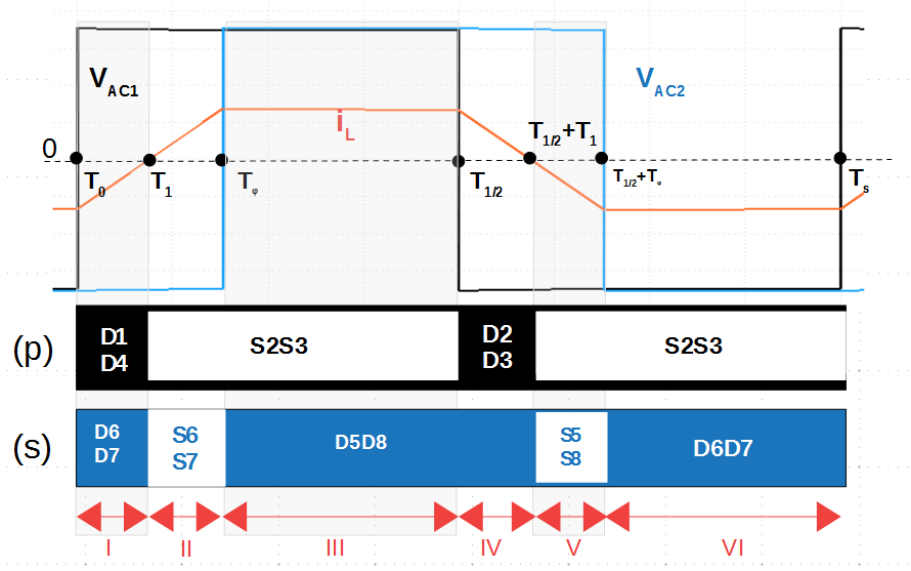
Figure 3.4: DAB conduction loss (DAB-CL) model

DAB-CL model includes the conduction loss of the DAB to derive the inductor current of the DAB. The on-state resistance of the upper and lower switches of the PM4 and PM5 connect in series with the inductor and the transformer when both switches are turned on. Similarly, the on-state resistance of upper and lower switches of the PM5 and PM4 connect in series with the inductor and the transformer when both switches are turned on. Therefore, there is a series connection among the two one-state resistances, leakage resistance of the inductor, and the total transformer resistance on the primary side. Equation 3.3 shows the total series resistance considered in the model of the DAB. This entire series resistance and the inductor along with the voltage sources generate the inductor current in the DAB-CL model.

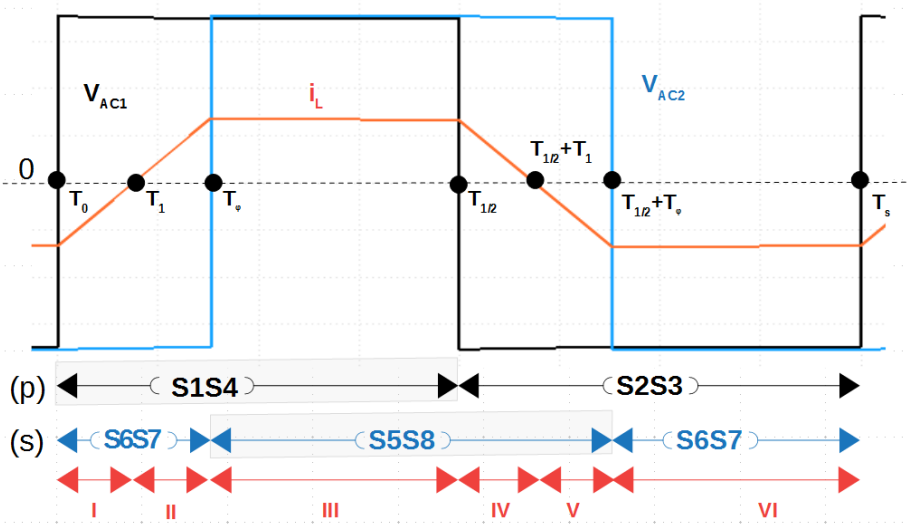
$$R = 2R_{ds,on} + R_L + R_{tr1} + n^2 R_{tr2} \tag{3.3}$$

3.3.3 Switching concept

There are two switching techniques possible for the switching of MOSFETs in the PMs presented in figure 3.5. These are soft switching (SS), and hard switching (HS).



(a) Soft switching during switch on and hard switching during switch off



(b) Hard switching during turn on and turn off as diode are ignored for finding maximum possible loss

Figure 3.5: Current and voltage waveform of DAB at steady state (p) conduction of primary side switches (s) conduction of secondary side switches

3.3.3.1 Soft Switching (SS)

Operating power electronic switches with zero voltage switching (ZVS) and/or zero current switching (ZCS) is known as the soft switching (SS). ZVS during turn-on is evident in the phase shift modulation incorporated in this system. In ZVS, Each

antiparallel diode conducts the inductor current before turning on each MOSFET switches. Figure 3.5a shows the SS operation for the investigated DAB converter. Whereas, the turn-off switching could not achieve the soft switching.

3.3.3.2 Hard Switching (HS)

The switching of power electronic switches neither at zero voltage nor zero current consider as hard switching (HS). In this study, HS refers to non zero voltage and or non zero currents during both turn-on and turn-off of the switches. Generally, in the phase shift modulation, HS does not happen during the turn-on of the switches. But for estimation of the losses for the thermal analysis in worst case scenario, HS during turn-on is also considered with HS turn-off. Figure 3.5b shows the HS of the DAB where the conduction through the diodes are ignored, and 180° conduction of switches are considered.

3.4 DAB-LL model-based calculation

The principle inductor current equation for DAB-LL model, described in section 3.3.1, is presented in equation 3.4. The switching currents, average current, and RMS current, required for semiconductor loss calculation referred to section 3.2, have been calculated using the equation 3.4 for evaluating losses in the categories 'DAB-LL and SS', and 'DAB-LL and HS' mentioned in article 3.3.

$$i_L(t) = \begin{cases} i_L(T_0) + \frac{V1+nV2}{L}\,(t - T_0)\,; & T_0 \le t \le T_\phi \\ i_L(T_\phi) + \frac{V1-nV2}{L}\,(t - T_\phi) & T_\phi \le t \le T_{\frac{1}{2}} \end{cases} \tag{3.4}$$

The switching currents are considered as the inductor current at the beginning of the switching time instant can be found according to equations 2.2 to 2.5. The average and RMS currents calculation use the piecewise linear integration method for the different time interval of the switching period. The average current calculation requires the integration of the inductor current whereas the RMS current calculation requires the square integration of the inductor current.

The integrations of the inductor current for different time interval, depicted in Figure 3.6, are derived and compiled in equations 3.5 to 3.7 and will be used to calculate the average current of that intervals.

$$\begin{aligned} I_{ZY} &= \int_{T_0}^{T_1} (a + b(t - T_0))dt \\ &= \int_{Z}^{Y} (a + b(t - Z))dt \\ &= \frac{1}{2}(Y - Z)(2a + b(Y + Z)) \end{aligned} \tag{3.5}$$

$$\begin{aligned} I_{YP} &= \int_{T_1}^{T_\phi} (a + b(t - T_1)dt \\ &= \int_{Y}^{P} (a + b(t - Y))dt \\ &= \frac{1}{2}(P - Y)(2a + b(P + Y)) \end{aligned} \tag{3.6}$$

$$\begin{aligned} I_{PT} &= \int_{T_\phi}^{\frac{T_s}{2}} (p + q(t - T_\phi))dt \\ &= \int_{P}^{\frac{T_s}{2}} (p + q(t - P))dt \\ &= \frac{1}{8}(2P - T_s)(-4p + 2qP - qT_s) \end{aligned} \tag{3.7}$$

where,

- $Z = T_0 = 0$, $Y = T_1$, $P = T_\phi$, and $T = \frac{T_s}{2}$
- $a = i_L(T_0)$, $b = \frac{V1+nV2}{L}$
- $p = i_L(T_\phi)$, $q = \frac{V1-nV2}{L}$

Similarly, **the square integrations of the inductor current** for different time interval, presented in Figure 3.6 are derived and compiled in equations 3.8 to 3.13 and will be used to calculate the RMS current of that intervals.

$$\begin{aligned} IR_{ZY} &= \int_{Z}^{Y} (a + b(t - Z))^2 dt \\ &= \frac{(a + b(Y - Z))^3 - (a)^3}{3b} \end{aligned} \tag{3.8}$$

$$\begin{aligned} IR_{YP} &= \int_{Y}^{P} (a + b(t - Y))^2 dt \\ &= \frac{(a + b(P - Y))^3 - (a)^3}{3b} \end{aligned} \tag{3.9}$$

$$\begin{aligned} IR_{PT} &= \int_{P}^{\frac{T_s}{2}} (p + q(t - P))^2 dt \\ &= \frac{(p + \frac{1}{2}q(T - 2P))^3 - p^3}{3q} \end{aligned} \tag{3.10}$$

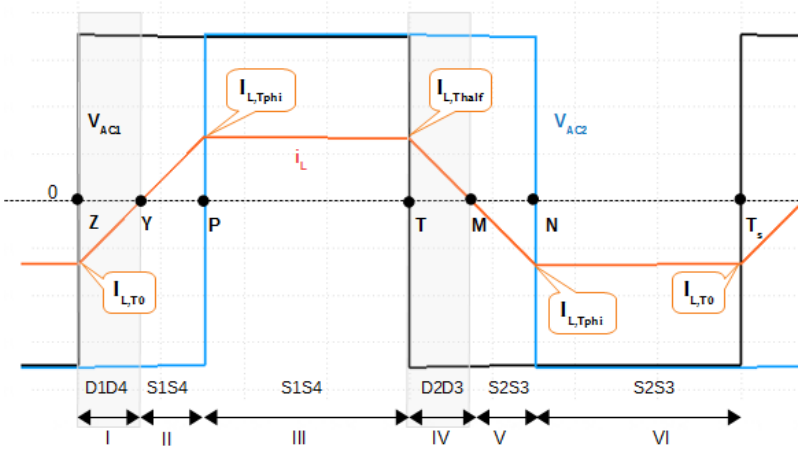
$$\begin{aligned} IR_{ZT} &= IR_{ZY} + IR_{YP} + IR_{PT} \\ &= \int_{Z}^{Y} (a + b(t - Z))^2 dt + \int_{Y}^{P} (a + b(t - Y))^2 dt + \int_{P}^{\frac{T_s}{2}} (p + q(t - P))^2 dt \\ &= \frac{(a + b(Y - Z))^3 - (a)^3}{3b} + \frac{(a + b(P - Y))^3 - (a)^3}{3b} + \frac{(p + \frac{1}{2}q(T - 2P))^3 - p^3}{3q} \\ &= \frac{(a + b(P - Z))^3 - a^3}{3b} + \frac{(p + \frac{1}{2}q(T - 2P))^3 - c^3}{3q} \end{aligned} \tag{3.11}$$

$$\begin{aligned} IR_{PT,q=0} &= \int_{P}^{\frac{T_s}{2}} (p)^2 dt \\ &= \frac{1}{2}p^2(T - 2P) \end{aligned} \tag{3.12}$$

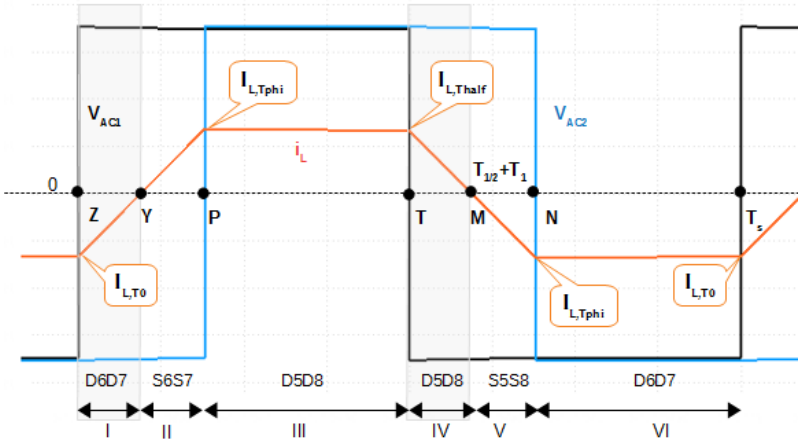
$$
\begin{aligned}
IR_{ZT,q=0} &= IR_{ZY} + IR_{YP} + IR_{PT,q=0} \\
&= \int_{Z}^{Y} (a + b(t - Z))^2 dt + \int_{Y}^{P} (a + b(t - Y))^2 dt + \int_{P}^{\frac{T_s}{2}} (p)^2 dt \\
&= \frac{(a + b(Y - Z))^3 - (a)^3}{3b} + \frac{(a + b(P - Y))^3 - (a)^3}{3b} + \frac{1}{2} p^2 (T - 2P) \\
&= \frac{(a + b(P - Z))^3 - a^3}{3b} + \frac{1}{2} p^2 (T - 2P)
\end{aligned}
\tag{3.13}
$$

When q = 0, the equations 3.12 and 3.13 will be used instead of equations 3.10 and 3.11 for calculating square integration of current of respective time intervals. Finally, the equation 3.5 to equation 3.13 are used to evaluate the average and RMS currents that are used to calculate the important losses across the semiconductor switches for the different time intervals.

3.4.1 Current for 'DAB-LL model and SS'



(a) Primary side conduction of switches for SS



(b) Secondary side conduction of switches for SS

Figure 3.6: Conduction of switches during SS

Figure 3.6 shows the conduction of MOSFETs and antiparallel DIODEs of the primary side PMs such as in PM4 and PM5 as well as of the secondary side PMs such as in PM5 and PM6 for the DAB-LL model. Figure 3.6 also presents that each antiparallel DIODE conducts before the turn-on of its pair MOSFET; hence the ZVS is achieved during turn-on. The duration of the conduction of the MOSFETs is higher than the length of the conduction time of the DIODEs in primary side whereas it is opposite in the secondary side of the DAB. Moreover, because of the half-wave symmetry of the inductor current, the interval ZY, YP, PT, and ZT are complementary identical to the interval TM, MN, NT_s, and TT_s. Finally, the essential switching currents at different time points are shown in the figure as $I_{L,T0}$, $I_{L,Tphi}$, and $I_{L,Thalf}$. Where, $I_{L,T0}$ is the current at time zero, $I_{L,Tphi}$ is the current at the time equal to the phase shift, and $I_{L,Thalf}$ is the current at the time corresponding to the half of the switching period T_s. Nevertheless, $I_{L,Tphi}$, and $I_{L,T0}$ are equal in magnitude, because of the unity transformer turn ratio, but opposite in direction with the current at the time point N and Ts.

3.4.1.1 Switching current

The switching currents for 'DAB-LL model and SS' is shown in figure 3.6 are derived and compiled in equations 3.14 to 3.17. The turn-on switching loss of all MOSFETs both in the primary side as well as in the secondary side of the DAB is zero because of the SS of the phase shift modulation. The only switching loss happens in all of the switches is the turn-off loss during SS. In the primary side, the current $I_{L,T0}$ is used to calculate the turn-off switching loss of the MOSFET switches S2S3 whereas $I_{L,Thalf}$ is used for S1S4. Similarly, on the secondary side, the current $I_{L,Tphi}$ is used to calculate the turn-off switching loss of the MOSFET switches S6S7 and S5S8.

$$I_{L,T0} = \frac{\pi\left(nV2 - V1\right) - 2\phi nV2}{4\pi f_s L} \tag{3.14}$$

$$I_{L,Tphi} = I_{L,T0} + \frac{V1 + nV2}{L} T_\phi \tag{3.15}$$

$$I_{L,Thalf} = I_{L,Tphi} + \frac{V1 - nV2}{L}\left(T_{\frac{1}{2}} - T_\phi\right) \tag{3.16}$$

3.4.1.2 Average and RMS current

It is explicit from the Figure 3.6 that the average and RMS current are equal for all diode at the primary side of the DAB as well as all switches at the secondary side as long as the transformation ration is one. Similarly, the same amount of RMS and average current flow through the all switches at the primary side of the DAB and the diodes of the secondary side of the DAB as long as the turn ratio is unity. The required average and RMS current are evaluated using the equations 3.17, 3.19, 3.18, and 3.20.

$$\begin{aligned} I_{sp,avg,D} &= \frac{1}{T_s} \times (-I_{ZY}) \\ &= n \times I_{ss,avg,S} \end{aligned} \tag{3.17}$$

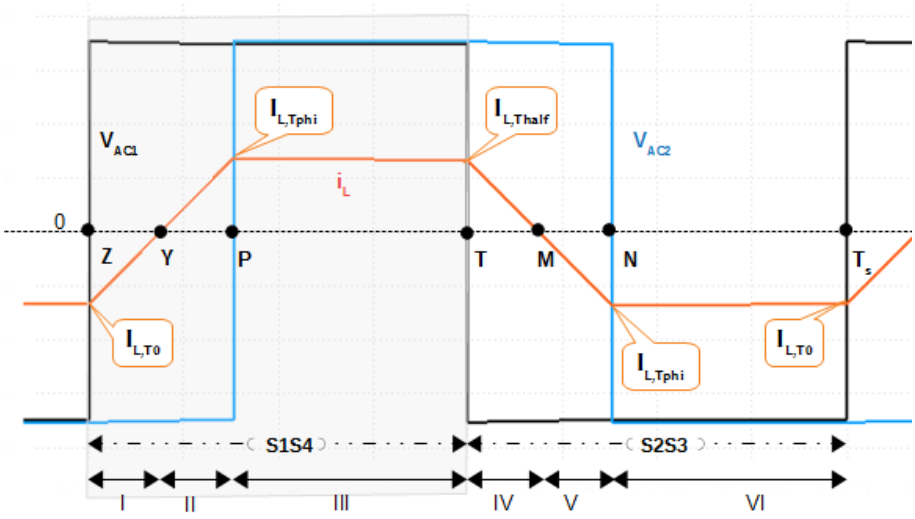
$$\begin{aligned} I_{sp,rms,D} &= \sqrt{\frac{1}{T_s} \times (IR_{ZY})} \\ &= n \times I_{ss,rms,S} \end{aligned} \tag{3.18}$$

$$\begin{aligned} I_{sp,avg,S} &= \frac{1}{T_s} \times (I_{YP} + I_{PT}) \\ &= n \times I_{ss,avg,D} \end{aligned} \tag{3.19}$$

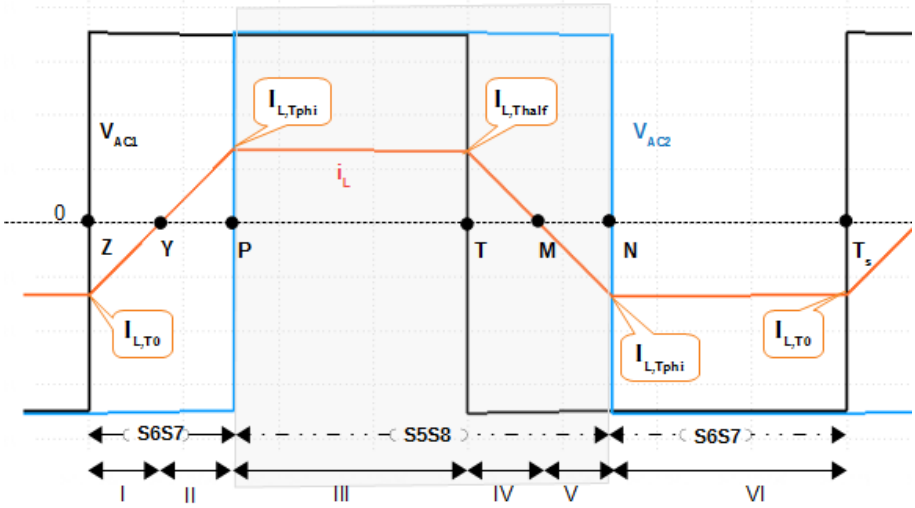
$$\begin{aligned} I_{sp,rms,S} &= \begin{cases} \sqrt{\frac{1}{T_s} \times (IR_{YP} + IR_{PT})}; & ifq \neq 0 \\ \sqrt{\frac{1}{T_s} \times (IR_{YP} + IR_{PT,q=0})}; & ifq = 0 \end{cases} \\ &= n \times I_{ss,rms,D} \end{aligned} \tag{3.20}$$

3.4.2 Current for 'DAB-LL model and HS'

The ZVS happens during turn-on of the switches in the SS technique is ignored in the 'DAB-LL and HS' case. Because of this, there is no conduction of DIODEs at all in the HS consideration. Each MOSFET of all PMs conducts for half switching cycle both in primary side as well as on the secondary side depicted in figure 3.7.



(a) Primary side conduction of switches for HS



(b) Secondary side conduction of switches for HS

Figure 3.7: Conduction of switches during HS

3.4.2.1 Switching current

The switching currents during turn-on and turn-off required for calculating switching losses are shown in figure 3.7.
In the primary side of the DAB, the switching current, $I_{L,T0}$ is used for evaluating the turn-on loss of the switches $S1S4$ and the turn-off loss of the switches $S2S3$. And the switching current, $I_{L,Thalf}$ is used for estimating turn-off loss of the switches $S1S4$ and the turn-on loss of the switches S2S3.
On the secondary side, the switching current, $I_{L,Tphi}$ is used for calculating turn-on and turn-off loss of the switches $S5$ to $S8$. The equations of all switching current are same as the switching currents equation described in equations 3.14 to 3.17.

3.4.2.2 Average and RMS current

According to the Figure 3.7 MOSFET switches S1 and S4 conduct from Z or T_0 to T or $T_{\frac{1}{2}}$ and S2 and S3 conduct from T or $T_{\frac{1}{2}}$ to T_s. The duration of conduction is equal, and all four switches carry the same average and RMS current throughout their conduction at the primary side of the DAB. On the secondary side of the DAB, all four switches S5, S6, S7 and S8 conduct for the equal amount of time and carry the equal amount of average and RMS current throughout their conduction time. S5 and S8 conduct from P or T_ϕ to N or $T_{\frac{1}{2}+T_\phi}$. The current during this interval is same as the current of the interval Z or T_0 to T of $T_{\frac{1}{2}}$. Hence the average and the RMS current that is needed and calculated in equation 3.21 and 3.22. In the equation $I_{hp,avg}$ and $I_{hp,rms}$ are the average current and RMS current following through each of the switches in the primary side of the DAB. Similarly $I_{hs,avg}$ and $I_{hs,rms}$ are the average and RMS current following through each of the switches at the secondary side of the DAB. In this case, MOSFET body DIODEs never conduct as because of synchronous rectification and negligibly small dead time described in [13].
Finally, equation 2 shows the total RMS current of the inductor for the case $q = 0$ and $q \neq 0$ described in section 3.4.

$$I_{hp,avg} = \frac{1}{T_s} \times (I_{ZY} + I_{YP} + I_{PT}) = I_{hs,avg} \tag{3.21}$$

$$I_{hp,rms} = \frac{I_{L,rms}}{\sqrt{2}} = I_{hs,rms} \tag{3.22}$$

$$I_{L,rms} = \begin{cases} \sqrt{\frac{2}{T_s} \times (IR_{ZY} + IR_{YP} + IR_{PT})}; & ifq \neq 0 \\ \sqrt{\frac{2}{T_s} \times (IR_{ZY} + IR_{YP} + IR_{PT,q=0})}; & ifq = 0 \end{cases} \tag{3.23}$$

3.5 DAB-CL model-based calculation

The conduction loss based DAB model includes all of the conduction loss in the model such as the on state resistance of the switch, resistance of the core of the inductor and the transformer. The resistances are lumped together and connected in series with the bridge inductor. Hence the full bridges on both side of the transformer remain ideal for the DAB-CL model. Based on the DAB-CL model in Figure 3.4, the current, voltage, power, and the power loss have been evaluated according to the equation stated in [13] and described in equations 3.24 to 3.26.

$$i_L(t) = \begin{cases} e^{\frac{-t}{\tau}} i_L(T_0) + \frac{V1+nV2}{R}(1 - e^{\frac{-t}{\tau}}); & T_0 < t < T_\phi \\ e^{-\frac{t-T_\phi}{\tau}} i_L(T_\phi) + \frac{V1-nV2}{R}(1 - e^{-\frac{t-T_\phi}{\tau}}); & T_\phi < t < T_{\frac{1}{2}} \end{cases} \tag{3.24}$$

$$Pin = \frac{2V1}{T_s} \int_0^{\frac{T_s}{2}} i_L(t)dt \tag{3.25}$$

$$Pout = \frac{2V2}{T_s} \int_{\frac{T_s}{2}}^{T_s} i_L(t)dt \tag{3.26}$$

The integrations of the inductor current of DAB-CL model for different time intervals are derived and compiled in the equations 3.27 to 3.31. These equations will be used to calculate the average current of the inductor for the required time interval for loss calculation.

$$I_{cZY} = b(Y - Z) + \tau(a - b)(1 - e^{\frac{-(Y-Z)}{\tau}}) \tag{3.27}$$

$$I_{cYP} = b(P - Y) + \tau(0 - b)(1 - e^{\frac{-(P-Y)}{\tau}}) \tag{3.28}$$

$$I_{cPT} = b(T - P) + \tau(p - q)(1 - e^{\frac{-(T-P)}{\tau}}) \tag{3.29}$$

$$I_{cZP} = b(P - Z) + \tau(a - b)(1 - e^{\frac{-(P-Z)}{\tau}}) \tag{3.30}$$

$$I_{cZT} = I_{ZP} + I_{PT} \tag{3.31}$$

$$T_{I_L=0} = -\tau \ln \frac{-\frac{V1+nV2}{R}}{I_{L,T0} - \frac{V1+nV2}{R}} \tag{3.32}$$

$$\begin{aligned} a &= I_{L,T0} \\ b &= \frac{(V1 + nV2)}{R} \\ p &= I_{L,Tphi} \\ q &= \frac{(V1 - nV2)}{R} \\ Z &= T_0 \\ Y &= T_{I_L=0} \\ P &= T_\phi \\ T &= T_{\frac{1}{2}} \end{aligned} \tag{3.33}$$

The square integrations of the inductor current of DAB-CL model for different time intervals are derived and compiled in the equations 3.34 to 3.37. These equations will be used to calculate the RMS current of the inductor for the required time interval for loss calculation.

$$IR_{cZY} = \tau(\frac{a^2}{2} + ab + (\frac{Y - Z}{\tau} - \frac{3}{2})b^2 - 2b(a - b)e^{(-\frac{Y-Z}{\tau})} - \frac{1}{2}(a - b)^2 e^{(\frac{-2(Y-Z)}{\tau})}) \tag{3.34}$$

$$IR_{cYP} = \tau(\frac{0^2}{2} + 0 \times b + (\frac{P - Y}{\tau} - \frac{3}{2})b^2 - 2b(0 - b)e^{(-\frac{P-Y}{\tau})} - \frac{1}{2}(0 - b)^2 e^{(\frac{-2(P-Y)}{\tau})}) \tag{3.35}$$

$$IR_{cPT} = \tau(\frac{p^2}{2} + pq + (\frac{T - P}{\tau} - \frac{3}{2})q^2 - 2q(p - q)e^{(-\frac{T-P}{\tau})} - \frac{1}{2}(p - q)^2 e^{(\frac{-2(T-P)}{\tau})}) \tag{3.36}$$

$$IR_{cZP} = \tau(\frac{a^2}{2} + ab + (\frac{P - Z}{\tau} - \frac{3}{2})b^2 - 2b(a - b)e^{(-\frac{P-Z}{\tau})} - \frac{1}{2}(a - b)^2 e^{(\frac{-2(P-Z)}{\tau})}) \tag{3.37}$$

3.5.1 Current for 'DAB-CL model and SS

The inductor current for 'DAB-CL model and SS' is similar in pattern and operation as the inductor current for 'DAB-LL model and SS' except the value of the inductor current. Hence, the switches in the primary side and the secondary side will be conducted at the same time interval as before. The value of the switching current, average current, and RMS current are calculated for 'DAB-CL model and SS' and mentioned in the upcoming sections.

3.5.1.1 Switching current

The switching currents required for switching losses calculation for 'DAB-CL model and SS' are derived using equation 3.24 along with equation 3.38 and 3.39 and presented in equation 3.40 to 3.42.

$$I_{L,T_{phi},a=0} = b(1 - exp(\frac{-T1}{\tau})) \tag{3.38}$$

$$I_{L,T_{half},a=0} = exp(\frac{-T2}{\tau})I_{L,T_{phi},a=0} + q(1 - exp(\frac{-T2}{\tau})) \tag{3.39}$$

$$I_{L,T0} = \frac{-I_{L,T_{phi},a=0}}{1 + exp(\frac{-T1}{\tau})exp(\frac{-T2}{\tau})} \tag{3.40}$$

$$I_{L,T_{phi}} = exp(\frac{-T_{\Phi}}{\tau})I_{L,T0} + b(1 - exp(\frac{-T_{\phi}}{\tau})) \tag{3.41}$$

$$I_{L,T_{half}} = exp(\frac{-T_{\frac{1}{2}} - T_{\phi}}{\tau})I_{L,T_{phi}} + q(1 - exp(\frac{-T_{\frac{1}{2}} - T_{\phi}}{\tau})) \tag{3.42}$$

3.5.1.2 Average and RMS current

The average and RMS current for the MOSFETs and the DIODEs on the primary side as well as on the secondary side of the 'DAB-CL model and SS' are derived and shown in equations 3.43 to 3.50.

$$I_{csp,avg,D} = \frac{1}{T_s} \times (-I_{cZY}) \tag{3.43}$$

$$I_{csp,avg,S} = \frac{1}{T_s} \times (I_{cYP} + I_{cPT}) \tag{3.44}$$

$$I_{css,avg,D} = n\frac{1}{T_s} \times (I_{cZY} + I_{cPT}) \tag{3.45}$$

$$I_{css,avg,S} = n\frac{1}{T_s} \times (I_{cYP}) \tag{3.46}$$

$$I_{csp,rms,D} = \sqrt{\frac{1}{T_s} \times (IR_{cZY})} \tag{3.47}$$

$$I_{csp,rms,S} = \sqrt{\frac{1}{T_s} \times (IR_{cYP} + IR_{cPT})} \tag{3.48}$$

$$I_{css,rms,D} = n\sqrt{\frac{1}{T_s} \times (IR_{cZY} + IR_{cPT})} \tag{3.49}$$

$$I_{css,rms,S} = n\sqrt{\frac{1}{T_s} \times (IR_{cYP})} \tag{3.50}$$

3.5.2 Current for 'DAB-CL model and HS

The inductor current's pattern of 'DAB-CL model and HS' is also similar to the current pattern of 'DAB-LL model and HS' shown in Figure 3.7. The switching instant, conduction time, conduction of the switches are also same as before. The only difference considered here is the calculation of the current value which is done using the equation 3.24 along with the equations 3.27 to 3.50.

3.5.2.1 Switching current

The switching current required for the switching loss calculation has been calculated using the equations 3.40 to 3.42 and the switching instant considered according to the description mentioned in section 3.4.2.1.

3.5.2.2 Average and RMS current

Equation 3.51 calculates the RMS current through the inductor and average current is ignored because of the zero forward voltage drop of MOSFETs to estimate the conduction loss in the system of 'DAB-CL model and HS' following the description made in section 3.4.2.2.

$$I_{L,rms} = \sqrt{\frac{2}{T_s}(IR_{cZP} + IR_{cPT})} \tag{3.51}$$

3.6 Loss in ACDC rectifier

A three-phase PWM rectifier is utilized to converter the grid ac voltage to a dc voltage around 700 V. And the ac line to line voltage is about 400 V. Besides these, An LCL filter is constructed to meet the harmonic requirements from the utility grid perspective. The grid RMS current (inductor phase current) in nominal condition can be calculated as: $I_{rms} = 152\ A$ and $I_p = \sqrt{2}I_{rms}$ and the switching frequency is $fs = 25\ kHz$.
The switching loss in the MOSFET and the diode are calculated according to the data sheet parameters based on the equations 3.52 and 3.53 respectively. But there is no reverse recovery current from the diode of the product CAS300M17BM2. Hence no switching loss is for the diode. The energy of switching on and switching off of the MOSFET has to be adjusted with the data sheet value for the switching voltage and current that are $V_s = 700\ V$ and $I_s = \frac{1}{\pi}\sqrt{2}I_{orms} = 68.50\ A$ for all of the switches in the rectifier.
The data sheet value of energy of switching on and switching off are $E'_{on} = 13\ mJ$ and $E'_{off} = 10\ mJ$ at $V'_s = 900\ V$ and $I'_s = 300\ A$ respectively. Based on the data sheet value and two others voltage and current values taken from the energy plots of the datasheet, equations 3.53a and 3.53b are solved, and the following coefficients have been found.

- $K_{I,on} = 0.647$
- $K_{V,on} = 1.83$
- $K_{I,off} = 1.26$
- $K_{V,off} = 1.17$

These coefficient along with data sheet value of energy could be used in the equations 3.53a and 3.53b to evaluate the switching on and switching off energy of the MOSFETs at any specific voltage (V_s) and current (I_s) [4]-[6].

$$P_sM = f_s\left(E_{on} + E_{off}\right) \tag{3.52}$$

$$P_sD = f_s\left(E_{on} + E_{off}\right) \tag{3.53}$$

$$E_{on} = E'_{on}\left(\frac{I_s}{I'_s}\right)^{K_{I,on}}\left(\frac{V_s}{V'_s}\right)^{K_{V,on}} \tag{3.53a}$$

$$E_{off} = E'_{off}\left(\frac{I_s}{I'_s}\right)^{K_{I,off}}\left(\frac{V_s}{V'_s}\right)^{K_{V,off}} \tag{3.53b}$$

The conduction loss of MOSFET and diode are estimated according to the formula given in [24] and presented in equation 3.54.

$$P_cM = R_{DSon}I_p^2\left(\frac{1}{8} + \frac{m_a cos\phi}{3\pi}\right) \tag{3.54}$$

$$P_cD = V_{SD}I_p\left(\frac{1}{2\pi} - \frac{m_a cos\phi}{8}\right) + R_{diode}I_p^2\left(\frac{1}{8} - \frac{m_a cos\phi}{3\pi}\right)$$

The parameters estimated to calculated the conduction are as below. And the

average value of the current calculated before is used to evaluate the conduction loss in MOSFET and in diode as suggested by [24].

- Modulation index, $m_a = 1$
- Displacement power factor, $cos\phi 1 = 1$
- $R_{DSon} = 12\ m\Omega$ and $R_{diode} = 5\ m\Omega$
- Diode forward voltage drop, $V_{SD} = 2.5\ V$

The Table 3.2 shows the calculated loss in ACDC rectifier. Here PcM, PcD, and Ps stand for the conduction loss in a MOSFET, conduction loss in a diode and switching loss in a MOSFET. Besides these, Module 1, Module 2 and Module 3 represent the total loss in a half bridge lag of ACDC rectifier consequently. Finally, the total loss in the ACDC rectifier is tabulated under P_{ACDC} which is calculated as 1.55 kW.

Table 3.2: Conduction and switching loss of ACDC rectifier

PcM	PcD	Ps	Module 1	Module 2	Module 3	P_{ACDC}
122.54	13.86	107.89	488.59	488.59	488.59	1.4685e+03

3.7 Conclusion

All of the necessary quantities such as the parameters of the selected switches, switching currents, conduction currents, and the required models of the system have been explicitly stated in this chapter to estimate the semiconductor losses of the system.

4

Results

4.1 Losses in the system

The losses in the system are separated as the loss in each module of the DAB, in the ACDC rectifier, across the inductor, and across the transformer. The fixed parameters are switching frequency, turn ratio of the transformer, the resistance of the inductor and the transformer, dc link voltage, and the phase shift angle. Two on-state resistance of the MOSFET such as 8 and 12 $m\Omega$, and three output voltage such as 560, 700, 840 V are considered for the loss calculation. Other losses are ignored during the calculation of the current values. The results of the system are presented in the following sections.

4.1.1 Total module loss for 'DAB-LL and HS'

The total losses per module in the DAB converter during 'DAB-LL and HS' model are presented in Table 4.1 and Table 4.2. Table 4.1 shows the result for the on-state resistance of 8 $m\Omega$ whereas Table 4.2 shows the result for the on-state resistance of the 12 $m\Omega$. The losses in the primary and the secondary side modules are same at the nominal output voltage of 700 V as long as hard switching considered. On the other hand that's are not the same for other voltages as they are different from dc link voltage.

Table 4.1: Loss per module for hard switching of DAB loss less model when $R_{dson} = 8\ m\Omega$ and $PS = 49.75\ ^oC$

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	767.7259	767.7259	767.7259	767.7259
840	753.5623	753.5623	1.2246e+03	1.2246e+03
560	808.0065	808.0065	455.9117	455.9117

Table 4.2: Hard switching $R = 12\ m\Omega$, $PS = 49.75\ ^oC$

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	889	889	889	889
840	906	906	1.3778e+3	1.3778e+3
560	912	912	560	560

Table 4.3: Hard switching for $R = 12\ m\Omega$, and $PS = 90\ ^oC$

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	1.8859e+3	1.8859e+3	1.8859e+3	1.8859e+3
840	2.1015e+3	2.1015e+3	2.6126e+3	2.6126e+3
560	1.6875e+3	1.6875e+3	1.2609e+3	1.2609e+3

4.1.2 Total Module loss for 'DAB-LL and SS'

Similarly, the total losses per module in the DAB converter during 'DAB-LL and SS' model are presented in Table 4.4 and Table 4.5. Table 4.1 shows the result for the on-state resistance of 8 $m\Omega$ whereas Table 4.2 shows the result for the on-state resistance of the 12 $m\Omega$. The losses in the primary side modules are higher than the secondary side modules at the output voltage equal or less than the dc link voltage as soft switching considered. On the other hand that's are opposite for voltages higher than the dc link voltage.

Table 4.4: Total loss at each module for soft switching of DAB loss less model for $R = 8\ m\Omega$

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	463.4380	463.4380	390.2972	390.2972
840	458.9093	458.9093	598.5113	598.5113
560	491.3120	491.3120	255.3650	255.3650

Table 4.5: Soft switching $R = 12\ m\Omega$, $PS = 49.75\ ^oC$

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	578	578	397	397
840	597	597	603	603
560	592	592	266	266

Table 4.6: Soft switching $R = 12\ m\Omega$, $PS = 90\ ^oC$

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	1.3947e+3	1.3947e+3	984	984
840	1.5336e+3	1.5336e+3	1.3002e+3	1.3002e+3
560	1.2646e+3	1.2646e+3	715	715

4.1.3 Total module loss for 'DAB-CL and HS'

Now the total losses per module in the DAB converter during 'DAB-CL and HS' model is shown in Table 4.7 which is for the on-state resistance of 8 $m\Omega$. Secondary side switches are stressed more if the output voltage is not the same as the dc link voltage.

Table 4.7: Total module loss for hard switching of DAB Conduction loss model

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	887.89	887.89	897.59	897.59
840	986.00	986.00	1.531e+03	1.531e+03
560	863.66	863.66	484.21	484.21

4.1.4 Total module loss for 'DAB-CL and SS'

Finally, the total losses per module in the DAB converter during 'DAB-CL and SS' model is shown in Table 4.8 which is for the on-state resistance of 8 $m\Omega$. Secondary side switches are stressed more if the output voltage is more than the dc link voltage.

Table 4.8: Total module loss for soft switching of DAB Conduction loss model

Output voltage (V)	Module 4 (Watts)	Module 5 (Watts)	Module 6 (Watts)	Module 7 (Watts)
700	602.09	602.09	426.74	426.74
840	725.24	725.24	772.89	772.89
560	557.50	557.50	209.06	209.06

4.1.5 Total Module loss of ACDC rectifier

In the ACDC rectifier, Table 4.9 shows the conduction losses, switching losses, and the per module losses. These losses are estimated as per the conditions mention in the previous chapter.

Table 4.9: Conduction and switching loss of ACDC rectifier

PcM	PcD	Ps	Module 1	Module 2	Module 3	P_{ACDC}
122.54	13.86	107.89	488.59	488.59	488.59	1.4685e+03

4.2 Efficiency of the system

The calculation of the efficiency of the system includes the losses in each component of the system. The losses across the inductor and the transformer are calculated based on the conduction current in considered models of the DAB. They are mentioned as P_{RL} and P_T respectively. There are 20 W of loss considered as auxiliary power loss of the system during the efficiency calculation of the system.

The efficiency of the ACDC part is calculated considering the power factor equal to $1, 0.95$, and 0.90. The procedure is mentioned below. The apparent power is given by $S = 3VrmsIrms$. And Considering $S = 105\ kVA$, Irms is calculated. The peak value of current is $\sqrt{2}Irms$. Based on this peak value, switching loss is estimated. The result of the ACDC rectifier is tabulated in table 4.10.

Table 4.10: Efficiency of ACDC rectifier considering different system power factor

PF ($cos\phi$)	Pin (kW)	Ploss (kW)	Efficiency (%)
1	105	1.47	98.60
0.95	99.75	1.46	98.53
0.90	94.5	1.47	98.44

The efficiencies of the DAB converter are shown in Table 4.11 and Table 4.12 whereas Table 4.11 shows the result for the on-state resistance of 8 $m\Omega$ and Table 4.12 shows the result for the on-state resistance of 12 $m\Omega$. The best case efficiency occurs during the SS techniques for both CL and LL models.

Table 4.11: DAB efficiency for $R_{ds,on} = 8\ m\Omega$

Rds, on $= 8\ m\Omega$		$P_{sc,DAB}$ (kW)	P_{RL} (kW)	P_T (kW)	P_{aux} (kW)	Pin (kW)	Efficiency (%)
Lossless Model	HS	3.070	0.083	0.158	0.020	98	96.60
	SS	1.707	0.083	0.158	0.020	98	97.99
Conduction loss Model	HS	3.0795	0.083	0.159	0.020	98.807	96.62
	SS	1.7146	0.083	0.159	0.020	98.807	98.00

Table 4.12: DAB efficiency for $R_{ds,on} = 12\ m\Omega$

Rds, on $= 12\ m\Omega$		$P_{sc,DAB}$ (kW)	P_{RL} (kW)	P_T (kW)	P_{aux} (kW)	Pin (kW)	Efficiency (%)
Lossless Model	HS	3.5595	0.083	0.158	0.020	98	96.10
	SS	1.9518	0.083	0.158	0.020	98	97.74
Conduction loss Model	HS	3.5744	0.083	0.159	0.020	99.068	96.13
	SS	1.9644	0.083	0.159	0.020	99.068	97.75

The system efficiency is estimated and presented in Table 4.13 and Table 4.14. Here, HS is for hard switching and SS is for soft switching. The efficiency is calculated

based on the nominal operating point meaning DC link voltage is considered 700 V, and the output voltage is considered 700 V as well.
The best efficiency should be around 96% at the nominal operating point. It will decrease if the power factor decrease and increase if the DAB output voltage decrease.

Table 4.13: System efficiency considering $R_{ds,on} = 8\ m\Omega$

Rds, on $= 8\ m\Omega$		P_{DAB} (kW)	P_{aux} (kW)	P_{ACDC} (kW)	Pin (kW)	Efficiency (%)
DAB-LL	HS	3.3128	0.020	1.55	105	95.43
	SS	1.9493	0.020	1.55	105	96.73
DAB-CL	HS	3.3228	0.020	1.55	105	95.42
	SS	1.9579	0.020	1.55	105	96.72

Table 4.14: System efficiency considering $R_{ds,on} = 12\ m\Omega$

Rds, on $= 12\ m\Omega$		P_{DAB} (kW)	P_{aux} (kW)	P_{ACDC} (kW)	Pin (kW)	Efficiency (%)
DAB-LL	HS	3.8014	0.020	1.55	105	94.96
	SS	2.1936	0.020	1.55	105	96.50
DAB-CL	HS	3.8181	0.020	1.55	105	94.95
	SS	2.2081	0.020	1.55	105	96.48

Table 4.15: Effieciency of DAB and the efficiency of the system based on unity power factor

		Ploss (DAB)	Pin (DAB)	Efficiency (DAB)	Ploss (ACDC)	Pin (ACDC)	Efficiency (System)
Lossless Model	HS	3.070	98	96.87	1.55	105	95.6
	SS	1.707	98	98.26	1.55	105	96.89
Conduction loss Model	HS	3.551	98.807	96.41	1.55	105	95.14
	SS	2.057	98.807	97.92	1.55	105	96.56

4.3 Conclusion

Based on the models in Chapter 3, losses are calculated and presented in this Chapter 4. The efficiency of the ACDC converter is more than 98%, and it is between 96% to 98% for DAB converter. However, the best case system efficiency is about 96%. Based on the loss calculated in this Chapter, the thermal analysis of the system will be done in the next chapter.

5

Thermal design of fast charging station

5.1 Introduction

This chapter represents the design of the cooling system for the investigated fast charging station (FCS) based on the losses calculated in the previous section. It has designed a power module (PM) and a cold plate in finite element method (FEM)'s simulator using the available datasheets parameters. It also verified the PM by comparing thermal resistance with a 14 stages RC thermal model obtained from the manufacturer. Finally, the thermal performance curve is found out for the system. The recommended fluid flow can be in between 6 to 8 liter per minutes (LPM) with a pressure drop of 187 to 314 *mbar* to control the maximum junction temperature below 129 ^oC for 6 LPM, 124 ^oC for 7 LPM and 110 ^oC for 8 LPM throughout the operating region.

5.2 Description of the thermal system

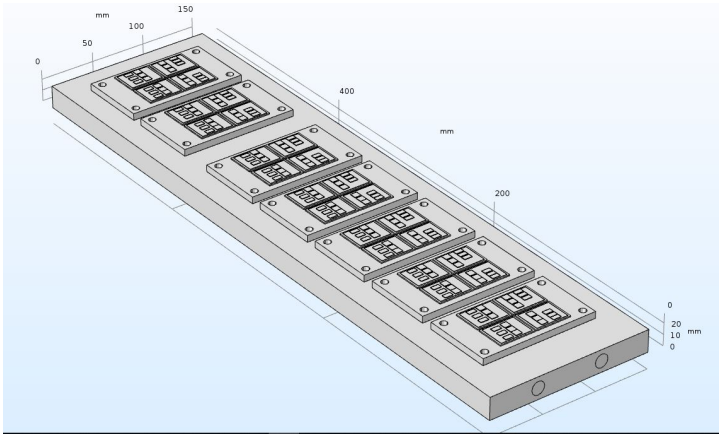


Figure 5.1: 3D view of the thermal system of FCS

The thermal system under study has three main parts that are clod plate (CP), liquid pipe (LP) and the single power module (PM). The LP is pass through the CP and carry the coolant with specific inlet temperature and velocity. Besides, there are seven identical PMs sit on the CP, and the base/-case of each PMs attached to CP through thermal interface material (TIM). Figure 5.1 shows the whole thermal system of the FCS representing CP with LP and seven PMs on it. The TIM layer is in between CP, and PMs.
Moreover, each PM consists of two semiconductor switches named as an upper

switch and a lower switch. Each switch includes one MOSFET and one DIODE. Six identical MOSFET chips manufacture each MOSFET, and similarly, six similar DIODE chips construct each DIODE. Figure 5.2 shows the top view of a single PM shows the die or chip location that has been provided by the manufacturer. It also shows the dimension of the PM. Each PM holds 106.4 mm width, 61.4 mm depth, and 6 mm height. Furthermore, it has multiples layer inside of it.

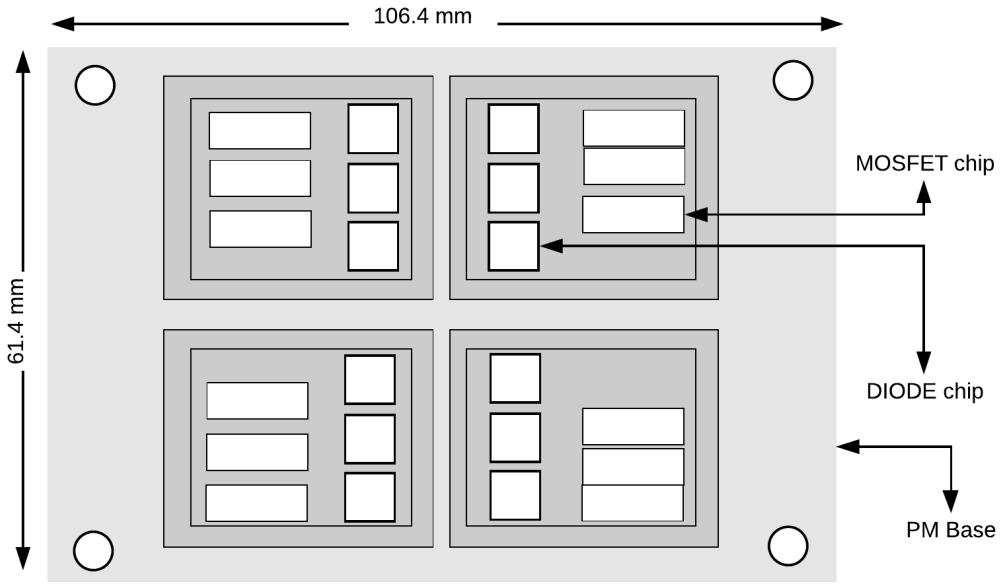


Figure 5.2: Die/chip location of a single PM

Finally, Figure 5.3 shows the dimensions of CP and position and radius of LP inside the CP. The CP is 570 mm long, 150 mm wide, and 20 mm in height. On the other hand, the LP has an inlet pipe and an outlet pipe connected to each other at the end of the cold plate. Inlet pipe passes through the CP and below the upper switches of each PMs. Similarly, outlet pipe passes through the CP and below the lower switches of each PMs.

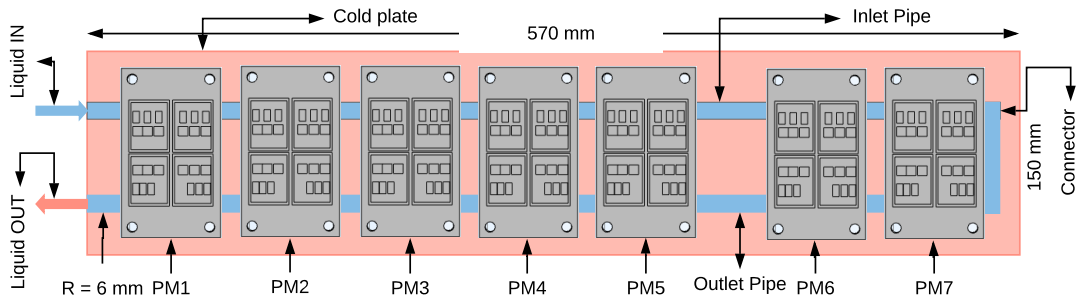


Figure 5.3: Dimension of cold plate and position of liquid pipe and PMs

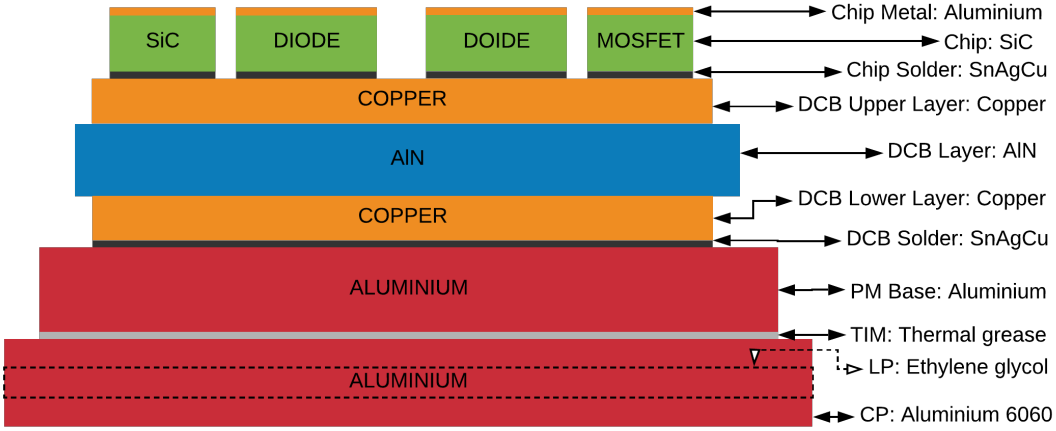


Figure 5.4: Layers information of the system

The dimension of layers of the thermal system is the essential parameters for the study of thermal performance. The thickness of the layers influences the thermal performance of the system. So, proper choice of thickness is necessary for having the excellent performance of the system. Figure 5.4 shows the vertical cross-section of the system and depicts the layers of the system. There are 11 layers of the system. CP and LP inside of it consist of two layers. The third layer is the TIM layer which is in between CP and each PMs. Besides these, eight layers form a single PM. Generally, an only PM like CAS300M17BM2 in this context has three crucial layers. These are a base layer, a DCB or DBC layer (double copper bounded-DCB or DBC), and a chip layer. A ceramic substrate which is bounded by lower and upper copper layers form the DCB layer. And the DCB layer is connected to the base through DCB solder layer. Each MOSFET or DIODE chip has one layer of semiconductor material. Plus there is a chip solder layer below the chip layer and a chip metal layer above the chip layer [16].

Table 5.1: The thickness of the layers of the system

Layer	Thickness (mm)	Comments
Cold plate (CP)	20	
Liquid pipe (LP)	12	Diameter
TIM	0.05	
Base plate (BP)	6	
DCBSol	0.1, 0.25	DCB Solder
DCBLcu	0.3	DCB lower layer copper
DCB	1	AlN
DCBUcu	0.3	DCB upper layer copper
ChipSol	0.1	Chip solder
Chip	0.38	MOSFET and DIODE
ChipMet	0.004	Chip metal

The actual dimension of the DCB layer of the PM is not available because of the confidentiality issue. Hence, this thesis uses the typical combination of the thickness of copper and ceramic layers which is in table 5.1. The thickness of the chip is from the manufacturer datasheet. Therefore, there are some fixed thicknesses of the layers which are CP, LP, DCB and its copper layers, silicon carbide (SiC) chip, and chip metal layers. The thicknesses of the layers such as TIM layer, DCB solder layer, and chip solder layer are optimized to keep the maximum junction temperature as lowest as possible. Table 5.1 shows the thickness of all layers with the essential notes.

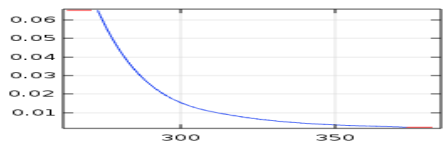
5.2.1 Materials properties

Table 5.2 records the nominal value of the essential materials properties such as heat capacity or specific heat capacity, C_p, density, ρ, and thermal conductivity, k of all the materials used in the system. The layers and its corresponding elements of materials are shown in figure 5.4 of earlier section. The time-dependent thermal properties of the listed items are not crucial for performance analysis, but it can not be ignored in the reliability and the lifetime assessment analysis of the system.

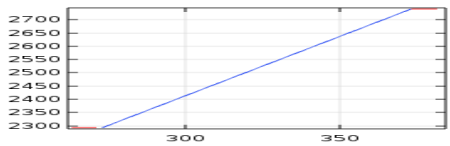
Table 5.2: Materials properties of the module

Materials	**Heat capacity,** C_p $(J/(kg.K))$	**Density,** ρ (kg/m^3)	**Thermal conductivity,** k $(W/(m.K))$
Aluminium 6060	900	2700	209
Ethylene glycol (50/50)	2400	1112	0.252
TIM	2600	1200	3
Copper	385	8960	400
SnAgCu	7370	220	57
AlN	3260	740	180
SiC	690	3216	490
Aluminium	900	2700	238

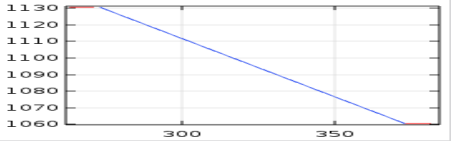
The only temperature dependents material properties considered is for the coolant, Ethylene glycol (50/50) solutions. Figure 5.5 illustrates these properties.



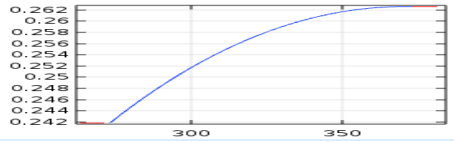
(a) Dynamic viscosity



(b) Heat capacity



(c) Density



(d) Thermal conductivity

Figure 5.5: Temperature dependent properties of the liquid Ethylene glycol

5.2.2 Heat source

The power losses in the system that mainly contribute to the thermal performance analysis of the system are the power losses in the power modules of the ACDC converter and the DCDC DAB converter. All others losses in the system are ignored in the thermal analysis by this report. The power losses considered in the thermal performance analysis of the system are tabulated in the table 5.3.

Table 5.3: Power loss in ACDC converter and DCDC converter for thermal analysis

Power loss in ACDC converter		
Components	Loss in W	Descriptions
sPM13	230.4334	Loss per switch in the PM 1 to PM 3
dPM13	13.8612	Loss per diode in the PM 1 to PM 3
Power loss in DAB converter		
Components (SS)	Loss in W	Descriptions
s1PM4 = s2PM5	281.01	equal in cross switches of PM4 and PM5
dPM45	8.86	Loss in each diode of PM4 and PM5
s2PM4 = s1PM5	279.83	equal in cross switches of PM4 and PM5
sPM67	120.24	Loss in each switch of PM6 and PM7
dPM67	81.87	Loss in each diode of PM6 and PM7
Components (HS)	Loss in W	Descriptions
hPM4	889	Loss per module
hPM5	889	Loss per module
hPM6	900	Loss per module
hPM7	900	Loss per module

There are fixed losses in the ACDC converter throughout the operational ranges. But the losses in the DCDC DAB converter vary during the soft switching (SS) and the hard switching (HS) technique as well as at the different operating points. Therefore, thermal performance analysis uses two different cases of heat sources. One is the SS heat source, and other is the HS heat source. In both cases, power modules of ACDC converter have the same heat sources as mentioned earlier. Table 5.3 shows heat sources in each MOSFET and its corresponding anti parallel DIODE for all of the modules with two different switching technique. There are no losses or heat sources in the DIODE during the HS technique, and all of the MOSFETs in the same module share the equal power losses. Hence, the per module power losses listed in table 5.3 is divided equally into the two switches of that module. Moreover, the power loss of each switch or each diode distributes into each chip of that switch or diode equally, because there are six chips in each switch or each diode mentioned before [19],[20].

5.3 Verification of PM: Choice of solder thickness

The classical simplified linear equation used to calculate the junction temperature if the case temperature, junction to case thermal resistance, and the power loss are

know, is shown in equation 5.1.

$$T_j = R_{th,jc} P_{Loss} + T_c \tag{5.1}$$

The further modification of the equation 5.1 gives the junction to case thermal resistance as a temperature difference between them or equal to the maximum junction temperature. It can be achieved by considering power loss equal is equal to one watt, and case temperature is equal to 0 °C and shown in equation 5.2.

$$R_{th,jc} = \frac{\Delta T_{jc}}{P_{Loss}} \tag{5.2}$$

Using the equation 5.1 and 5.2 and ignoring the others factors, the modeled PM is verified with the available 14 stages RC thermal model of the PM [21]. The 14 stages RC thermal model of the PM is shown in figure 5.6, and values of each RC components are considered from the datasheet. The standard junction to the case thermal resistance of the PM is 0.067 $°K/W$, and the maximum value is 0.071 $°K/W$ described in [25].

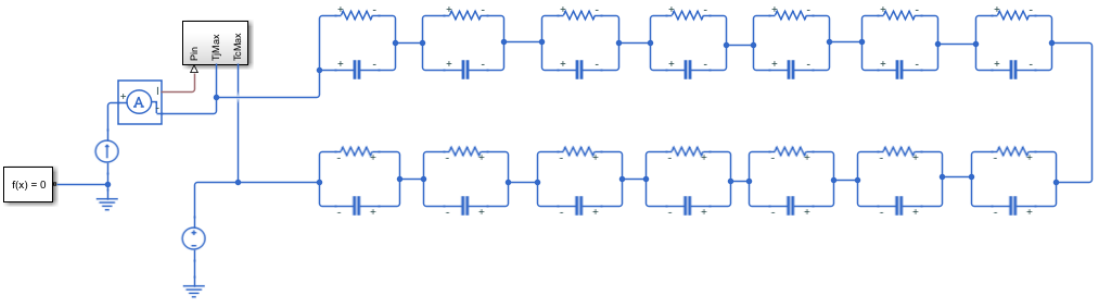


Figure 5.6: 14 stages RC thermal model of a MOSFET

The simulation for verification of the PM model is done using 1 W heat source on a MOSFET switch of a PM with 0 °C case temperature. The result gives the thermal resistance from junction to the case as a maximum junction temperature. The location of the points for the temperature measurements and the temperature distributions are shown in figure 5.7.

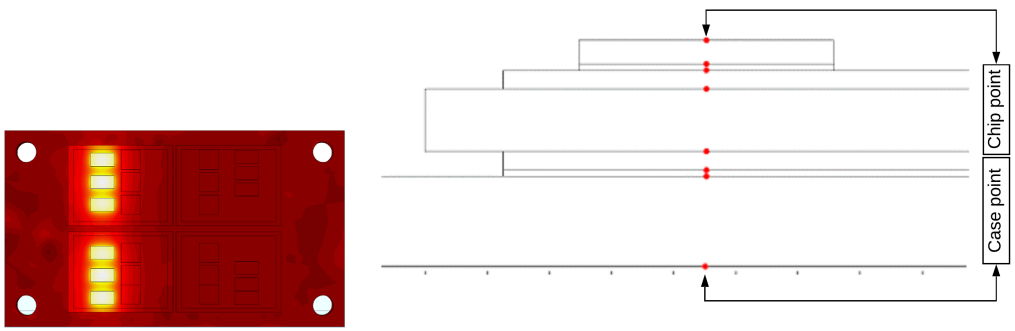


Figure 5.7: Thermal distribution over the PM and the point locations for temperature measurement

The simulation considered three different cases to get the closest value of the junction to the case thermal resistance for the modeled PM and plot against the chip numbers. In the first case, chip solder thickness and DCB solder thickness were 50 mm and 100 mm respectively, and the result shown in figure 5.8.

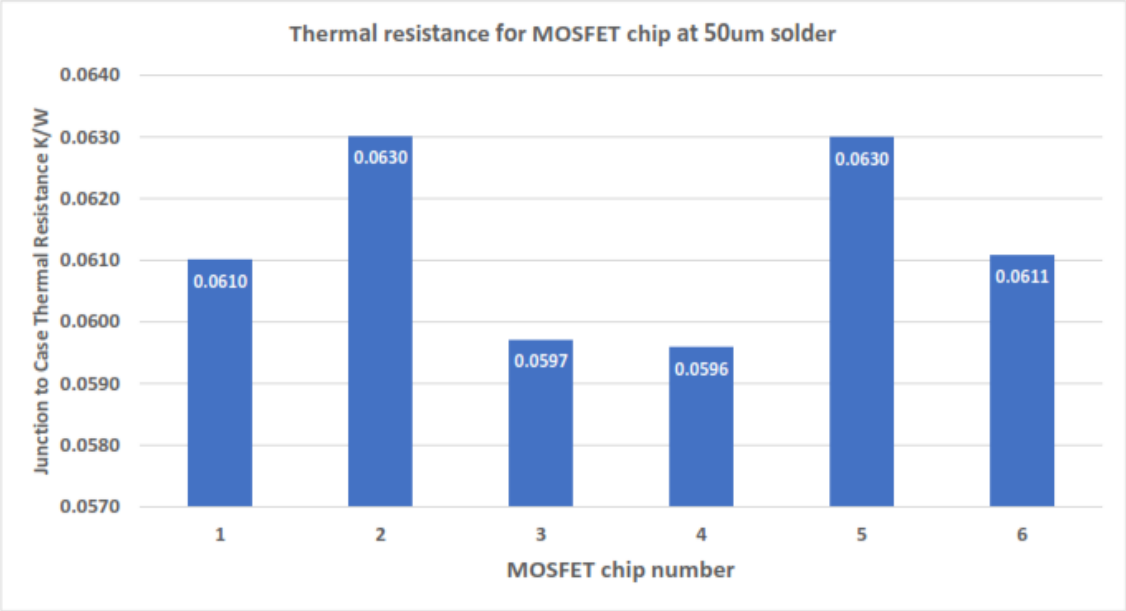


Figure 5.8: Junction to case thermal resistance for DCB solder thickness 50 um

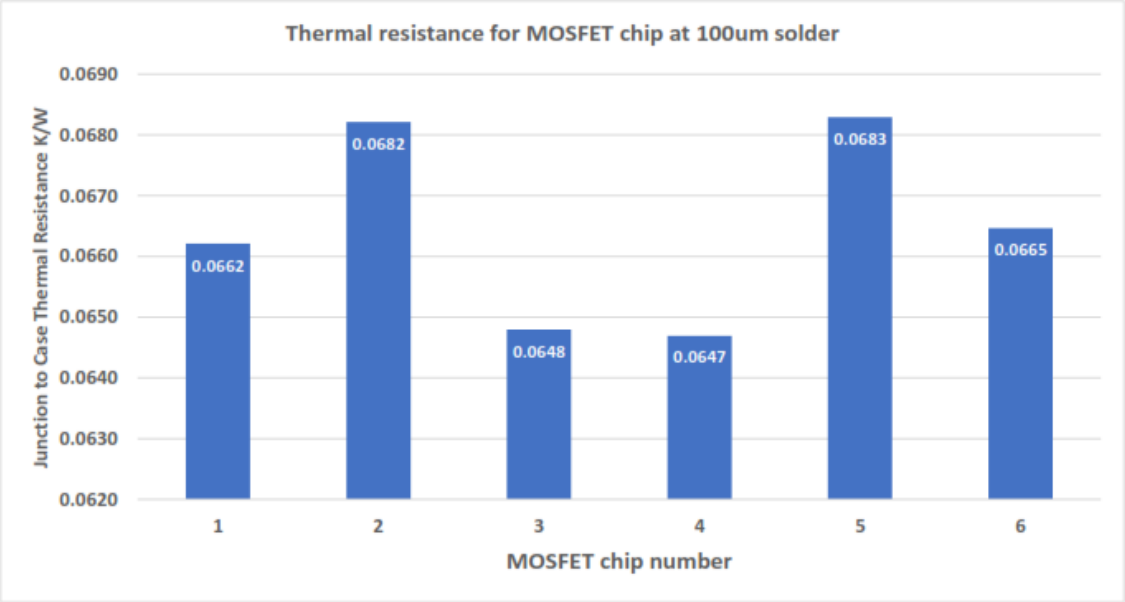


Figure 5.9: Junction to case thermal resistance for DCB solder thickness 100 um

Figure 5.9 shows the result of the second case which used both the chip solder thickness and DCB solder thickness as 100 mm. The last case used the chip solder thickness of 100 mm, and DCB solder thickness of 250 mm and figure 5.10 shows

the result of it. In all the cases above, other thicknesses remained fixed as described in Table 5.1.

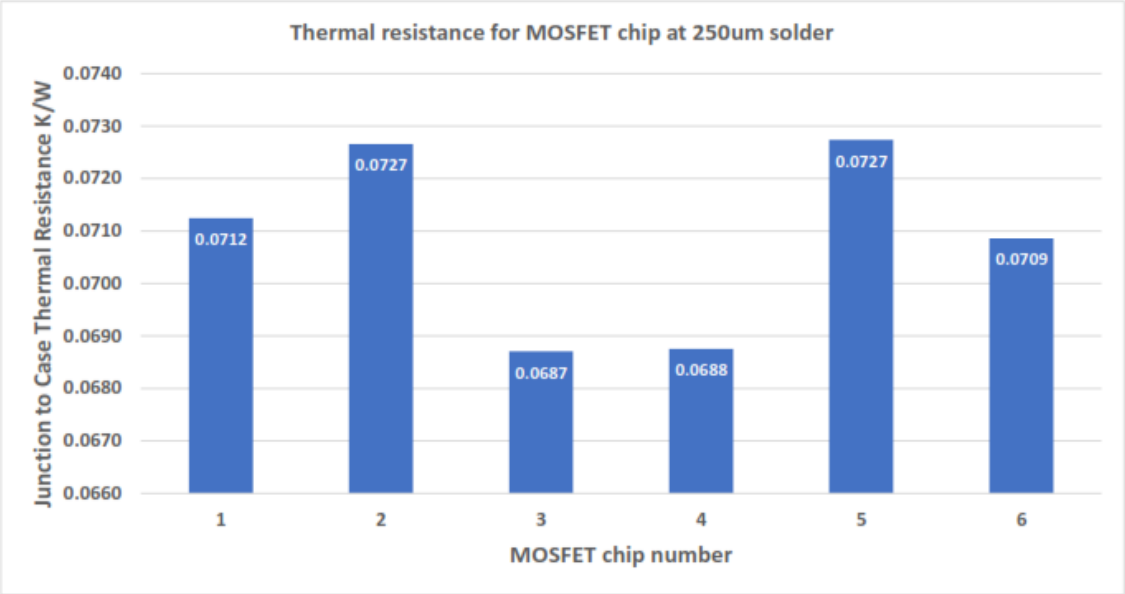


Figure 5.10: Junction to case thermal resistance for DCB solder thickness 250 *um*

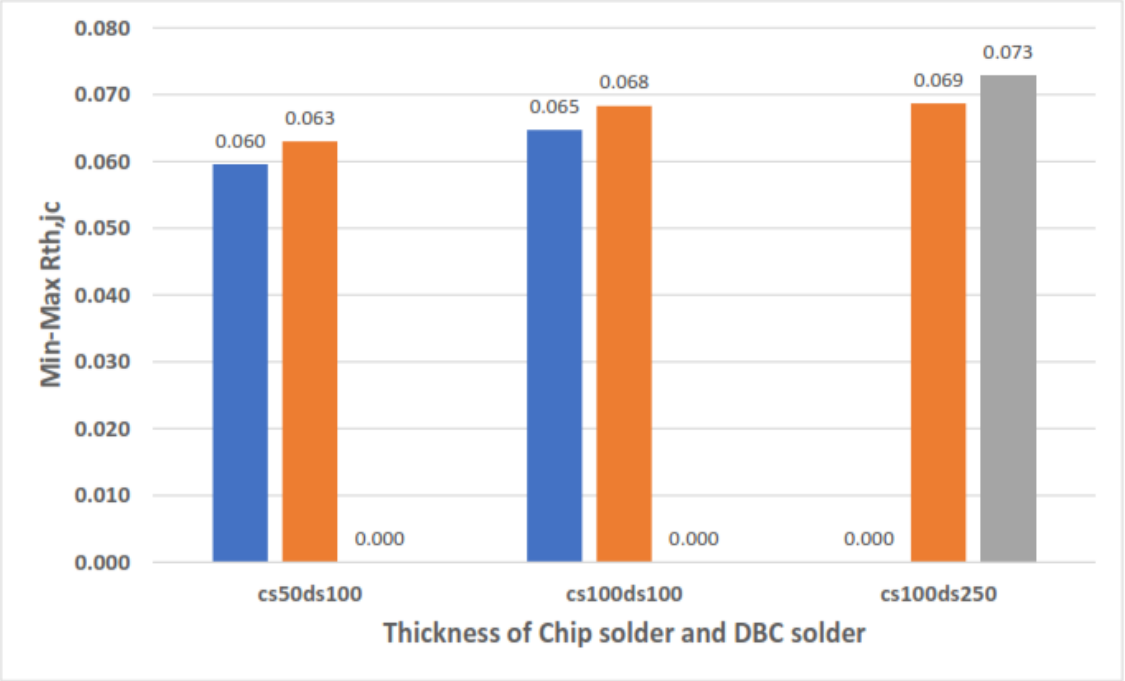


Figure 5.11: Maximum junction to case thermal resistance for PM

Figure 5.11 shows the summary of the results of three different cases. The reason for resulting different thermal resistance is due to the thermal cross-coupling effect among the chips of a single switch [16]. Hence, maximum temperature, as well as the maximum temperature difference, occurred at the second and the fifth chip

among the six chips of a single switch. The other chips surround both of them that's why maximum thermal resistance happened in one of them. It also shows that closest value of thermal resistance result for both solder thicknesses of 100 mm or the chip solder and DCB solder thicknesses combination of 100 mm and 250 mm respectively. The earlier one is a bit lower than the datasheet value, and later one is a bit higher than the datasheet value. The first one is chosen for the system performance analysis in coming section.

5.4 Temperature margin

The simulation has used a single PM without CP and LP to find the temperature margin at the case or base of the PM. It is essential to know the maximum possible case or base temperature to estimate the maximum junction temperature and to estimate the required temperature difference between the liquid coolant and the base. The maximum ambient temperature considered during the simulation is 50 $°C$. Hence, the inlet temperature of the liquid is fixed at 50 $°C$. On the other side, maximum junction temperature is evaluated for the different case or base temperature and the various power losses. The minimum power loss in a single switch is about 120 W during soft switching, and the maximum power loss in a single switch is about 450 W during hard switching. So, the power loss per module in the simulation is varied between 400 W and 1000 W, and the case temperature is changed between 60 $°C$ and 100 $°C$ to see the maximum possible junction temperature. Figure 5.12 shows that the maximum junction temperature results below 125 $°C$ for maximum case temperature of 90 $°C$ and power loss per module of 1000 W.

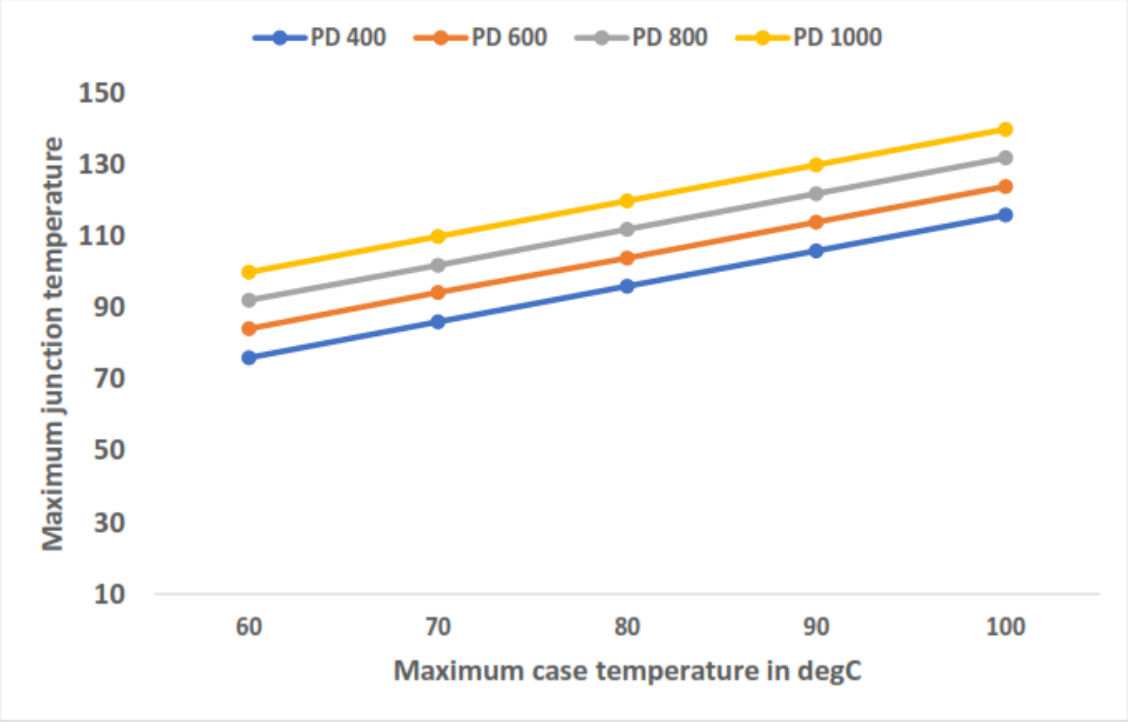


Figure 5.12: Thermal margin for the case and the cold plate

Therefore the temperature margin for the case could be 30 $°C$ considering case temperature in between 60 $°C$ and 90 $°C$ for any power losses per module below 1000 W. Furthermore, the temperature difference between the coolant and the case should be 10 $°C$ to 40 $°C$ which must be maintained by the proper liquid flow rate and pressure drop.

5.5 Temperature distribution: TIM thickness

Once the verification of PM is done, and the inlet temperature of the liquid is selected, it is time to optimized the TIM thickness. The whole system is built in the FEM simulator. It includes seven PMs on the cold plate, and seven individual TIM layers between each PM and CP. The coolant enters the LP with specific inlet temperature and flow rate. Figure 5.13 shows the temperature distribution for TIM thickness of 100 um and figure 5.14 shows the same for TIM thickness of 50 um.

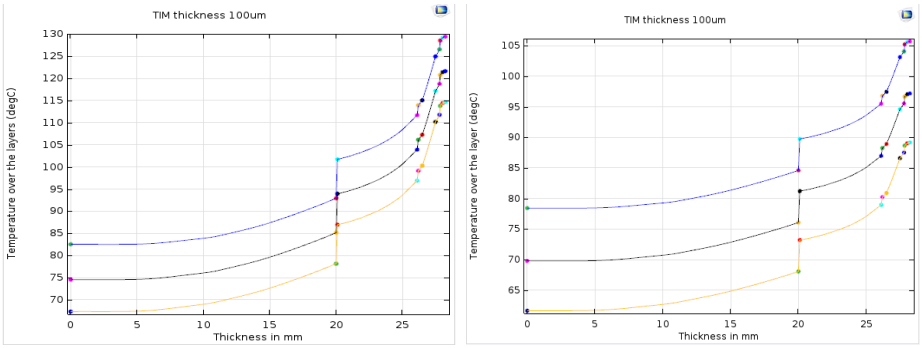


Figure 5.13: Maximum junction temperature for TIM thickness of 100 um, left: HS, right: SS

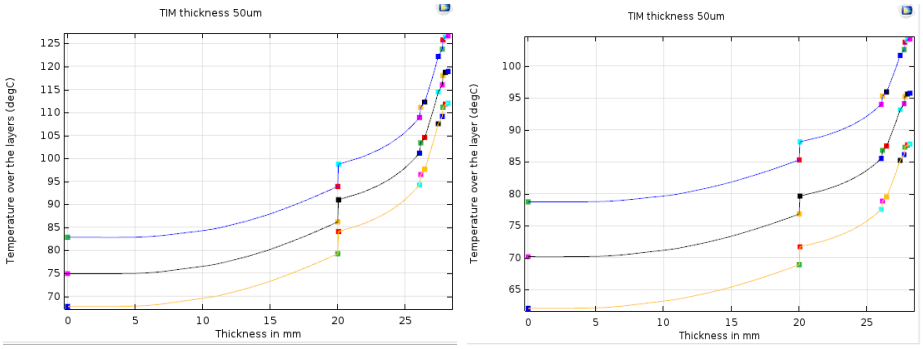


Figure 5.14: Maximum junction temperature for TIM thickness of 50 um, left: HS, right: SS

The temperature at the terminal points of each layer was measured and plots in the figure 5.13 and 5.14. The left side plots of both figures show the temperature distribution considering the power losses during HS. Similarly, the right side plots consider the power losses during SS. Moreover, it shows that the maximum junction temperature for TIM thickness of 100 um is about 115 $°C$ and 90 $°C$ for HS and

SS respectively. Similarly, the maximum temperature is about 112 $°C$ and 87 $°C$ for TIM thickness of 50 um. Therefore, thermal performance analysis uses the TIM thickness of 50 um in the upcoming section.

5.6 Cross coupling: Selection of hottest chip

The temperature induced in the neighbor switch because of the heat source in a switch considered as cross-coupling. The maximum temperature among all the switches in one module with cross-coupling effect is supposed to investigate the performance of heat sink. Hence, it is essential to check the cross-coupling in a single PM [16].
A single PM is placed on the cold plate with TIM layer, and the upper MOSFET is powered with a heat source of about 500 W. And the lower MOSFET, as well as both anti-parallel DIODE, remained unpowered.

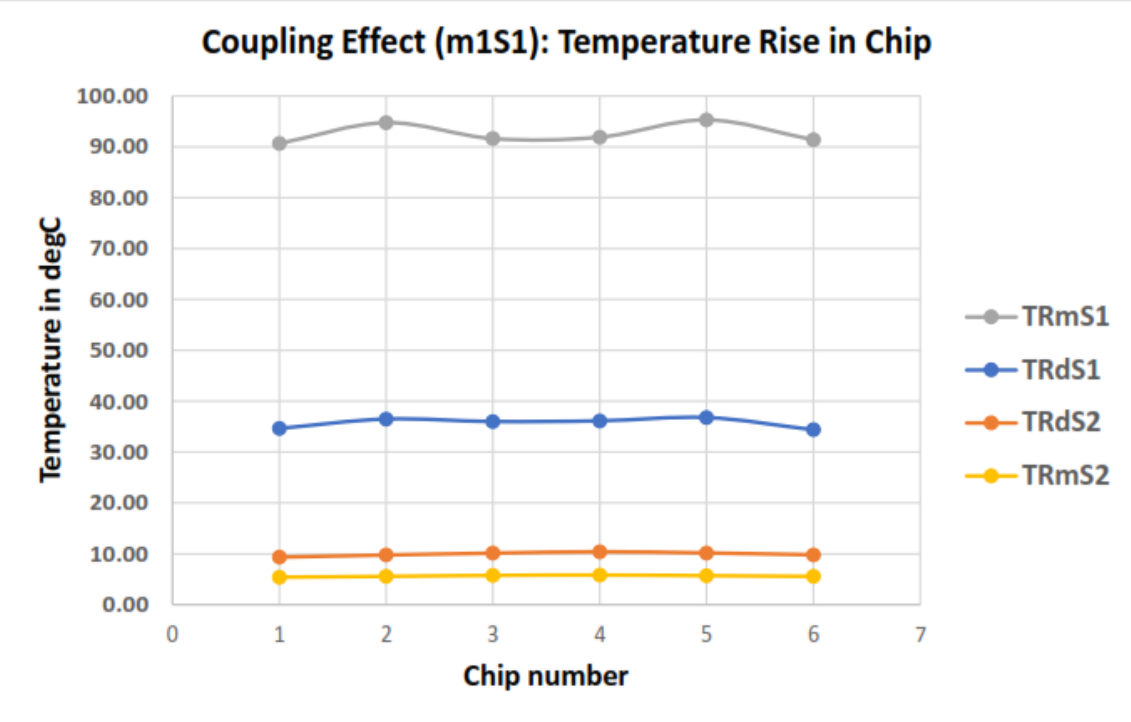


Figure 5.15: Temperature rise in switch two due to the heat source at switch one

The surface middle point of each chip of both MOSFETs and DIODEs are selected to measure the maximum temperature. Similarly, six points, which are below the six chips of upper MOSFET, inside the inlet pipe and six points, which are below the six chips of lower MOSFET, inside the outlet pipe are chosen to measure the minimum temperature. Then the temperature differences are calculated between chips temperature of the upper switch and selected points temperature of the inlet pipe. A similar procedure is followed for the chips of the lower switch and selected points of the outlet pipe. The rise in temperature in each chip of MOSFETs and

DIODEs are shown in figure 5.15.

Finally, the percentage rise of temperature in the unpowered chips of MOSFETs and DIODEs are calculated based on the temperature in the chips of powered MOSFET. The results show in figure 5.16.

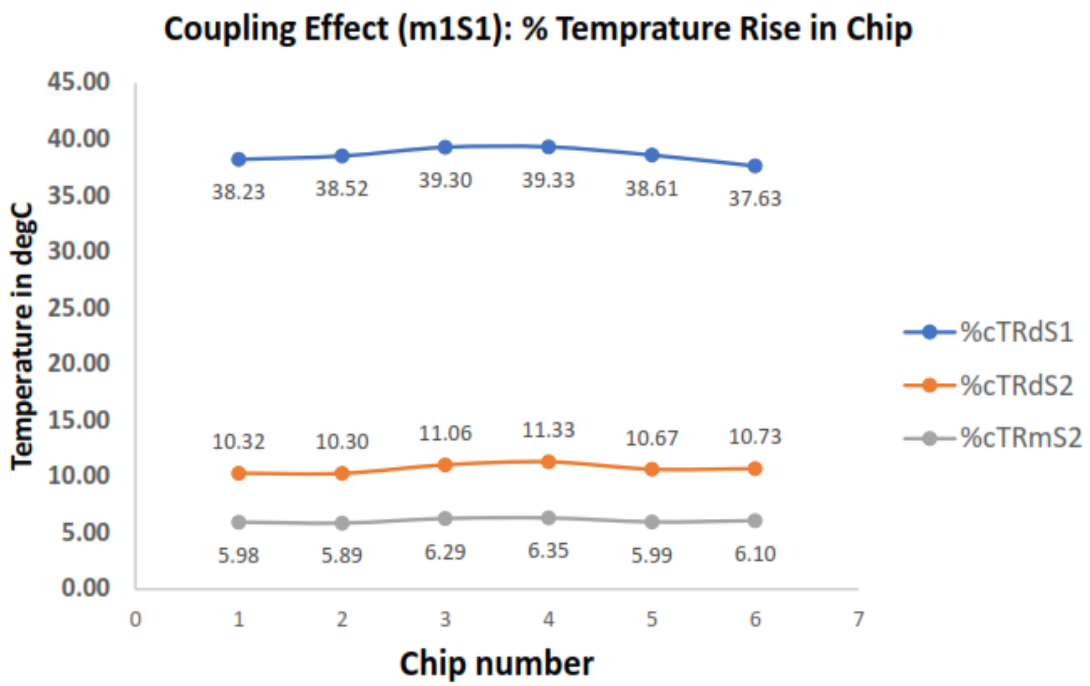


Figure 5.16: Percentage temperature rise in switch two due to the heat source at switch one

The result shows that there is cross coupling effect of about 40% at the DIODE chips ($\%TRdS1$), which is the antiparallel diode of the powered MOSFET ($m1S1$). On the contrary, it's almost 11% at the antiparallel DIODE ($\%TRdS2$) of unpowered MOSFET and about 6% at the unpowered MOSFET ($\%TRmS2$).

As a result, showed that the cross-coupling effect was less than 6% at unpowered MOSFET of the same PM which is below the 10%. Hence, cross-coupling effect is negligible in this case.
As there is negligible cross-coupling between the switches of each PM, the thermal performance of the system is done based on the hottest chip in each switch of the PM. Therefore, there are 14 hottest chips for seven PMs, one chip from one upper switch and one chip from one lower switch of a single PM, and corresponding points inside the LP are considered for the thermal performance analysis.

5.7 System performance analysis

The goal of the performance analysis is to find the system performance thermal resistance between junction and liquid, $R_{th}(JL)$ and required pressure drop for different liquid flow rate in LPM. The is achieved by following two steps.

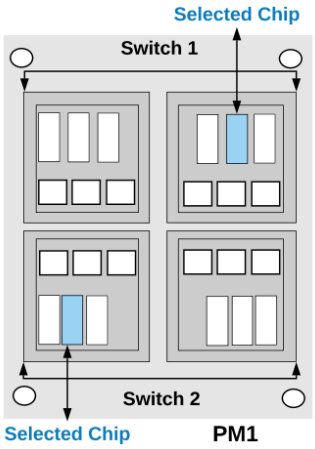


Figure 5.17: Selected chip of each PM

In the first step, the simulation ran for the verified and optimized thermal system and measured the hottest chips temperature in each switch of each PM. There are 14 temperature points whereas seven are in the upper switches of PMs and seven are in the lower switches of PMs. Similarly, there are 14 temperature points inside the LP below the hottest chips whereas seven are at the inlet pipe and seven are at the outlet pipe. Based on the selected locations, the temperature distribution over the layer was found for different fluid flow rate in LPM. Figure 5.18 shows the selected point in the liquid pipe, which are below the chosen chips of PMs. There are seven points inside the inlet pipe and seven points inside the outlet pipe at 10 mm above the origin. Figure 5.17 shows the PM1 and its switches with the selected chips. The second chip is selected for the upper switch, and the fifth chip is selected for the lower switch. The second chip of each upper switch of PMs experiences the highest temperature because of the cross-coupling by neighbor chips. The liquid is also getting heated when flowing from the inlet towards the outlet. For the same reason, the fifth chip of the lower switch of PMs experiences the maximum temperature.

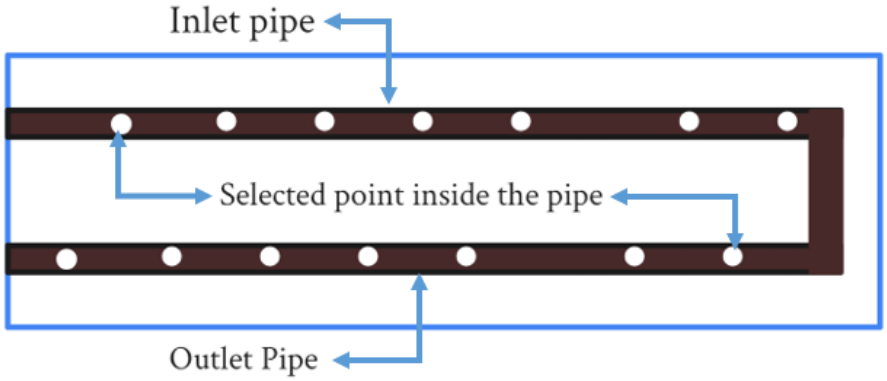
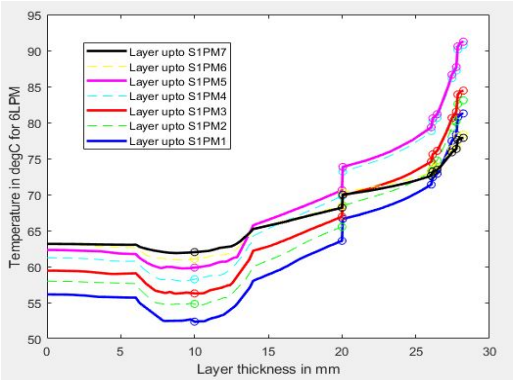


Figure 5.18: Selected points inside the pipe which are below the selected chip of the switch (dimension are not accurate)

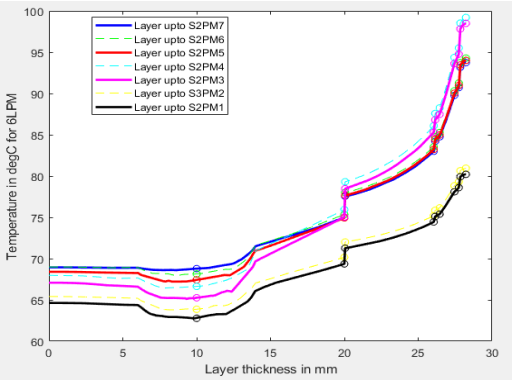
In the second step, the junction to liquid thermal resistance, $R_{th}(JL)$ was derived by dividing temperature rise in each switch by the total power loss in it. There is 14 thermal resistance calculated for 14 switches of seven PMs.
Finally, the similar procedure is followed for the SS power losses and HS power losses

5.7.1 Temperature distribution over the layer

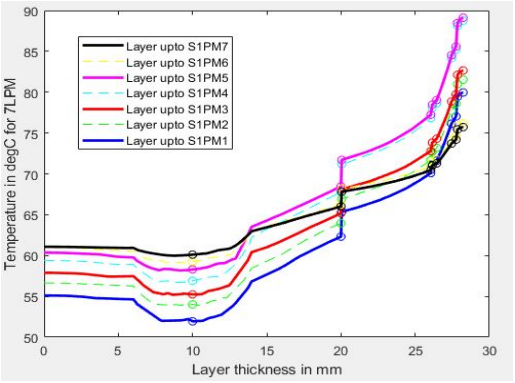
The temperature distribution across the layer at upper switch side of each PM and across the thickness at lower switch side of each PM with different fluid flow rate are depicted in figure 5.19 and 5.20. The figure 5.19 is for the soft switching (SS) power losses whereas figure 5.20 is for the hard switching (HS) power losses.



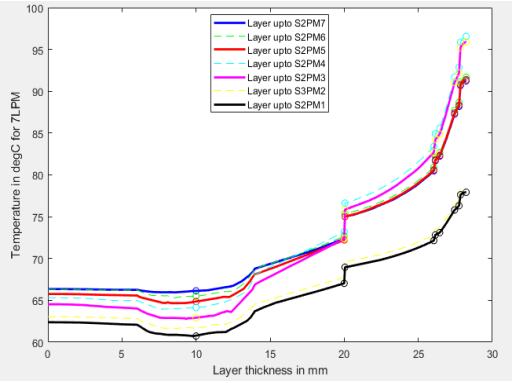
(a) Upper switches and 6 LPM



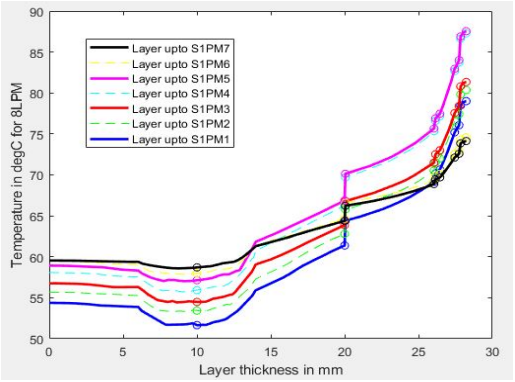
(b) Lower switches and 6 LPM



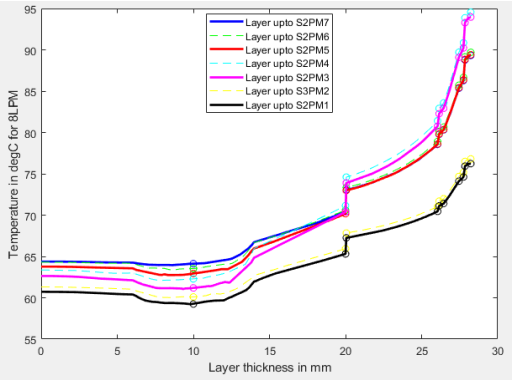
(c) Upper switches and 7 LPM



(d) Lower switches and 7 LPM

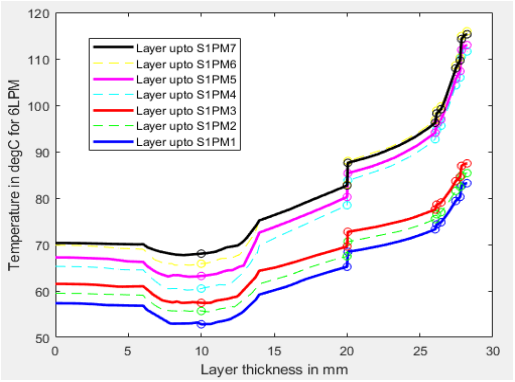


(e) Upper switches and 8 LPM

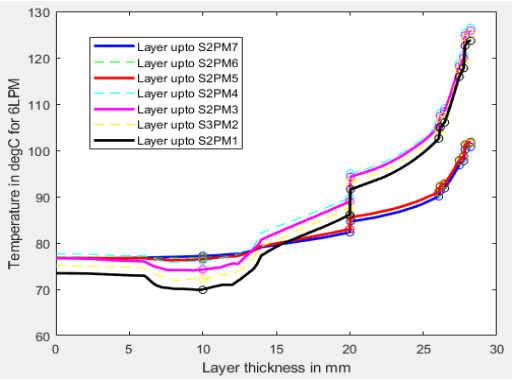


(f) Lower switches and 8 LPM

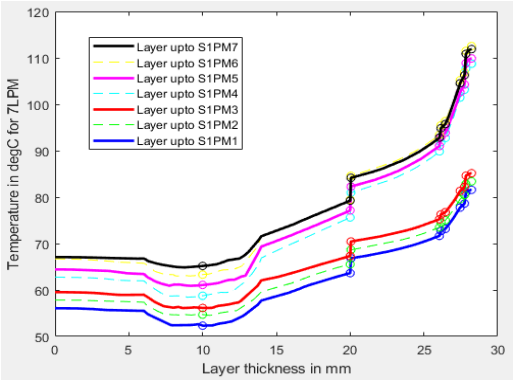
Figure 5.19: Temperature distribution, based on soft switching losses, over the layer of all PMs in different switches and for different liquid flow rate. In (a) upper switches and 6 LPM, (b) lower switches and 6 LPM, (c) upper switches and 7 LPM, (d) lower switches and 7 LPM, (e) upper switches and 8 LPM, and (f) lower switches and 8 LPM liquid flow rate



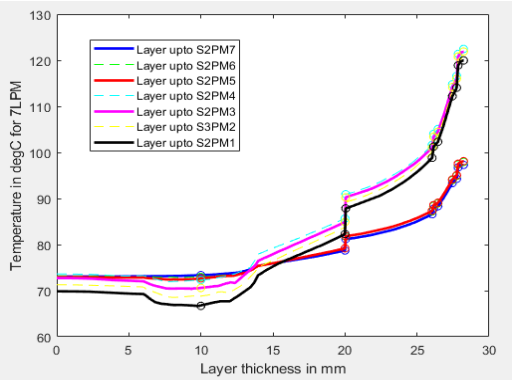
(a) Upper switches and 6 LPM



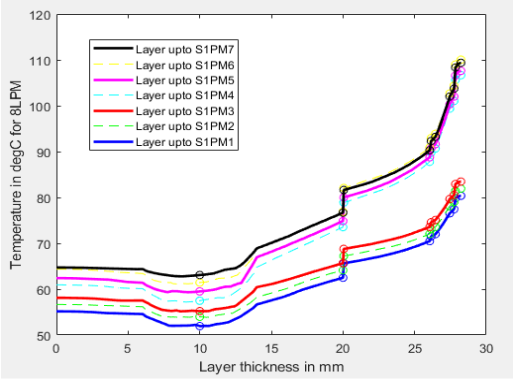
(b) Lower switches and 6 LPM



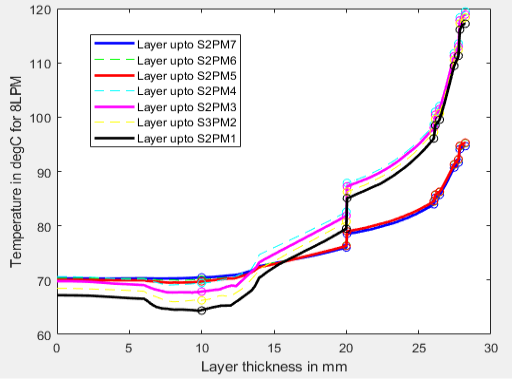
(c) Upper switches and 7 LPM



(d) Lower switches and 7 LPM



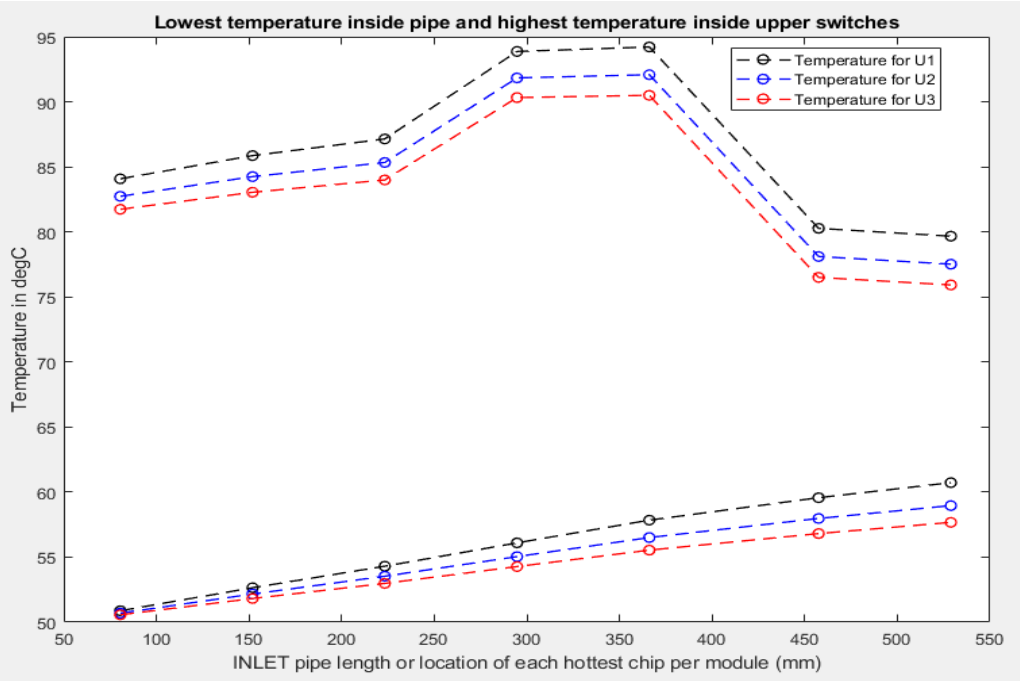
(e) Upper switches and 8 LPM



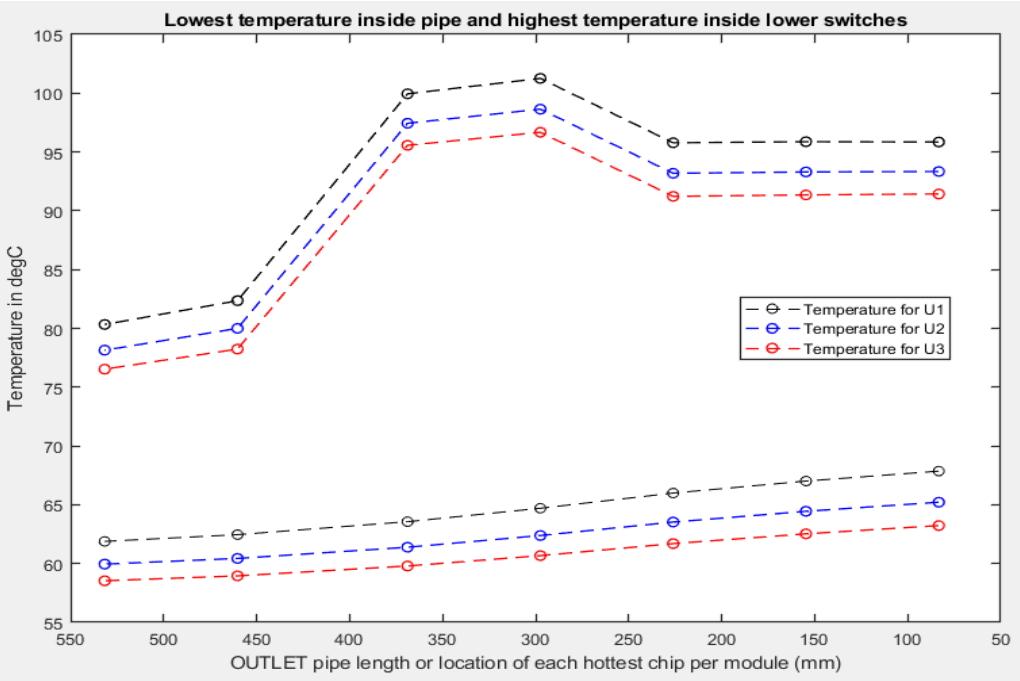
(f) Lower switches and 8 LPM

Figure 5.20: Temperature distribution, based on hard switching losses, over the layer of all PMs in different switches and for different liquid flow rate. In (a) upper switches and 6 LPM, (b) lower switches and 6 LPM, (c) upper switches and 7 LPM, (d) lower switches and 7 LPM, (e) upper switches and 8 LPM, and (f) lower switches and 8 LPM liquid flow rate

Figure 5.21, and figure 5.22 show the location of selected points and their maximum temperatures. The minimum temperatures happen in the liquid pipe, and maximum temperatures occur in the chips. So, the top lines are for the temperature of the chips, and bottom plots are for the temperature of the liquid for different fluid flow rate. Figure 5.21 is for the SS heat sources, figure 5.22 is for HS heat sources. In both cases, lower switches of the fifth PM experience the maximum stress.

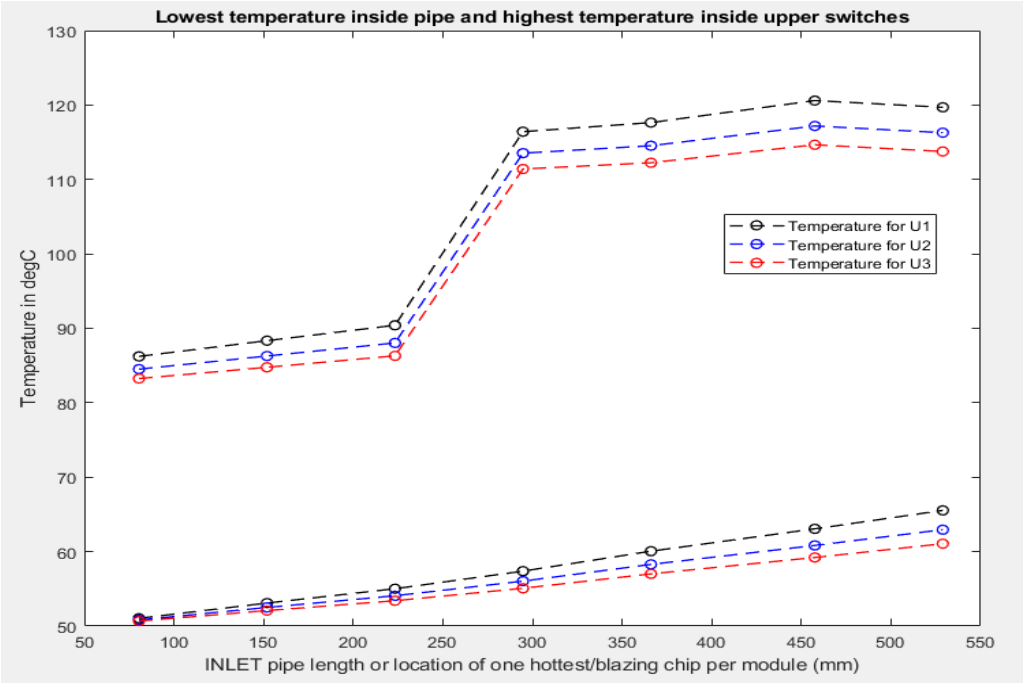


(a) Temperatures at hottest chip of each upper switches and inside the inlet pipe below that chips.

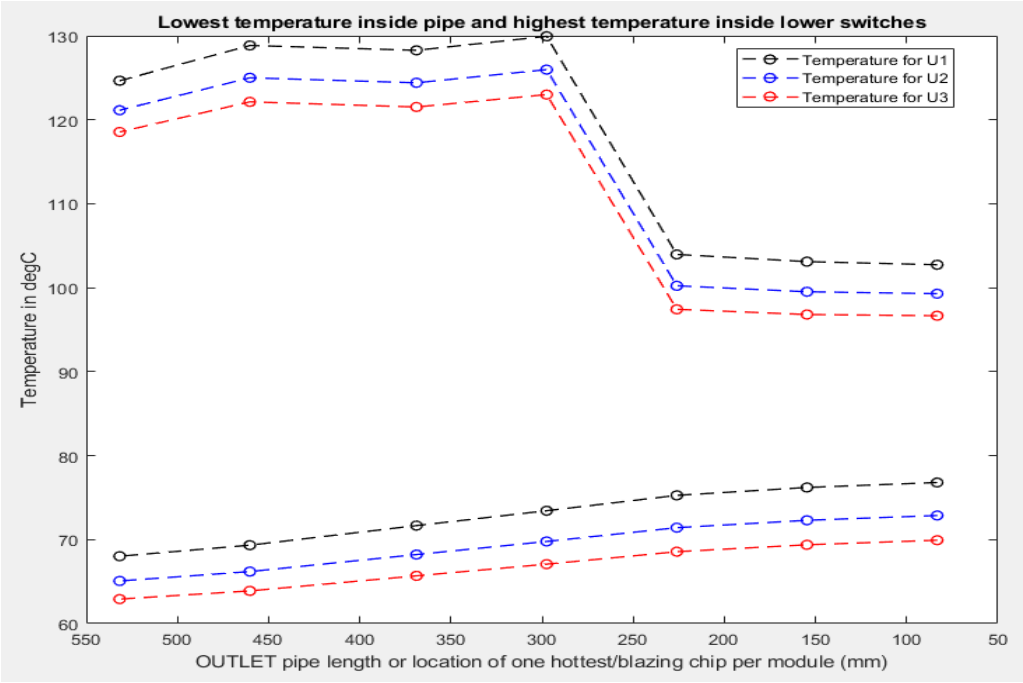


(b) Temperatures at hottest chip of each lower switches and inside the outlet pipe below that chips.

Figure 5.21: The minimum layer temperature inside the liquid pipe and maximum layer temperature at the each switches of the power module, based on soft switching losses, for different liquid flow rate (a) shows the inlet pipe and upper switches, and (b) shows the outlet pipe and lower switches of all PMs.



(a) Temperatures at hottest chip of each upper switches and inside the inlet pipe below that chips.



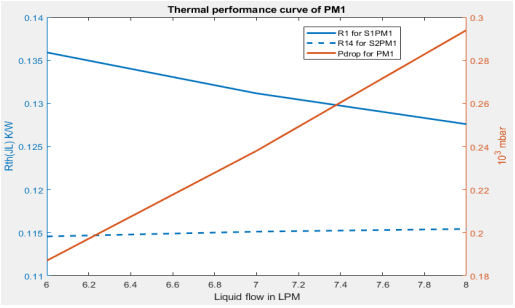
(b) Temperatures at hottest chip of each lower switches and inside the outlet pipe below that chips.

Figure 5.22: The minimum layer temperature inside the liquid pipe and maximum layer temperature at the each switches of the power module, based on hard switching losses, for different liquid flow rate (a) shows the inlet pipe and upper switches, and (b) shows the outlet pipe and lower switches of all PMs.

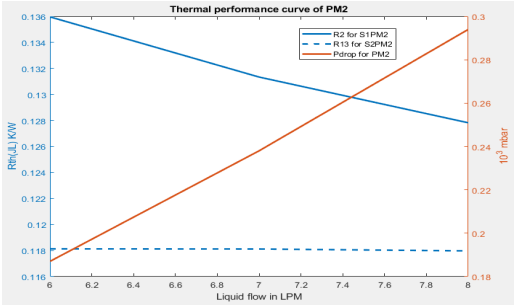
For SS heat source, the lower switch of the fifth PM experienced the highest temperature, which is about 95 $°C$, 98 $°C$, and 102 $°C$ for the 8 LPM, 7 LPM, and 6 LPM fluid flow respectively. The outlet temperatures of the liquid are 60, 63, and 67 $°C$ with 8 LPM, 7 LPM, and 6 LPM respectively.
Similarly, for the HS heat source, the maximum temperatures are about $110 - 120$ $°C$, 124 $°C$, and 130 $°C$ at the lower switch of the fifth PM with 8, 7, and 6LPM respectively. Moreover, the outlet temperatures are almost 65, 70, and 75 $°C$ respectively for 8, 7, and 6 LPM.
The crucial points in the result being that there is 10% extra power considered during the simulation in both SS and HS heat source. Hence, the recommended flow rate should be 7 LPM to keep the maximum temperature around 100 $°C$ for SS and below 120 $°C$ for HS. But in the practical device, HS does not occur frequently.

5.7.2 Thermal resistance (Junction to liquid)

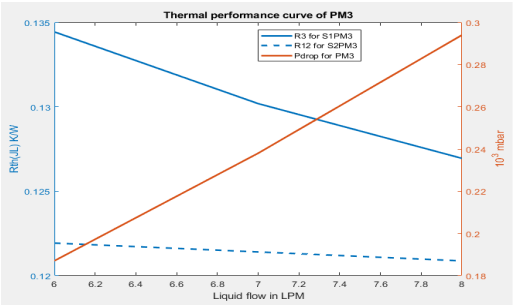
There are 14 thermal resistances for the junction to liquid calculated to evaluate the performance of the system. One thermal resistance is for one switch. Hence, each PM gets two thermal resistances. $R1$ and $R14$ are for the PM1, $R2$ and $R13$ are for PM2, $R3$ and $R12$ are for PM3, $R4$ and $R11$ are for PM4, $R5$ and $R10$ are for PM5, $R6$ and $R9$ are for PM6, and $R7$ and $R8$ are for PM7, whereas R1 to R7 are for the upper switches and R8 to R14 are for the lower switches.
Figure 5.23 and figure 5.24 show the performance thermal resistance of each module along with the pressure drop of the system. Figure 5.23 is for the SS heat source and figure 5.24 is for the HS heat source. Figure 5.25 and Figure
5.26 show the performance thermal resistance for all upper and all lower switches together with pressure drop. Figure 5.25 is for SS heat source, and figure 5.26 is for the HS heat source. The pressure drops for the system during the SS are 198, 254 and 314 $mbar$ respectively for the liquid velocity of 6 LPM, 7 LPM, and 8 LPM. These quantities are 187, 238, and 294 $mbar$ respectively for 6 LPM, 7 LPM, and 8 LPM with HS heat source.
The result shows that the thermal resistance curve intersects with the pressure drop plot in between 7 LPM and 8 LPM velocity for the first, second, and third PMs. It happens in between 6 LPM and 7 LPM velocity for the sixth, and seventh PMs of the system. Almost 6 LPM results for the PM4.
The PM1 to PM3 sits at the beginning of the inlet pipe and the end of the outlet pipe of the LP. They get the coolant having the lower temperature across the upper side switches, and higher temperature at the lower side switches. Their heat source remains fixed for the both SS and HS heat source consideration mentioned before. The losses in PM1 to PM3 are smaller than the losses in PM4 to PM7.
On the other side, PM4 and PM5 get the preheated coolant from PM1 to PM3. That coolant is passed through the PM6 and PM7 and return through outlet pipe in reverse order.
There is also a tendency of increasing thermal resistance at high velocity in the lower switches of the PM1 and PM2.



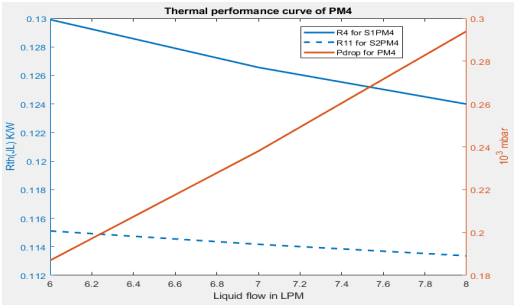
(a) R1 and R14 for PM1



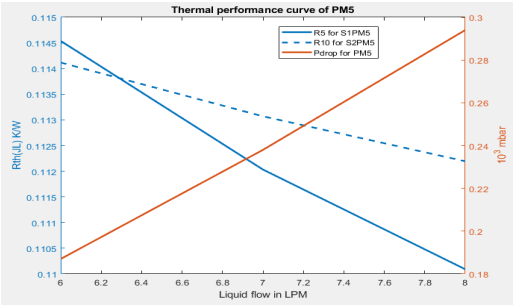
(b) R2 and R13 for PM2



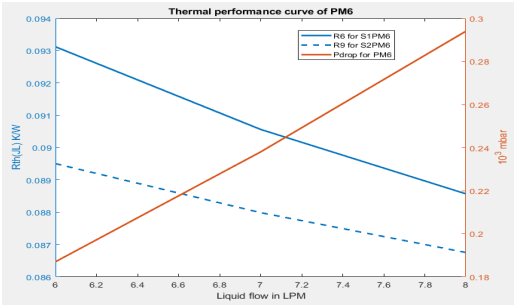
(c) R3 and R12 for PM3



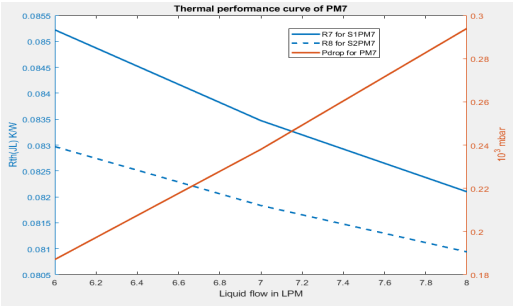
(d) R4 and R11 for PM4



(e) R5 and R10 for PM5

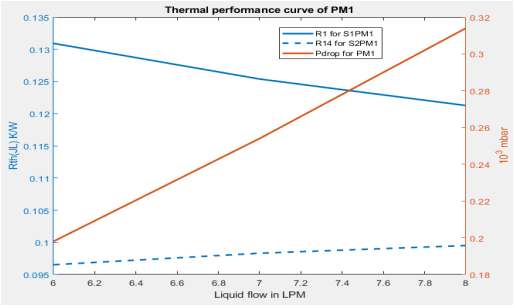


(f) R6 and R9 for PM6

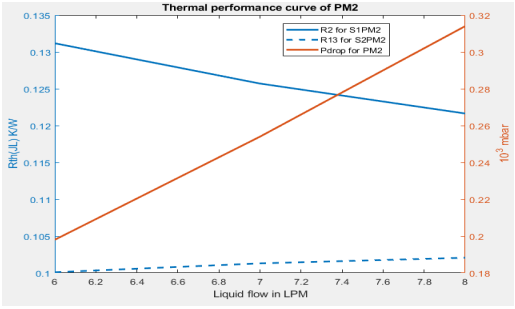


(g) R7 and R8 for PM7

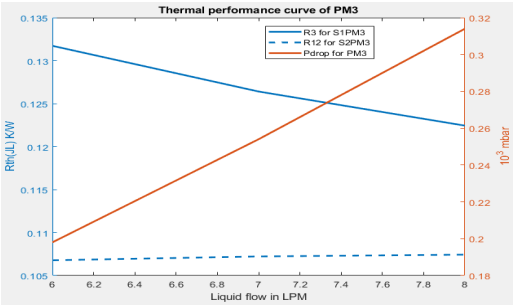
Figure 5.23: Thermal performance of the system based on soft switching losses, and different flow rate of the liquid. In (a) for PM1, (b) for PM2, (c) for PM3, (d) for PM4, (e) for PM5, (f) for PM6, and (g) for PM7.



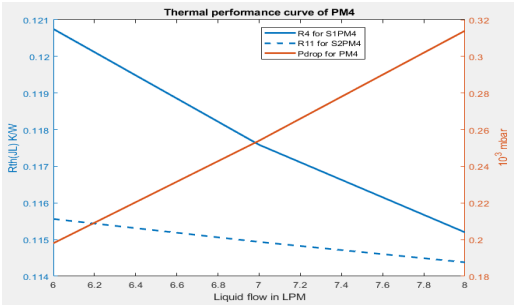
(a) R1 and R14 for PM1



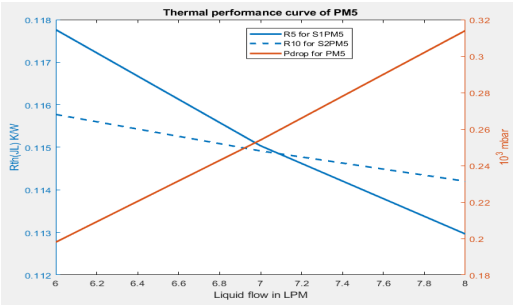
(b) R2 and R13 for PM2



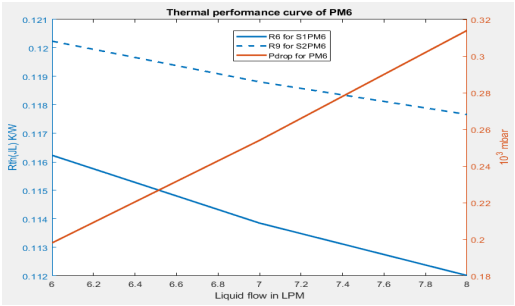
(c) R3 and R12 for PM3



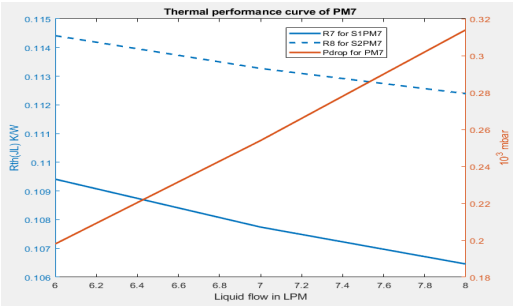
(d) R4 and R11 for PM4



(e) R5 and R10 for PM5

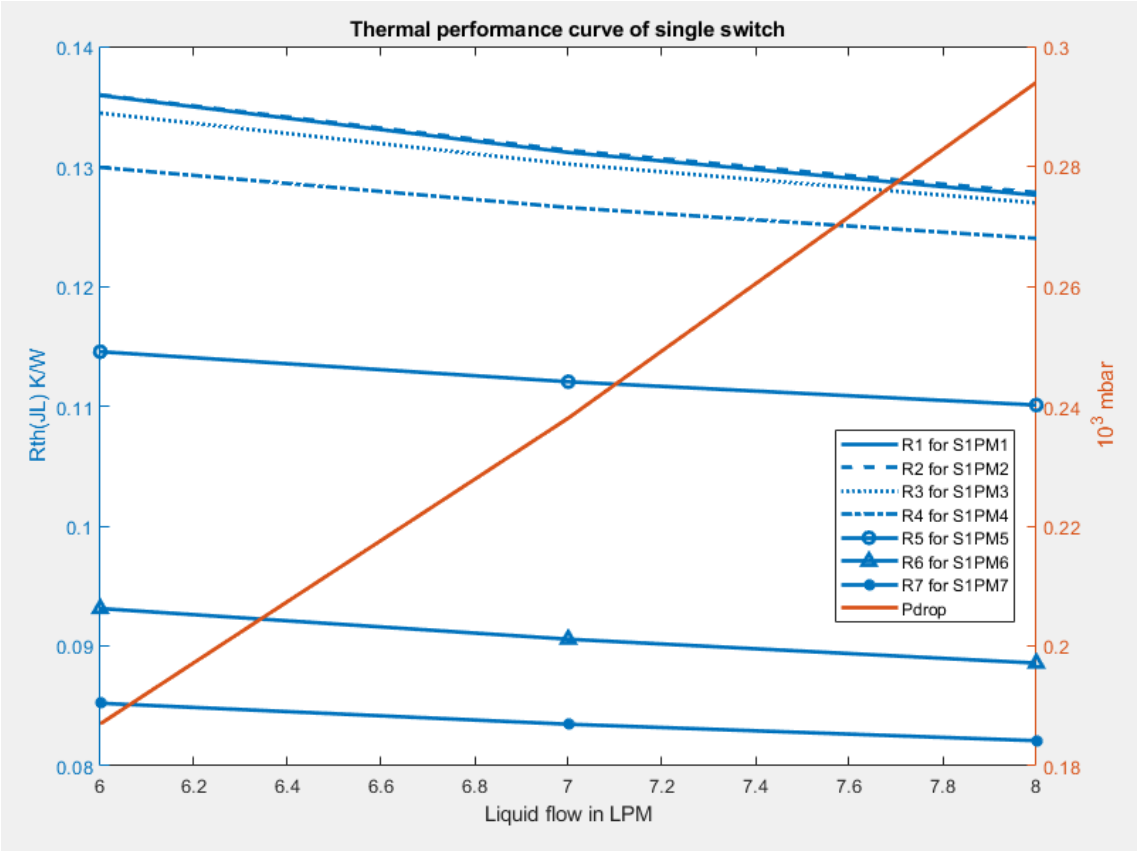


(f) R6 and R9 for PM6

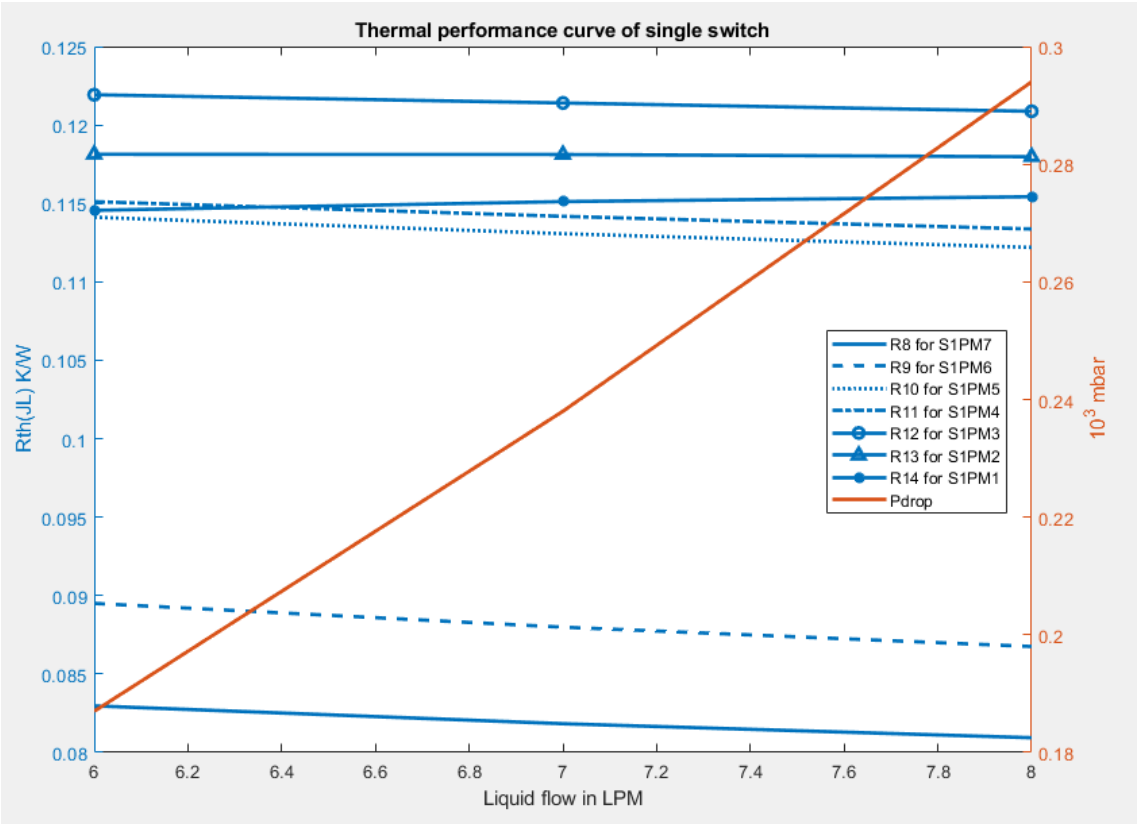


(g) R7 and R8 for PM7

Figure 5.24: Thermal performance of the system based on hard switching losse, sand different flow rate of the liquid. In (a) for PM1, (b) for PM2, (c) for PM3, (d) for PM4, (e) for PM5, (f) for PM6, and (g) for PM7.

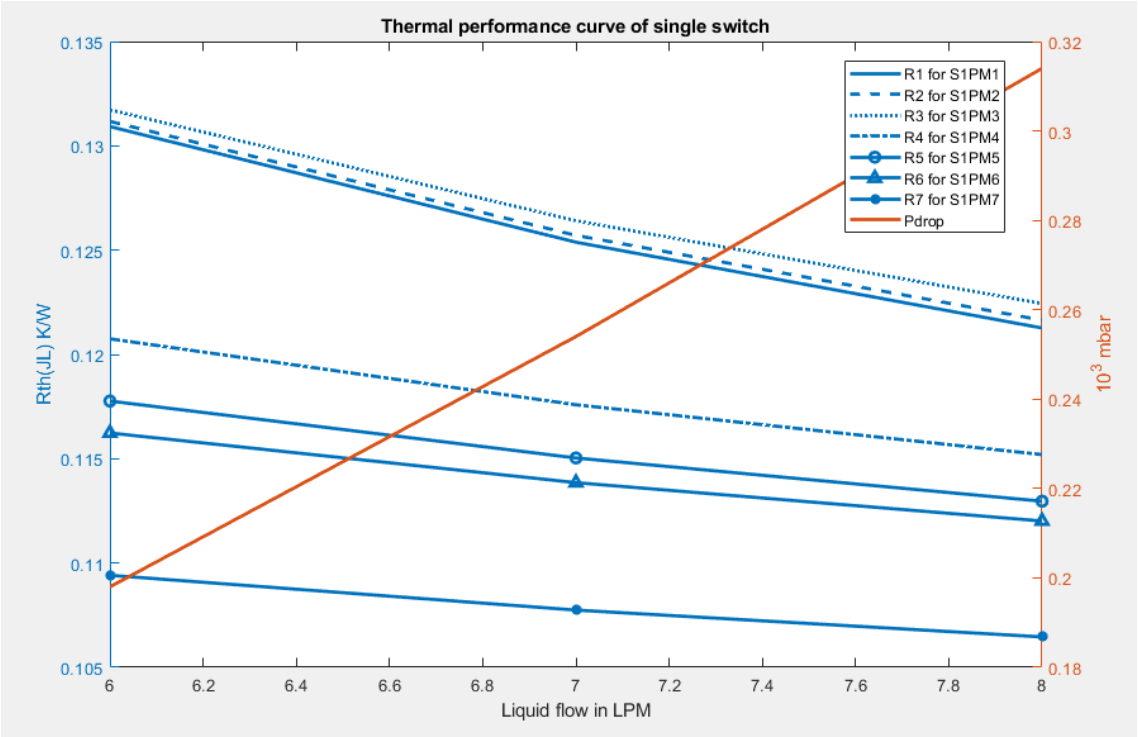


(a) Upper switches of all modules

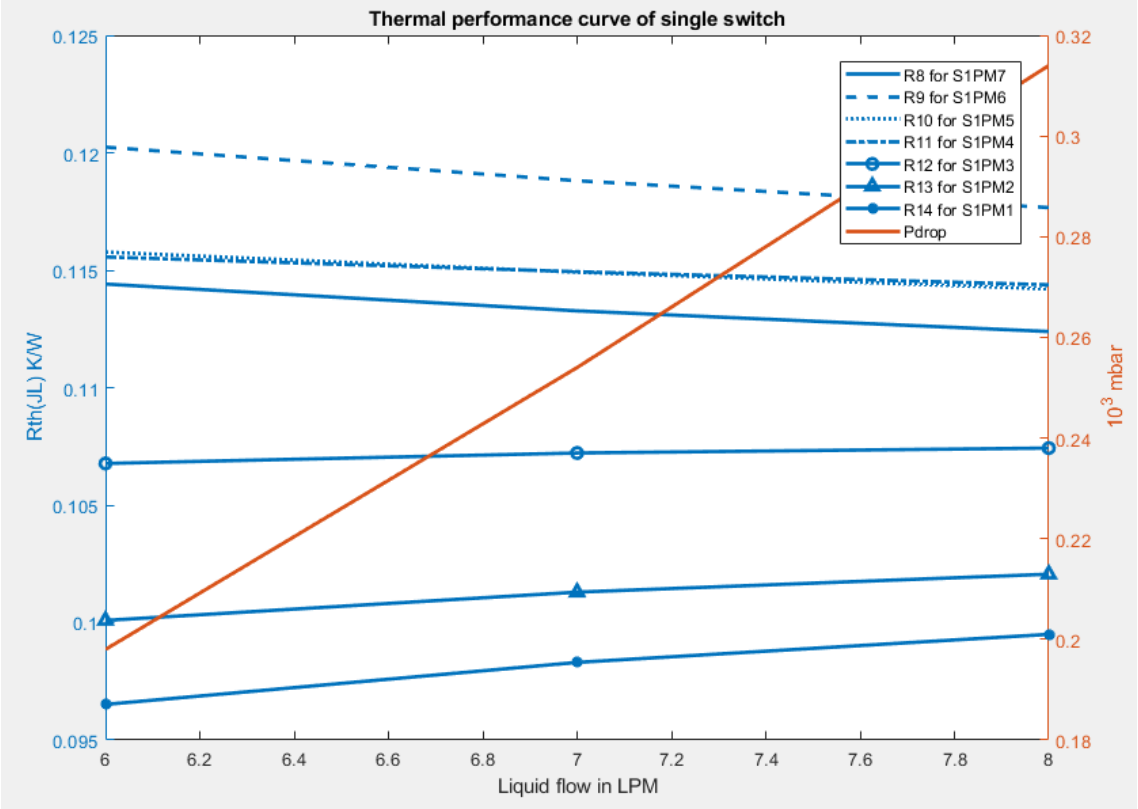


(b) Lower switches of all modules

Figure 5.25: Soft switching losses based thermal performance of all modules. In (a) for upper switches, (b) for lower switches.



(a) Upper switches of all modules



(b) Lower switches of all modules

Figure 5.26: Hard switching losses based thermal performance of all modules. In (a) for upper switches, (b) for lower switches.

5.8 Conclusion

This chapter explicitly presented the modelling of the power module in the FEM simulator. It also verified the module and designed the cold plate for the FCS. The performance of the cooling system is presented and shows that the 6 to 8 LPM liquid flow rate is enough to keep the maximum junction temperature 15% below the permissible limit within the whole operating range.

6
Conclusion

In this study, the analytical loss calculation of a fast charging station (FCS) is presented explicitly. Based on the losses, a thermal cooling system is designed in FEM simulator, and its performance analysis is done. Besides these, the PM model is verified with its datasheet parameters. Hence, the first two aims of the project are completed and exhibited in chapter 3 and chapter 4. The remaining goals are achieved in chapter 5. Finally, this design would be suitable for the investigated FCS with 6 to 8 LPM liquid flow rate, 50 $^{\circ}C$ inlet temperature, and 187 to 314 $mbar$ pressure drop.

6.1 Future work

In this study, only the steady-state losses are considered, based on the losses, the thermal system is designed, and its performance is analyzed. Hence, the transient loss analysis and performance of the thermal system for that could be one of the future studies on this project. Furthermore, the reliability analysis of the PMs and the lifetime study of the system are the interesting cases for the further research. Moreover, The cross heating effect of combining three 100 kW module could also be examined. Finally, different layouts of the cold plate could be investigated for improvement of the thermal performance of the system.

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