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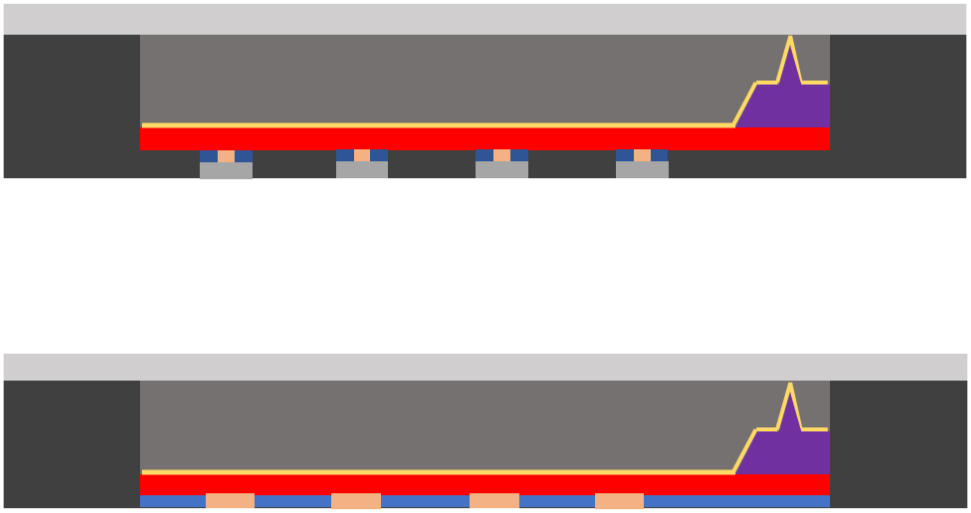

Reliability Study of One TSV Based Ultra-thin Fingerprint Sensor Package

An improvement of the packaging process

Master's thesis in Product Development

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Department of Mechanics and Maritime Sciences
CHALMERS UNIVERSITY OF TECHNOLOGY
Gothenburg, Sweden 2019

Master's thesis 2019

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Master's Thesis 2019:73
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Cover: The cross section of the TSV based ultra-thin fingerprint sensor package.
Typeset in LaTeX
Gothenburg, Sweden 2019

Abstract

Through silicon via (TSV) technology is a vertical electrical interconnection that is etched into a silicon wafer or a die. The primary benefit of using TSV technology is to shortening the interconnection path and further reducing the die thickness. Therefore, the TSV based packages are widely used in fingerprint sensors. In Fingerprint Cards AB (FPC), a new TSV based ultra-thin fingerprint sensor package along with an improvement of the manufacturing process was developed, which enables to further reduce the thickness of the fingerprint sensor package.

This thesis report is focused on the reliability study of a newly designed TSV based ultra-thin fingerprint sensor package, to verify and check if it can pass the qualification standards for the consumer electronics products. The new package was designed based on one of the widely-used fingerprint senor package in FPC. A design of experiments (DOE) study regarding the design of the new TSV based ultra-thin fingerprint sensor package was conducted, a set of changes in design parameters were generated according to the requirements of both FPC and the phone original equipment manufacturers (OEMs). The reliability of the new TSV based fingerprint sensor package was analyzed and compared to the reference package by conducting the FEA simulations, such as warpage simulation, ball drop simulation and bending simulation.

Based on analysis of the result of the FEA simulations, the TSV based ultra-thin fingerprint sensor has been proved to be qualified to pass the relevant in-house qualification standards of Fingerprint Cards AB, but new studies need to be continued and engineering samples need to be built and test if the phone OEMs want to apply this new TSV based fingerprint sensor to its consumer electronics products.

Keywords: TSV, Packaging design, Process improvement, Fingerprint sensor, DOE, Finite element analysis, Warpage simulation, Bending simulation

Acknowledgements

I would like to give my sincerest thanks to Håkan Johansson, my examiner and supervisor at Chalmers University of Technology. He gave me a huge support in terms of thesis planning, research methodology, instructing FEA simulations and the thesis paper writing.

I would also like to thank my supervisor at Fingerprint Cards AB, Nils Lundberg for offering me this thesis work within in the cutting-edge technology field. It is a great chance for me to acquire more knowledge and develop my interest in semiconductor packaging technology, a totally brand new filed for me before I started this thesis. An additional thanks to Wei Mu and Staffan Hägglund for guiding me about packaging technology, DOE study and the specific thermomechanical simulation in COMSOL.

Meanwhile, I want to thank all my friends and colleagues that I have been working with at Fingerprint Cards for their honest support and help during my study and work in Sweden.

Finally, my deep and sincere gratitude to my family for their continuous and unparalleled love and support. During the entire time of my master study at Chalmers, my sister was always being there as a friend, her company helped me pass through the hardest times in 2018 and 2019. My parents and my brother were definitely the ones who make all this happen, their selfless love encouraged me to pursue my dreams and become the person I want to be. This journey would not have been possible without them, and I dedicate this milestone to them.

Rui Zhang, Gothenburg, July, 2019

Abbreviations

TSV Through Silicon Via

CTE Coefficient of Thermal Expansion

DOE Design of Experiments

EMC Epoxy Molding Compound

FEA Finite Element Analysis

FPC Fingerprint Cards AB

JEDEC Joint Electron Device Engineering Council

BGA Ball Grid Array

LGA Land Grid Array

PCB Printed Circuit Board

OEM Original Equipment Manufacturer

OSAT Outsourced Semiconductor Assembly and Test

uHAST Unbiased Highly Accelerated Temperature and Humidity Stress Test

HTSL High Temperature Storage Life

RDL Redistribution Layer

Ridge The high section of a fingerprint

SMF Solder Mask Face

UBM Under Bump Metallization

Stack-up All the materials of a sensor package

Valley The low section of a fingerprint

Contents

List of Figures **xiii**

List of Tables **xv**

1 Introduction **1**
1.1 Background . . . 1
1.2 Challenge Description . . . 2
1.3 Aim . . . 2
1.4 Scope . . . 3

2 Theory **5**
2.1 The Capacitive Fingerprint Sensing Technology . . . 5
2.2 The Fingerprint Sensor Module . . . 6
2.3 Through Silicon Via (TSV) Technology . . . 7
2.4 The Packaging Process of the TSV Die and the Process Improvement 9
2.4.1 Package Stackup-1 . . . 11
2.4.2 Package Stackup 2 . . . 12
2.5 The Reliability and Qualification Tests . . . 13
2.5.1 High Temperature Storage Life . . . 14
2.5.2 Preconditioning . . . 15
2.5.3 Temperature Cycling . . . 15
2.5.4 Unbiased Highly Accelerated Temperature and Humidity Stress Test . . . 16

3 Methods **17**
3.1 Design of Experiments . . . 17
3.1.1 Design of Experiment Methodology . . . 17
3.1.2 Design of the Fingerprint Sensor Package . . . 17
3.2 Warpage Simulation . . . 21
3.2.1 Warpage Behavior and the Theoretical Calculation . . . 21
3.2.2 Calculation Principle of the Simulation in COMSOL Multiphysics . . . 21
3.3 Bending simulation . . . 25
3.3.1 Industrial Standard of Bending Simulation for Fingerprint Sensor Package . . . 25
3.4 Experimental Verification Test . . . 27

4 Results **29**
4.1 Results of Warpage simulation 29
4.1.1 Reference Package 29
4.1.2 DOE Study of the New Package Stackup-2 30
4.2 Results of Bending Simulation 31
4.2.1 Reference Package 31
4.2.2 DOE Study of the New Package Stackup-2 32

5 Discussion and Future Work **37**
5.1 Discussion of the Results of the Warpage Simulation 37
5.2 Discussion of the Results of the Bending Simulation 37
5.3 Future Work 38

Bibliography **41**

List of Figures

2.1 Capacitive sensing principle: The measured capacitances varies with the ridges and valleys of the fingerprint [2] 6
2.2 Fingerprint sensor module 7
2.3 The cross-section image and description of a typical wire bond fingerprint sensor package 7
2.4 The layout and the cross-section of the TSVs in one of FPC's Fingerprint sensors 8
2.5 SEM cross-section image of a polymer filled TSV structure [7] 9
2.6 The cross-section image and description of a TSV based fingerprint sensor package 9
2.7 Typical process of single chip packaging 10
2.8 Schematics of the TSV die manufacturing and the packaging process 10
2.9 Schematic of one process improvement of the TSV based package stackup 12
2.10 Schematic of one process improvement of the TSV based package stackup 13
2.11 Flowchart of the qualification process of a new fingerprint sensor package in FPC 14

3.1 The stackup of the reference fingerprint sensor package 18
3.2 The 2D drawing of the reference TSV based fingerprint package[16] . 18
3.3 The Stackup-1 of the upgraded fingerprint sensor package 19
3.4 The Stackup-2 of the upgraded fingerprint sensor package 19
3.5 The cross section of the CAD model of the reference package and the new package Stackup-2 22
3.6 The fixed constraint of the CAD model for the Solid Mechanics physics in COMSOL 22
3.7 The location of the heat source for the Heat Transfer in Solids in COMSOL 23
3.8 The warpage calculation model of the fingerprint sensor package . . . 23
3.9 The front face of the package where the maxima and minima deformation value are picked 24
3.10 The left and right edges on the front face of the package where the maxima and minima value are picked 24
3.11 Position of test package and the bending test setup 26
3.12 The CAD model of the bending simulation 26

4.1 The surface displacement plot of the reference package 29
4.2 The plots of the surface displacement of the DOE study of the new Stackup-2 30
4.3 The comparison of the warpage between the reference package and DOE variants of the new Stackup-2 31
4.4 The plot of the von Mises stress of the reference package under the ultimate load (44N) 32
4.5 The plot of the total displacement of the reference package under the ultimate load (44N) 32
4.6 The plots of Von Mises stress of the DOE variants (F=44N) 33
4.7 The plots of the total displacement of the DOE variants (F=44N) . . 34
4.8 The comparison of the von Mises stress between the reference package and DOE variants (F=44N) 34
4.9 The comparison of the total displacement between the reference package and DOE variants (F=44N) 35
4.10 The von Mises stress plot of the bending simulation under a set of loads 36
4.11 The total displacement plot of the bending simulation under a set of loads 36

List of Tables

3.1 The parameters of the DOE variants of the package Stackup-2 20
3.2 List of materials used in the package model and the material properties 20
3.3 Load for the bending simulation 27

4.1 The warpage deformation values of the DOE study 30
4.2 The von Mises stress and the total displacement value of the bending simulation 33

1
Introduction

Fingerprints is recognized as the oldest known biometric recognition method, since fingerprint has very high level of uniqueness and can stays almost a permanent pattern during the whole lifespan of a person. In ancient times, the fingerprint recognition was done with paper and ink, and then the identification has evolved over time along with the publication of the anatomical features, details and the classifications of the fingerprint were proposed in the 18th and 19th century [1]. Nowadays, the fingerprints can be used in a smarter way, which is it can be captured by the so-called fingerprint sensor or fingerprint scanner and then processed by the matching algorithms in the electronic terminal equipment.

1.1 Background

Fingerprint sensors were widely used as the main user recognition and identification portal in consumer electronic products, such as smart phones, tablets and laptops. Generally, the fingerprint sensors are classified as swipe sensors and touch sensors based on the mode of operation. The touch sensors are considered as the better solution since it has a faster authentication speed and it is more convenient to use from the user's perspective. Optical sensors, capacitive sensors, ultrasonic sensors, thermal sensors and pressure sensitive sensors are the main five type of fingerprint sensors, the capacitive sensors are the one that are most commonly used in the handheld terminal equipment like smartphones since it has a very low power consumption, a higher image quality and a low cost comparing with other technical solutions [2].

With the trend of thinner body and larger display of the current smartphone design, the components and modules inside the phone should be shrunken and thinned down. Fingerprint sensor package, as the main component of the fingerprint sensor module, is inevitable to be reduced in terms of thickness and size to create more room for the flexible printed circuit board (PCB) of the liquid crystal display (LCD) screen and USB Type-C connector. Prior to the fingerprint sensor integrated into the display, an ultra-thin capacitive fingerprint sensor module becomes a solution to achieve the larger display design goal, as well as being able to place the sensor on the front panel of the smartphone without occupying big space. Also, it is widely accepted that the placement of the fingerprint senor on the front side is more convenient for the users comparing to put it on the back or side of the phone, this make development of the new ultra-thin capacitive fingerprint senor more promising.

1.2 Challenge Description

The capacitive fingerprint sensors are the mainstream technology in the fingerprint sensor application, especially in the smartphone industry. The capacitive fingerprint sensors are packaged in different types of protective encapsulations such Land Grid Array (LGA), a packing technology with a matrix of solder pads on the underside of the package and optional customized coating on the upside. The silicon sensor die connects the solder pads for electrical connection, the solder pads underneath connects the sensor to the PCB of the smartphone. Wire bond is a conventional interconnection between the silicon sensor die and the solder pads, it was a reliable interconnection method, but it will increase the entire package thickness since more packaging materials such as Epoxy Mold Compound (EMC) are used to cover the sensor die and the bonding wire for protection. Through silicon via (TSV) is another interconnection method, it provides advantages of shortening interconnection paths and thinner package size, which could generate a high image quality of the fingerprints.

In this thesis project, an improvement of the microelectronics packaging process for the TSV die is introduced. By applying this process improvement, the thickness of the package can be further reduced, thus the TSV based fingerprint sensor package with an ultra-thin thickness can be produced. However, before the new package goes to mass production, its design need to be verified by passing the qualification standards both internally in FPC and phone OEMs [3]. The demand of the reliability of the fingerprint senor is very high, the fingerprint sensor modules need to proper functioning longer than the service life of the products which it will be integrated into. The entire qualification process is time-consuming and has a high cost. In general, different lots of engineering samples of the fingerprint sensor package and modules need to be produced and then send to corresponding Outsourced Semiconductor Assembly and Test companies (OSATs) for different experimental test, the whole process could take several months. Thus, packaging engineers in FPC and OSATs are always committed to develop simpler and cost-effective test methods, one of the common way that used in FPC is to conduct a finite element analysis (FEA) to verify the design of the fingerprint sensor package along with a design of experiments (DOE) study to find out the optimal design parameters. Most of the proven FEA simulations have been used for addressing the traditional chip-package interactions, and have therefore mostly modeled physical deformations, such as die cracking, package delaminating or fracturing [4]. Comparing to the experimental test, the FEA method is simpler, quite reliable and most importantly, have a short iteration period.

1.3 Aim

The new ultra-thin TSV based fingerprint sensor package has a different stack-up and material composition comparing with the current package design. During the molding process the TSV sensor die need to pass through a high temperature

environment where warpage could be induced which is mainly attributed to the Coefficient of Thermal Expansion (CTE) mismatch of the constituent materials. In addition, the fingerprint sensor package is very vulnerable under high mechanical pressure and unpredicted collisions, as a result, a comprehensive study of the mechanical behavior of the new package stack-up need to be conducted [3].

The aim of the thesis is to analyse the reliability of the TSV based ultra-thin fingerprint sensor package before it can go to the mass production. A well-functioning TSV based fingerprint sensor package was introduced as a reference. Corresponding FEA simulations will be processed, specifically, warpage simulations, bending simulations or ball drop simulations will be conducted upon the general wire bonding solution and the TSV based solution.

A DOE study will also be done along with the FEA simulation in order to better evaluate the performance and reliability of the newly developed ultra-thin fingerprint sensor package and find out the optimal design parameters. An optimal design can be generated based on the DOE study, which can not only pass all the qualification standards but also has a minimum thickness.

1.4 Scope

This thesis project is a customer research project that focus on the development and reliability study of a TSV based ultra-thin fingerprint sensor package in FPC due to the improvement of the packaging technology. A reference TSV based fingerprint sensor package produced following the previous manufacturing process is introduced as a design reference, this reference sensor package has passed all the industrial reliability qualification tests and has been widely used by many well-known dominating phone OEMs in China.

Regarding the design of the package stack-up, the geometry of the new TSV based fingerprint sensor package generally follows the reference package in terms of the width and the length of the package layout, the thickness of the coating and the location of the sensor die. The general constituent materials of the sensor package will be shared.

2

Theory

This chapter aims to address the theoretical knowledge and background that is required to understand the thesis topic and the relevant technologies. The principle of the capacitive fingerprint sensor is described, the packaging technologies such as wire bond method, the TSV based package and the process improvement of the package molding process are also presented by demonstrating the package Stackup structures and the process schematics. Furthermore, the relevant qualification standards and tests of the Joint Electron Device Engineering Council (JEDEC) are introduced, such as High Temperature Storage Life test, Preconditioning test, Unbiased Highly Accelerated Temperature and Humidity Stress test and the Temperature Cycling test.

2.1 The Capacitive Fingerprint Sensing Technology

A fingerprint sensor is an electronic device which is used to capture a digital image of the fingerprint. There are five different type of fingerprint sensors, which are optical sensors, active capacitive sensors, thermal and active thermal sensors, ultrasonic sensors and pressure sensitive sensors. The active capacitive sensor is the winner for the smartphone application since it highly meets the requirements in terms of the cost, power efficiency, size, convenience and technology maturity [2]. In this thesis, the study is conducted within the active capacitive fingerprint sensor.

Capacitance represents a physical entity's ability to hold electrical charge. In a capacitive fingerprint sensor, the image capturing area contains an array of small pixel capacitor plates. These thousands of small pixel capacitor plates have the same function as one plate of the parallel-plate capacitor, while the electrically conductive dermal layer of the finger act as the other plate of the parallel-plate capacitor. As shown in Figure 2.1, when the finger placing on the sensing area of the senor, the electrical charges are created. The distribution of the electrical charges makes up a pattern because of the surface of the finger consists of ridges and valleys. The pattern of the electrical charges is digitized by the digital control logic and then sent to the connected microprocessor for further analysis and processing.

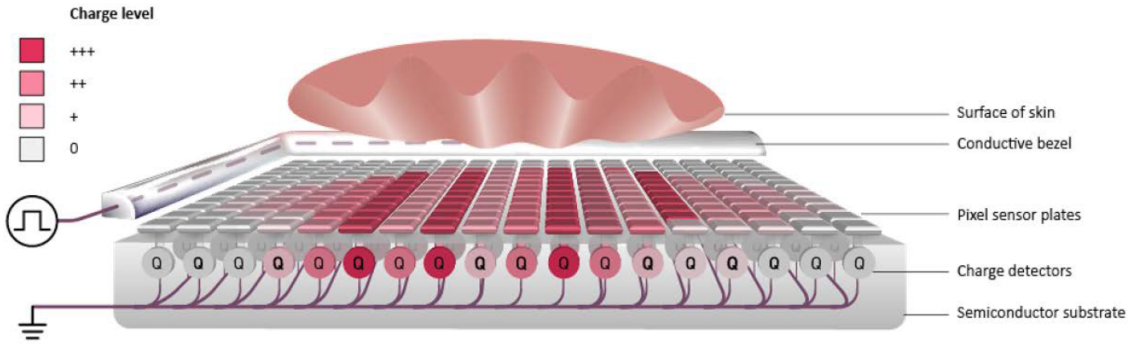

Figure 2.1: Capacitive sensing principle: The measured capacitances varies with the ridges and valleys of the fingerprint [2]

The Capacitance of the finger-senor composed parallel-plate capacitor can be expressed as:

$$C = \varepsilon_\gamma \varepsilon_0 \frac{A}{d} \tag{2.1}$$

Where C is the capacitance, ε_γ is the dielectric constant (relative permittivity), ε_0 is the dielectric permittivity of vacuum, A is the overlapping area of the two opposing plates and d is the distance between the plates. Based on Equation 2.1 , a conclusion can be drawn that a shorter distance between the two capacitor plates and a higher permittivity of the materials in between could cause a higher capacitance.

Comparing to other fingerprint identification technologies, the active capacitive fingerprint sensor has a very high security performance, it cannot be fooled by a high-quality photograph since the capacitive sensor relies on the physical presence of a human finger which has the ridges and valleys to form an electrical charge pattern. There are other benefits by using the active capacitive fingerprint sensor, e.g., it has lower power consumption and cost, it is also very compact which enable the product designer to integrate the fingerprint sensor into the portable devices (a very important factor in the smartphone design considerations).

2.2 The Fingerprint Sensor Module

The fingerprint sensor module is a fingerprint sensor package integrated with the complete physical enclosure and accessories, such as substrate, flexible PCB, companion chip, passives, bezel and a board-to-board connector, as shown in Figure 2.2. The fingerprint sensor module can be directly integrated into an electronic terminal product, for example a smartphone or a tablet.

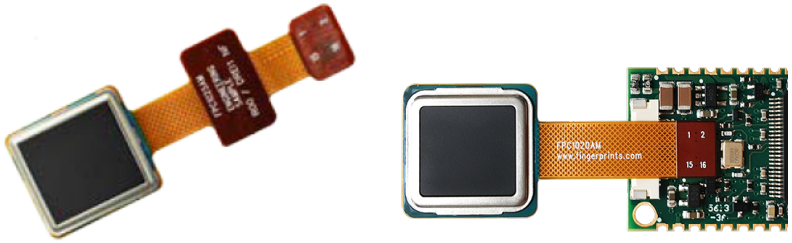

Figure 2.2: Fingerprint sensor module

The fingerprint sensor package is the major component of the module. Generally, it consists of a fingerprint sensor die, a substrate, the EMC encapsulation and coatings on the front side. The fingerprint sensor die is a very thin piece of sensitive silicon, it need to be protected and interconnected to external circuits. Thus, a fingerprint sensor package demands provision of mechanical protection, power supply, cooling, and electric and mechanical connection of microelectronics chips and elements to the outside worlds while minimizing the influence on their electrical performance [5].

The general method to achieve the electrical interconnection between the silicon sensor die and external circuits, for example the substrate, is by using the wire bond technology. As we can see in Figure 2.3, the silicon sensor die is attached on the PCB substrate with a layer of die attach film in between, gold wires are connected the bond pads of the silicon sensor die and the PCB substrate for the electrical interconnection. The gold wires are encapsulated by the EMC material to avoid the external physical damage. Wire bonding technology plays a very important role in the microelectronics engineering for its maturity, simple technique, low cost, and strong applicability, and it is still in developing [5].

Figure 2.3: The cross-section image and description of a typical wire bond fingerprint sensor package

2.3 Through Silicon Via (TSV) Technology

Through silicon via is a type of via connection which completely passes through a silicon die or wafer, it is another major way for electrical interconnection between the silicon sensor die and the substrate. Compared with wire bond interconnections, TSV technology has many advantages, it can shorten the length of the interconnections, it also enables a higher communication speed, a lower power consumption and

have the possibility to contain a huge number of interconnections in a limit space [6]. As shown in Figure 2.4, the TSVs are usually located in the end of the silicon die for interconnections.

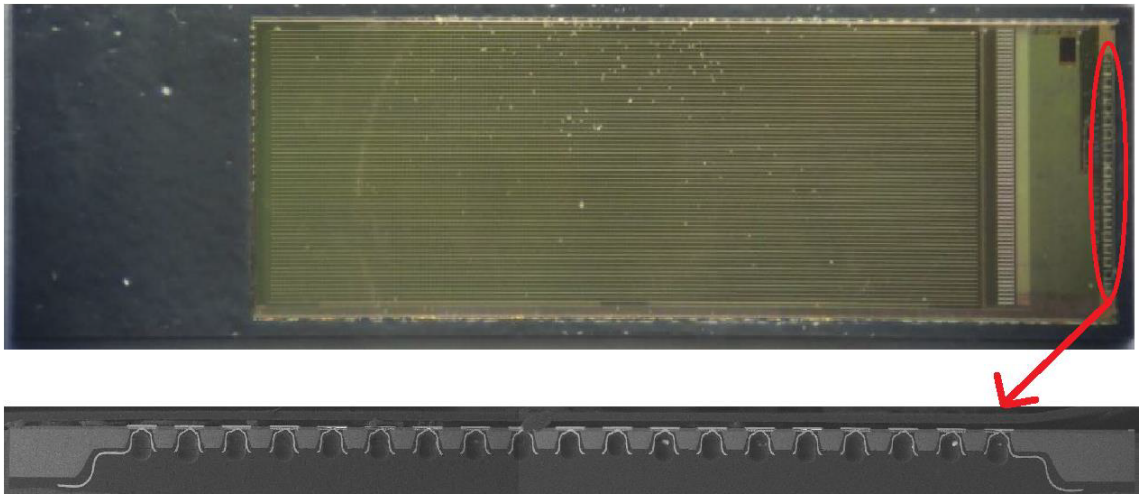

Figure 2.4: The layout and the cross-section of the TSVs in one of FPC's Fingerprint sensors

The types of the TSV structure can be divide by the filled materials during the manufacturing process. Polymer, Copper are the two main filled materials. Another classification method is based on the process sequence of the TSV structure during the whole manufacturing, via last TSV and via first TSV are the two types of the TSV [6]. Via last means that the TSV structure is processed after the integrated circuit fabrication. In Fingerprint sensors, the polymer filled via last TSV is used based on considerations. The polymer filled via last TSV structure consists of different parts and different materials, for example, the bond pad, the redistribution layer (RDL), the passivation layer, the solder mask and the trench fill. The bond pad is made of aluminum in general. The redistribution layer is used for the external connection between the silicon sensor die and the pads on the substrate of the package. The redistribution layer consists of four layers of materials: copper, nickel, titanium and gold, the copper is the major material in the composition [8].

The typical structure of the TSV is shown in the Figure 2.5. As shown in the figure, besides the redistribution layer (RDL), a dielectric polymer layer, so-called passivation layer is created to separate the silicon die and the RDL layer. On the other side of the RDL layer, a solder mask layer is added with the same function as the dielectric polymer layer, which will provide protection to the RDL metallization layer from inside. The TSV structure is filled with polymers as the trench fill, which increases the mechanical strength and performance of the TSV structure [9].

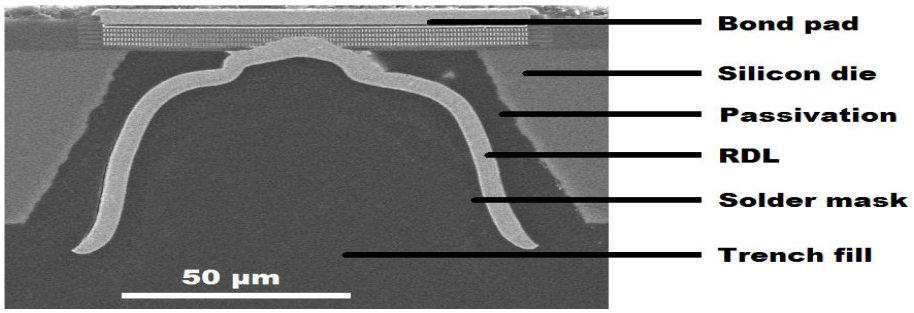

Figure 2.5: SEM cross-section image of a polymer filled TSV structure [7]

The package design of the TSV die is quite different with the normal silicon die, since the TSV die has the internal interconnection which enable it to have more packaging flexibility and options. The general package of a TSV die is shown in Figure 2.6. By applying the TSV structure in fingerprint sensor die, one prominent advantage is the over molding thickness on the top of the silicon sensor die can be reduced comparing to the general wire bond package in Figure 2.3, thus the distance between the sensor die and the finger can be reduced in the actual application, a shorten distance will lead a higher image quality and a thinner package will also give the phone designers more flexibility to put other modules into their designs.

Figure 2.6: The cross-section image and description of a TSV based fingerprint sensor package

2.4 The Packaging Process of the TSV Die and the Process Improvement

A typical process of a single chip packaging is shown in Figure 2.7, including silicon die dicing, die mounting on the substrate with die attach glue, create bonding connection between the die and the substrate, make encapsulation molding with EMC material, add wafer coating, marking, leads or solder ball fabrication and unification of the final product [5].

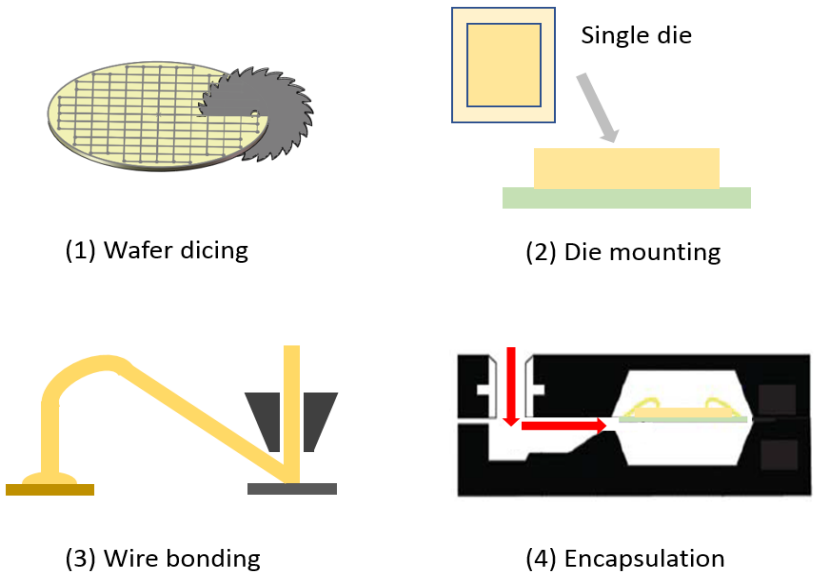

Figure 2.7: Typical process of single chip packaging

The packaging process of a TSV silicon die is basically divided into two phases, in this thesis, the TSV manufacturing and the package assembly. During this two phases, two OSATs are involved: OSAT A, which produce the TSV die and conduct the Open/Short (O/S) test for functional verification, then the verified TSV die will transfer to OSAT B for LGA package assembly. The general process is demonstrated as in Figure 2.8.

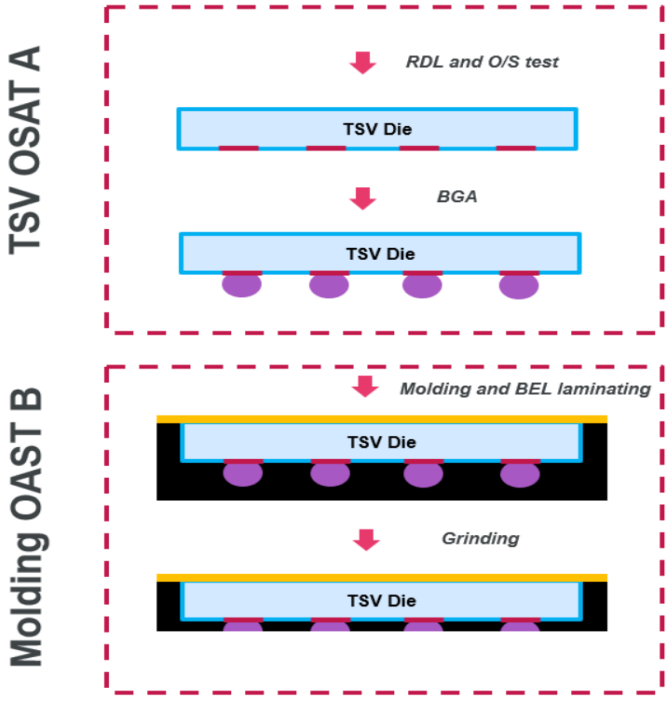

Figure 2.8: Schematics of the TSV die manufacturing and the packaging process

As we can see in the Figure 2.8, at OSAT A, the TSV die is produced, the RDL layer is added and the finished TSV die need to pass the O/S test before it goes to the next step. The passed TSV tie will go through a Ball Grid Array (BGA) process to add the bonding solder bumps for the external connection. The TSV die from OSAT A then will be shipped to OSAT B for molding process, which will improve the mechanical properties of the package and protect the die from contamination. In this case, the EMC material is selected for the molding. A buffer coating will be added on the top of the TSV die as an insulating and passivation layer in order to improve the package's mechanical performance. The encapsulated package then is shipped for grinding, as shown in Figure 2.8, the bottom of the package is grinded in order to reduce the total thickness and to protrude the solder bumps. In the end, a well encapsulated fingerprint sensor package with EMC material on four sides and the bottom is produced.

In order to further reduce the total thickness of the fingerprint sensor package, the film assisted molding technology was introduced. One film tape on the mold chase will be used as the supporting platform during the film assisted molding process, as a result, a four-sided EMC molding package which have a thinner thickness can be produced. According to the TSV die manufacturing process, two alternative packages based on the new process improvement were created, package 'Stackup-1' and package 'Stackup-2'. These two stackup variants will be illustrated in terms of structure, material and process in the following subsections.

2.4.1 Package Stackup-1

At OSAT A, during the TSV die manufacturing, solder bumps are added on the bottom side of the die after the redistribution layer layout, a BGA based die is generated. Then the die with solder bumps will be grinded and go through a O/S test for functional verification before it going to the package assembly in OSAT B.

At OSAT B, the TSV die will go through the molding process and the final test. In the beginning, the TSV die is placed on a film tape on the mold chase, then the EMC material will be injected for encapsulation. After the molding process, the tape will be released, a four-sided LGA fingerprint sensor package will be formed. Since there is no EMC molding material on the bottom side of the package, the package thickness can be further decreased compared with the general package with EMC molding material both in four sides and the bottom. The flowchart of the process improvement of package Stackup-1 is shown in Figure 2.9.

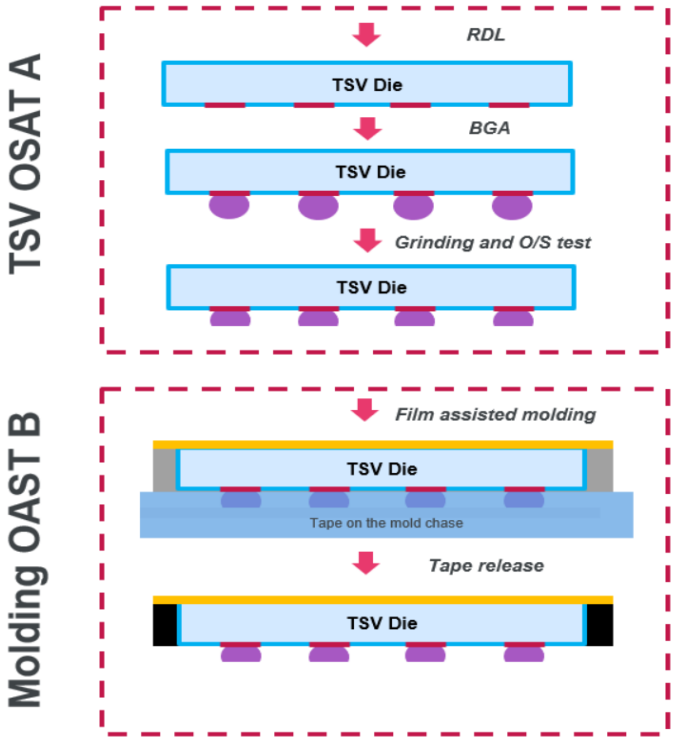

Figure 2.9: Schematic of one process improvement of the TSV based package stackup

2.4.2 Package Stackup 2

The solder bumps can be removed during the TSV die manufacturing process, since the package can be integrated in the phone with modules or PCB by using other connecting techniques. By omitting the BGA process in the manufacturing of Stackup-1, a new LGA package stackup could be fabricated. The flowchart of the process improvement is shown in Figure 2.10.

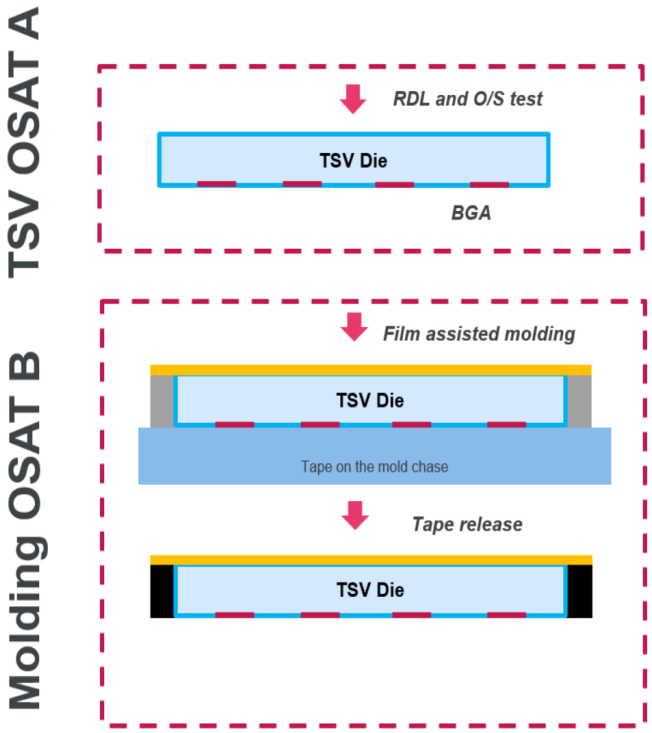

Figure 2.10: Schematic of one process improvement of the TSV based package stackup

As shown in Figure 2.10, the entire die manufacturing and package assembly process is much simpler than fabrication of the general package and the package 'Stackup-1'. Theoretically, the process improvement could reduce the cost of the production, and the resulted LGA package has a thinner thickness, which could meet the design requirements of the new trend and demand of the smartphone industry.

2.5 The Reliability and Qualification Tests

Smartphones are portable consumer electronic products which should be characterized as high-volume and low-cost devices. Thus, the phone OEMs have to make sure its products could pass the industrial standardized reliability test and achieve a high quality and productivity at the same time. Reliability is defined as the probability that a product will perform its designed function under all the operating conditions that could encountered for a specified period. Products that passed the reliability test not only could bring a perceived quality, but also get a high customer satisfaction. In FPC, the reliability verification of the fingerprint sensors is defined following the JEDEC standards [10].

The flowchart of the qualification process for a new developed fingerprint sensor package is shown in Figure 2.11. Generally, a fingerprint sensor contains a silicon sensor die and a companion chip, thus, in order to avoid the affection of the difference among each production lots, 3 non-consecutive lots sensor wafer and another 3

non-consecutive lots companion chip wafers are selected and created 3 even lots of fingerprint sensor packages. There are in total 225 package engineering samples are built, according to the FPC's qualification standard, 75 engineering samples (25 of each lot) are picked and going through different kinds of qualification tests which follows JEDEC standards and FPC's internal requirements. All these 225 engineering samples need to pass the final test and the scanning acoustic tomography (SAT) in order to make sure that the integrated circuits are fully functioning without failure damage, an Open/Short test is included to find out the open or short signals. SAT scan is a general way to identify whether a package has a mechanical defect such as delamination by probing the ultrasonic sound waves on it.

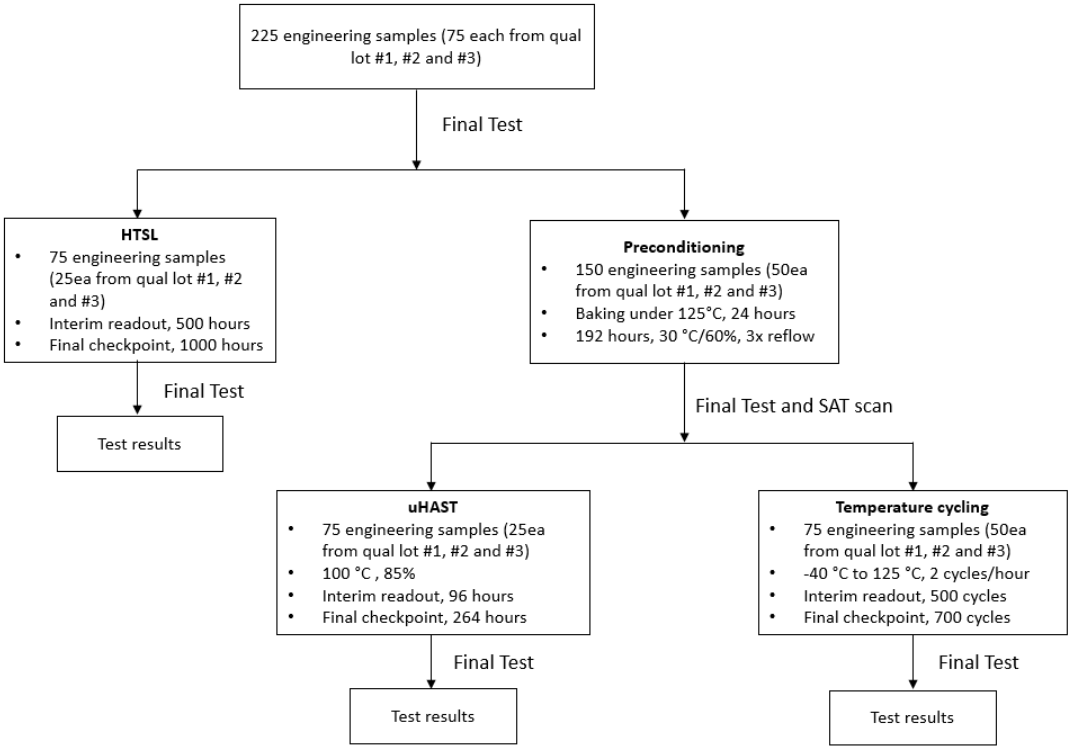

Figure 2.11: Flowchart of the qualification process of a new fingerprint sensor package in FPC

According to the JEDEC standards, four types of tests are generally processed, which is high temperature storage life test (HTSL), unbiased highly accelerated temperature and humidity stress test (uHAST), preconditioning test and temperature cycling test.

2.5.1 High Temperature Storage Life

The high temperature storage life test is used to determine the effects of the time, temperature under certain storage conditions [11]. During the HTSL test, the accelerated stress temperatures are usually applied. A temperature controllable chamber is the main apparatus of the HTSL test. In FPC's test scheme, the fingerprint sensor

engineering samples are subjected to a continuous storage temperature of 150°C for 10000 hours, which is a typical duration for the certain temperature. The interim and the final electrical test measurement are conducted after 500 hours and when the test is completed. After the HTSL test, all the engineering samples will go through another final test, and the test result shall be consistent as the final test prior to the HTSL test. An engineering sample will be considered a high temperature storage failure if the parametric limits are exceeded, the mechanical damage, such as cracking, chipping or breaking of the samples will also be checked [11]. To be qualified, all the engineering samples need to pass the Open/Short test and no mechanical damage is found.

2.5.2 Preconditioning

The remaining 150 engineering samples is going through a preconditioning test before it goes to the uHAST test and the temperature cycling test in order to simulate the floor life of the fingerprint sensor package during the module assembly process [12]. During the preconditioning test, all the engineering samples are subjected to processes within a baking oven, a moisture soaking chamber and solder reflow equipment. Initially, all the 150 engineering samples go through a baking process in the baking oven under 125°C for 24 hours with the aim to remove all the moistures inside. Then the samples transfer to a moisture soak chamber under 30°C and a relative humidity of 60% for 192 hours. Finally, the samples go through the solder reflow for 3 times in order to simulate the module assembly process. All the 150 engineering samples need to pass a final test and SAT scanning to verify if it is still well functioning when the preconditioning test is completed. The 150 engineering samples are then divided, which half goes through the TC test and the other half goes through the uHAST test.

2.5.3 Temperature Cycling

Temperature cycling test is conducted in order to determine the ability of the package component and the TSV interconnections to withstand mechanical stresses and strains induced by the alternating extreme temperatures during the temperature cycling [13]. Physical or electrical damage could be caused from the mechanical stresses during the temperature cycling which will generate a failure problem. The root cause of the mechanical stresses during the temperature cycling is the difference of the material properties such as the coefficient of thermal expansion.

In FPC's qualification standard, half of the fingerprint sensor engineering samples that passed the preconditioning are subjected to a specified cycling temperature between -40°C and 125°C for 700 cycles, each cycle takes half an hour and the interim readout is conducted after 500 cycles. All the engineering samples need to go through a final test and an Open/Short test to be qualified when the temperature cycling test is completed.

2.5.4 Unbiased Highly Accelerated Temperature and Humidity Stress Test

After preconditioning, the other half of the engineering samples go through a uHAST in order to evaluate the reliability of the fingerprint sensor package in humid environments. During the test, all the engineering samples will be placed into a pressure chamber that capable of maintaining an environment which has 110°C and 85% relative humidity for 264 hours, the interim readout is at 96 hours [14]. The test is highly accelerated since the combination of the high pressure and high humidity enhance the penetration of the moisture through the encapsulation material. All the engineering samples need to go through a final test and an Open/Short test to be qualified when the uHAST test is completed.

3
Methods

3.1 Design of Experiments

3.1.1 Design of Experiment Methodology

A DOE study was performed in order to find out the optimized design parameters of the new package stackup based on the packaging process improvement. The DOE study, also known as design of experiments, was initially developed to systematically conduct a series of experimental tests to analyze the impact of input factors under certain conditions that are hypothesized to reflect the output factors [15]. In general, by applying the DOE study, researchers can predict the outcome or output variables by introducing changes of the input variables. During the experimental design process, some input variables are assumed as constant to prevent external factors from affecting the results, only the control variables have the impact on the experimental results.

In this thesis, the geometry of the package design is selected as the control variable, the constituent materials of the package and TSV silicon die is not taken into account since the materials are predetermined by FPC and will also be shared by the current general design and the new package stackups. Regarding the design and the geometry of the new package stackup, the overall layout is determined as a constant, e.g., the length, width and the radius at the ends of the package, the position of the silicon die in the package is also fixed. The total thickness of the package and the die thickness are selected as the design input variables which affects the experimental results.

A set of new package stackup variants with different combinations of total package thickness and die thickness are created, by conducting the DOE study and FEA simulation, the reliability of new package stackups can be evaluated. The optimized design parameters, e.g., the thickness of each layer of the materials can be determined.

3.1.2 Design of the Fingerprint Sensor Package

In order to verify the reliability of the newly developed TSV based ultra-thin fingerprint sensor package with only four sided EMC molding material and make the comparison with the standard package, a reference TSV fingerprint senor package produced based on the general packaging method in Figure 2.8 is introduced. This

reference fingerprint sensor package was already qualified for mass production and has been widely used in many smartphones that made by Chinese phone OEMs. The stackup of the reference fingerprint sensor package was designed following the design guidelines of FPC and the requirements of the phone OEMs, the stackup is shown in Figure 3.1.

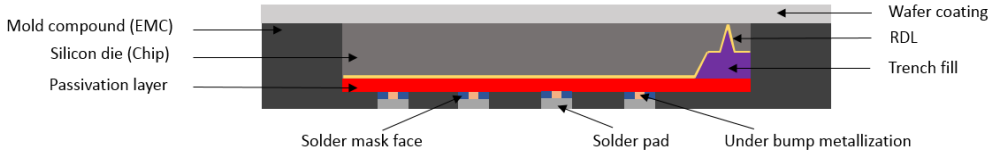

Figure 3.1: The stackup of the reference fingerprint sensor package

As shown in Figure 3.1, the TSV die is encapsulated with EMC material on both sides and the bottom, the external connection is achieved via RDL and the under bump metallization (UBM). Solder pads are added in order to increase the contact face for better connection.

The 2D engineering drawing of the package is shown in Figure 3.2. In the 2D package drawing, the layout, the structure and the basic dimensions are demonstrated. As shown in Figure 3.2, the overall size is 15,64 mm × 4,74mm (fixed), the die size is 10,77mm × 3,54mm (fixed). The position of the die is also fixed. This dimension of the package layout will be uses as the standard design parameters for all the packages in the thesis project.

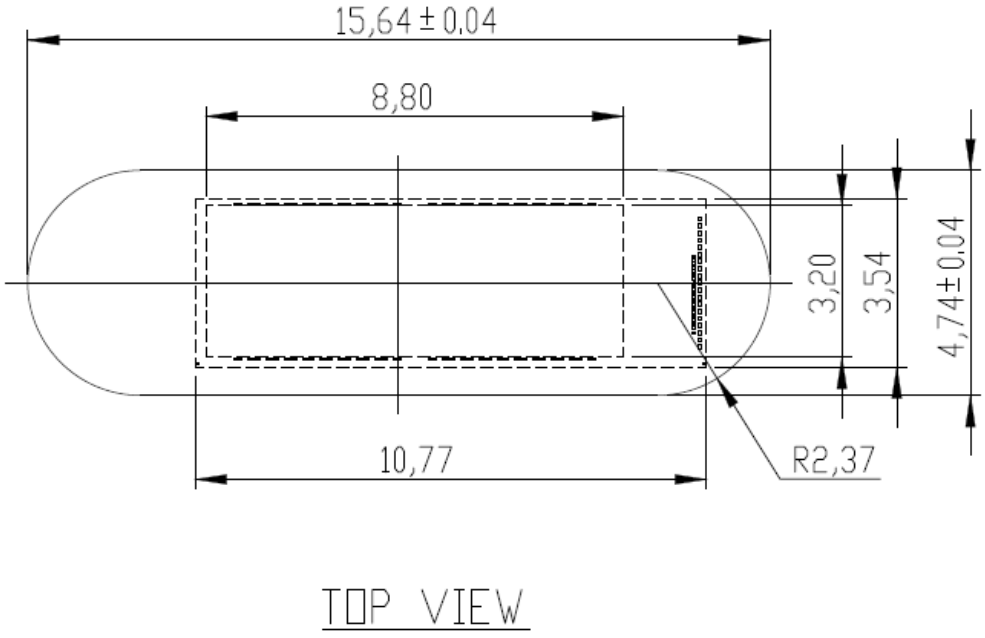

Figure 3.2: The 2D drawing of the reference TSV based fingerprint package[16]

By introducing the film assisted molding technology, two new stackups are created. Stackup-1 which is a BGA package with only EMC on sides that produced based

on process improvement in Figure 2.9. As shown in Figure 3.3, the thickness of the package Stackup-1 is decreased by removing the EMC molding material on the bottom side of the package.

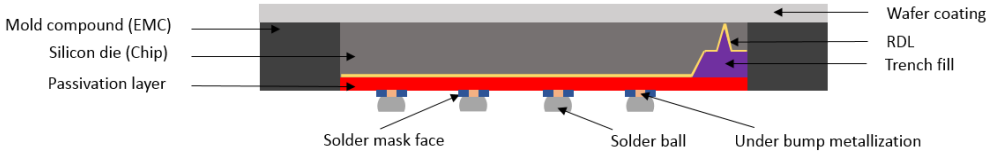

Figure 3.3: The Stackup-1 of the upgraded fingerprint sensor package

Stackup-2 is a simplified version of Stackup-1, designed by omitting the BGA process and applying the UBM as the external contact pads which is produced based on the process improvement in Figure 2.10. The package lamination is shown in Figure 3.4.

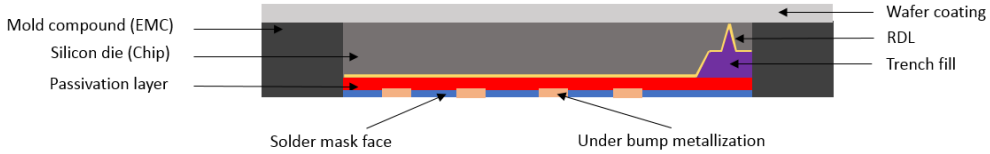

Figure 3.4: The Stackup-2 of the upgraded fingerprint sensor package

By comparing of the lamination of package Stackup-1 and package Stackup-2, the main difference of the two stackups are the external connection structures. Unlike the package Stackup-2, the silicon die of the package Stackup-1 went through a BGA process after the RDL process, extra solder bumps are added beneath the UBM, thus, package Stackup-2 is thinner than the package Stackup-1 if both of them have the same die thickness. On the other hand, the enlarged UBM area could act as the solder pads for external connections. Both stackups were sent to phone OEMs for evaluation, Stackup-2 of the upgraded fingerprint sensor package was selected for further development and verification after serious consideration in terms of thickness, cost and design aspects.

A DOE study of the Stackup-2 of the upgraded fingerprint sensor package is created. Since the new Stackup-2 has the same layout as the reference fingerprint sensor package, as mentioned in chapter 3.1.1, the total thickness and the thickness of the sensor die are selected as the design input variables. The thickness of the PI coating, the passivation layer and the solder mask face stay constant. Based on the design requirements of the phone OEMs, the total thickness of the new package stackup are set to 270μm, 240μm, 220μm and 200μm, the die thickness is changed respectively. The detail dimensions is shown in the Table 3.1.

Table 3.1: The parameters of the DOE variants of the package Stackup-2

Stackup-2	Total Thickness	Die Thickness
DOE1	$270\mu m$	$200\mu m$
DOE2	240 μm	170 μm
DOE3	220 μm	150 μm
DOE4	200 μm	130 μm

The reference fingerprint sensor package and the new stackups are using the same materials, the data of its properties is mainly obtained from FPC's internal laboratory and the OSATs. Some common materials, e.g., silicon, its material property could be obtained from COMSOL directly. In order to simplify the modeling process, mini structures which almost have no effect on the reliability simulation are neglected, in this case, the TSV structure is neglected. The materials and its properties of the remaining structure of the fingerprint sensor package are shown in Table 3.2.

Table 3.2: List of materials used in the package model and the material properties

Materials	Heat capacity at constant pressure [J/kgK]	Density/ρ [kg/m^3]	Thermal conductivity [W/(mK)]	CTE [1/K]	Young's modulus [GPa]	Poisson's ratio	Data source
Wafer Coating	1100	1300	0.15	34E-6	2.7	0.34	OSAT B
Silicon	700	2329	130	2.6E-6	190	0.28	Comsol
EMC	1100	1300	0.15	7E-6	24	0.25	OSAT B
SMF	1100	1300	0.15	78E-6	4.8	0.4	OSAT B
PA	1100	1300	0.15	78E-6	4.8	0.4	OSAT A
UBM	385	8960	400	17E-6	110	0.35	Comsol

3.2 Warpage Simulation

3.2.1 Warpage Behavior and the Theoretical Calculation

Warpage is a common behavior that happens to a micro-electronic package during the temperature changing production process. The asymmetric layout and mismatch of coefficient of thermal expansion of the composed materials is the main cause of the warpage behavior, it could lead the die cracking, the delamination between different stackup layers [17]. Thus, the warpage is a significant factor for the reliability analysis and the qualification test.

The warpage can be quickly calculated with some thermomechanical analysis software. The package stackup is generally simplified as laminated plates, the analytical expression of the thermal warpage is derived from solving the differential equation based on the elastic mechanics of lamination theory. This method only applies to packages which have very thin silicon, big size or extremely small size, it is not suitable for the general fingerprint sensor packages [17]. The silicon die and the EMC molding material are equivalent to a composite layer based on the lamination theory, but this two part have different material properties and are independent, so, the general lamination simplified method cannot calculate and predict the warpage precisely.

3.2.2 Calculation Principle of the Simulation in COMSOL Multiphysics

The warpage FEA simulation was conducted in COMSOL Multiphysics in order to obtain the thermal deformation of the reference fingerprint sensor package and the package Stackup-2 variants induced by the temperature change during the manufacturing process. The aim of the warpage simulation is to predict the warpage deformation and make a comparison of the new package with the reference package.

The CAD model were created based on the 2D engineering drawing of FPC's one fingerprint sensor, see Figure 3.2. The TSV structure and the trench fill which has little or no effect for the thermal simulation results were neglected in order to simplify the model and the calculation time, the actual CAD model used in the simulation is shown in Figure 3.5. The CAD were created in SolidWorks and then imported to the COMSOL Multiphysics for set up, the material properties were specified based on the date resource from the OSATs, the material of bond pads and UBM were set as copper because it is the element it consists the most of. The silicon and the copper were added directly from the material library in COMSOL Multiphysics. The material properties are shown in Table 3.2. The coupled interfaces in the Multiphysics setup were Solid Mechanics and Heat Transfer in Solids. The heat source and the heat transfer were processed in the Heat Transfer in Solids module, and the result will affect the structure in the Solid Mechanics module.

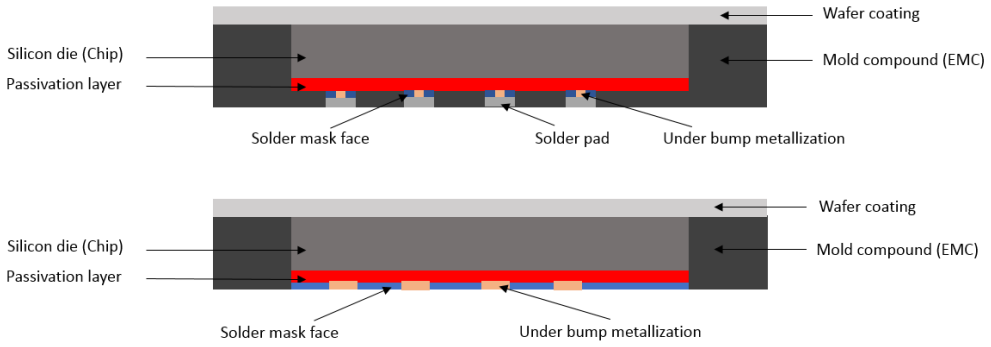

Figure 3.5: The cross section of the CAD model of the reference package and the new package Stackup-2

In the Solid Mechanics physics setup, all the composed materials in the CAD model of the package were specified as linear elastic materials and isotropic materials. The entire CAD model except one solder pad or UBM were set as free, see Figure 3.6, and this single solder pad or UBM on the bottom side of the package was the only fixed constraint, which will offer the most degree of freedoms to the package for deformation upon the heat transfer and temperature cycling.

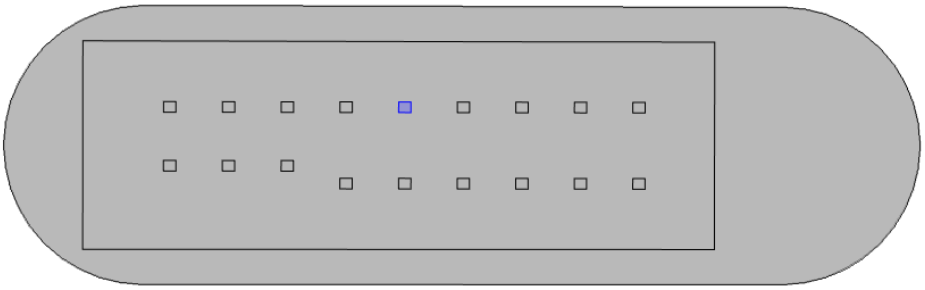

Figure 3.6: The fixed constraint of the CAD model for the Solid Mechanics physics in COMSOL

The entire CAD model was selected as the domain for the heat transfer physics, the initial value of the temperature was set as 200°C, the temperature will drop to 20°C which is the final value. The heat source was applied on the bottom face of the EMC material, see Figure 3.7, and the external surface of the other parts were set as thermal insulation in order to avoid heat diffusion and loss.

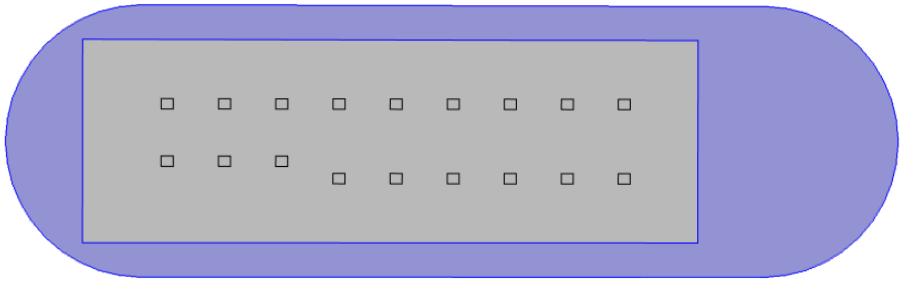

Figure 3.7: The location of the heat source for the Heat Transfer in Solids in COMSOL

After defined the multiphysics of the simulation model, free quad and free triangular mesh with fine mesh size for different parts of the model was created, and the entire setup of the simulation model in COMSOL Multiphysics was completed. After creating the mesh, the next step is to run the simulation for the thermal-mechanical problem. The model is computed with stationary study, the results are solved and saved. In order to get the warpage value of the fingerprint CAD model, the results were postprocessed by adding the derived values.

The fingerprint sensor package could be simplified as a laminated plate, based on the elastic mechanics of lamination theory, the warpage value is derived by subtracting the minimum deformation value from the maximum deformation value on the same layer of the fingerprint sensor package model since it has a laminated structure and each layer of the stackup model has almost the synchronous deformation. As shown in Figure 3.8, the warpage deformation value W is equal to the distance from the vertex point C to the straight line that pass through point A and B.

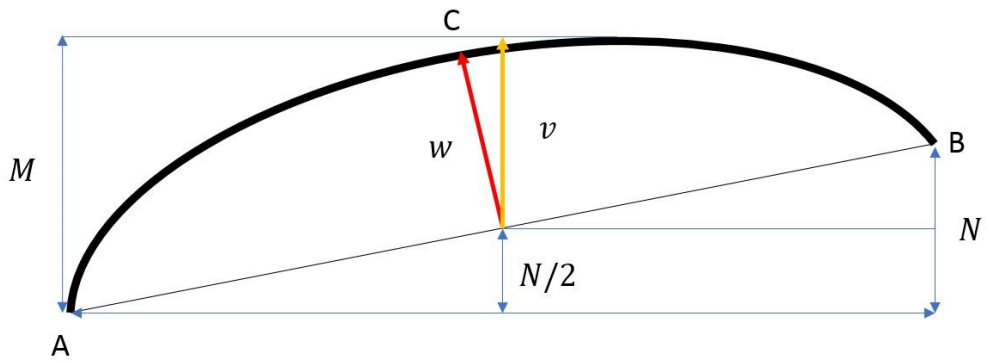

Figure 3.8: The warpage calculation model of the fingerprint sensor package

The simulation is running in an approximate free boundary setting and the only fixed constraint of the solid mechanics physics is one solder pad in the bottom side of the package, in order to accurately calculate the warpage deformation value, the deformation values on the same direction are picked, as shown in Figure 3.8, the

point A which has the minimum deformation value in one end is set as the reference point, the maximum deformation value M of the entire package is obtained in the result data set. The minimum deformation value in the other end (point B) of the package is also obtained in the result date set. The warpage deformation value w is approximately equal to v, where,

$$v = M - \frac{1}{2}N \tag{3.1}$$

Thus, the expression of the warpage deformation w is estimated as,

$$w \approx M - \frac{1}{2}N \tag{3.2}$$

In the definitions of the component, data of the maxima and minima of the deformation value are selected and defined for the warpage calculation. All the maxima and minima values are derived from the top surface of the CAD model. As shown in the Figure 3.9, the maxima deformation value $maxop1(w)$ and minima deformation value $minop1(w)$ on the front face of the package in the direction that perpendicular to the front surface are picked.

Figure 3.9: The front face of the package where the maxima and minima deformation value are picked

The maxima deformation value $maxop2(w)$ and minima deformation value $minop2(w)$ on the left circular edge of the front surface are selected as shown in Figure 3.10. On the right circular edge of the front surface, the maxima deformation value $maxop3(w)$ and minima deformation value $minop3(w)$ are selected.

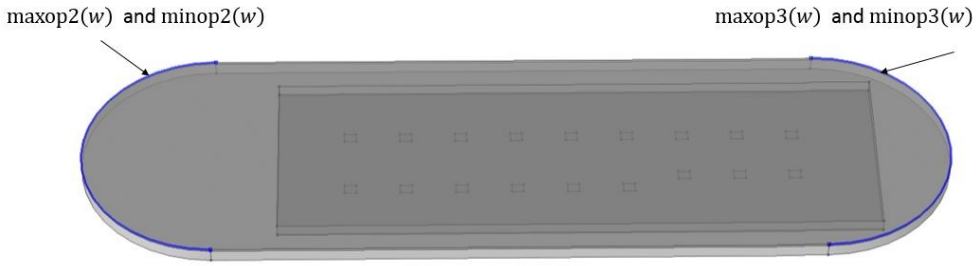

Figure 3.10: The left and right edges on the front face of the package where the maxima and minima value are picked

These variables are created to describe the deformation on the front face by measuring the change in distance between the points where it has the maxima and minima value, based on the Equation 3.2, the expression of the warpage in the COMSOL is defined in the global evaluation of the data postprocessing phase as:

$$w = |maxop1\,(w) - minop1\,(w)| - \frac{1}{2}\,|minop2\,(w) - miniop3\,(w)| \tag{3.3}$$

After running the simulation, the data set is solved and saved in the results, the warpage value w is calculated in the derived values. The deformation value and warpage value are also demonstrated in the plots where the deformation and the heat transfer diffusion is visualized.

3.3 Bending simulation

3.3.1 Industrial Standard of Bending Simulation for Fingerprint Sensor Package

Bending test and simulations of the microelectronic packages are carried out in order to verify the mechanical performance of the TSV based ultra-thin fingerprint sensor. Fingerprint sensors, which serve as the security portal and home button for the smart phones, are one of the microelectronics modules that have a high quality requirement. Therefore, a corresponding reliability study of the mechanical performance is indispensable for evaluation of the new TSV based ultra-thin fingerprint sensor package. According to the JEDEC standards, a ball drop test which followed recommended procedures and conditions need to be conducted. However, it is time-consuming to run a ball drop test, since the package samples from different batches need to be prepared before the test [18]. Thus, FPC and OSATs have developed a simpler and cheaper method to do this, a bend test and simulation is introduced instead of to use the ball drop test for the reliability study. In this thesis, a refined bending simulation was created bases on a 3 roll bending test. In the bending test, the test package is placed on the support blocks and the static pressure is loaded from the block on the top of the test package [19].

The requirements for the support blocks and the pressure loading block is shown in Figure 3.11. The length, width and thickness of the test specimen are specified as w, b and h, the support blocks and the loading block are placed in parallel with each other. The distance (L) between the two supports need to be shorter than the length of the test specimen, the location of the supports is placed near the end of the silicon die in order to simulate the installation and application in the real case. The width of the supports ($B1$ and $B2$) is bigger than the width of the test specimen (b), the hardness of the tip of the support and loading block need to be above the HRc60 of the ISO/DIS 6508-1 standard, and the roughness of the tip of the loading block need be smaller than $1.6\mu m$ of the ISO 468 standard [10].

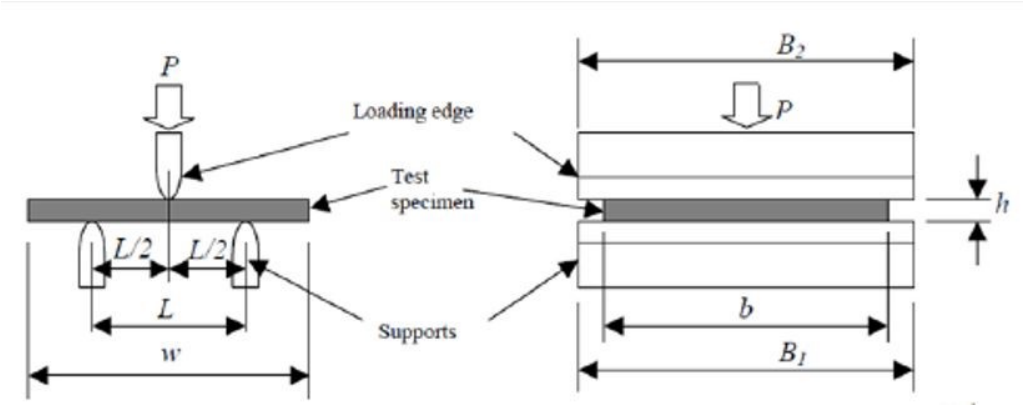

Figure 3.11: Position of test package and the bending test setup

The bending simulation were conducted in the COMSOL Multiphysics, the model setting of the bending simulation was modified according to the requirement of the phone OEMs in terms of the placement of the fingerprint sensor package, the structure of the module, the underneath PCB design and the size of the bezel. The supporting blocks were changed to bigger rectangular supporting blocks in order to simulate the actual installation, the pressure loading block was modified to a semicircular cylinder to achieve simulated effect of the fingerprint touch on the fingerprint senor surface. As shown in Figure 3.12, the load is applied on the top surface of the pressure loading block, the entire CAD model is assumed as the linear elastic material, the bottom surface of the two supporting blocks are fixed constraints, the displacement of the loading block is prescribed in the vertical direction that perpendicular to the surface of the fingerprint package.

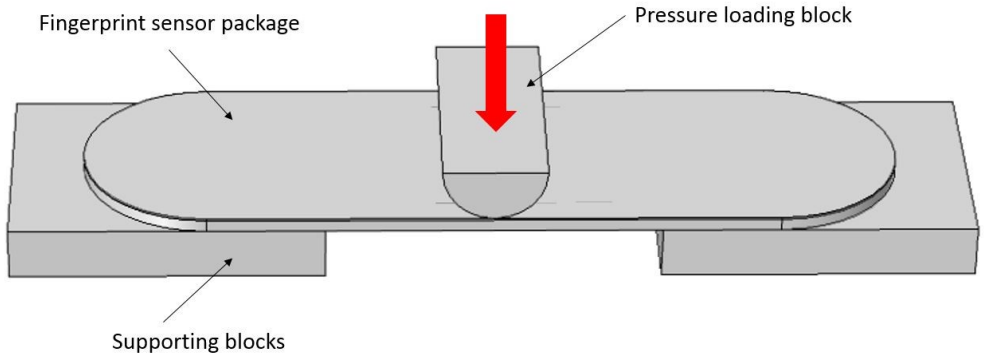

Figure 3.12: The CAD model of the bending simulation

The load is applied starting with 8N and then increased to 44N which is the maximum value that have been approved to be satisfied to the common fingerprints sensor bending simulations. The value table of the load will be specified as shown in Table 3.3. The materials of the fingerprint sensor package in the bending simulation was see as in Table 3.2, metal was used for the supporting blocks and the pressure loading block, the surface of the pressure loading block was pre-defined in terms of the roughness and the hardness.

Table 3.3: Load for the bending simulation

F (N)	p (Pa)	F (N)	p (Pa)	F (N)	p (Pa)
0.5	5208.33	8	833333.33	16	1666666.67
2	208333.33	10	1041666.67	18	1875000
4	416666.67	12	1250000	20	2083333.33
6	625000	14	1458333	44	4583333.37

3.4 Experimental Verification Test

To requalify the new TSV based fingerprint sensor package based on the manufacturing process improvement, the ball drop test is conducted in order to assess the fragility of the package and simulate the shocks that may encounter during the manual and mechanical handling [10]. The other reason for the ball drop test is to rigorously replicate the impact that might occur during the production, distribution, installation, integration and daily use scenarios.

The engineering samples for the ball drop test are selected from 3 different production lots, during the test, the engineering samples are placed on the ball drop test equipment and the iron ball is placed in the certain height [20]. The weight of the iron ball and the dropping height can be changed according to the customers' needs for the qualification standards.

4

Results

4.1 Results of Warpage simulation

Within the warpage simulation in COMSOL, the temperature range in the model physics is increased from room temperature 20°C to 200°C and then drop to the original temperature 20°C. During the post processing process, since the model was parametrized, the warpage values are calculated from the derived values by computing the customized expressions (Equation 3.3). The warpage deformation value can be read directly in the result plots.

4.1.1 Reference Package

The reference package with EMC modeling materials on both sides and the bottom has been verified to meet the qualification standards and already applied in the smartphones. The Total thickness of the reference package is 270μm, the thickness of the silicon die is 170μm and the thickness of the EMC molding material in the bottom of the package is 30μm. The OSTAs have conducted the warpage experimental test for the reference package, the value of the warpage deformation was 47μm. In the thesis, the warpage simulation in COMSOL Multiphysics was processed rigorously based on the experimental data that gathered from OSTAs in terms of the geometry, the material properties and the cycling temperature. The derived value of the warpage deformation in the post processing is 44.67μm, which is very close to the experimental test and thus the setup of the warpage simulation in COMSOL Multiphysics is considered as reliable. The surface displacement plot from the initial warpage simulation in COMSOL is shown in Figure 4.1.

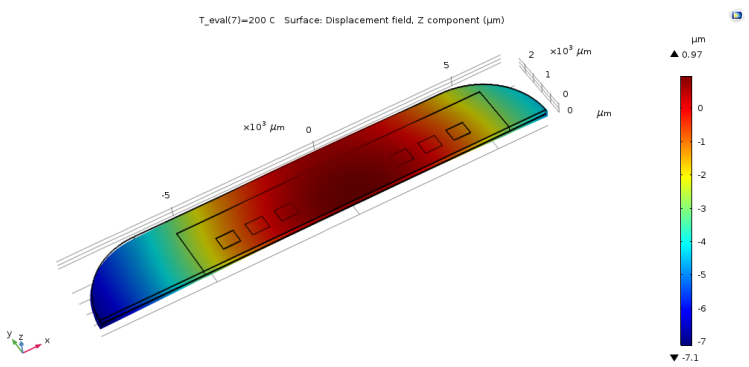

Figure 4.1: The surface displacement plot of the reference package

4.1.2 DOE Study of the New Package Stackup-2

The warpage simulation of the new TSV based fingerprint sensor package Stackup-2 were conducted within the same model setting as the reference package in terms of the geometry parameters for the derived value calculation, the material selection and the material properties, the boundary conditions and constraints in the physics of the solid mechanics, the location of the heat source and the cycling temperature in the physics of the heat transfer in solids, the mesh type and size, the solvers in the study setup and the postprocessing for the results. The simulation results are presented respectively according to the DOE study as the following table.

Table 4.1: The warpage deformation values of the DOE study

Stackup-2	Total Thickness	Die Thickness	Value of the warpage
DOE 1	$270\mu m$	$200\mu m$	$31.1\mu m$
DOE 2	$240\mu m$	$170\mu m$	$42.8\mu m$
DOE 3	$220\mu m$	$150\mu m$	$55\mu m$
DOE 4	$200\mu m$	$130\mu m$	$73.3\mu m$

The plots of the surface displacement of the DOE study are shown in Figure 4.2. The comparison of the warpage deformation of the reference package and the DOE variants is shown in Figure 4.3.

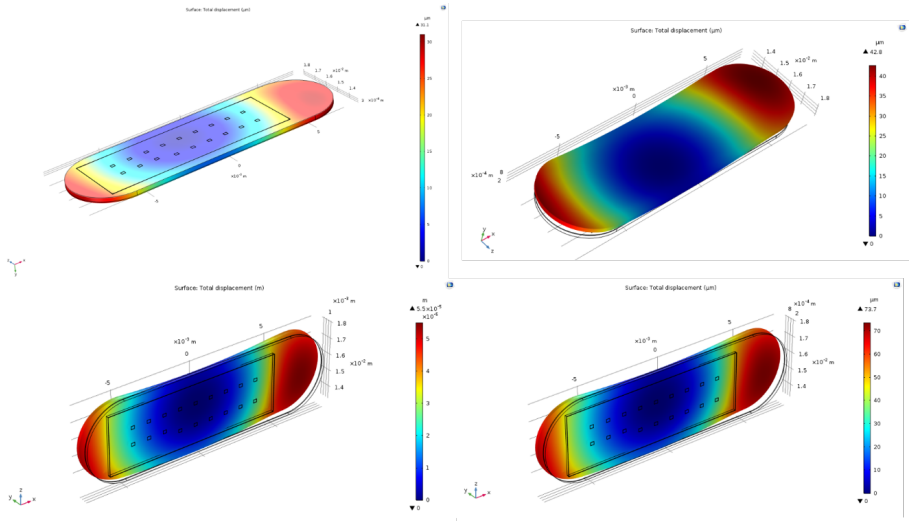

Figure 4.2: The plots of the surface displacement of the DOE study of the new Stackup-2

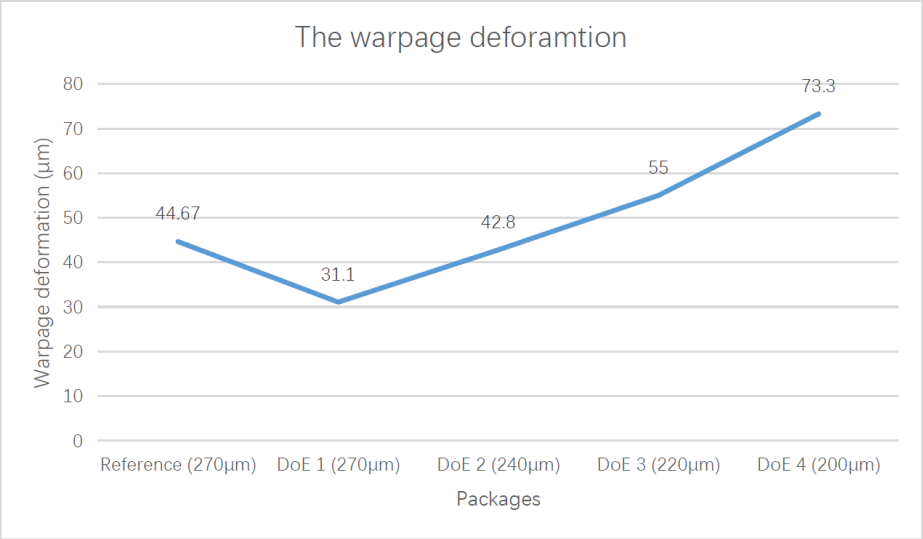

Figure 4.3: The comparison of the warpage between the reference package and DOE variants of the new Stackup-2

4.2 Results of Bending Simulation

The bending simulation is developed based on a 3 roll bending test with two supporting bricks and one pressure loading block which has been applied by the OSATs. The load is applied in the Y direction on the surface of the pressure loading block, the bottom of the supporting bricks is set as fixed constraints. The value of the displacement on the loading bricks is prescribed as 0 in X and Z direction. See Figure 3.12, the bending simulation was conducted by applying a set of loads. In the beginning, the bending simulation under the biggest load force (F=44N) was conducted in order to verify the ability of the bending resistance of the package.

4.2.1 Reference Package

By applying the ultimate load (F=44N) on the top surface of the pressure loading block, the reference package is deformed, as shown in Figure 4.4 and Figure 4.5, the von Mises stress and the total displacement value of the package can be got from the simulation results, where the von Mises stress is 1.22 $\times 10^3$ MPa, the total displacement is 173μm.

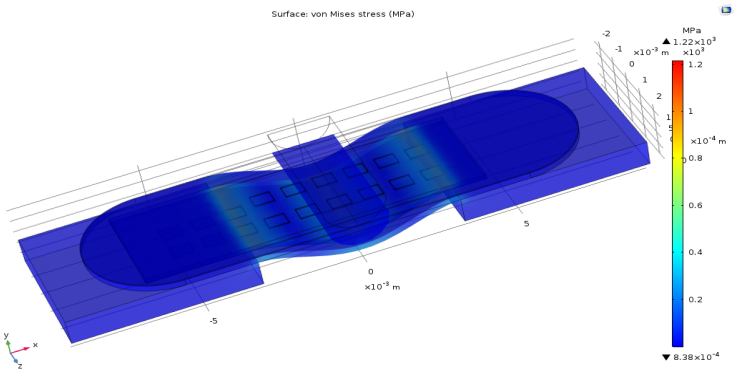

Figure 4.4: The plot of the von Mises stress of the reference package under the ultimate load (44N)

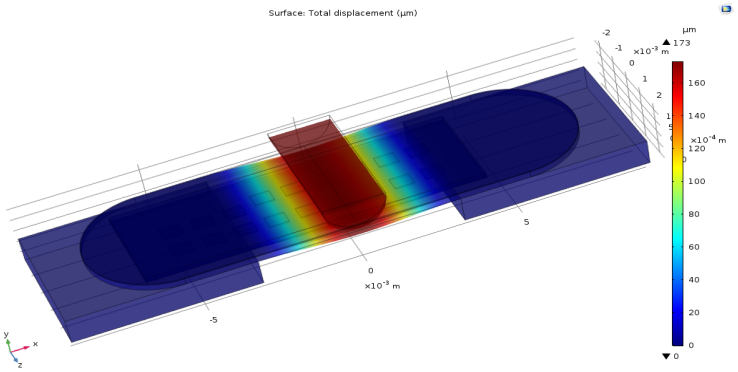

Figure 4.5: The plot of the total displacement of the reference package under the ultimate load (44N)

During the experimental bending test in the OSATs, the load applied from the indenter was 44.9 N, the indenter displacement of the reference package was 159μm, which is close to the simulation results and the setup of the bending simulation in COMSOL Multiphysics is considered as reliable.

4.2.2 DOE Study of the New Package Stackup-2

The bending simulation of the new TSV based fingerprint sensor package Stackup-2 was conducted within in the same model settings as the reference package in terms of the geometry parameters of the supporting blocks and the pressure loading block, the material selection and the material properties, the fixed constraints and loads, the mesh type and size, the solvers in the study setup and the postprocessing for the results. Initially, the bending simulation results under a 44N load are presented respectively according to the DOE study as the following table.

Table 4.2: The von Mises stress and the total displacement value of the bending simulation

DOEs	Total Thickness	Die Thickness	Von Mises stress	Total displacement
DOE 1	270μm	200μm	1.17 $\times 10^3$ MPa	135μm
DOE 2	240μm	170μm	1.33 $\times 10^3$ MPa	210μm
DOE 3	220μm	150μm	1.69 $\times 10^3$ MPa	296μm
DOE 4	200μm	130μm	1.63 $\times 10^3$ MPa	438μm

The plots of the von Mises stress and the total displacement of the deformation of the DOE variants of the new package Stackup-2 are shown in Figure 4.6 and Figure 4.7.

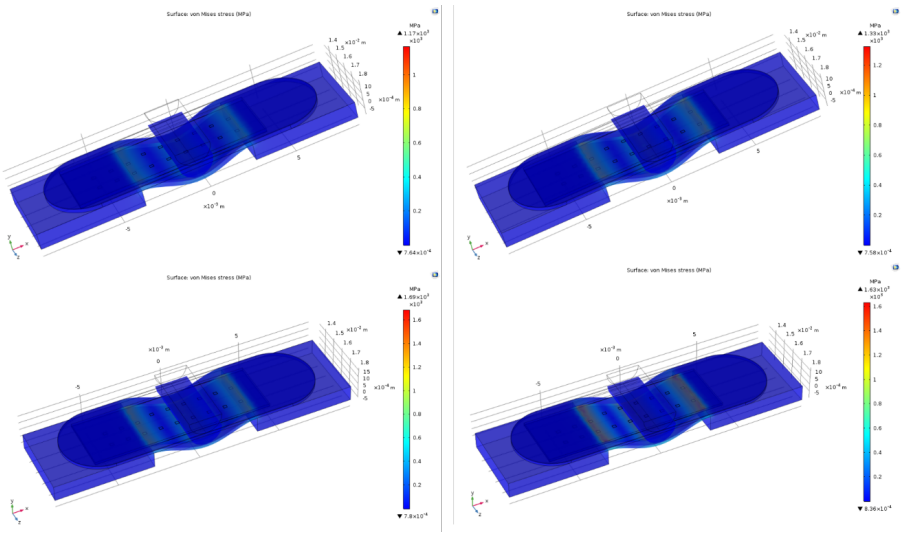

Figure 4.6: The plots of Von Mises stress of the DOE variants (F=44N)

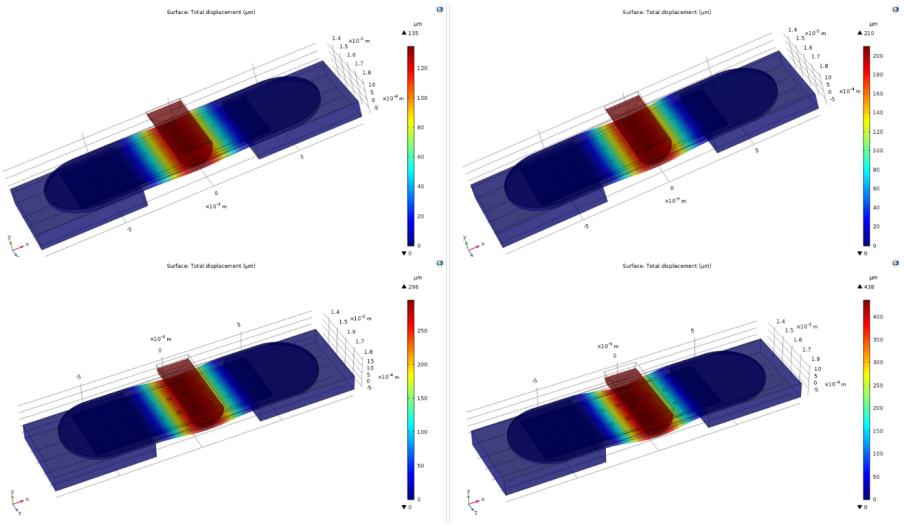

Figure 4.7: The plots of the total displacement of the DOE variants (F=44N)

The comparison of the von Mises stress and the total displacement value (F=44N) of the reference package and the DOE variants of the new package stackup are visualized in the Figure 4.8 and Figure 4.9.

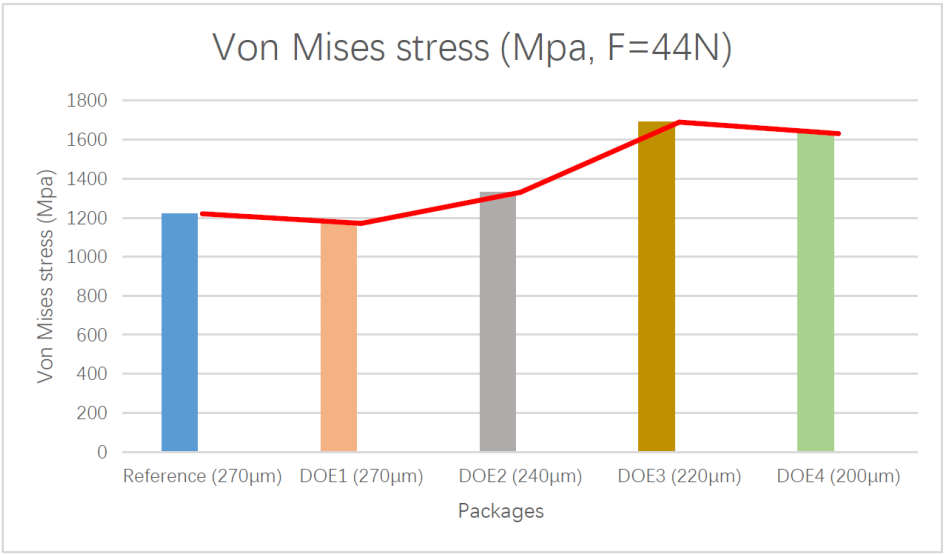

Figure 4.8: The comparison of the von Mises stress between the reference package and DOE variants (F=44N)

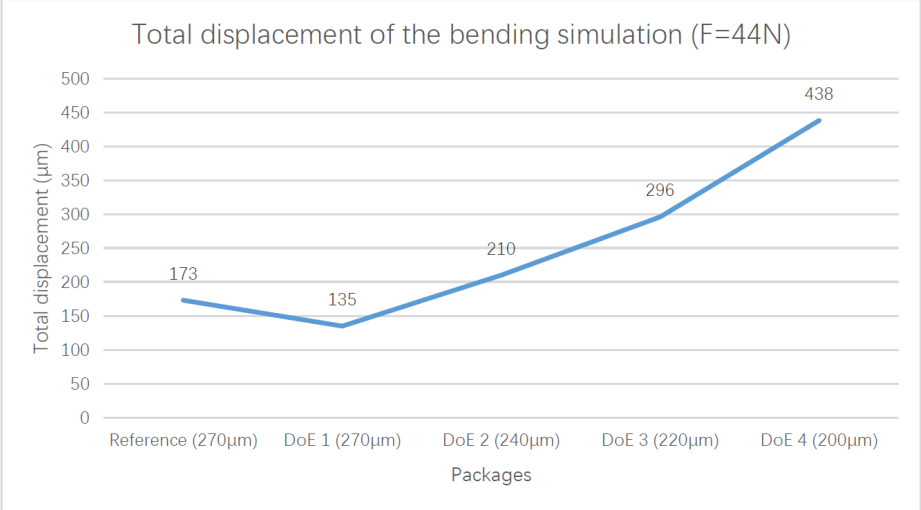

Figure 4.9: The comparison of the total displacement between the reference package and DOE variants (F=44N)

As shown in the Figure 4.8 and Figure 4.9, the value of the von Mises stress and the maximum total displacement drops when switch the package from the reference package to the DOE1 package variant. Comparing the DOE variants, the simulation results value is increased along with the decrease of the total thickness. The results illustrate that mechanical properties could be improved by adopting the new design of the Stackup-2, the total thickness of the package could be decreased and a thinner fingerprint sensor package could produce with the same or even better thermomechanical properties.

In order to predict and evaluate the mechanical behavior of the fingerprint sensor package under different using conditions, and also compare the similarity between the reference package and the new package stackup, the bending simulation were performed with a set of load force. The load and its corresponding pressure is shown in Table 3.3.

The data of the load is obtained from the packaging laboratory of FPC, the range of the load covers the general usage scenarios. The entire physics model was set up as linear elastic materials, the Yong's modulus and the Poisson's ratio are acquired from the material database which is shared by the FPC and the OSATs and has been approved to be reliable.

The plot of the von Mises stress and the total displacement of the reference package and the DOE variants under a set of loads are shown in Figure 4.10 and Figure 4.11.

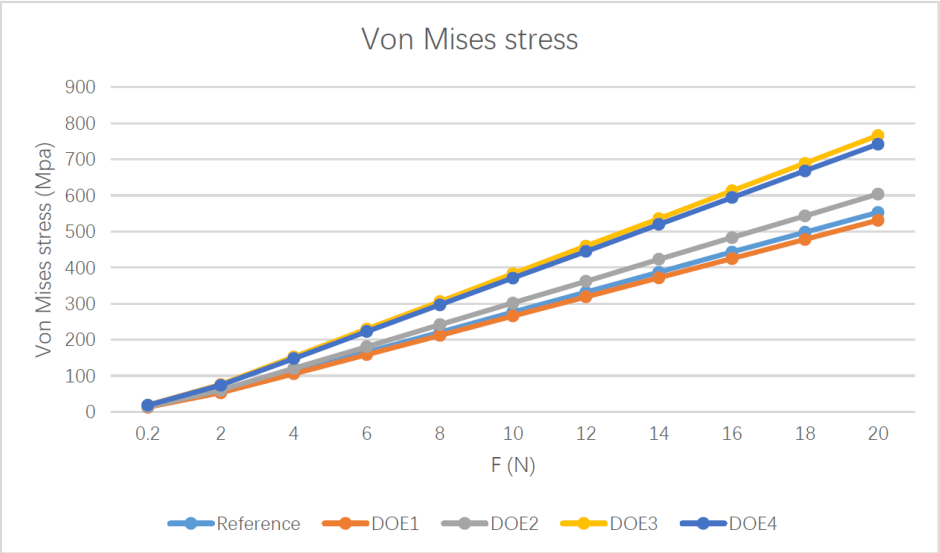

Figure 4.10: The von Mises stress plot of the bending simulation under a set of loads

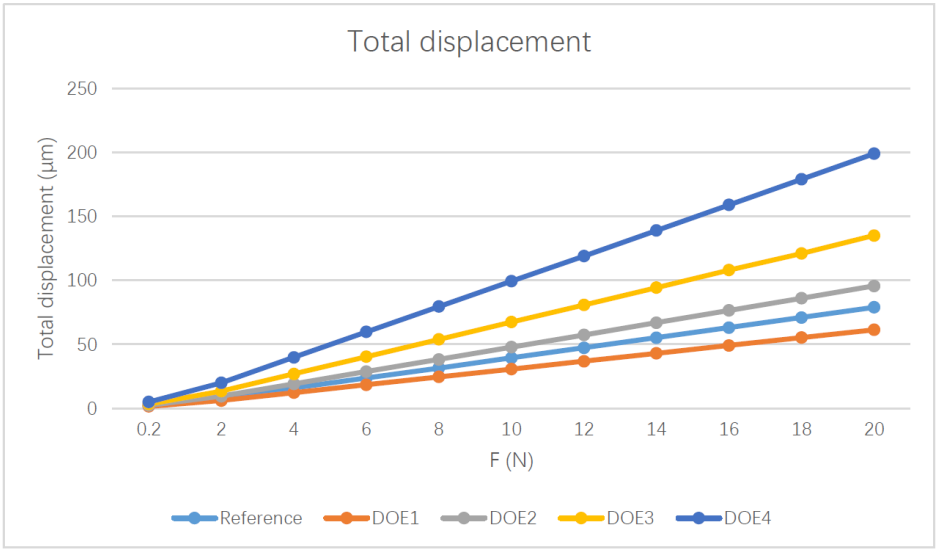

Figure 4.11: The total displacement plot of the bending simulation under a set of loads

As shown in the Figure 4.10 and Figure 4.11, for both the von Mises stress distribution and the total displacement maximum value, the curves of the reference fingerprint package are above the DOE1 package stackup which has the same total thickness as the reference package. This indicates that the new developed fingerprint sensor package stackup has bigger stiffness than the reference package with the same thickness.

5

Discussion and Future Work

In this chapter, the results of both the warpage simulation and bending simulation are compared and discussed. The factors that could affect the simulation results with respect to the setup of the COMSOL Multiphysics and the operation of the experimental test are analyzed and investigated. The future work of the thesis and the design suggestion for the new TSV based ultra-thin fingerprint senor package are also specified.

5.1 Discussion of the Results of the Warpage Simulation

The warpage simulation is considered as reliable by inheriting the setting of the previous simulation of the reference package which has been qualified and widely used. All the setup in terms of the geometry parameters, materials, physics, mesh generation and study are kept the same.

By analyzing the simulation results in Figure 4.3, the warpage behavior clearly decreased when changing the design from the reference package which have EMC molding material on both sides and the bottom to the new package Stackup-2 with EMC molding material only on sides. The reason is that the EMC material have a much bigger CTE than the silicon, so when replacing the EMC on the bottom with a thicker silicon die, the warpage behavior will be decreased. However, when keep reducing the thickness of the package the warpage behavior is getting worse since the percentage of the silicon is also reduced and the rest layer of the package such as the wafer coating and the passivation layer have bigger CTE than the silicon.

5.2 Discussion of the Results of the Bending Simulation

The bending simulation in this thesis was developed from the 3 roll bending test which is commonly used in package qualification and reliability studies. For the package with same thickness and the package design, the results of the bending simulation in COMSOL Multiphysics have an obvious deviation comparing with the experimental test that conducted in the OSATs. The factors that might attribute to the difference are hard to find and track since there is limited data of the setting of the experimental test in OSATs, so it is impossible to replicate the entire

setup of the experimental bending test with simulations, there exist deviations in terms of the constraints and the load applying method. Every OSAT have its own setting and requirements for the bending test, e.g. the radius and the hardness of the indenter, the placement of the supporting blocks. Generally, the OSATs will perform a bending test for engineering sample form each lots and the design of the package could be changed in each lots based on the feedback from the phone OEMs. The diversity of the same batch of samples, the molding machine could also bring inevitable deviation for samples even within in the same batch since the production deviation is always exist.

The trend in the smartphone industry changes so fast, the design is more about to please the customers instead of concerning from the engineering perspective. As a result, the coating of the package is frequently changed in order to meet the new specific needs, for example, to add pattern or logo on the coating, and the change of coating material will lead a different result for the bending simulation.

Without considering the deviation between the result of experimental test and the result of the simulation in COMSOL, as shown in the Figure 4.9, the value of total displacement was decreased when switching from the reference package to the new package stackup. By viewing the material properties, it can be found that the silicon has a much bigger Young's modulus than the EMC material and the rest material of the stackup lamination, so when replacing the EMC on the bottom with a thicker silicon die, the stiffness will be increased and the deformation of the package will be decreased. However, when keep reducing the thickness of the package the deformation of the package is getting bigger since the total thickness is reduced, the percentage of the silicon in the total thickness is also reduced and the rest layer of the package such as the wafer coating and the passivation layer have smaller Yong's modulus than the silicon.

Even though part of the simulation results are different with the one derived from OSATs, but the result in this thesis is still sufficient to evaluate and verify the new package stackup and draw a conclusion since all the simulation were performed in the same setting with the same material properties. The comparison between the reference package and new package Stackup-2 could give the package development engineers a brief overview of the mechanical property of the new TSV based ultra-thin fingerprint sensor package.

5.3 Future Work

Engineering samples has been planned to be produced, but the implementation of the production depends on the actually needs of the phone OEMs, factors such as the trend of the phone design and the development of other biometirc recognition technology are also play big roles in the design consideration. And obviously the customer's preferences contribute a huge factor in the design trend of the smartphone.

Besides the application of the new ultra-thin TSV based fingerprint sensor package stackup, the simulation results can be used as a research foundation and reference of the design of the future capacitive fingerprint sensors, and this study is also a technical verification of the new progress improvement of the molding technology.

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