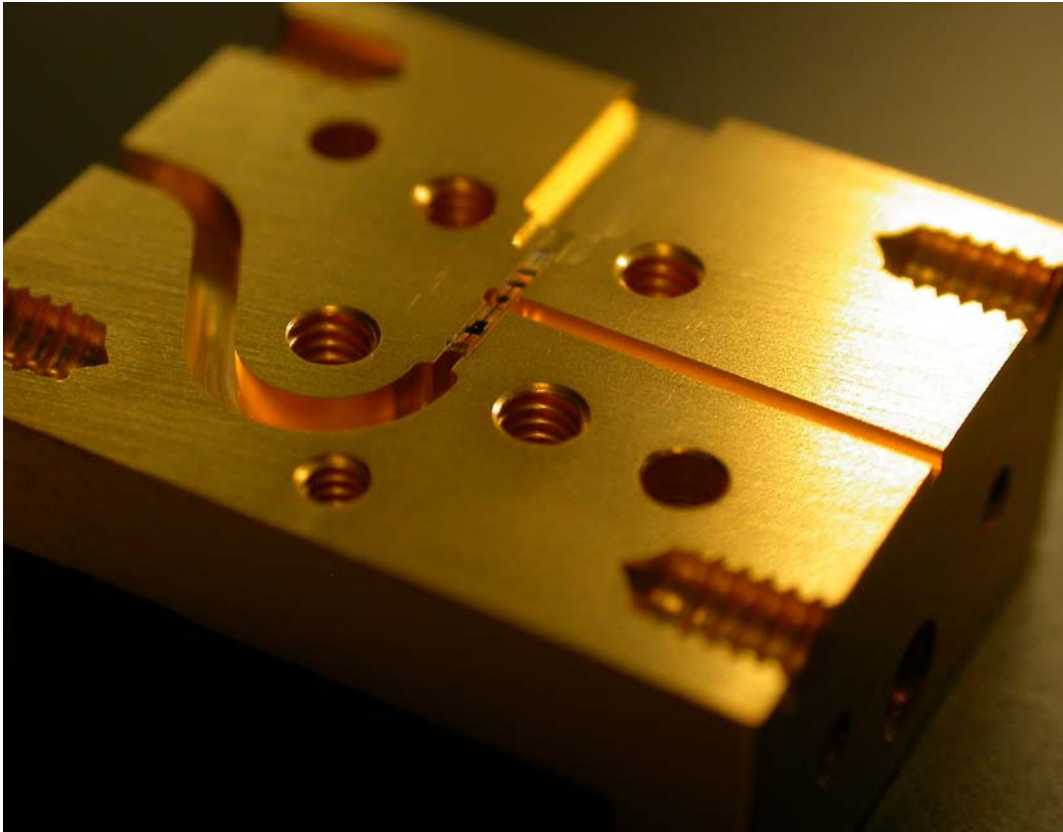


# CHALMERS



## Modelling and Characterisation of a Broadband 85/170 GHz Schottky Varactor Frequency Doubler

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Göteborg, Sweden, 2011



Thesis for the degree of Master of Science in Integrated Electronic  
System Design

Modelling and Characterisation of a Broadband  
85/170 GHz Schottky Varactor Frequency  
Doubler

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Cover: Exploded view of the fabricated hybrid balanced frequency doubler  
This report is written in L<sup>A</sup>T<sub>E</sub>X  
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## Abstract

In this thesis, a frequency doubler is designed to produce a broadband local oscillator signal (LO) around 200 GHz. A linear array of four Schottky varactors are incorporated into a GaAs flip-chip in a balanced anti-series configuration [1], so as to generate the second harmonic of the incoming signal. The varactor chip is soldered to a suspended microstrip quartz circuit, which constitutes the input/output embedding circuit, the DC bias filter and the output E-probe. A E-plane waveguide split block is used to accommodate the doubler quartz circuit, along with an input (WR-10) and an output (WR-5) waveguide interface. Generally, an iterative design process is carried out to make a trade-off among the doubler bandwidth, the conversion efficiency and the power handling capability of the GaAs Schottky varactor chip. At room temperature, a peak output power of 10 mW is measured at an output frequency of 168 GHz, with a pump power of 50 mW and a corresponding conversion efficiency close to 20%. Under a pump power of 45 mW, a peak output is obtained at around 165 GHz, with a conversion efficiency of 16%, as well as an output power of 7 mW and an estimated 3-dB fractional bandwidth of 15%. Combined directly with the power amplifier chain, the measured peak output power is around 20 mW.

Keywords: Terahertz sources, frequency multipliers, varactors, harmonic generation, Schottky diodes, balanced doublers, harmonic balance, finite element analysis



# Acknowledgements

I owe my deepest gratitude to my examiner, Prof. Jan Stake, who offered me the opportunity to participate in his fascinating research of THz technology. Without his tolerance and encouragement, it was not possible for me to finalize the thesis work. From the initial to the final stage, my examiner offers me enormous guidance and inspiration, which not only enabled me to develop a deep understanding of the subject, but also laid a firm foundation for my future career in the THz field.

Also I heartily thank my supervisor, Tekn.lic. Peter Sobis, for his patient instructions regarding the entire design methodology as well as the build-up of the detailed circuit model. Indeed, it was his laborious work that helped me capture sets of measurement data for the doubler performance evaluation. Furthermore, I never forget the opportune support from Aik Yean Tang at the beginning stage, which rendered me a comprehensive understanding of the working principle of the Schottky diode. During the circuit design phase, Dr. Tomas Bryllert also gave me many tips from a circuit point of view. Simultaneously, I am indebted to Vladimir Drakinskiy who fabricated the varactor diode chip for measurement use, as well as Johanna Hanning who offered me the standard Latex template and Carl Magnus Kihlman who was responsible for fabricating the waveguide metal block. Lastly, I offer my regards and blessings to all the staff working in Terahertz and Millimetre Wave Laboratory which facilitates an intensive academic atmosphere and a sincere cooperation among colleagues.

This work was in part funded by the European Space Agency under ESTEC project No. 21867/08/NL/GLC.





# Abbreviations

$A$	Device area (junction area)
$CV$	Capacitance versus Voltage
$C_j$	Junction capacitance
$C_{fp}$	Finger to pad capacitance
$C_{pp}$	Pad to pad capacitance
$f_c$	Cut-off frequency
$f_p$	Pump frequency
$HEMT$	High electron mobility transistor
$HBV$	Heterostructure barrier varactor
$i_d$	Displacement current
$i_c$	Conduction current
$i_t$	Total current
$IV$	Current versus Voltage
$I_0$	Reverse saturation current
$LO$	Local oscillator
$L_n$	Conversion loss
$L_f$	Air-bridge finger inductance
$MMIC$	Monolithic microwave integrated circuit
$N_d$	Doping concentration
$P_f$	Pump power
$R_{epi}$	Resistance existing in the un-depleted region of the epitaxial layer
$R_{spread}$	Spreading resistance from epitaxial layer to buffer layer
$R_{buffer}$	Buffer layer resistance
$R_{ohmic}$	Ohmic pad resistance
$R_s$	Series resistance
$R_j$	Nonlinear resistance of diode junction
$V_j$	Voltage across the diode junction
$V_t$	Voltage across the total varactor device
$V_{br}$	Reverse breakdown voltage
$Z_s$	Source impedance
$Z_d$	Diode impedance
$Z_i$	Diode embedding impedance from the input embedding circuit
$Z_o$	Diode embedding impedance from the output embedding circuit
$Z_{in}$	Input impedance of the whole doubler system
$\eta$	Conversion efficiency
$\phi_b$	Forward conduction barrier potential
$\varepsilon_s$	GaAs dielectric permittivity



# Contents

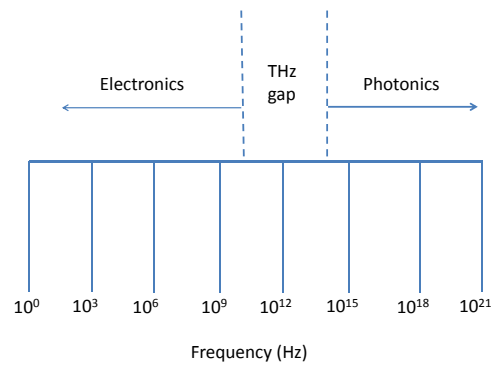
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**References**



# Chapter 1

## Introduction

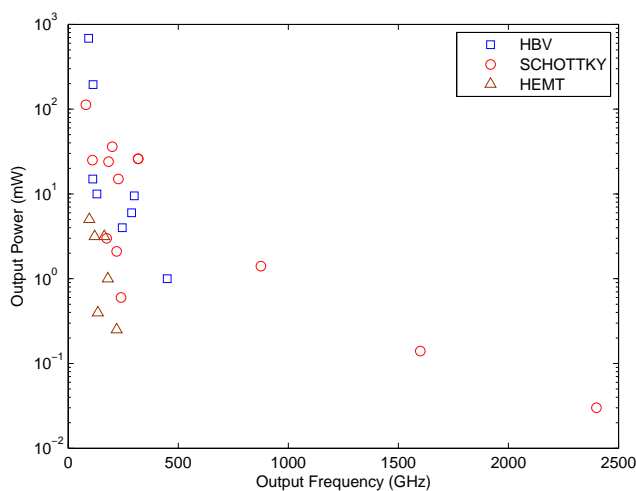


**Figure 1.1:** THz gap in the electromagnetic spectrum

Today, terahertz is broadly applied to the wavelength range between 1000-100  $\mu m$  (300 GHz-3 THz) [2]. During the past decades, there was a rapid development within the field of THz sources, such as solid state oscillators, quantum cascade lasers, optically pumped solid state devices [3] and vacuum tube devices. THz sources can be used as the local oscillator signal (LO) for the heterodyne receiver system in astronomy, Earth and planetary science [4]. In the past, Travelling Wave Tubes (TWT) and Backward Wave Oscillator (BWO) have been explored as notable vacuum tube sources. However, those kinds of LO source is usually bulky, requiring high voltage, having short operational lifetime, low reliability and stability issue [5]. Although some similar THz sources with improved structures have appeared and succeeded in removing the bulky support system for a stronger frequency scaling capability, such as the reflex klystron [6] and the micro-fabricated TWT [7], their operational lifetime are still being questioned. Meanwhile, two-terminal diode based solid-state oscillators are competitive alternatives, like the Resonant Tunneling Diode (RTD) [8] and the Transferred-Electron Device (Gunn-diode) [9]. Particularly, the Gunn-diode is widely used as a LO source in light of its low noise and compactness. Additionally, the Uni-Traveling Carrier Photo Diode (UTC-PD) [10] has been

developed rapidly. It utilises the photo-mixing effect, which enables the generated LO source to possess a strong tuning capability over a wide frequency band. However, this approach is not suitable for the sensitive receiver system unless its sideband noise in the LO can be inhibited.

Considering producing a reliable 170 GHz signal source for pumping the mixer of the heterodyne receiver, a frequency multiplier chain is preferable for its compactness, large thermal tolerance, high efficiency and stability. Indeed, varieties of nonlinear semiconductor device can be utilised as a frequency multiplier, such as the Heterostructure barrier varactor (HBV), the High electron mobility transistor (HEMT) and the Schottky varactor.



**Figure 1.2:** State-of-the-art terahertz source survey (1999-2010): Output power versus frequency up to 2.4 THz based on HBV, Schottky and HEMT respectively ([11–31])

Generally the HBV and the Schottky diode based frequency multipliers have large power potential in the THz range. Specifically, the former device is more commonly used as a tripler or a quintupler, due to its natural property of even-order harmonics suppression. However, HBV performance tends to be undermined at the higher frequency region (above 500 GHz). Similarly, the output power of the HEMT based frequency multipliers turn out to suffer from a large parasitic loss when its operating frequency goes up to several hundred GHz. As a consequence, the HEMT devices are mostly applied to the multi-functional integrated circuits operating in the lower part of THz range. By contrary, Schottky diode based frequency multipliers with medium output power and small LO noise, have been developed over a wide frequency band spanning from the microwave range into a few THz.

This master thesis work focus on the modelling and characterisation of a 85/170 GHz frequency doubler in connection to an ESA (European Space Agency) project [32]. The following table lists all the original design specifications.

Frequency doubler	
Output frequency (GHz)	170
Bandwidth (%)	10
Output power (mW)	> 10
Input frequency (GHz)	85
Conversion efficiency	To be maximized
Input, output interface	Waveguide

**Table 1.1:** Nominal design specification

Indeed, the thesis design goal slightly deviates from the ESA project specification, in the sense that a design priority has been made to deliver a broadband characteristic, combined with an assurance of the strong power handling capability for the Schottky varactor chip. Conversely, the conversion efficiency has to be compromised to facilitate the fulfilment of the updated designed goal. Generally the frequency doubler is designed to convert a pump microwave signal close to 100 GHz to its second harmonic at around 200 GHz, based on the nonlinear voltage-dependence of the diode junction capacitance of the Schottky varactor. Instead of a single Schottky diode, an anti-series balanced diode array is used for suppressing all the odd harmonics, as well as enabling an orthogonal access for the input and the output signal to the diode array. Practically, through an input WR-10 waveguide interface, the pump power is fed into a 3-terminal discrete GaAs flip-chip where a linear array of four Schottky varactors is incorporated in the anti-series configuration. Then, a quartz circuit soldered to the GaAs flip-chip is inverted and suspended in a shielded channel inside a mechanically E-plane split waveguide block, constituting all the peripheral functional units, such as the embedding circuits which transform the port impedances to the optimum circuit impedances presented to the varactor chip terminals, and the output E-probe in conjunction with a DC bias filter, which couples the excited second harmonic frequency component well into an WR-5 output waveguide. Overall, the complete procedures of doubler modelling, assembly and test are described in this report.





## **Chapter 2**

# **Theory**

In this chapter, theories for designing the frequency doubler are introduced to clarify the underlying principles of varactor model, Schottky diode characteristics and implementation of the hybrid balanced frequency doubler.

## 2.1 Varactor

### 2.1.1 Varactor model

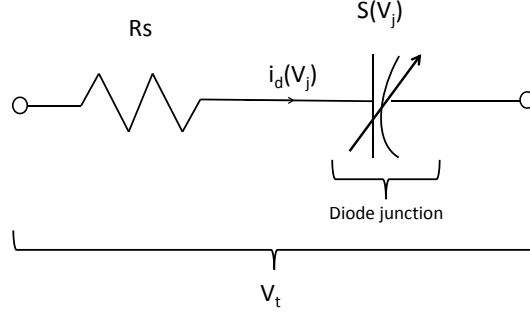
A varactor is a nonlinear reactance device used for harmonic generation, parametric amplification, mixing, detection, and voltage-variable tuning [33]. Generally the property of the harmonic generation is increasingly being utilised for the frequency multiplier operation, in which the varactor behaves like a nonlinear voltage-dependent capacitance. Particularly, a reverse biased Schottky diode is commonly applied to the varactor operation, taking advantages of small size and low noise. To describe the essence of the frequency multiplier, Manley-Rowen formula [34] is firstly introduced in a reduced version, which reflects the general relationship of the power flowing in a lossless nonlinear reactance at pump frequency  $f_p$  and the desired output harmonic frequency  $nf_p$ .

$$P_f = -P_{nf} \quad (2.1)$$

$P_f$  and  $P_{nf}$  represent the flowing input power at pump frequency  $f_p$  and desired output harmonic frequency  $nf_p$  respectively. It is noted that this derivative formula is valid only when the frequency multiplier is designed specifically so that the real power flow can exist only at  $f_p$  and  $nf_p$ . In this situation, the formula (2.1) means a theoretical 100% conversion efficiency  $\eta$  or in other words, 0 dB conversion loss  $L_n$ . However, practically the ideal maximum conversion efficiency is not achievable due to the existence of the series resistance. Alternatively, varistor device can be used to realize the frequency multiplier as well, but with quite limited conversion efficiency [35]

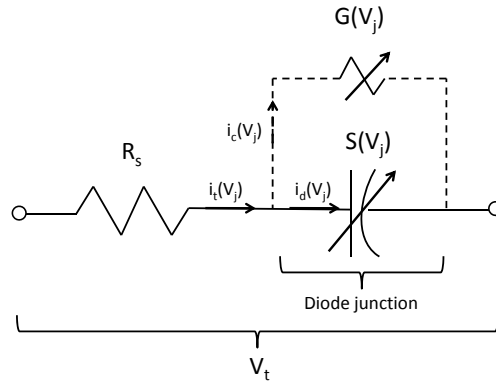
$$\frac{P_f}{P_{nf}} \geq n^2 \quad (2.2)$$

The varistor operation is subject to its maximum attainable conversion efficiency ( $1/n^2$ ) compared to the varactor (100%), but gains much from its broadband performance. By contrary, the embedding circuit design for varactor operation is more severe, which results in a strict bandwidth limitation. To be utilized as a frequency multiplier in the space-borne platform, a varactor based frequency multiplier is preferable since conversion efficiency usually has higher priority. An ideal equivalent circuit for a pure varactor includes a diode junction characterised by its voltage-dependent capacitance, as well as a diode series resistance which should degrade the conversion efficiency of the varactor diode based frequency multiplier.



**Figure 2.1:** Ideal equivalent circuit of varactor model [36].

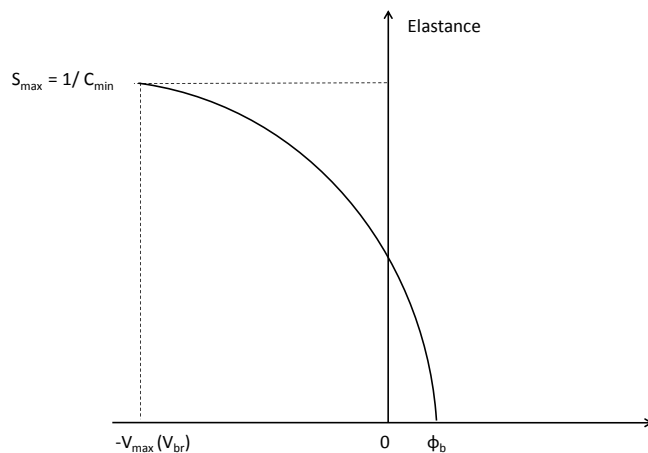
Here  $V_j$  denotes the terminal voltage across the diode junction while  $V_t$  denotes the whole voltage drop through the varactor model, where an extra voltage drop induced by the series resistance  $R_s$  has to be added. Considering the series connection, the differential elastance of the diode junction  $S(V_j)$  rather than the differential capacitance  $C(V_j)$ , is applied to present the slope of voltage-charge relation of the junction [37],  $S(V_j) = 1/C(V_j) = dV_j/dQ_j$ . Under the varactor operation, a displacement  $i_d(V_j)$  flowing the nonlinear junction capacitance is dominant. However, with the pump power increasing, the pure varactor operation should be replaced by either a mixed operation between varactor mode and varistor mode, or even a pure varistor operation. As a consequence, a conduction current  $i_c(V_j)$  flowing the nonlinear junction resistance tends to grow up and ultimately overwhelm the displacement current  $i_d(V_j)$ . Therefore, a more realistic varactor model would look like



**Figure 2.2:** Realistic equivalent circuit of varactor model.

The part which is added as dotted line accounts for the potential conduction current caused by the nonlinear junction resistance. Indeed, the total current  $i_t(V_j)$  flowing the entire varactor model should be given by  $i_t(V_j) = i_d(V_j) +$

$i_c(V_j)$ .



**Figure 2.3:** Elastance as a function of voltage for asymmetric junction diodes

Asymmetric junction diodes like Schottky diodes have an asymmetric curve for the elastance as a function of junction voltage. The maximum allowable elastance occurs to the junction reverse breakdown voltage ( $V_{br}$ ) while the minimum elastance corresponds to the junction forward conduction barrier potential ( $\phi_b$ ). Generally  $V_{br}$  and  $\phi_b$  are the lower and upper boundaries of the junction voltage for maintaining the varactor operation.

### 2.1.2 Pumping

Pumping means the process in which a large current signal at input frequency ( $f_p$ ) flows the varactor. During a pumping cycle, the varactor turns out to be a time-varying elastance  $S(t)$  and power is dissipated by the series resistance when the displacement current is passed through. The total varactor voltage ( $V_t$ ) in the figure (2.2) is described by the equation

$$V_t(t) = i_t(t)R_s + \int S(t)i_t(t)dt \quad \text{Under the varactor operation, } i_t \approx i_d \quad (2.3)$$

The boundary equations which refer to the embedding circuits at all harmonics, need to be taken into account together with the equation (2.3). Since frequency domain analysis is more adaptable for those equations mentioned, Fourier series are introduced to rewrite  $V_t(t)$ ,  $i_t(t)$  and  $S(t)$  as

$$\begin{aligned}
V_t(t) &= \sum_{k=-\infty}^{\infty} V_k e^{jk\omega_p t} \\
i_t(t) &= \sum_{k=-\infty}^{\infty} I_k e^{jk\omega_p t} \\
S(t) &= \sum_{k=-\infty}^{\infty} S_k e^{jk\omega_p t}
\end{aligned} \tag{2.4}$$

Since  $V_t(t)$ ,  $i_t(t)$  and  $S(t)$  are real quantities,  $V_{-k} = V_k^*$ ,  $I_{-k} = I_k^*$  and  $S_{-k} = S_k^*$ . As a consequence,

$$V_k = R_s I_k + \frac{1}{jk\omega_p} \sum_{l=-\infty}^{\infty} I_l S_{k-l} \tag{2.5}$$

This equation provides a general approach to analyze the varactor. Based on the existing relation between the Fourier coefficients  $S_k$  and  $I_k$ , the equation (2.5) turns to be nonlinear type and hard to solve [37]. Fortunately, most microwave simulation software provide harmonic balance [38] to solve those nonlinear equations.

### 2.1.3 Conversion efficiency analysis

Conversion efficiency is the main concern for the frequency multiplier design. As a critical figure-of-merit for the varactor design, dynamic cut-off frequency ( $f_c$ ) should be made as high as possible since it is proportional to the conversion efficiency. The state-of-the-art cut-off frequency of a varactor can reach is several THz.

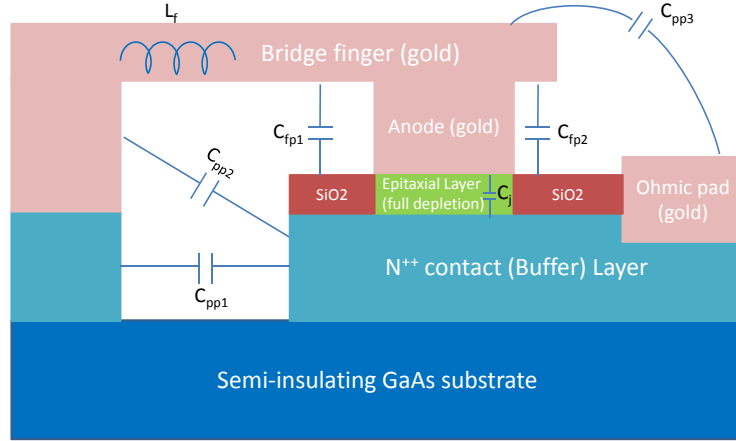
$$f_c = \frac{S_{max} - S_{min}}{2\pi R_s} \tag{2.6}$$

According to this formula, obviously a large differential elastance swing but a low series resistance is required to achieve high conversion efficiency. From the circuit point of view, the series resistance is largely determined by the layout geometry of the varactor diode array. Alternatively, more efforts can be transferred to improve the elastance swing, and thus the diode junction voltage swing. Therefore, "full" drive state [39] where the diode junction voltage swings between the reverse breakdown voltage and forward conduction barrier potential should be maintained during each pumping cycle, since it offers the allowable maximum elastance swing for achieving high enough cut-off frequency and associated optimum conversion efficiency. On the other hand, designing the embedding circuit in an appropriate way is also indispensable to achieve high conversion efficiency. For the ideal circuit simulation, the diode embedding impedance at the undesired higher order harmonics should be set to  $\infty$  or zero such that large amount of power dissipation can be avoided at those frequencies. Simultaneously, the diode embedding impedance at the pump frequency ( $f_p$ ) and the used harmonic frequency ( $nf_p$ ) should be well defined to ensure the maximum power transfer available from the source, the strong power absorption by the load as well as the effective signal isolation between the pump frequency and the desired harmonics.

## 2.2 Schottky diode

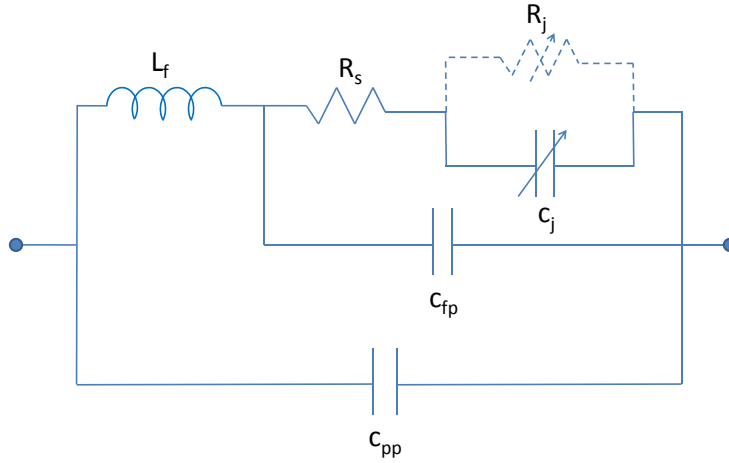
Schottky-barrier diode is a two-terminal semiconductor device that utilises the nonlinear properties of a metal-semiconductor contact [40].

### 2.2.1 Diode structure



**Figure 2.4:** Schottky Contact

A Schottky junction is created by the deposition of metal (such as Platinum or Titanium) on the surface of an appropriate semi-conducting material (such as n-doped GaAs) [20]. The non-linear behaviour stems from the electrostatic barrier between the metal and semiconductor. On the side of the semiconductor, a thin epitaxial layer (lightly doped) is included on top of a thicker (heavily doped) buffer layer. When an increasing reverse bias voltage is applied to diode, the depletion inside the epitaxial layer starts to expand, and therefore a diode junction capacitance  $C_j$  is formed within the depletion region. Furthermore, there are other existing parasitic elements induced by the diode geometry, such as pad to pad capacitance  $C_{pp} = C_{pp1} + C_{pp2} + C_{pp3}$ , finger to pad capacitance  $C_{fp} = C_{fp1} + C_{fp2}$  and finger inductance  $L_f$ . Meanwhile, the substrate is made of semi-insulating GaAs and an ohmic pad provides an electrical contact to the buffer contact.



**Figure 2.5:** Equivalent circuit of the Schottky diode working in varactor mode [20]

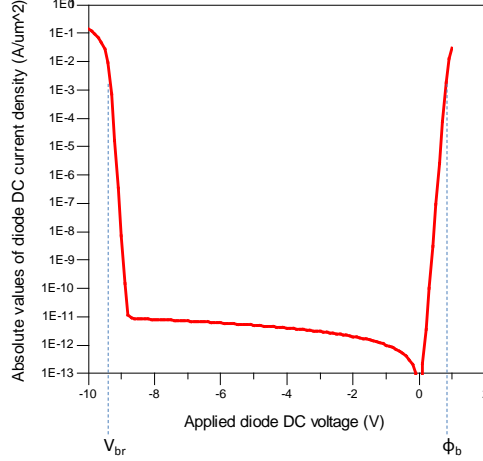
Besides the series resistance  $R_s$ , nonlinear junction capacitance  $C_j$  and the potential nonlinear junction resistance  $R_j$ , parasitic elements displayed in the figure (2.4) are also added to make the equivalent circuit of the Schottky varactor more realistic.

### 2.2.2 IV characteristic

The IV characteristic relates the junction voltage across the Schottky contact to the conduction current flowing.

$$I(V_j) = I_0 \left( e^{\frac{qV_j}{kT}} - 1 \right) \quad (2.7)$$





**Figure 2.6:** IV characteristic of Schottky diode with junction area of  $1 \mu\text{m}^2$

$I_0$  represents the reverse saturation current and the formula is valid only when the reverse bias voltage does not exceed the reverse breakdown voltage  $V_{br}$ . From figure (2.6), it is just the flattened region that is utilised for varactor operation. Generally the avalanche phenomenon happens when the junction voltage  $V_j$  drops below the reverse breakdown voltage, while a conduction current becomes obvious when  $V_j$  exceeds the forward conduction barrier potential  $\phi_b$ . Additionally, the applied diode DC voltage should be given by

$$V_t = V_j + i_t(V_j)R_s \quad (2.8)$$

Particularly the reverse breakdown voltage  $V_{br}$  of the Schottky diode is defined as the minimum reverse bias that causes the diode current to exceed a certain preselected minimum value [20], in case that diode would be ruined by large amount of heat generation resulting from an excessive reverse current. Essentially the reverse breakdown voltage is roughly inverse proportional to the doping concentration of the epitaxial layer. As a result,  $V_{br}$  can be synthesized by means of manipulating the epitaxial doping, so as to determine the power handling capability of the Schottky diode.

### 2.2.3 Diode junction capacitance

The nonlinear diode junction capacitance is quite similar to the parallel plate capacitor because of the existence of charge separation across the depletion region [20] which is created and controlled by the reverse bias voltage across the diode junction. Therefore, the pertinent formula can be used.

$$C_j = \frac{\varepsilon_s A}{w} \quad (2.9)$$

'A' stands for the cross-section area of the depletion region of Schottky diode,

while 'w' is referred to the depletion region thickness. The following formula reveals the frequency-dependence of 'w' and thus  $C_j$ .

$$w = \sqrt{\frac{2\varepsilon_s(\phi_b - V_j)}{qN_d}} \quad (2.10)$$

Here  $N_d$  is referred to the doping level of the epitaxial layer. This formula shows that the biggest thickness of depletion region appears just when the reverse breakdown voltage is fulfilled across the diode junction. In most cases, the real thickness of the epitaxial layer is made a little larger than the possible maximum thickness of depletion region so as to avoid the pinch-off of the epitaxial layer. After the fringing fields effect of the epitaxial layer has been taken into account, the final version of the formula regarding the diode junction capacitance is given by [20].

$$C_j(V_j) = A\gamma(V_j)\sqrt{\frac{qN_d\varepsilon_s}{2(\phi_b - V_j)}} \quad (2.11)$$

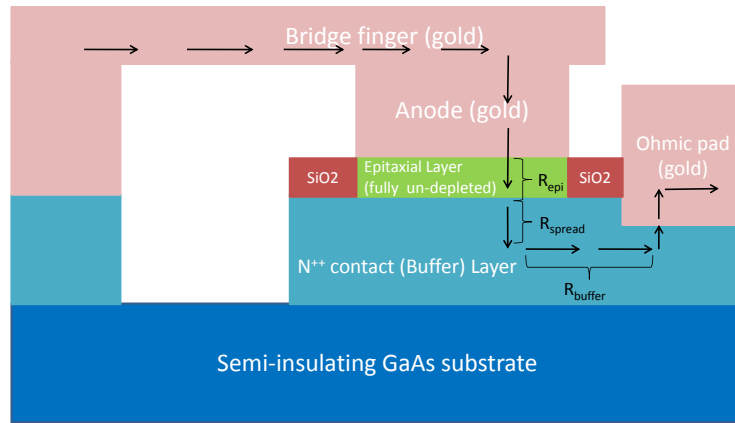
$\gamma(V_j)$  is the correcting factor for the fringing fields effects

## 2.2.4 Series resistance

The series resistance is tightly associated with the geometry of the Schottky diode, consisting of the following parts in series connection: the resistance existing in the un-depleted region of epitaxial region ( $R_{epi}$ ), the spreading resistance arising out of ohmic losses in the buffer layer below the anode as the vertical column of current spreads out into the bulk of the buffer [20] ( $R_{spread}$ ), the resistance of buffer layer ( $R_{buffer}$ ), as well as the ohmic contact resistance ( $R_{ohmic}$ ) which is usually ignored due to its smaller value.

$$R_t = R_{epi} + R_{spread} + R_{buffer} + R_{ohmic} \quad (2.12)$$

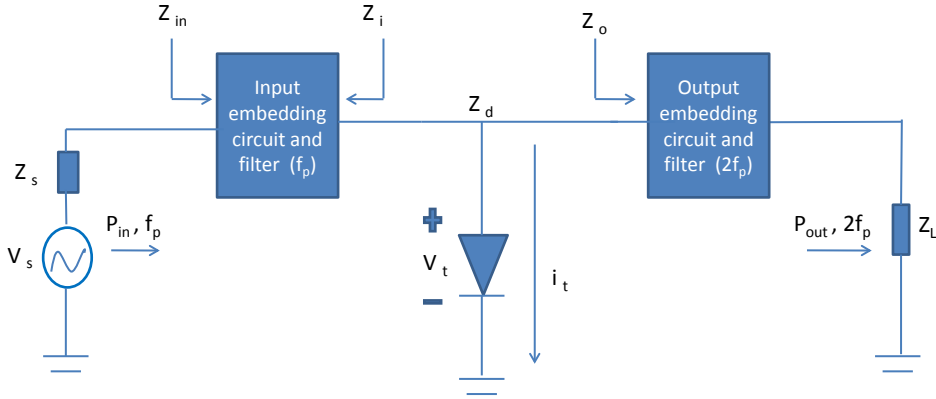
The four kinds of series resistances are illustrated below, as well as the arrows indicating the current flow.



**Figure 2.7:** Series resistance across the Schottky diode

## 2.3 Hybrid balanced frequency doubler

### 2.3.1 Equivalent circuit for single diode based frequency doubler



**Figure 2.8:** Block scheme of a frequency doubler circuit based on single Schottky diode

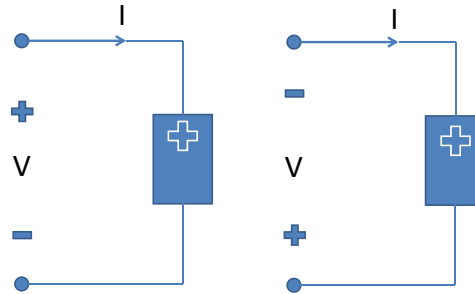
Based on the Schottky diode behaviour as a varactor, ideal frequency doubler circuit could be built according to this block scheme. The source power  $V_s$  at pumped frequency  $f_p$  feeds the doubler circuit while the second harmonics  $2f_p$  is available in the load, depending on the nonlinear characteristics of the Schottky.  $Z_d$  is single diode impedance which can be defined by Fourier series of the diode voltage  $V_t$  and the diode current  $i_t$ .

$$Z_d(n) = V_t(nf_p)/I_t(nf_p) \quad (2.13)$$

In order to achieve a maximum conversion efficiency  $Conv = 100 * P_{out}/P_{in}$ , the optimum embedding impedances ( $Z_i(f_p)$  and  $Z_o(2f_p)$ ) need to be presented to the diode, and they are acquired by transforming the source impedance  $Z_s$  and load impedance  $Z_L$  through the corresponding embedding circuit. Additionally, both the input and output filters (which is actually integrated with the embedding circuit) are designed so that  $Z_i(2f_p) = \infty$  and  $Z_o(f_p) = \infty$ , that is, as close to open circuit as possible to ensure the isolation can be realized between the radiations at  $f_p$  and  $2f_p$ . For the higher order harmonics, their embedding impedances ( $Z_i$  and  $Z_o$ ) are set to zero to turn the short circuit effect into reality.

### 2.3.2 Balanced structure

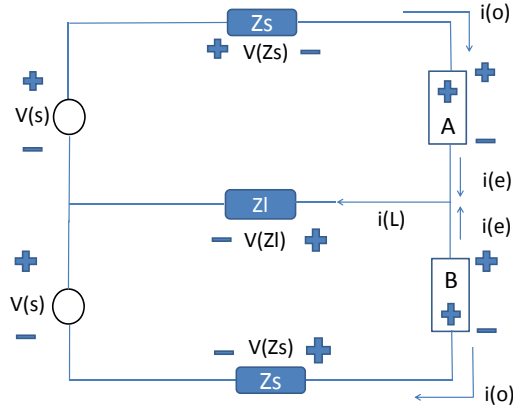
As a balanced structure, anti-series configuration is preferable for frequency doubler design, since it can enhance the power handling capability due to the increasing number of the applied diode, as well as the achievable potential for high conversion efficiency by suppressing the odd harmonics which are unused for the doubler case. Next the working principle of anti-series diode configuration would be given.



**Figure 2.9:** Two ways to impose source voltage on the conductance with different voltage polarities

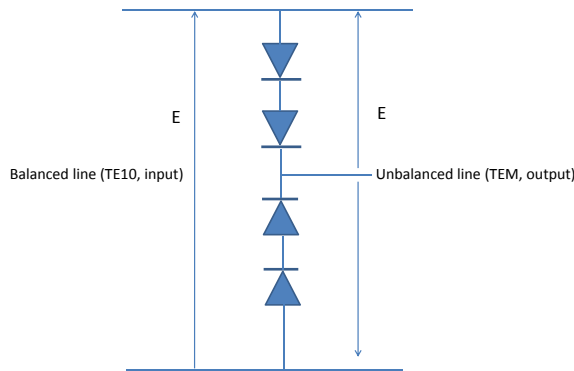
The following formulas describe the nonlinear IV relationships which occur to the conventional and reverse polarity of the source voltage respectively.

$$\begin{aligned} I &= f(V) = aV + bV^2 + cV^3 + dV^4 + eV^5 \\ I &= f(-V) = -aV + bV^2 - cV^3 + dV^4 - eV^5 \end{aligned} \quad (2.14)$$



**Figure 2.10:** Anti-series configuration for two identical nonlinear conductances (A and B) [41], where  $i(e)$  and  $i(o)$  stand for the even and the odd harmonic components of the current flowing in each conductance respectively, as well as the current  $I_{loop}$  circulating in the internal circuit loop

Under two out-of-phase sinusoidal excitations,  $V_A$  and  $V_B$  share the same value due to the symmetry of the anti-series configuration. According to the formulas (2.14),  $I_L = I_A + I_B = 2bV^2 + 2dV^4 + \dots = 2i(e)$  and  $I_{loop} = aV + cV^3 + \dots = i(o)$ , which shows that the output current flowing the load only contains even-order harmonics while all the odd-order harmonics only exist in the internal loop of the circuit. As a result, the even frequency components are rendered separated from the odd ones by the anti-series configuration. Practically, the real anti-series diode array structure would be mounted onto the planar quartz circuit and the housing waveguide block.

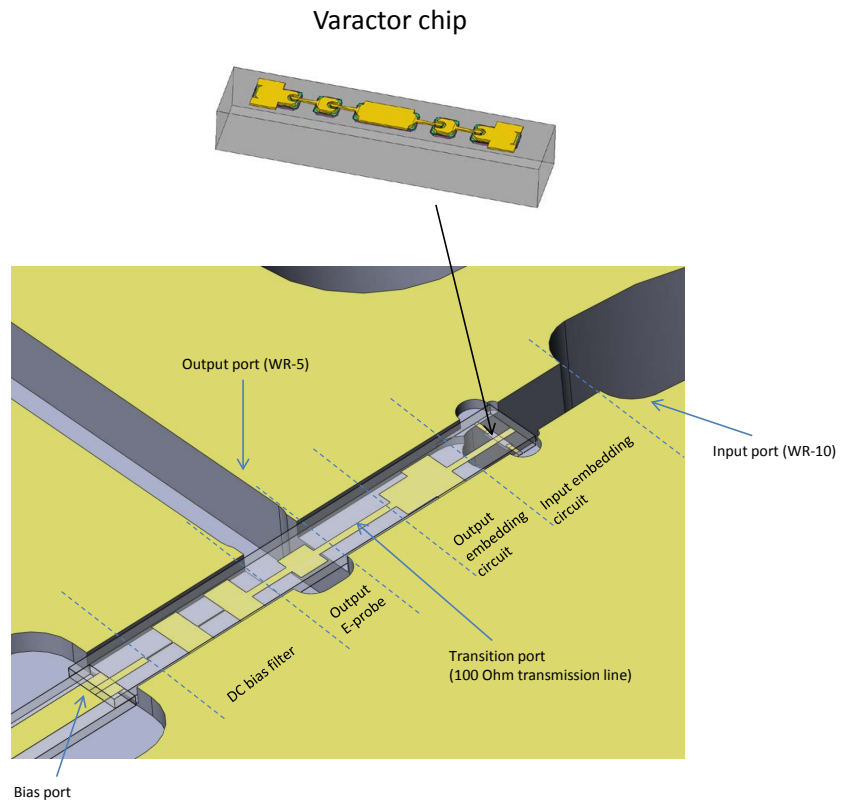


**Figure 2.11:** Illustration of the mode orthogonal strategy used in the frequency doubler design [19]

In the real microwave circuit, the diodes are in series across the input waveguide and are parallel coupled into the output waveguide [1]. The incident signal

would feed the anti-series diode array in a balanced mode (TE<sub>10</sub>) which is dominant mode in the input rectangular waveguide. By contrary, the excited second harmonics would propagate along the suspended microstrip line in an unbalanced mode (TEM). Accordingly, effective isolation between the input and the output radiations can be achieved due to the mode orthogonal.

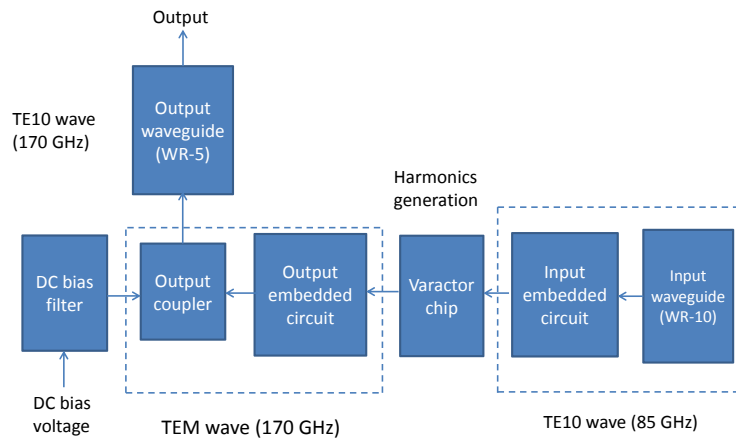
### 2.3.3 Implementation



**Figure 2.12:** Split-plane view of the 85/170 GHz frequency doubler

The practical structure of the hybrid balanced frequency doubler is depicted as above. Three well-defined wave ports are presented, that is, the input port (WR-10), the output port (WR-5) as well as the bias port (suspended microstrip line). The GaAs chip incorporates a discrete 4-diode array in anti-series configuration, then soldered to planar quartz circuit through solder pads. Particularly, in the locations of Schottky diode junctions, four lumped ports are inserted with the port impedances defined by the diode impedance acquired from the earlier simulations. Since effective signal isolation between the input and the output side can be realised due to the mode orthogonal induced by the balanced structure, the embedded filter which tends to degrade the circuit bandwidth can be avoided. Meanwhile, the quarter-wave transformer based on

the reduced-height waveguide is the main body of the input embedding circuit, while the suspended microstrip transmission lines with varying characteristic impedances are inserted to construct the output embedding circuit, aimed for coupling the excited second harmonics to the output E-probe. In conjunction with a fixed output frequency back-short and a DC bias filter, E-probe can guide the incident second harmonics to the output waveguide (WR-5). Moreover, the DC bias voltage can feed each Schottky diode through the suspended microstrip metalization.



**Figure 2.13:** Illustration of the functional partition and signal flow of the 85/170 GHz frequency doubler



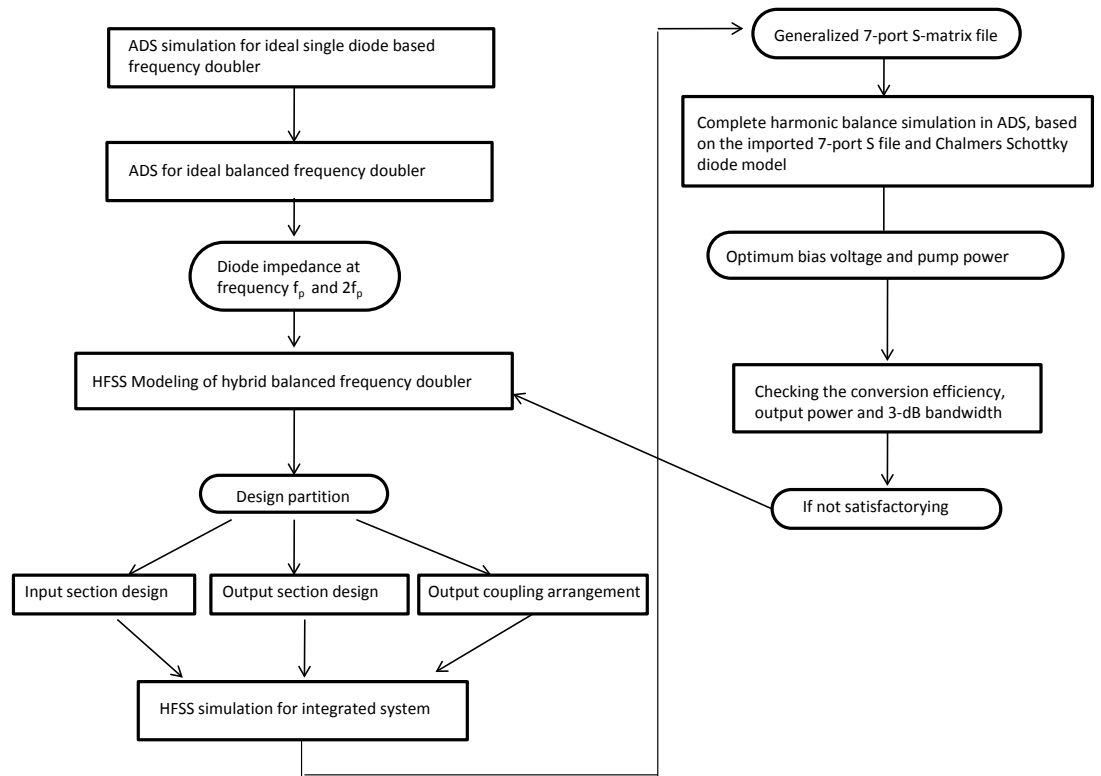


## Chapter 3

# Method

After the relevant theories regarding the doubler operation have been clarified, it comes to the circuit implementation phase which is characterised by interactive and iterative usage of two circuit simulation tools, Advanced Design System (ADS) and High Frequency Structure Simulator (HFSS). The system complexity of the frequency doubler escalates from an ideal balanced circuit model in ADS to a comprehensive hybrid structure model in HFSS. During the optimisation process, more priorities are put to realise a broadband design while the conversion efficiency has to be compromised to some extent. Finally, harmonic balance simulation is launched to evaluate the complete doubler performance, where four Chalmers Schottky diode models are combined with an imported S parameter file representing the essence of the chip package structure, the doubler circuits and the waveguide interface.

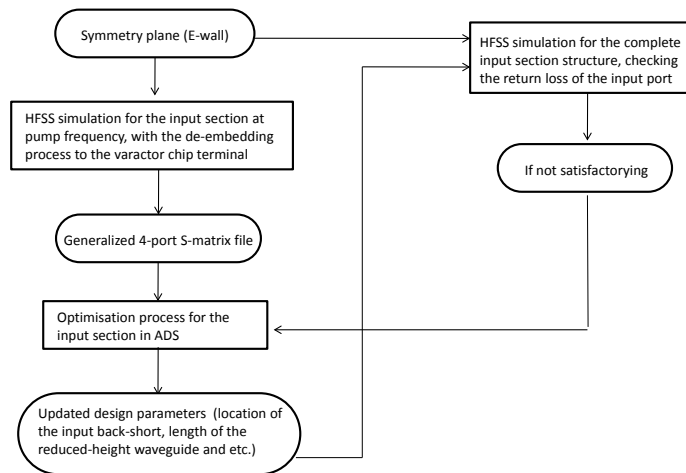
### 3.1 Design flow



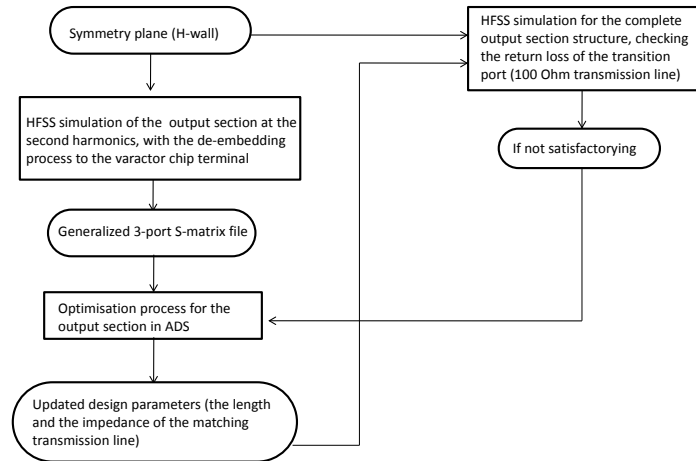
**Figure 3.1:** Design flow of the 85/170 GHz frequency doubler

The design process of the hybrid balanced frequency doubler, is characterized by the interactive and iterative usage between Advanced Design System (ADS) based on the harmonic balance technology for nonlinear circuit analysis and High Frequency Structure Simulator (HFSS) offering the linear electromagnetic solution to the specified physical structure based on the finite element analysis [42]. Initially, the harmonic balance simulation for single diode based frequency doubler was carried out in ADS, so as to enable us to be familiar with all kinds of circuit setup for nonlinear analysis. Then, a balanced (anti-series) structure of diode array consisting of four Chalmers Schottky diode model, is used to replace the single diode structure for enhancing the power handling capability and suppressing all the unused odd harmonics. Subsequently, the harmonic balance simulation is carried out to find out the single diode impedance at  $f_p$  and  $2f_p$ . Next, the real structure of the GaAs Schottky varactor chip based on the balanced structure simulated above, is drawn in AutoCAD and then imported to HFSS in conjunction with the specified physical structures of the embedding and coupling circuits. Aiming to ease the requirements for the computer memory during HFSS simulation, the whole doubler structure is divided into three

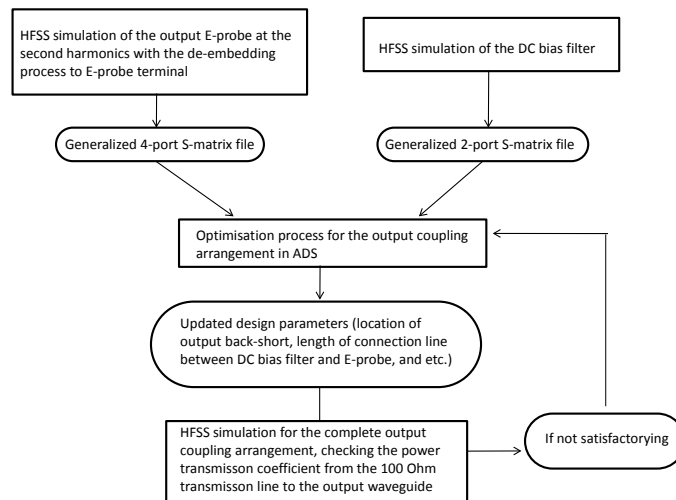
functional parts which can be solved individually, that is, the input section, the output section and the output coupling arrangement. A large amount of geometry perturbation for the sub-functional parts is analyzed and hence all the critical physical dimensions are optimised and updated, considering the trade-off between conversion efficiency and 3-dB bandwidth. Finally all the functional parts are integrated in HFSS for a complete linear electromagnetic structure simulation. As a consequence, the generalized 7-port S-matrix file with the well-defined wave ports and lumped ports is imported to ADS, combined with four Chalmers Schottky diode models connected to the lumped ports. Harmonic balance analysis is launched to evaluate the simulated performance of the full-structure hybrid balanced frequency doubler. If the simulation results were not satisfying, the doubler structure in HFSS should be re-optimised to fulfil the design specification.



**Figure 3.2:** Design flow of the input section of the 85/170 GHz frequency doubler



**Figure 3.3:** Design flow of the output section of the 85/170 GHz frequency doubler



**Figure 3.4:** Design flow of output coupling arrangement of the 85/170 GHz frequency doubler

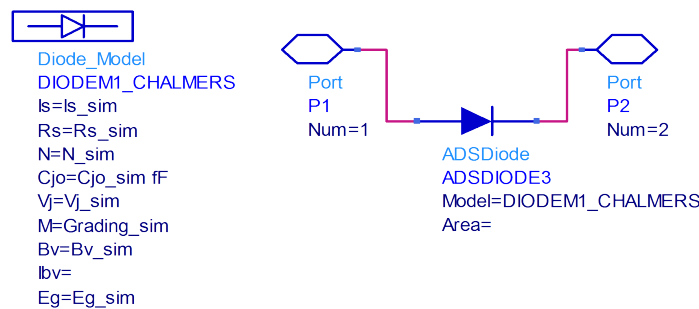
Particularly, the interactive and iterative usage between ADS and HFSS simulator also took place during the partition design phase. As for certain sub-functional part, the preliminary HFSS simulations are responsible for generating the generalized S-matrix files, which enclosed the electromagnetic solution to the appointed de-embedding terminals for that part, like the varactor chip terminal serving the embedding circuit design, or the E-probe terminal used for the

output coupling design. Then the S-matrix files are imported to ADS, combined with the ideal device components representing the peripheral structures in HFSS, where all kinds of critical physical dimensions are involved. Therefore, instead of HFSS simulations which are quite time-consuming, the optimisation process for those critical physical dimensions is carried out in ADS effectively, since the direct control could be exerted to the ideal device components and quick circuit responses are achievable. After the optimisation process had been done in ADS, the critical physical dimensions belonging to the sub-functional structure are updated in HFSS and the linear electromagnetic structure simulation is launched to evaluate the relevant performance. Iterative process took place here in the sense that the operation of the de-embedding and S-file import would be carried out again for the re-optimisation process in ADS, if the circuit performance in HFSS had still deviated from our expectations. Additionally, the symmetry plane is fully utilized during the embedding circuit design, which proved effectively reducing the simulation time in HFSS.

## 3.2 Simulation setup

### 3.2.1 Single diode based frequency doubler

A specified Chalmers Schottky diode model is applied to the ideal circuit simulation.



**Figure 3.5:** Sketch of the Chalmers Schottky diode model used in ADS

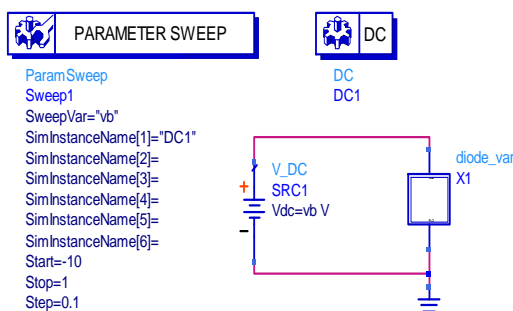
Diode junction area per anode( $\mu m^2$ )	20
Doping of epitaxial layer ( $cm^{-3}$ )	$2 \times 10^{17}$
Doping of buffer layer ( $cm^{-3}$ )	$5 \times 10^{18}$
Thickness of epitaxial layer ( $\mu m$ )	0.27
Thickness of buffer layer ( $\mu m$ )	2
Electron mobility of epitaxial layer ( $cm^2/V - s$ )	3900
Electron mobility of buffer layer ( $cm^2/V - s$ )	1830
Energy gap ( $eV$ )	1.42

**Table 3.1:** Fixed design parameters of Chalmers Schottky diode model

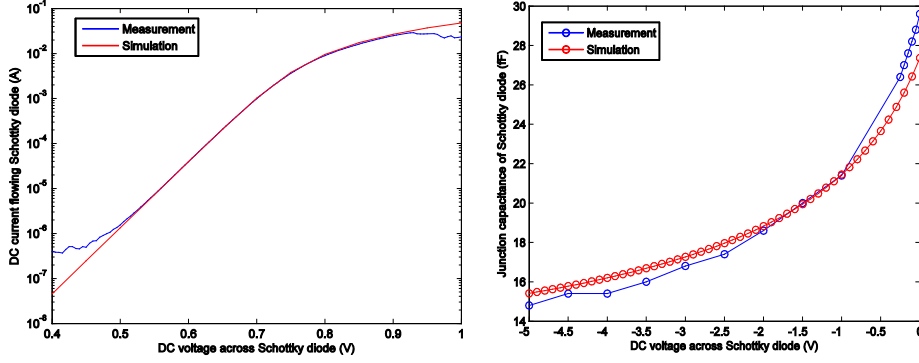
Reverse saturation current density ( $A/\mu m^2$ )	$1 \times 10^{-15}$
Parasitic capacitance due to the diode package ( $fF$ )	0
Forward conduction barrier potential ( $V$ )	1
Series resistance ( $\Omega$ )	4

**Table 3.2:** Adjustable design parameters of Chalmers Schottky diode model, as well as their initial values

There are some flexible prime parameters which can be tuned to facilitate an agreement between the simulation and measurement. In order to verify this diode model, curve fittings are made in terms of IV and CV characterisation, between the real Schottky diode fabricated for measurement use and the Chalmers Schottky diode model for circuit simulation in ADS.



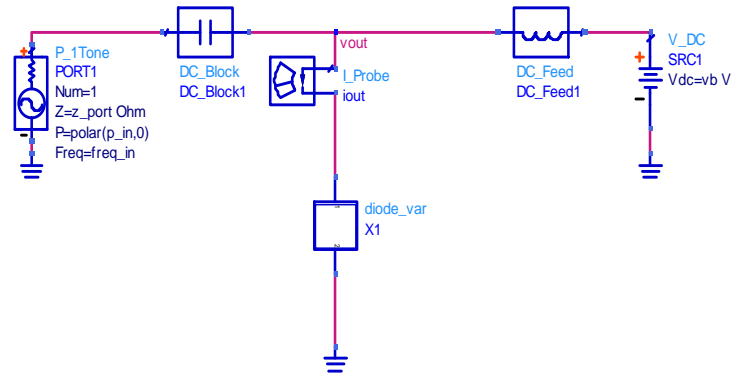
**Figure 3.6:** Circuit setup of DC simulation for single Schottky diode in ADS (The empirical formulas do not show up here which are used to calculate the CV characteristic curve for single diode model)



**Figure 3.7:** IV and CV curve fitting between the real Schottky diode and the Chalmers Schottky diode model with the diode junction area of  $15 \mu m^2$

The curve fittings for the diode IV and CV characteristic are made in different ranges of applied DC bias voltage, that is, the forward conduction region for the former case and the reverse bias region for the latter thing. For some reasons, the comparison is made with the junction area of  $15 \mu m^2$  rather than the appointed junction area of  $20 \mu m^2$ . For the CV characteristic, the curve fitting can be available by adjusting the diode parasitic capacitance and the forward barrier potential which are applied to the circuit setup, while the series resistance and the reverse saturation current density played a dominant role in determining the IV characteristic. As a result, strong curve fittings are available for both IV and CV characteristic and hence the Chalmers Schottky diode model proved reliable enough to be put into use. Since this kind of diode model is scalable with the diode junction area, the fitting results are also adaptable to the other area cases.

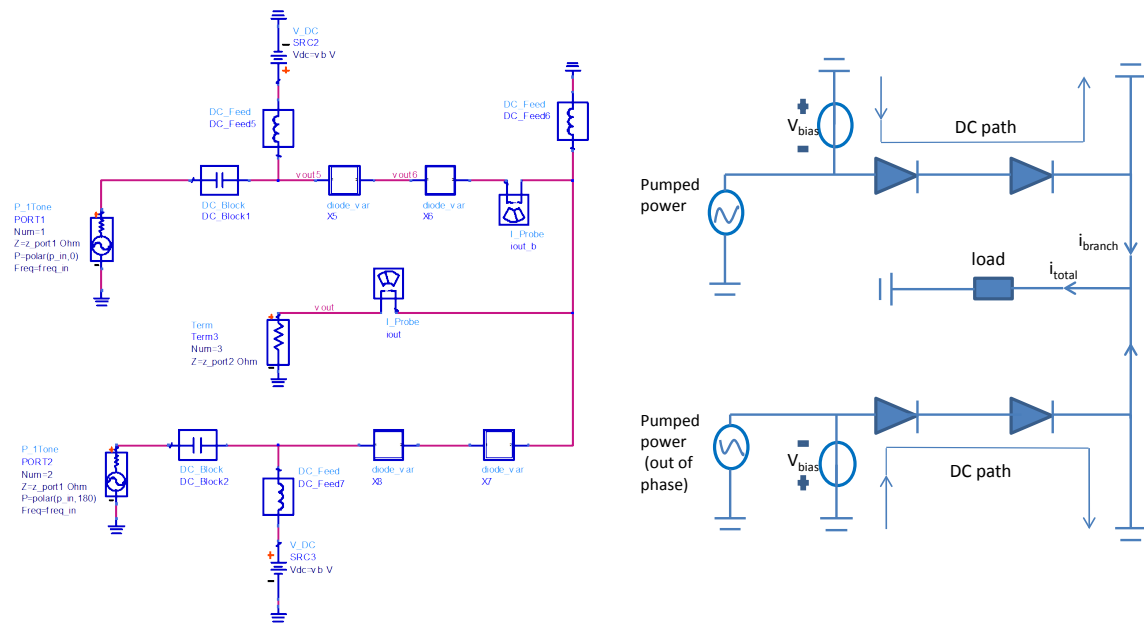




**Figure 3.8:** Schematic of the circuit simulation setup in ADS for the 85/170 frequency doubler based on single Schottky diode (just warm-up, not useful for the following circuit designs)

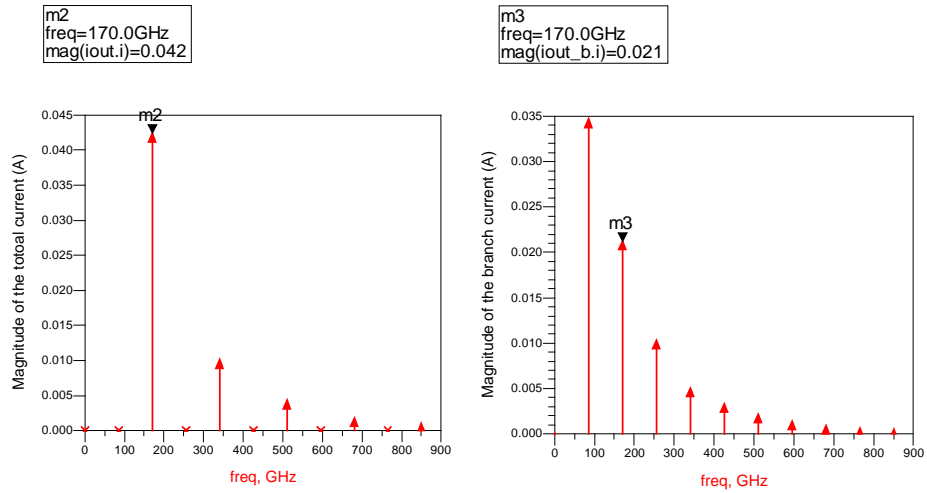
In this circuit setup, both the input and output termination are merged into the pump source and the diode embedding impedance can be specified directly. On the other hand, the DC path is differentiated from the RF path by adding the "DC Block" and the "DC Feed". Particularly a pump power at 1 mW is pushed into the Schottky diode such that the bias voltage can be excluded from the optimising parameter list. Therefore, only the diode embedding impedances are left to determine the circuit performance.

### 3.2.2 Balanced Frequency Doubler



**Figure 3.9:** Schematic and illustration diagram of the circuit setup of ADS harmonic balance simulation for the 85/170 GHz frequency doubler in an anti-series configuration of diode array

Anti-series structure is composed of upper and lower meshes pumped with out-of-phase power source. In the figure (3.9), DC path can be explicitly specified by two "DC Block" which are placed next to the power source in case that the bias DC voltage ruins the RF source, and a pair of "DC feed" in each mesh which are used to isolate the DC voltage source from the RF signal and create DC ground as well. Furthermore, in order to enhance the power handling capability, two diodes in series connection are applied in each mesh, which can be considered as an equivalent single Schottky diode but twice the reverse breakdown voltage. Finally the generated power at the second harmonics is supposed to be absorbed by the load as much as possible.



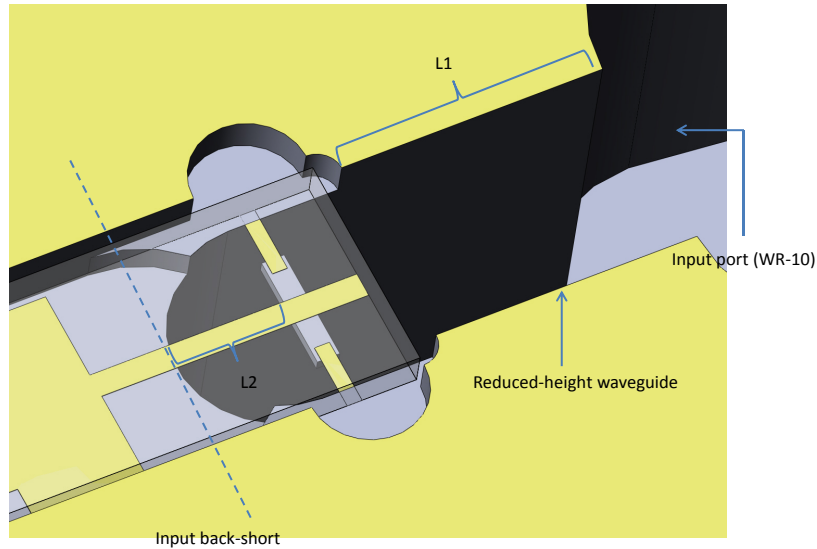
**Figure 3.10:** Power spectrum of the total current  $i_{total}$  and the branch current  $i_{branch}$

By the comparison of the two power spectrum shown above, the main advantage of the anti-series configuration is visualized that the suppression of the undesired odd harmonics takes effect in the load, while the magnitude of the second harmonic component can be doubled.

### 3.2.3 Hybrid Frequency Doubler

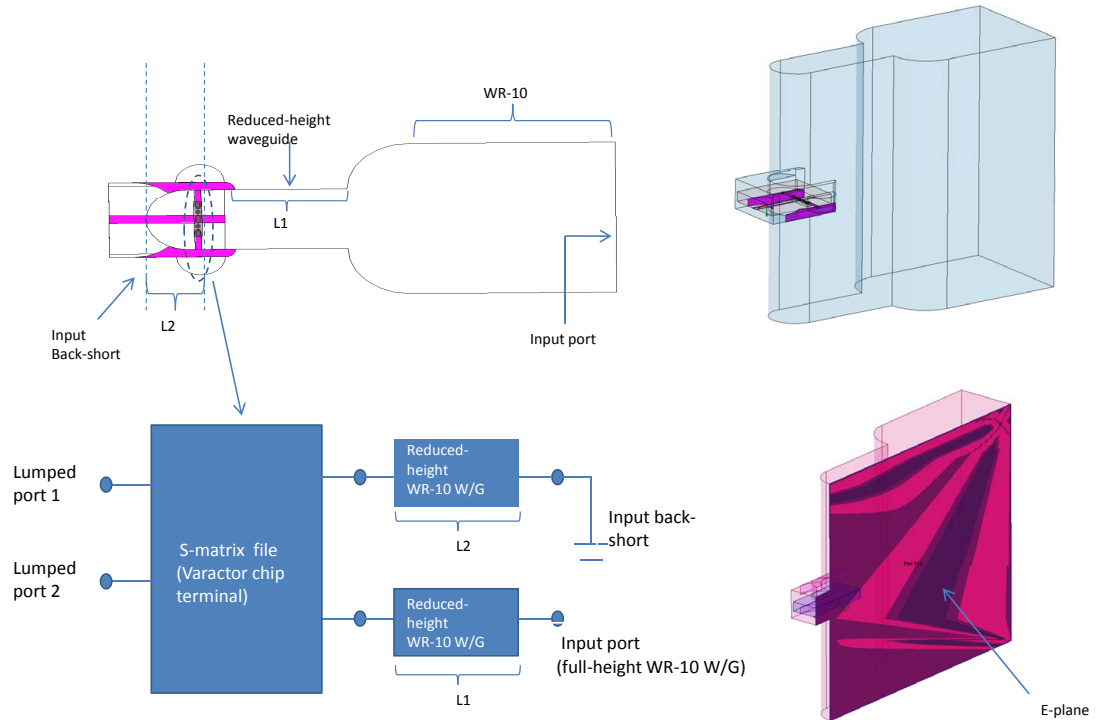
Thickness of GaAs substrate ( $\mu m$ )	50
Thickness of the perfect center conductor ( $\mu m$ )	2
Thickness of the quartz substrate ( $\mu m$ )	100

**Table 3.3:** Material thickness used in the HFSS modelling



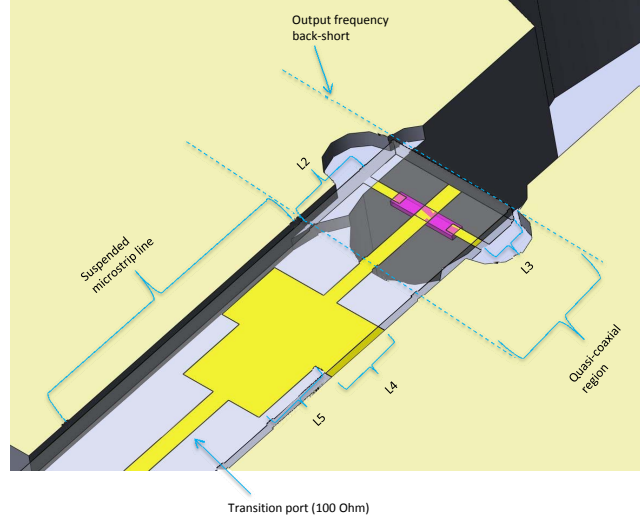
**Figure 3.11:** Structure of the input section for the 85/170 GHz frequency doubler

As is depicted in this structure, the input port of the whole doubler system is provided by the full-height input waveguide (WR-10). Then a quarter-wave transform strategy based on the input reduced-height waveguide is applied to form the input embedding circuit, in conjunction with an effective input back-short. At the pump frequency TE<sub>10</sub> is the only wave mode allowed to propagate in the input waveguide, while the effective input back short would turn the TE<sub>10</sub> into a evanescent mode due to the enlarged cut-off frequency in the following reduced-width waveguide channel. As a result,  $Z_i(f_p)$  and  $Z_o(f_p)$  in the figure (2.8) are respectively well-defined by the input embedding circuit and the effective input back-short. Generally the length of the reduced-height waveguide (L1) and the location of the input back-short (L2) are optimised to achieve a small return loss in the input port, along with an utilisation of symmetry E-plane for the input section.



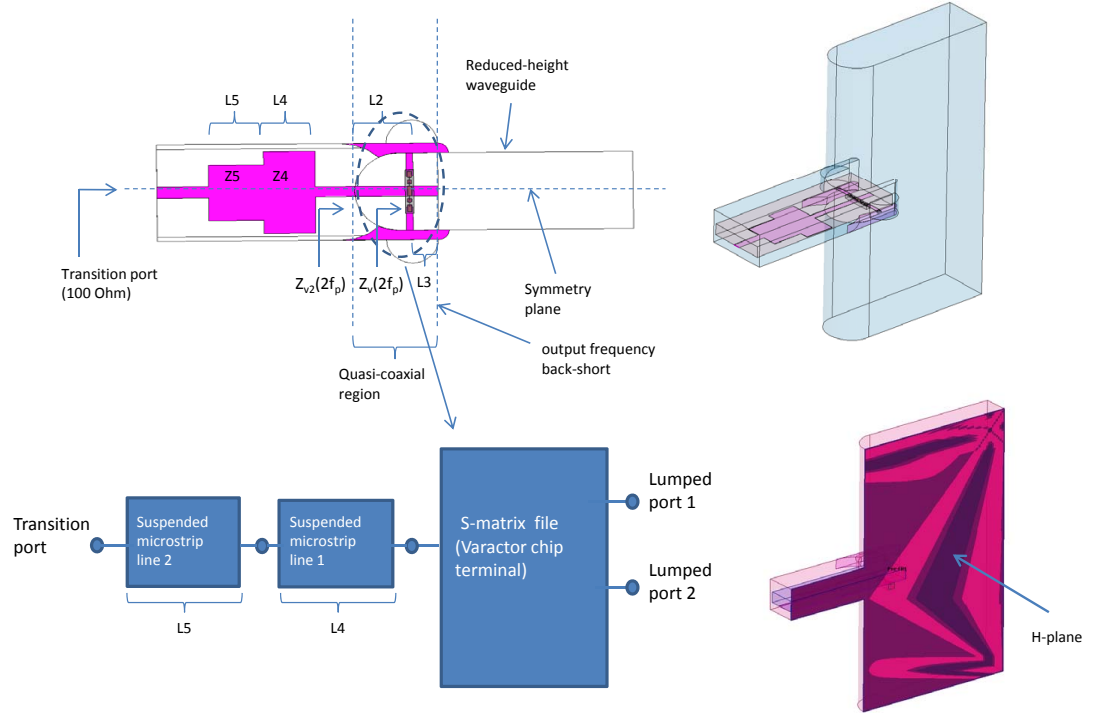
**Figure 3.12:** HFSS and ADS modeling of the input section design for the 85/170 GHz frequency doubler

For the sake of convenience, the specific circuit components applied in ADS setup are replaced here by the simplified functional blocks. Since symmetry E-plane is used for the input section analysis, the imported S file representing the Schottky varactor chip only includes two one-sided lumped ports which would be connected to the diode impedance at pump frequency. Both the input reduced-height waveguide and the input back-short are represented by the corresponding equivalent circuit components in ADS. The optimisation process for the length of the reduced-height waveguide L1 and the location of the input back-short L2 are carried out in ADS. Generally a strong input section design can be identified if the return loss of the input port were below -15dB over a broad bandwidth.



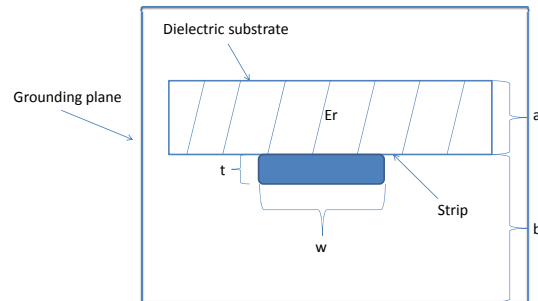
**Figure 3.13:** Structure of the output section for the 85/170 GHz frequency doubler

The output section consists of the effective output frequency back-short caused by the input reduced-height waveguide, and the suspended microstrip quartz circuit which can be classified into two parts. The first part next to the varactor chip is characterised by the quasi-coaxial region, while the second part which forms the output embedding circuit is the standard suspended microstrip transmission line. The excited second harmonic component is radiated in the unbalanced wave mode TEM, passes through the quasi-coaxial region between the varactor chip terminal and the input back-short, and then coupled into the  $100\Omega$  transition port by two-section matching transmission line. On the other hand, many kinds of unbalanced wave modes can propagate in the input section at output frequency. In order to prevent them coupling to the TEM field distribution at output frequency, the input reduced-height waveguide is designed to block the propagation from TM<sub>11</sub> wave mode which has the lowest cut-off frequency among those undesired wave modes in the input section. As a consequence, an effective output frequency back-short is formed as shown in the figure (3.13). Overall,  $Z_i(2f_p)$  and  $Z_o(2f_p)$  in the figure (2.8) are respectively well-defined by the effective output frequency back-short and the output embedding circuit.



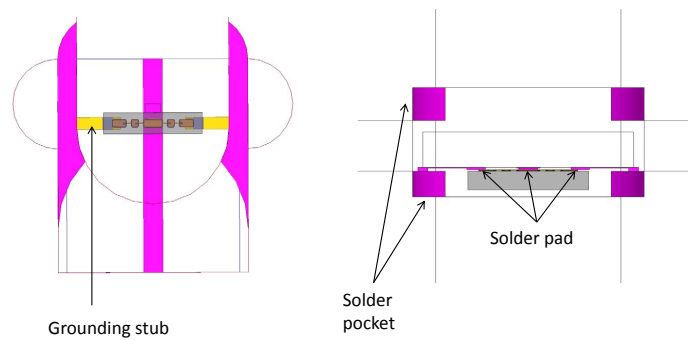
**Figure 3.14:** HFSS and ADS modeling of the output section design for the 85/170 GHz frequency doubler

Aiming to synthesize an appropriate impedance of Schottky varactor chip at output frequency  $2f_p$ ,  $L2$  and  $L3$  are optimised through HFSS simulation and the initial chip impedance  $Z_v(2f_p)$  would be transformed to  $Z_{v2}(2f_p)$  which can ease the output embedding circuit design. Subsequently, the generated S file including the essence of the updated Schottky varactor chip interface would be imported to the ADS equivalent circuit accounting for the output section design. The two section matching transmission line is applied to transform  $Z_{v2}(2f_p)$  to the transition port impedance  $100 \Omega$  as close as possible, and this matching circuit is characterised by the length ( $L4, L5$ ) and the characteristic impedance ( $Z4, Z5$ ) of each section, which are mainly optimised in ADS. Additionally, symmetry H-plane is applied for the output section design and the two lumped ports remaining are connected to the diode impedance at frequency  $2f_p$ .



**Figure 3.15:** Inverse suspended microstrip structure used in HFSS modelling

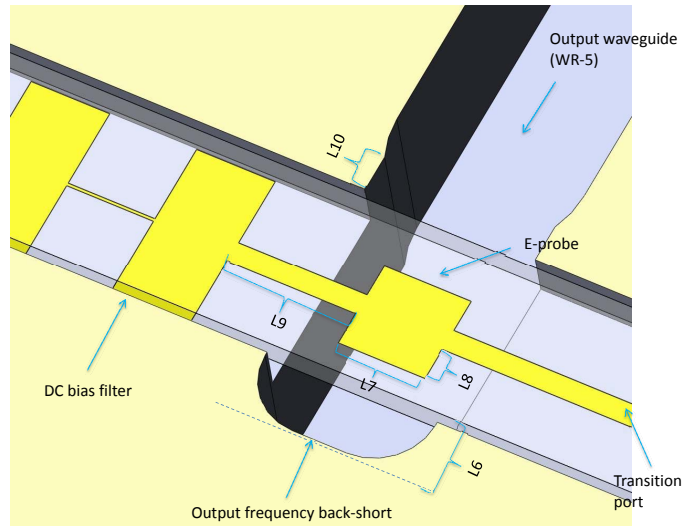
Shield inverse suspended microstrip transmission line is used to ease the mounting process and relieve the system operating sensitivity to the quartz substrate thickness. Its characteristic impedance is directly manipulated by adjusting the width of the centre conductor  $W$ . As a consequence, a look-up table can be built to present the one-to-one correspondence between the centre conductor width and the associated characteristic impedance.



**Figure 3.16:** Profile of the structure set-up for soldering

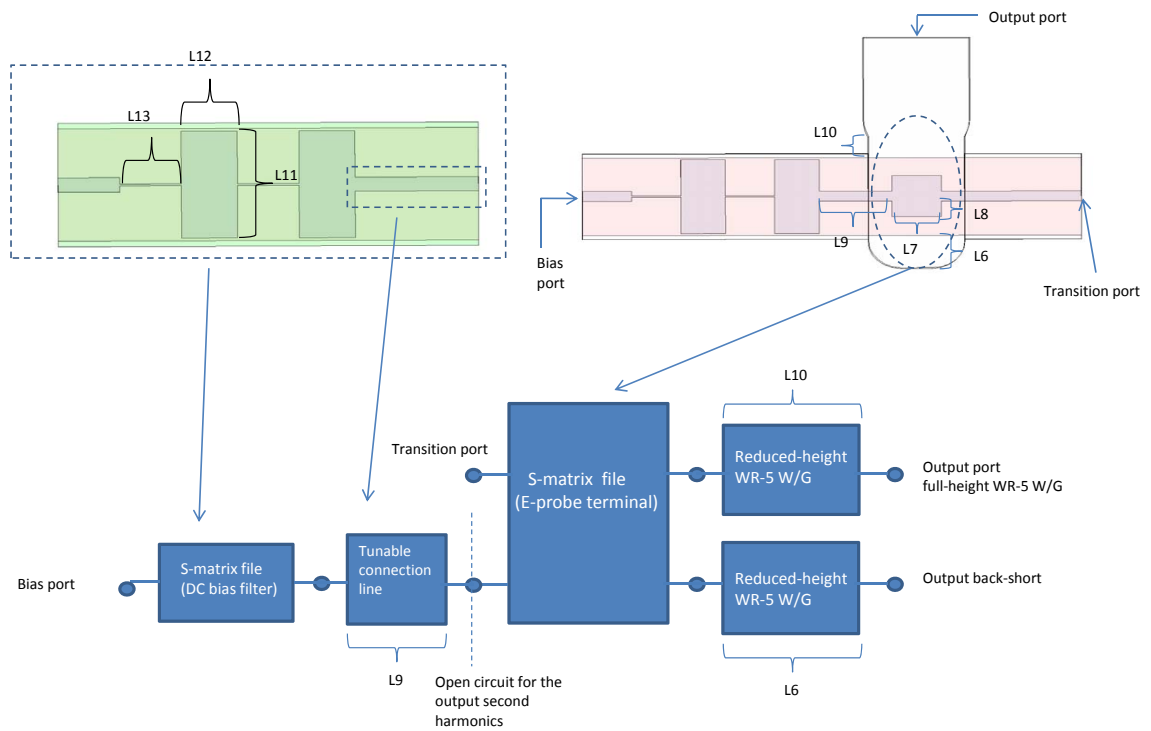
By the solder pads shown above, the balanced GaAs Schottky varactor chip is soldered to the quartz circuit. Then, the assembly process is carried out by mounting the quartz circuit into the E-plane split waveguide cavity. Indeed, each end of the chip grounding stub is merged with the silver epoxy filling in the solder pocket.





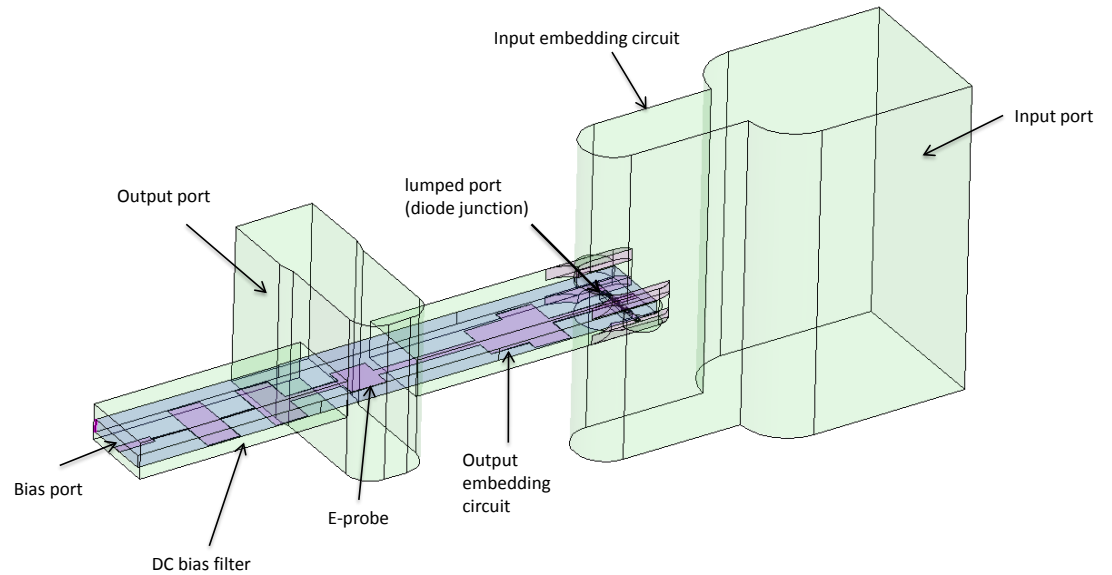
**Figure 3.17:** Output coupling arrangement for the 85/170 GHz frequency doubler

The main body of the output coupling arrangement is E-probe, in conjunction with a DC bias filter, output back-short and an output reduced-height waveguide. Generally the output coupling arrangement serves to couple the radiated power at output frequency of  $2f_p$  from the suspended microstrip transmission line ( $100 \Omega$ ) to the output waveguide (WR-5) as much as possible. The return loss of the transition port would be measured to quantify the coupling effects.



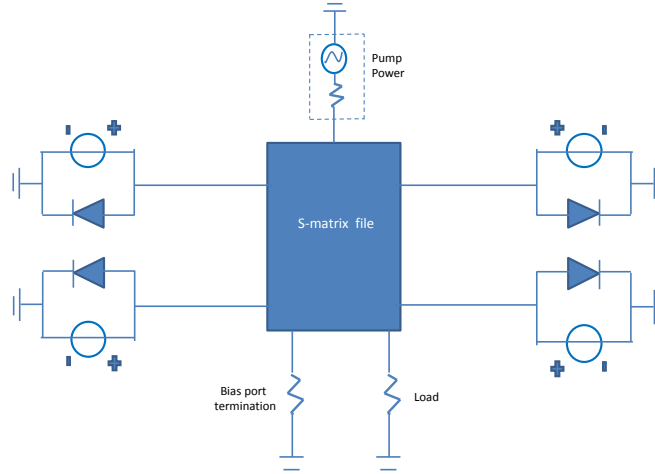
**Figure 3.18:** HFSS and ADS modeling of the output coupling arrangement for the 85/170 GHz frequency doubler

Quarter-wave transformer based filter design is optimized in HFSS to open circuit the output second harmonics at left E-probe terminal, depending on the physical dimensions L9, L11, L12 and L13. Meanwhile, the sizes of E-probe L7 and L8 have been specified prior to importing the S matrix file of E-probe terminal to ADS. Generally, the location of the fixed output back-short L6 and the length of the output reduced-height waveguide L10 are played around in ADS to realize a maximum output power coupling from the transmission line to the output waveguide.



**Figure 3.19:** HFSS modeling of the complete structure of the 85/170 GHz frequency doubler

Finally, all the sub-functional parts of the frequency doubler are integrated in HFSS based on the specified structure shown above. After the linear electromagnetic structure simulation had been done, the generated S matrix file with three wave ports (input, output and bias) and four lumped ports inserted to the location of Schottky diode junction, is imported to ADS so that the nonlinear harmonic balance analysis for the complete doubler structure could be carried out in such a way



**Figure 3.20:** Functional diagram of ADS harmonic balance simulation for the complete structure of the 85/170 GHz frequency doubler

It is noted that the bias port is rendered obsolete and terminated with a matching load, since the imported S matrix file had not included the DC solution. Therefore, Schottky diode is still individually biased by the specified DC voltage source (3.2 V). On the other hand, the source impedance and load impedance are set to be equal to the characteristic impedances of the input waveguide (WR-10) and output waveguide (WR-5) respectively.



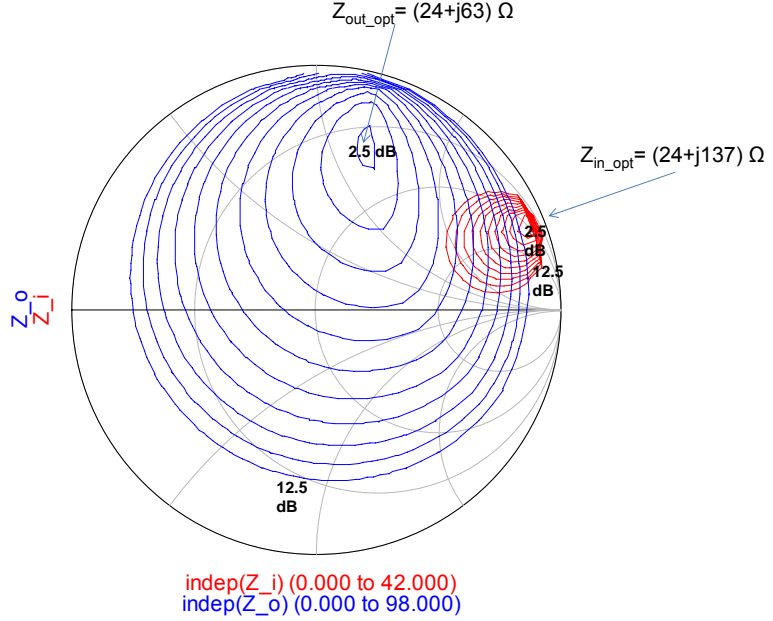
## Chapter 4

# Results

In this chapter, both the large signal simulation results from the harmonic balance analysis and the realistic measurement results, are presented and compared to characterise the fabricated frequency doubler. By exploring the underlying causes for the discrepancies between them, the limitations of the hybrid approach are gradually revealed.

## 4.1 Simulation results

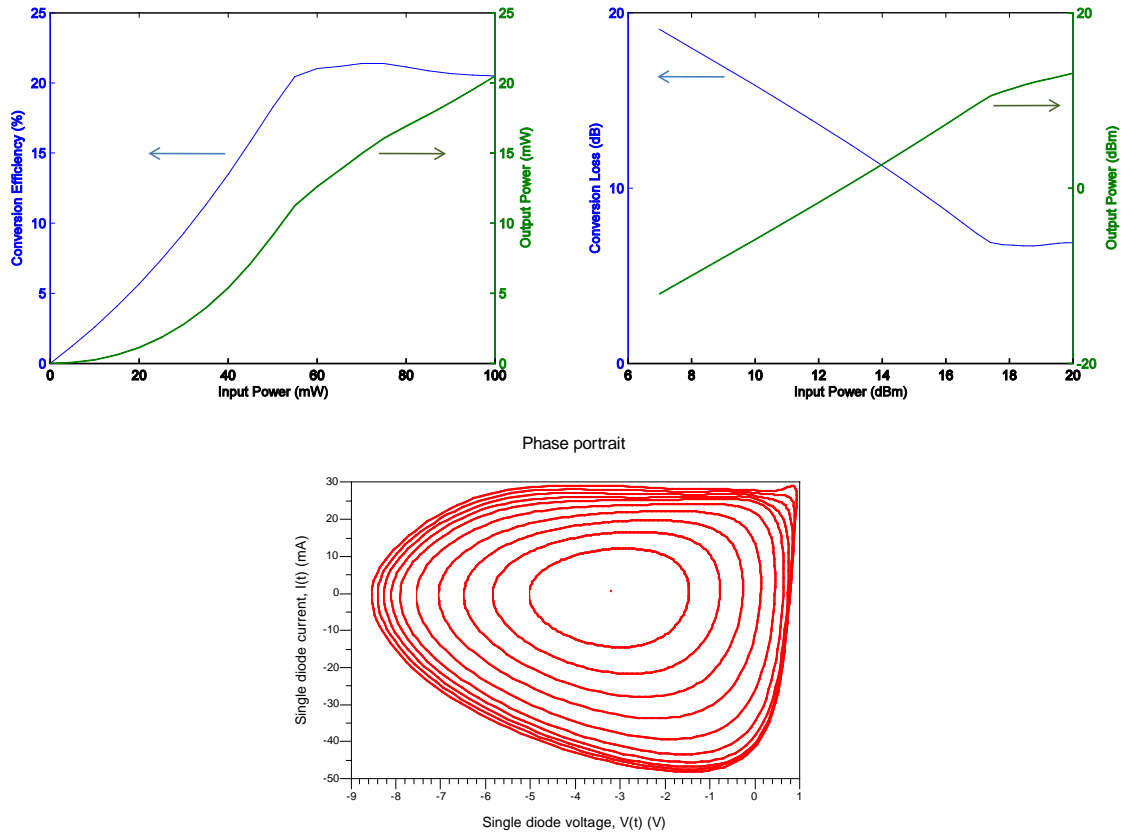
### 4.1.1 Contour plot analysis for the ideal balanced frequency doubler circuit



**Figure 4.1:** Contour loss contours versus input and output diode embedding impedance, obtained from load-pull harmonic balance simulations in ADS for the ideal 85/170 GHz balanced frequency doubler, with a diode junction area of  $20 \mu m^2$ , a bias voltage of 3.5 V for single Schottky diode model and a total pump power of 40 mW. The minimum conversion loss is 2.5 dB and the contours correspond to 1 dB increment of the conversion loss

The efficiency contour plot makes it possible to conduct a trade-off between the diode embedding impedances, the conversion loss and the bandwidth. Apparently, the contours show that the conversion efficiency is more sensitive to the input diode embedding impedance than the output. Furthermore, theoretically the minimum conversion loss can be acquired only when the simultaneous conjugate matching conditions are fulfilled both the input and the output section. In other words, if the optimum diode embedding impedances for the minimum conversion loss have been found in the contour plots, the diode impedances can be obtained through the conjugate transformation of those optimum diode embedding impedances. As a result, the diode impedances at pump frequency  $Z_d(f_p)$  and the second harmonic frequency  $Z_d(2f_p)$  are found to be  $(24-j137) \Omega$  and  $(24-j63) \Omega$  respectively, which would be used in the HFSS simulation as the lumped port impedance.

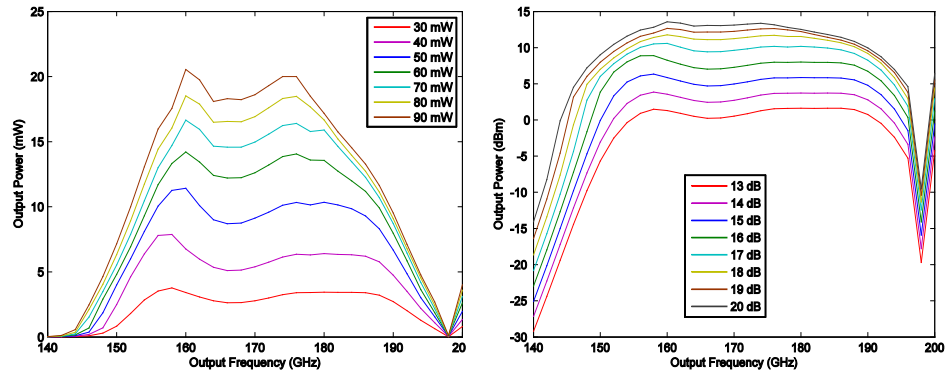
### 4.1.2 Harmonic balance analysis for the complete structure of the hybrid balanced frequency doubler



**Figure 4.2:** Simulated output power and conversion efficiency versus pump power for the 85/170 GHz frequency doubler at the nominal output frequency of 170 GHz with a bias voltage of 3 V for each diode, as well as time domain terminal voltage  $V(t)$  versus time domain flowing current  $I(t)$  for each diode model with the varying pump power levels at the nominal output frequency of 170 GHz

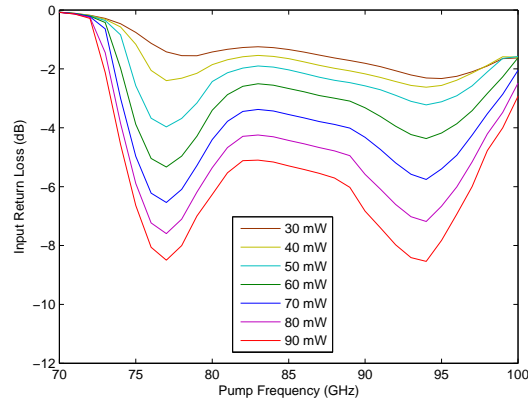
Corresponding to a maximum conversion efficiency (21 %) at the nominal output centre frequency of 170 GHz, the pump power is found at 70 mW along with an output power of 15 mW. The diode  $I(t)$  vs  $V(t)$  characteristic curve shows that during the pumping cycle, the minimum voltage across the diode terminal is still larger than the reverse breakdown voltage (-9.3 V), even with the optimum pump power. Therefore, there is still some room for the improvement of the diode operating conditions, so to reach the "full" drive for each Schottky diode to achieve the maximum conversion efficiency.





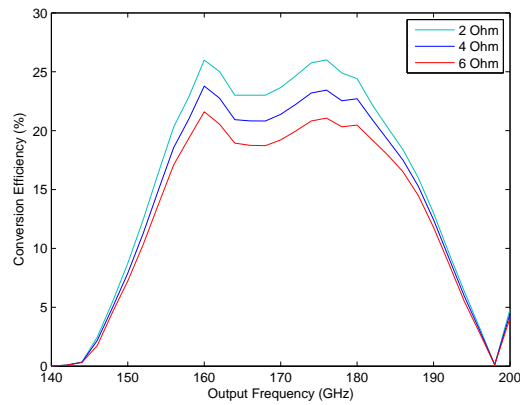
**Figure 4.3:** Simulated output power versus output frequency for the 85/170 GHz frequency doubler, with a bias voltage of 3 V for each diode at varying pump power level

According to these simulation results, the frequency doubler turns out to be a broadband design as expected, where two resonances become more and more obvious when the pump power increases, and the doubler performances at the output centre frequency are more or less compromised. With a pump power of 70 mW, the simulated 3-dB fractional bandwidth is up to 22% with a peak output power around 16 mW at the output frequency of 160 GHz and 177 GHz respectively.



**Figure 4.4:** Simulated input return loss versus output frequency for the 85/170 GHz frequency doubler with a bias voltage of 3 V for each diode at varying pump power level

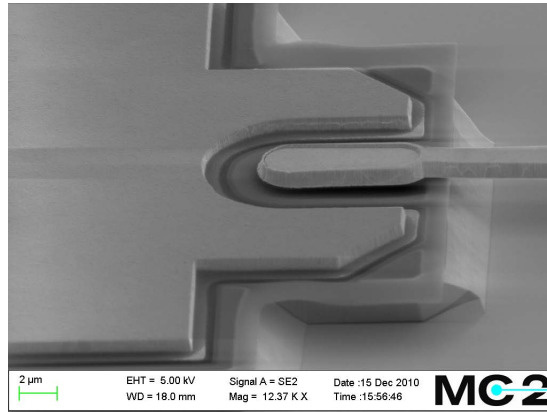
In accordance with the previous simulations, the broadband character is also verified by the simulated trends of the input return loss of the doubler input port, especially for a large pump power. However, the simulated values of the input return loss are quite far away from the expected, which may be one of the main sources limiting the doubler conversion efficiency.



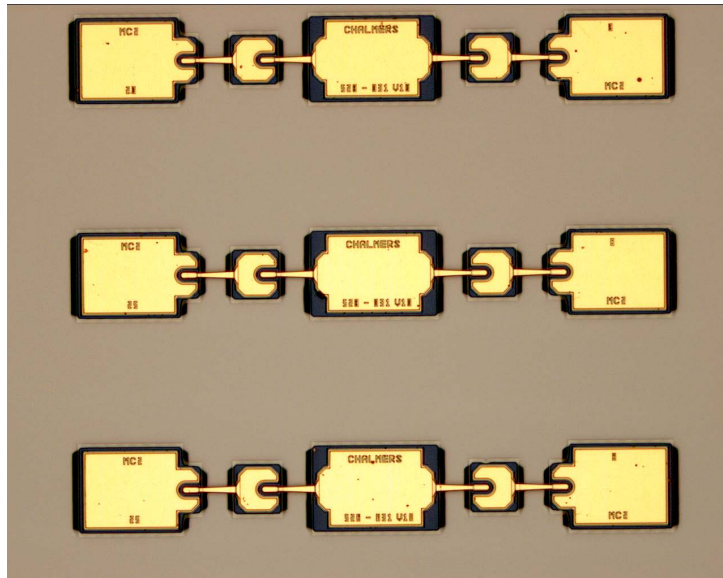
**Figure 4.5:** Simulated conversion efficiency versus output frequency for the 85/170 GHz frequency doubler with a pump power of 70 mW, a bias voltage of 3 V for each diode but varying series resistance

These simulation results prove the theoretical assumption that the conversion efficiency is inversely proportional to the series resistance. However, through the fabrication and mounting process, the real existing series resistance may deviate from the corresponding empirical value applied to the earlier circuit simulations. Accordingly, a large design uncertainty is inevitably introduced.

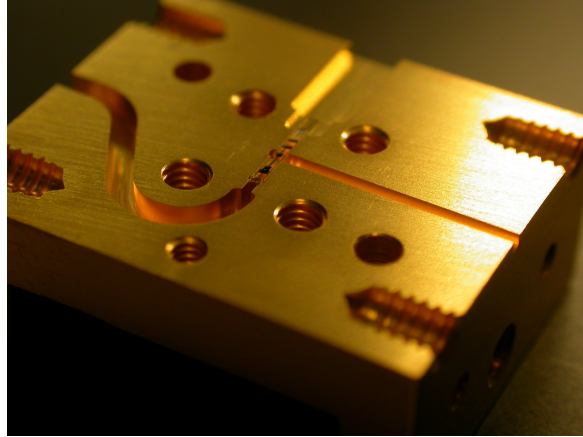
## 4.2 Measurement Results



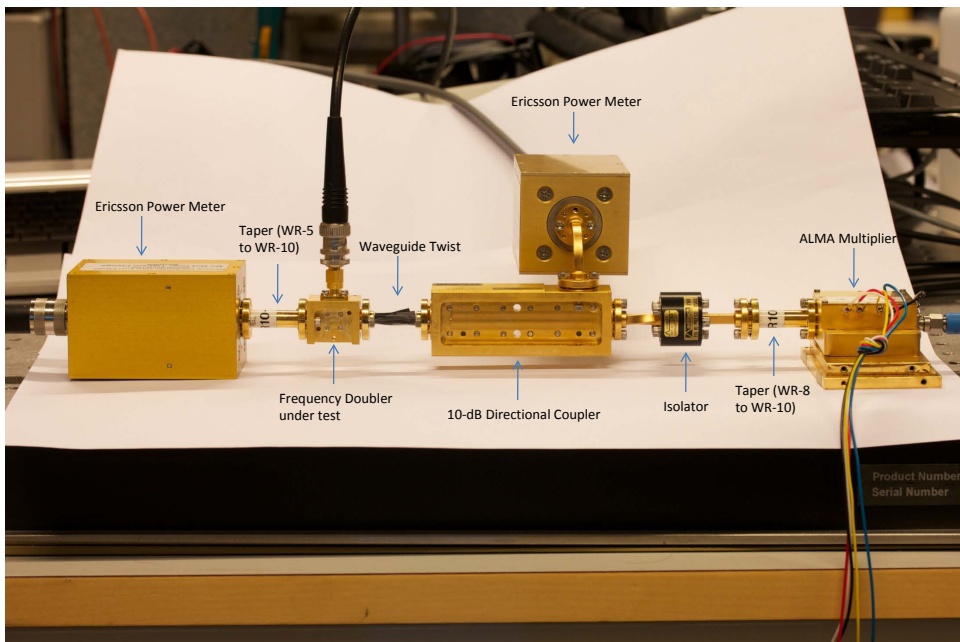
**Figure 4.6:** A scanning electron microscopic photograph showing the Schottky diode geometry with the anode area of  $20 \mu\text{m}^2$



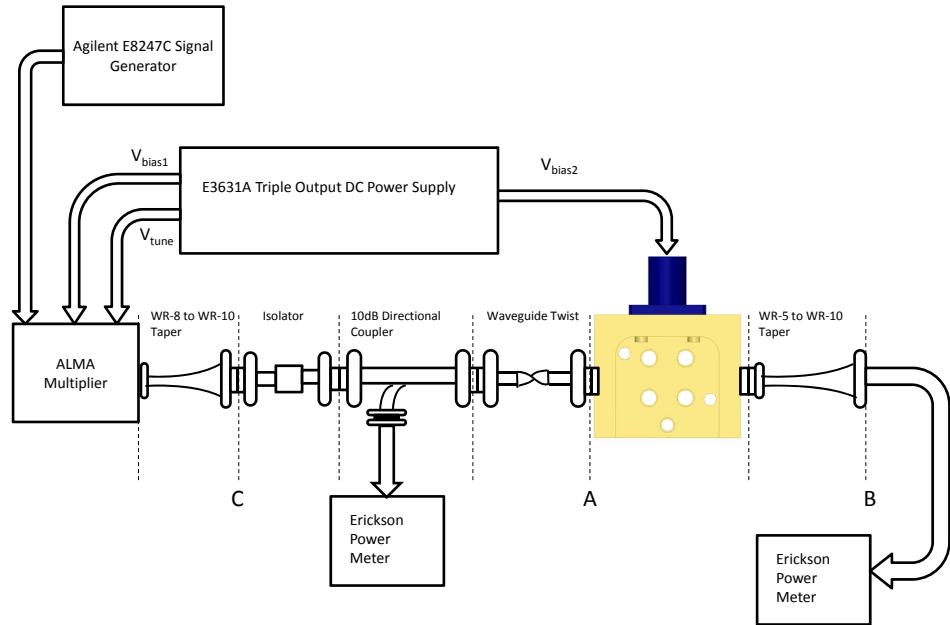
**Figure 4.7:** Micrograph of the planar Schottky varactor chip where four diodes are connected in the anti-series configuration



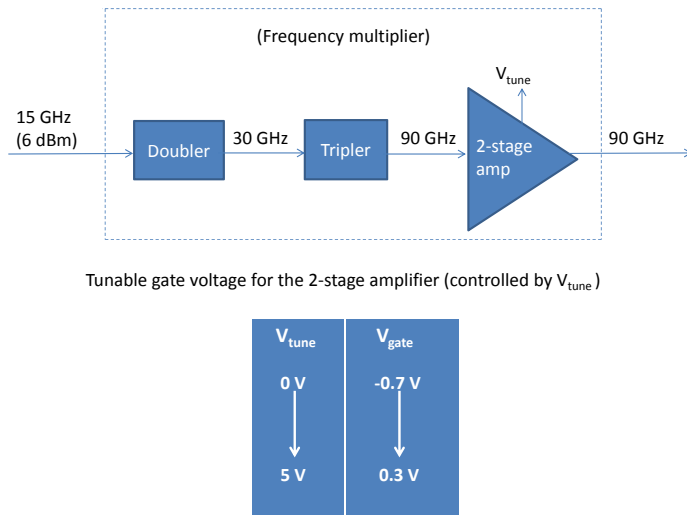
**Figure 4.8:** Exploded view of the hybrid balanced frequency doubler



**Figure 4.9:** Measurement setup for the characterisation of the frequency doubler



**Figure 4.10:** Illustration of the measurement setup for the characterisation of the frequency doubler

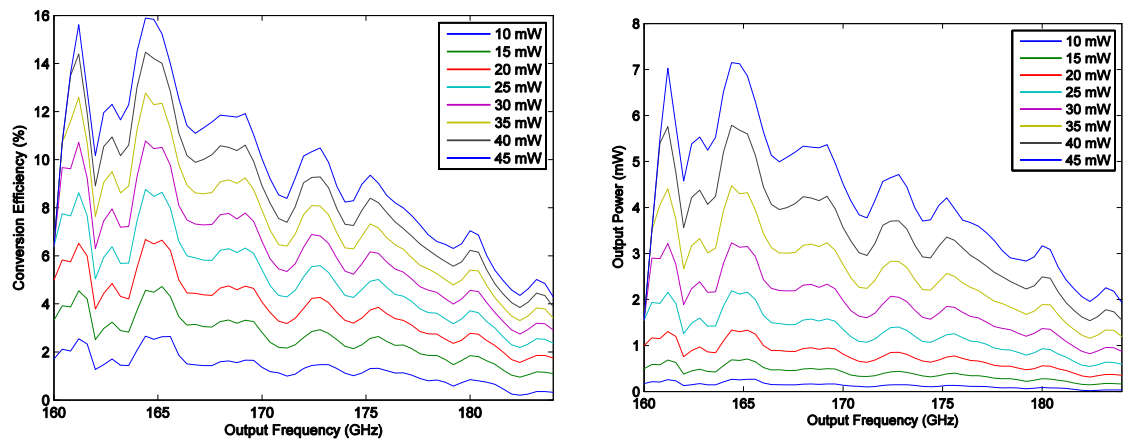


**Figure 4.11:** Constitution of the commercial frequency multiplier applied to the source signal generation

Combining the Agilent E8247C signal generator with the ALMA W-band water-vapour radiometer active frequency multiplier ( $\times 6$ ), an adjustable pump source from 80 to 90 GHz is available, with a wide tuning range of the pump power from 0 to 80 mW (in case of extreme drive). As is shown in figure (4.11), the ALMA frequency multiplier consists of a frequency doubler, a cascaded frequency tripler and a two-stage power amplifier in the end. The E3631A Triple Output DC Power Supply provides bias voltage  $V_{bias1}$  to ALMA frequency multiplier for its normal operation, while a second bias voltage  $V_{tune}$  feeding the gate terminal of the two-stage amplifier, is used to control the generated pump power out of the ALMA frequency multiplier.

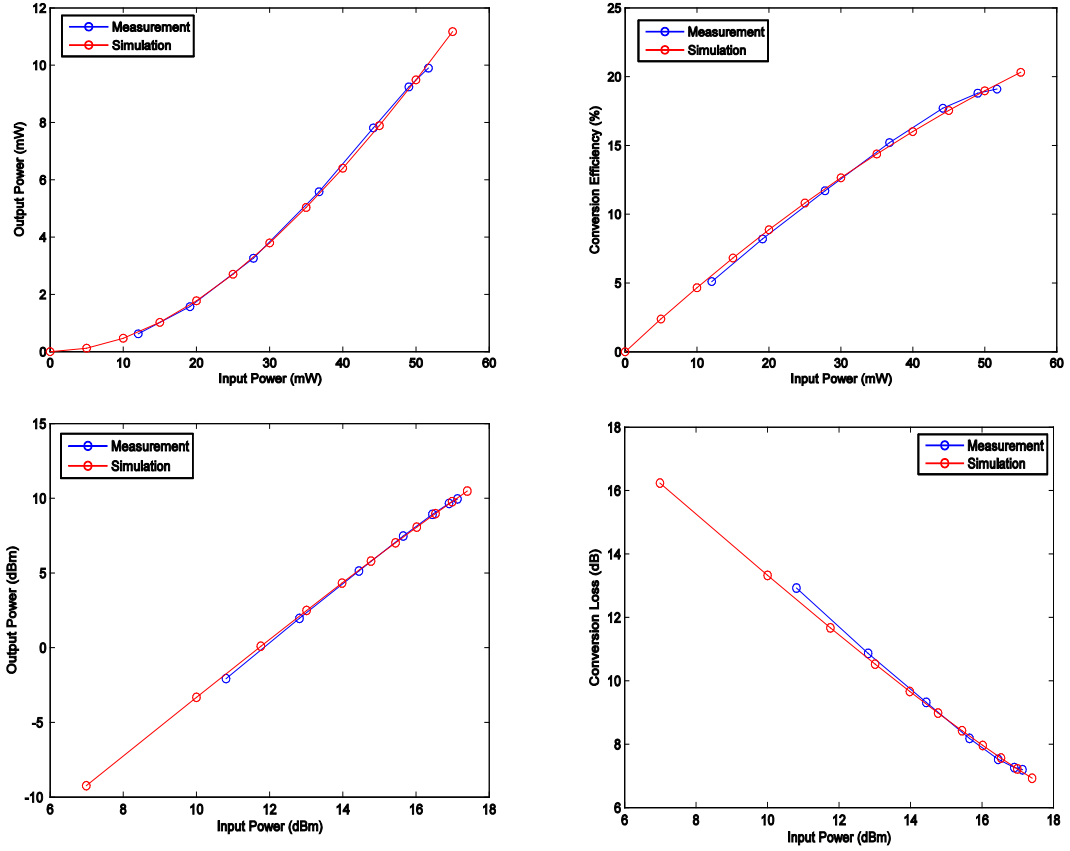
After that, an isolator is inserted to minimize the reflected standing wave emanating from the rest of the measurement setup. Also, a 10-dB directional coupler is placed in front of the frequency doubler under test for the measurement of the input return loss. Preliminarily the reference point "A" and "B" should be connected directly without the doubler block, and the real pump power  $P_f$  can be captured by the Erickson Power Meter from the through port of directional coupler. After reconnecting the frequency doubler, a portion of the reflected pump power  $P_{coupling}$  out of the coupling port of the directional coupler can be read, and the total reflected pump power  $P_{reflection}$  can be restored through the following mathematic manipulation:  $P_{reflection} = P_{coupling} * 10 + P_{loss}$ , where  $P_{loss}$  accounts for the extra loss induced by the waveguide twist which is considered integral to the directional coupler.

The frequency doubler is precisely biased by  $V_{bias2}$  from the remaining unoccupied output port of the E3631A Triple Output DC Power supply. Finally, the output power  $P_{2f}$  of the frequency doubler would be detected by the Erickson Power Meter and associated conversion efficiency can be calculated out. The following measurement results are used to characterise the fabricated frequency doubler with a diode junction area per anode of  $20 \mu m^2$ .



**Figure 4.12:** Measured output power and conversion efficiency versus output frequency for the 85/170 GHz frequency doubler, with the  $V_{bias2}$  of -5.3 V and varying pump power level

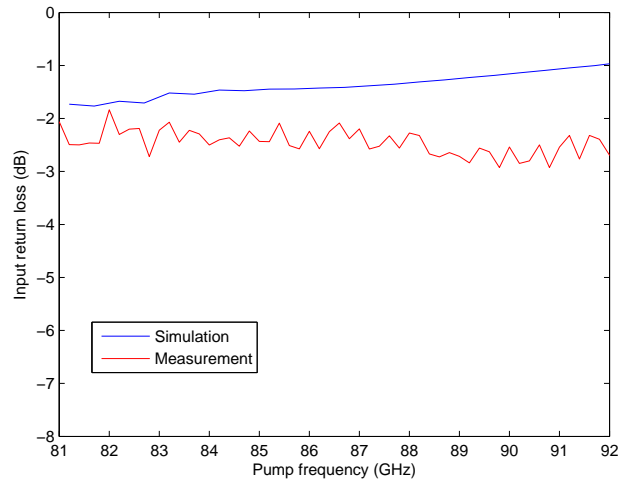
It turns out that a peak output power of 7 mW is available at 165 GHz with a conversion efficiency of 16%. However, the 3-dB bandwidth cannot be extracted from these measurement results since the doubler performances at lower frequency band (below 160 GHz) have been distorted, due to the band limitation from the power amplifier being used in the generator system. If a broadband power amplifier were available, the doubler performance could be possible to be retrieved for the missing frequency band. If so, the 3-dB fractional bandwidth of the doubler is estimated to be 15% for a medium pump power. On the other hand, the applied maximum pump power is only 45 mW temporarily due to the lack of a high power source.



**Figure 4.13:** Curve fitting for both the output power and the conversion efficiency versus the pump power between the simulation and the measurement, for the 85/170 GHz frequency doubler at the output frequency of 168 GHz with the  $V_{bias2}$  of -5.3 V

The measured conversion efficiency turns out to be directly proportional to the pump power at output frequency of 168 GHz. When the pump power goes up to 50 mW, the measured conversion efficiency approaches 20% with an output power of 10 mW. For a higher pump power, the frequency doubler enters into the saturation region gradually. Meanwhile, a resultant curve fitting can be made between the measurement and simulation, by adjusting those tuning prime parameters of the diode model, such as the series resistance, the parasitic capacitance and the forward conduction barrier potential. Compared to the initial values which are listed in the table (3.2), the parasitic capacitance, the series resistance and the forward conduction barrier potential are set to be 13 fF, 2  $\Omega$  and 0.8 V respectively for achieving an agreement between simulation and measurement. In other words, both the package parasitic capacitance and the effective diode series resistance prove not being precisely referred during the modelling process.

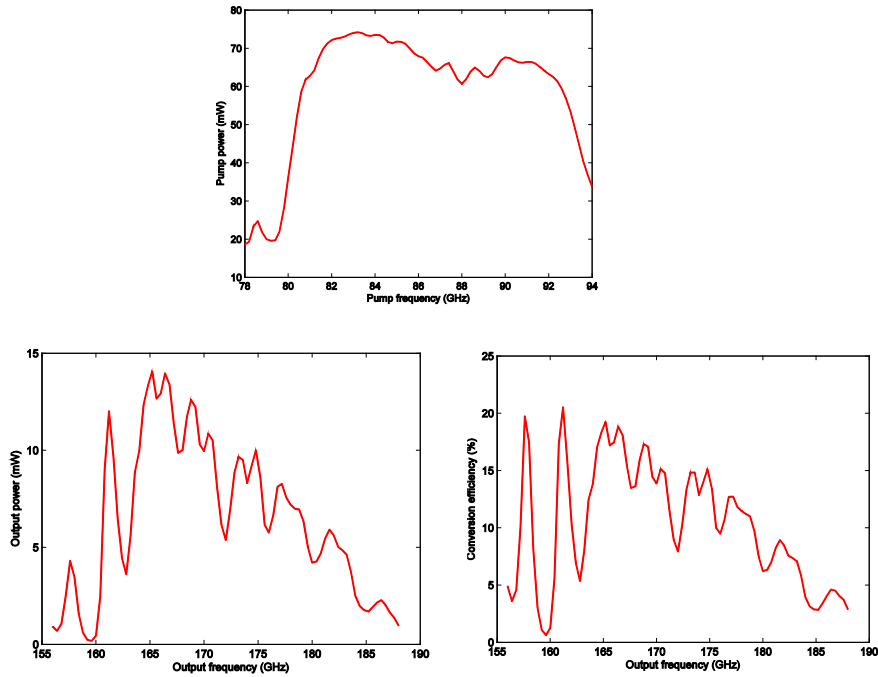




**Figure 4.14:** Comparison of the input return loss versus output frequency between the measurement and the simulation, where the relevant design parameters of the diode model have been updated according to the last simulation (4.13), for the 85/170 GHz frequency doubler with the  $V_{bias2}$  of -5.3 V and a pump power of 30 mW

Generally, 1 dB discrepancy on average is found in the input return loss results between the measurement and simulation. It is partly due to the extra circuit loss existing in the experimental setup. Obviously the measured excessive input return loss could be the main factor limiting the doubler conversion efficiency. Therefore, it is speculated that the bottleneck of the doubler system should be the input section which is tightly associated with the input return loss.

Finally, in order to reveal the full power potential of the doubler, some adjustments are done to the existing measurement setup for generating more pump power. One more power amplifier is added to the generator system and the isolator is removed to facilitate the interaction between the generator and the frequency doubler under test.



**Figure 4.15:** Measured pump power, output power and conversion efficiency for the 85/170 GHz frequency doubler, with the  $V_{bias2}$  of -5.3 V under the updated measurement setup

Under the safe drive level for the power amplifiers, the frequency doubler can handle at least 70 mW of pump power, with a corresponding output power of 14 mW and conversion efficiency of 17%. Although this measurement result tends to reflect more things about the essence of the whole integrated system rather than the pure characterisation of the doubler itself, it can still offer the profile of the power handling capability of the frequency doubler. Furthermore, an excessive doubler output level of 20 mW is also observed when pushing the power amplifiers into compression.



## Chapter 5

# Conclusion

Although the expected broadband output of the frequency doubler cannot be fully presented due to the restrictions of the realistic experimental setup, an estimated 3-dB fractional bandwidth of 20% is still given under a medium pump power. In order to explore the full power potential of the doubler under test, some adjustments are done to the initial measurement setup to boost the pump power. As a result, the maximum output power the doubler can achieve is observed to be 20 mW if the power amplifiers is driven to compression region. Generally, both the broadband characteristic and the strong power handling capability are roughly achieved by the doubler. On the other hand, as we anticipated, the measured conversion efficiency turns out to be more or less compromised for the bandwidth extension. Besides the inherent design strategy, another source limiting the conversion efficiency is the unsuccessful input section design, which is revealed by the excessive measured input return loss. Given more time, there is a strong need to re-optimize the input section combined with those solder structures shown in the figure (3.16). Additionally, a further thermal analysis should be carried out to evaluate the operational condition of the GaAs Schottky varactor chip in the future, especially for high power cases.

Talking of the discrepancies between simulations and measurements, one of main causes is the diverse measurement environments which introduces varieties of extra circuit loss. Furthermore, the solder pads required by the hybrid approach, could bring in some extra parasitic capacitance and extra series resistance which aggravate the deviations between the chip 3D package modelling in HFSS and the real fabricated chip structure. Therefore, the harmonic balance simulation results fail to fully reflect the essence of the doubler. In spite of that, rough performance agreements between the measurement and the simulation, are still achievable at certain output frequency, by fitting the parasitic capacitance and the series resistance into the practical values as close as possible, through harmonic balance simulations. Moreover, another source of design uncertainty arising from the hybrid approach is the varying length of the chip grounding stub shown in the figure (3.16). During the assembly process, the conductive silver epoxy filling in the solder pocket is likely to cause perturbation to the length of the grounding stub, which is a critical circuit parameters in terms of sensitivity.

To cope with those kinds of design uncertainty sources induced by the hybrid approach, more sensitivity analysis of the doubler operating condition have

to be implemented prior to the fabrication stage, so as to ensure the current design is robust enough to afford those design parameter perturbations in the assembly process. Meanwhile, developments of more subtle modelling for those engineering uncertainty sources, are worth the efforts to bridge the gap between the simulation and the measurement. Nevertheless, with the operating frequency increasing, it becomes a more and more severe task to compensate for the limitations of the hybrid approach, since any associated design uncertainty is supposed to exert more negative influence on the measurement performances once the doubler circuit dimension shrinks. Alternatively, a monolithic approach (MMIC) is more suitable for the frequency doubler design at several hundred GHz because the tedious assembly process can be avoided. Accordingly, diverse sources of design uncertainty should be eliminated effectively and more reliable simulation results can be obtained to estimate the realistic doubler performance precisely. Until now, Schottky diode based frequency doublers have been reported to manage to operate up to 800 GHz [43], with a fixed-tuned broadband and an output power large enough to pump mixers of various kinds.

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