CHALMERS

Design of a Bidirectional On-board Battery Charger in Hybrid Electric Vehicle Applications

Thesis for the degree of Master of Science

Mehdi Javdani Erfani

Division of Electric Power Engineering
Department of Energy and Environment
Chalmers University of Technology
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MASTER OF SCIENCE THESIS 2011

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Abstract

The main objective of the thesis is to design an onboard battery charger which consists of a bidirectional ac <-> DC bridge and a bidirectional DC-DC fullbridge converter. The thesis is divided in two parts: Power losses analysis and controller design.

Power losses analysis is performed for the transformer, inductor and switch losses. For different switches, MOSFETs and IGBT types, losses are calculated and compared. Also losses, when the synchronous rectification method is used, are calculated. Finally a comparison between the switch losses of the bidirectional and the unidirectional converter has been drawn.

Using Fourier analysis to determine the flux harmonic components, it is seen that transformer core losses contribute around 30% of the total DC-DC converter losses for this application. For a battery voltage of 400V, the total switch losses for the best MOSFET and IGBT are 122W and 78W respectively which corresponds to 78% and 67% of the total DC-DC full bridge buck converter losses. It is realized that for this application, IGBTs have lower switch losses. Moreover, synchronous rectification does not reduce the losses in this application significantly. While Schottky diodes have a generally lower voltage drop than P-n power diodes and do not have reverse recovery losses, it is found that in some MOSFETs, their fast body diode can perform as good as an external Schottky diode.

For the DC-DC buck converter, with the selected elements and cores, the total efficiency of 94.5-96.5% is observed (for the output power of 3.6kW, it means 150W losses) and this value for the DC-DC boost converter (in discharging mode) is 95-96.5%.

The whole onboard charger efficiency for charging and discharging mode is 93.5-94.5% and 93.3-94.8% respectively (depending on the battery voltage).

The second part of the thesis consists of the design of a controller for the onboard charger. It is composed of the design of controllers for the DC-DC converter, the rectifier and the inverter.

The ac< >DC bridge should satisfy the harmonic current limitations based on standards like IEC 61000. For the rectifier with a cascaded PI compensator, a THD of 2.5% and PF of 0.99 are achieved. For the inversion mode, with utilizing PWM unipolar switching and PI compensator, a THD of 0.5 % and PF of ~1 were obtained. For the DC-DC converter, with the help of a compensator, with high phase and gain margin, the output voltage became overshoot free.

Acknowledgement

First and foremost I would like to express my deepest gratitude to my Examiner and supervisor, Professor Torbjörn Thiringer, not only for his kind support and guidance in all phases of this work, but also for his generosity in sharing untouched ideas, neat suggestions and in general, a whole new perspective on the way of observations, researching and skeptical and full-dimensional analysis of phenomena he gave me during the last year. His friendly and earnest attitude, created a constructive environment which could bring out the best in me and I wish this friendship lasts.

I would also like to thank Saeid Haghbin, PhD student at department of Electric Power Engineering (EPE), who gave me courageous and great support, such as worthwhile academic discussions and guidance and introducing great references whenever I needed.

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I would also like to appreciate Andreas Karwonen, PhD student at department of EPE for his help on reverse recovery losses calculation.

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The last but not least, I would like to thank Dr. Ghasem Aghdam for introducing such a challenging and interesting subject and his help during the first stages of the work when I was orientating towards the subject.

"All of us failed to match our dreams of perfection. So I rate us on the basis of our splendid failure to do the impossible"

-William Faulkner

I would like to dedicate this work to Kaveh, my brother. I wish him fortune and good luck in the future.

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1 Introduction

1.1 Background, definitions and basic concepts

Nowadays, due to oil price, and increasing need of energy sources on one hand, and environmental issues on the other hand, there is a strong willingness, especially among developed countries to reduce the portion of fossil fuel consumption. There is a great demand in vehicle industry to reduce CO2 emission. Consequently some different energy sources have been introduced. But still some of them have environmental impact and maybe not economically acceptable for customers.

Hybrid Electric Vehicles (HEVs) are the most convenient kinds of HVs, because they have some advantages over their competitors:

1. The amount of energy that batteries can store is increasing everyday and now HEVs can travel some hundred kilometres with improved Lithium-ion batteries (LIB). By introducing (Lithium-ion polymer) Li-Pol batteries in 2008, a major effect on Electric Vehicle industries can be expected. [1]

2. A rough calculation shows that Electricity is much cheaper that oil for vehicle owners:

At the moment with 2*kWh* energy, a conventional hybrid car can reach 10 *km* and further more[1] (At light traffic). The battery capacity, $W_{Battery}$ of such a car can be 20*kWh* (such as some models of Toyota Pirus). It means that with a conventional Li-ion battery, 100*km* range is not a wrong expectation. Electricity price, Ep is around $1kr/kWh$:

$$Electricity\ price(for\ 100km) = W_{Battery}\ E_P = 20 \times 1 = 20\ SEK$$

This should be added to the battery cost. Based on Deutsche Bank claim, Li-ion battery package price[2] for each kWh is as low as 3500 SEK [2] (Deutsche Bank forecasts that this price will be reduced dramatically in near future) for a 20kWh battery this will cost around 70000 *SEK*. A battery should be able to work for around 7-8 years and with the rate of one deep discharge cycle per day, it should be able to provide 2560-3000 cycles in its lifetime:

$$Battery\ price\ (for\ 100km) = Battery\ price\ for\ each\ cycle = \frac{70000}{3000} = 23\ SEK$$

This results in total costs of 43 SEK for 100km travel

Currently oil price, *Op* in Sweden is around 12*kr/litter*.

While at the same time the price of petroleum to reach 100 *km* for a normal gasoline car (with 7 litter consumption per 100*km*) would be:

$$Totlal\ price(100km) = 7 \times O_p = 7 \times 12 = 84\ SEK$$

Comparing these values show that latter case is around 2 times more expensive. [2]

3. Environment friendly.

---

[1] Tesla Roadster with 53 kWh (Li-ion battery) capacity obtains Electric range of 393 km.While lighter cars like the EV1 use about 11 kWh/100 km (halved)

[2] Package price Includes the wiring and configuring of battery packs into a battery array, plus the battery management system that monitors and manages the battery performance

Bidirectional PEHV: Bidirectionality means the possibility of power flow in both directions: from battery (Vehicle) to the grid (V2G) and from grid to the battery (G2V).

V2G operation is a key feature of the smart grid: Due to increasing oil price trend and the environmental issues, there are strong motivations and inceptions towards using local sustainable environmental friendly energy sources such as solar cells and micro turbines. Utilizing Vehicle batteries as a local storage becomes meaningful in this frame. Car batteries can help the grid stability and demand especially at peak hours.

A bidirectional PEHV needs a bidirectional charger to fulfil V2G operation, and accordingly investigations around their design, functionality and efficiency is of at most interest.

It is just recently that this topic becomes interesting for both industry and university. This thesis deals with these state of the art chargers in academic level and discuses some aspects of a bidirectional converter such as power losses and control stages.

1.2 Aim and layout of the thesis

The main objective of this project is to propose and design a bidirectional on-board charger with the aim of charging a plug-in vehicle battery. More in detail, different parts of the bidirectional onboard charger including a rectifier (PFC), an inverter, and a DC-DC converter have to be designed and simulated. The target is to find the efficiency of each converter and the total onboard charger as well.

Additionally, although in some articles different aspects of unidirectional full-bridge converters have been studied, few of them thoroughly investigate the power losses in bidirectional converters. Especially the effect of reverse recovery current of the diodes in the full bridge topology is not fully formulated. The same can be said about the transformer core losses, when immediate flux variations in a core can cause excessive losses. It is found out that regarding switching and core losses, some general simplifications are not quite correct.

Finally, for each converter a robust and a simple controller have to be implemented and the controllers' back to back operation should be verified.

The charger have to convert 220Vac on the grid side to 300~400VDC on the battery side.

In Chapter 1 a short description about basic concepts and some benefits of using Electric vehicle is presented. At chapter 2, more technical issues and different solutions are discussed briefly and finally one of them is chosen to be our ultimate topology. In chapter 3, old theories regarding different converters, filter design, transformer and inductor design criteria and finally in the last part battery study which contains battery types, their pros and cones, modelling and charging methods are included. Most of the materials in chapter 1, 2 and 3 are gathered from different sources and they can be skipped if the reader already has some command on them.

Chapter 4 discusses the sources of power losses in a converter. The effect of reverse recovery charge is less known. If the components are not chosen wisely, the converter efficiency can be reduced significantly. This chapter may be a key to understand next chapters as some equations and concepts which will be used later, are introduced in chapter 4.

The focus in chapter 5 is on switch losses. The role of reverse recovery and two methods to calculate it, is studied and the losses of 20 MOSFETs and 5 IGBTs are compared with each other. IGBT thermal effect, P-n and Schottky diode losses and losses of synchronous rectification method are investigated in this chapter.

The total losses and efficiency of the DC-DC converter in buck and boost operation mode are investigated in chapter 6 and 7 respectively.

Chapter 8 discusses about the control design of the DC-DC full bridge converter and the way to design a robust compensator, without any output voltage overshoot.

In chapter 9, a control system for ac <-> DC bridge is proposed which the simulation shows that it can bring very good THD and PF. Comparing the harmonics with IEC 61000 standard proves the good performance of the controller.

In Appendix B the effect of different variables like core shape (including the effect of airgap), material, frequency and voltage on transformer losses are studied.

2 Different topologies and previous work

ac <-> DC bidirectional converters can be implemented in several different topologies. Some of the convenient ones that have been studied in different literatures and papers are presented in this chapter. Each of these are useful for specific purpose and voltage/ power ratings.

2.1 A simple Bi-directional ac <-> DC converter with active power factor correction

Principle of operation:

This topology was discussed in [3].The topology consists of 2 modules as it can be seen in Fig.2. 1:

ac-DC Bridge consists of bidirectional switches $T1$ *to* $T4$ preferably SCR thyristors as they are low cost and robust and also can be commutated naturally.

DC-DC Buck Boost Converter is based on $D1, D2$ and $S1$ and $S2$ (bidirectional switches). Both of these topologies will be explained in chapter 3 thoroughly.

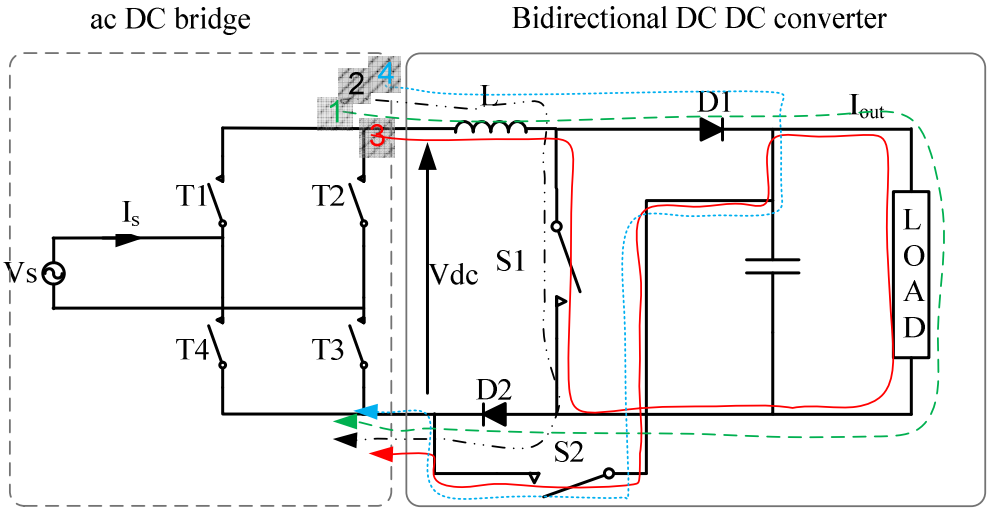


Fig.2. 1 a Bidirectional ac-DC converter topology

2.1.1 DC-DC boost operation, grid-> battery charging

$L, D1$ and $S1$ form a boost converter. L is charged when $S1$ conducts (path2 in Fig.2. 1) and delivers power through $D1$ when $S1$ is off (Path1). Path1 is represented by green dashed line through Load, $D1$ and $D2$. Path2 is shown by black dashed line through $D1$, and $S1. S2$ in the boost operation should be off, all the times.

2.1.2 DC-DC buck operation, battery-> grid discharging

In this mode Load acts as a DC generator (or Battery). The inductor current follows in the same direction as before. The $S2$ is turned on and $D2$ is reverse biased for all the times. As it can be seen in Fig.2. 1 (path3) during $S1$ turn-on period, $D1$ is reverse biased by Load voltage and the current passes through $S1$, load and $S2$ towards V_{dc}. In this path, L is charged (I_L is increased). When $S1$ is off, $D1$ takes the current and $V_L = -V_{dc}$ (L is discharged)

2.1.3 ac <-> DC Bridge

For G2L mode, *Vs* should be in phase of *Is*. The current drawn from the grid has ripple due to the presence of inductance.

For L2G mode, *T1* and *T2* are operated in anti-phase with the operation in G2L mode, so that power can be fed back to the ac power supply.*T2* and *T4* are turned on in the positive half cycle of *Vs* while *T1* and *T3* are turned on in the negative half cycle. *T1-T4* should be pre-triggered. Pre triggering of opposite switches of inverter in L2G mode results in natural commutation. (No extra control circuit)

2.2 A DC-DC converter with galvanic isolation

The DC-DC part is similar to the topology which is chosen for this thesis. This converter is suitable for applications that galvanic isolation is needed. The DC-DC converter with a galvanic isolation necessitates the use of a transformer. This topology can be seen in Fig.2. 2.

As it can be seen, the whole converter can be divided in two modules. Buck-boost converter that (in motoring mode) decreases voltage to V_{d2} ($V_{d2} < V_d$) and Boost-buck full-bridge converter that (in motoring mode) boosts the voltage to Vo. With two bidirectional converters (with opposite functionality) in series, in theory we can vary the load voltage, Vo to every desired value. The only difference between this topology and the chosen topology for this thesis is the location of inductor which will be explained in more details in chapter3. We will talk about functionality of each module and its overall principle of operation briefly in chapter3.

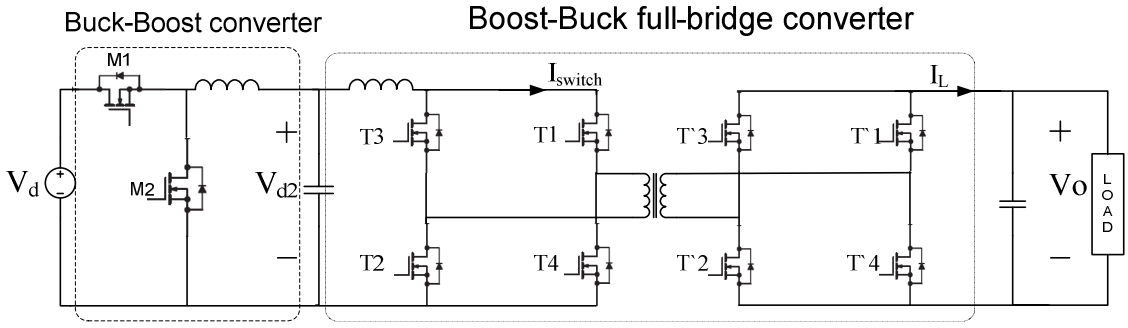


Fig.2. 2 a Bidirectional DC-DC converter topology with galvanic isolation. *Vo* can be higher or lower than *Vd*

3 Mature Theory

3.1 DC-DC Buck, Boost and Buck-Boost converter

In order to understand a Bidirectional Full bridge converter, it is important to study the Buck converter, Boost converter and Buck-Boost converter principle of operation before. Fig.3. 1 illustrates different DC-DC converters:

Buck operation: The current direction is from V_d to V_o and $V_d > V_o$. During the period that M1 is conducting, $t_{on} = DT_s$, inductor L is charged (M2 is reverse biased by V_d) and when M1 is off ($t_{off} = T_s - t_{on}$) inductance current will flow through M2. Fig.3. 1 shows the Buck converter scheme.

Boost operation: The current direction is from V_o to V_d and $V_d > V_o$. During the period that M2 is conducting, $t_{on} = DT_s$, inductor L is charged and when M2 is off ($t_{off} = T_s - t_{on}$) inductance current will be discharged through M1. Fig.3. 1 shows the Boost converter scheme.

Bidirectional Buck-Boost Operation: by combining two above converters a two quadrant converter is obtained that can operate bidirectionally: From V_d to V_o in Buck and from V_o to V_d in Boost mode. Changing the position of L and M1 changes Buck-Boost converter to Boost-Buck converter and that is the only difference between the Buck-Boost and Boost-Buck converter. (It should be noted that *bidirectional* Buck-Boost converter topology is different from conventional *unidirectional* Buck-Boost converter topology. The latter can be found on P:178 of [4])

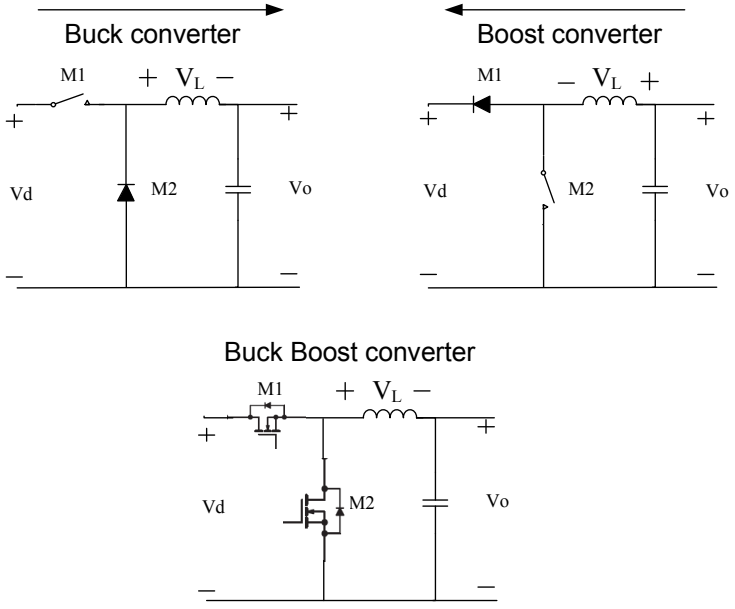


Fig.3. 1 bidirectional Buck-Boost , Buck and Boost converter

3.2 DC-DC Full-Bridge converter

Generally for power rates higher than 500W, fullbridge converters are the most common types of converters [5]. One advantage of them is the possibility to have galvanic isolation that separates battery side from the grid side (protection and EMC reduction purposes)

3.2.1 Full-Bridge Voltage Source Converter (FBVSC)

A full bridge Voltage Source Converter structure is shown in Fig.3.2. As full-bridge converters are supplied with a voltage source, they are voltage source converters. Voltage source full-bridge converters are derived from step-down (buck) converters.

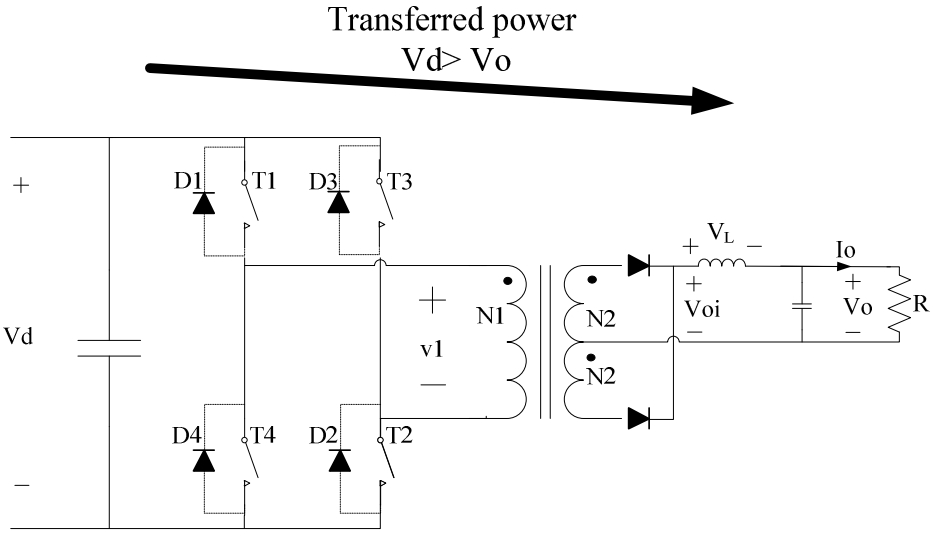


Fig.3. 2 Full-Bridge Voltage Source Converter (FBVSC) with a centertapped transformer

A period (T_s) consists of four intervals:

$$\begin{cases} T1,T2: on \rightarrow v_{oi} = \dfrac{N2}{N1}V_d \rightarrow v_L = \dfrac{N2}{N1}V_d - V_o \\ All\ switches: off \ \rightarrow \ v_{oi} = 0 \ \rightarrow \ v_L = -V_o \\ T3,T4: on \rightarrow v_{oi} = \dfrac{N2}{N1}Vd \rightarrow \ v_L = \dfrac{N2}{N1}V_d - V_o \\ All\ switches: off \ \rightarrow \ v_{oi} = 0 \ \rightarrow \ v_L = -V_o \end{cases}$$

Inductor current can be calculated in the following way:

$$i_L = \frac{1}{L}\int v_L.dt + i_{Lo} \tag{3.1}$$

In Fig.3. 3 some important waveforms of a full-bridge converter can be observed:

Since in steady state, inductor voltage integration over a time period should be zero, the output to input voltage ratio can be calculated as:

$$\frac{Vo}{Vd} = 2D\frac{N2}{N1} \quad , \quad D < 0.5 \tag{3.2}$$

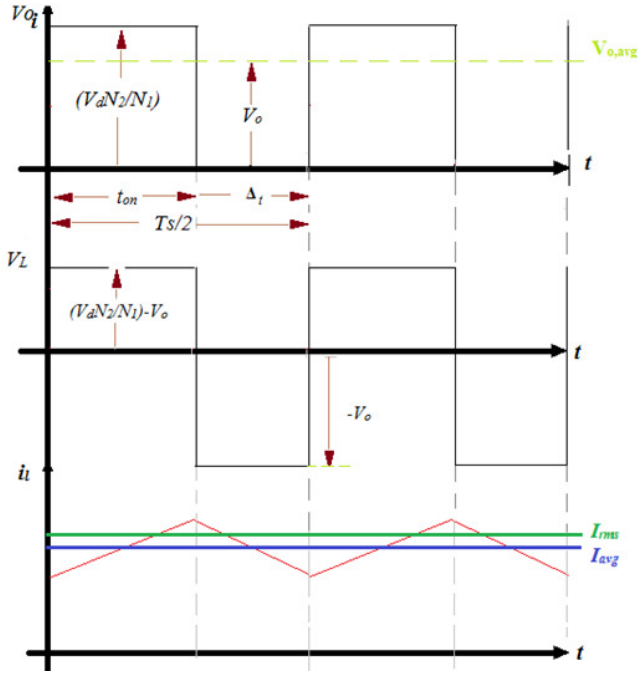


Fig.3. 3 Buck Full-Bridge wave forms

For practical limitations, we have to consider a dead band to prevent the simultaneous switching which can cause a high short circuit current. Normally $D_{max} < 0.45$ is set to be the maximum duty cycle boundary.

3.2.2 Full-Bridge Current Source Converter (FBCSC)

If an inductor is inserted at the input of full bridge circuit and switches operate with $D > 0.5$ (which means simultaneous switch conduction) we will have a Full-Bridge Current Source Converter which is derived from the boost (step-up) converter. Here, Inductor acts as a current source.

Fig.3. 5 shows Full-Bridge Current Source Converter and the parameters used in the following equations. In Fig.3. 4 the waveforms of FBCSC are demonstrated.

Like VSC, a time period *Ts* can be divided in four different time intervals:

$$\begin{cases} T'1, T'2: on \rightarrow v_1 = \dfrac{N1}{N2} V_o \rightarrow v_L = V_d - \dfrac{N1}{N2} V_o \\ All\ switches:\ on \quad \rightarrow \quad v_L = V_d \\ T'3, T'4: on \rightarrow v_1 = \dfrac{N1}{N2} V_o \rightarrow v_L = V_d - \dfrac{N1}{N2} V_o \\ All\ switches:\ on \quad \rightarrow \quad v_L = V_d \end{cases}$$

The output to input voltage ratio can be obtained by zeroing the inductor voltage integration over a time period. Eq. (3.3) describes the output to input voltage ratio:

$$\frac{Vo}{Vd} = \frac{N2}{N1} \frac{1}{2(1-D)}, \quad D > 0.5 \tag{3.3}$$

The principle of operation is explained in the next section (3.2.3.1).

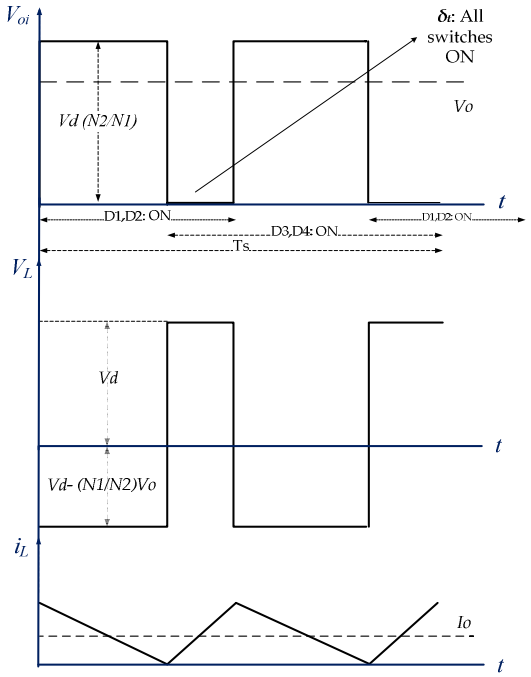


Fig.3. 4 Boost Full-bridge waveforms, Inductor current is shown in boundary conditions (between continuous and discontinuous mode) the parameters are defined in Fig.3. 5

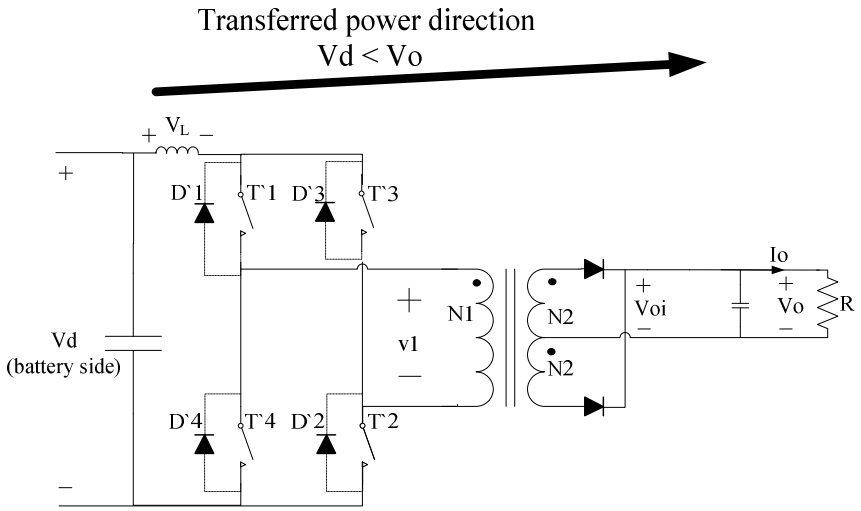


Fig.3. 5 Full-Bridge Boost Current Source Converter topology (FBCSC)

3.2.3 Bidirectional Double-Leg Full-Bridge DC-DC Converter

By combining the FBVSC and the FBCSC, in principle we can obtain a (2 quadrant) BUCK-BOOST converter. In order to do this, the diodes of FBVSC and FBCSC should be replaced with switches. This results in Bidirectional Double-Leg Full-Bridge DC-DC Converter which is illustrated in Fig.3. 6.

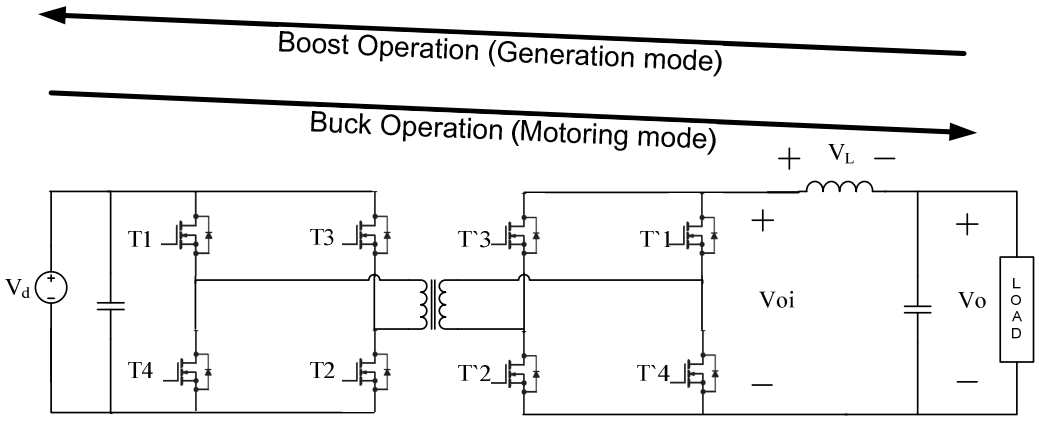


Fig.3. 6 Bidirectional Double-Leg Full-Bridge DC-DC Converter topology

3.2.3.1 Principle of operation (Duty cycle control)

Buck Operation: in buck operation or motoring mode, $T1$, $T2$ and $T3$, $T4$ are controlled together. There is no need of any control on secondary side. All secondary switches ($T^{'}1, T^{'}2, T^{'}3, T^{'}4$) should be off (no conduction by any switch) and only anti-parallel diodes conduct. For example, when T1 and T2 are conducting in primary side, in order to have a continuous current in inductor, the only way that current can flow in secondary side is via anti-parallel diodes of $T^{'}1, T^{'}2$ ($D^{'}1$ and $D^{'}2$). (Refer to Fig.3. 2)

Boost Operation: In this operation mode, power (and so the current) is transferred from V_o toV_d . In order to make it possible, V_d should be higher than V_o and that's the reason it is called boost operation mode. In boost operation or generation mode, $T^{'}1, T^{'}2$ and $T^{'}3, T^{'}4$ are controlled together. There is no need of any control on primary side. All primary switches 1, $T2$, $T3$, $T4$ have to be open and only anti-parallel diodes conduct. The whole period can be divided in 4 phases:

1. First $T^{'}1$ And $T^{'}2$ conduct in secondary side, the only way that current can flow in primary side towards the grid is via anti-parallel diodes of $T1$, $T2$ ($D1$ and $D2$). (Refer to Fig.3. 5) the inductor is discharged and V_L would be negative (By refereeing to Fig 3.4 pole sign) the inductor current decreases linearly (Fig.3. 2)

2. Then all switches have to be on to make a path for inductor current. At this interval $v_L = V_o$, and this charges the inductor and the current increases linearly (For waveforms refer to Fig.3 .2)

3. $T^{'}1$ And $T^{'}2$ conduct in secondary side. The only way that current can flow in primary side towards the grid is via anti-parallel diodes of $T1$, $T2$ ($D1$ and $D2$).

4. Finally again All switches have to be on to make a path for inductor current. At this interval $v_L = V_o$, and this charges the inductor and the current increases linearly again.

Based on parameters used in Fig.3. 5 we can sum up all four phases in equations below. They are basically are the same as FBCSC equations. Just pay attention to parameters' naming.

$$\begin{cases} T'1, T'2: on \rightarrow v_L = V_o - \dfrac{N1}{N2} V_d \\ All\ switches: on \rightarrow\ v_L = V_o \\ T'3, T'4: on \rightarrow v_1 = \dfrac{N1}{N2} V_o \rightarrow\ v_L = V_o - \dfrac{N1}{N2} V_d \\ All\ switches: on \rightarrow\ v_L = V_o \end{cases}$$

3.3 Power Factor Correction (PFC) circuit

3.3.1 Introduction

As we know Power Factor (PF) is defined as ratio of the real power over the apparent power. It is desired that this ratio be as close as possible to 1. In order to increase PF especially in non linear loads such as rectifiers that distort the line current, Active Power Factor Corrections (APFC) have to be utilized to counteract this distortion and improve the PF, while in the linear loads, a Passive PFC (PPFC) is maybe enough.

3.3.1.1 Passive PFC vs. active PFC

Different passive PFC topologies with different performance and THD are discussed in [6] one of the most convenient passive PFCs can be seen in Fig.3. 7(A). It consists of a diode rectifier bridge and a Low Pass Filter (LPF) which removes the high frequency harmonics and improves the line current drawn from the grid. It is obvious that we can't have any control over the amplitude of voltage in this method. Also Passive PFC needs larger inductor and capacitor (heavier) in comparison with Active PFC as it works with power frequency. Additionally, passive PFC cannot have a good THD, but still the total price of Active PFC maybe higher due to control systems and utilizing switches (complexity)

In Active PFC, instead of LPF another stage is required: an ac-DC converter. An APFC with a proper control strategy can reduce harmonic pollutions by keeping the power factor close to 1. This means that the grid voltage and input current are in phase and the line current is kept sinusoidal. With an APFC, current THD of 1% is feasible.

A unidirectional APFC circuit is illustrated in Fig.3. 7(B). It consists of two parts: (1) diode rectifier (2) Buck, Boost or Buck-Boost converter (active wave shaping of input current). In boost PFCs the input current has lesser high-frequency components resulting in lower EMI and reduced filtering requirement [7]. So boost PFCs are more popular

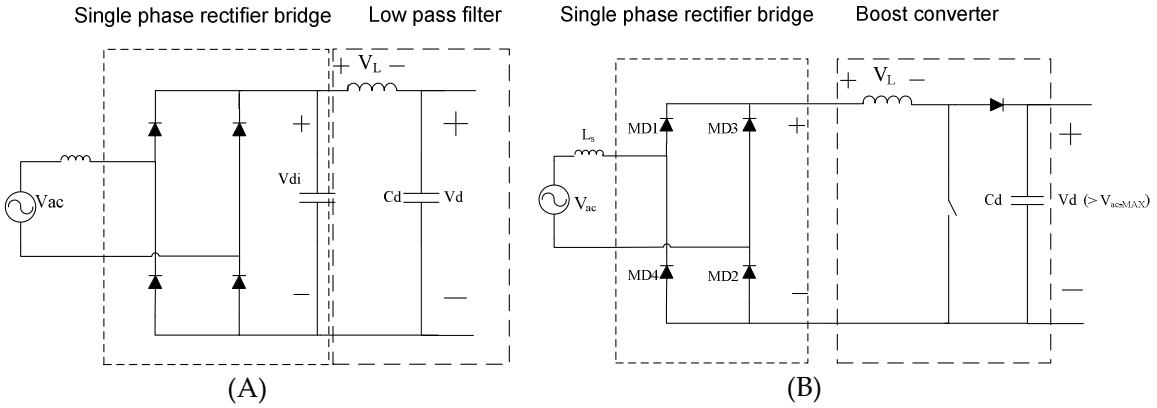


Fig.3. 7(A): Passive PFC circuit (B) unidirectional active PFC. For different topologies and comparisons see: [7]

3.3.2 Active PFC with bidirectional functionality

In order to have a bidirectional circuit (V2G and G2V) some modifications have to be done in fig.3. 7(B): Instead of diodes, bidirectional switches have to be replaced. Fig.3. 8 (A) illustrates the bidirectional realization of Fig.3. 7(B).

Generally two types of bidirectional PFCs are more popular. These can be seen in Fig.3. 8. A short description on their operation is given here:

3.3.2.1 Rectification mode (Boost operation (G2V))

Power Frequency Rectifier, PFR (Fig.3. 8 (A)): It consists of two stages: (1) a diode bridge $MD1-4$[1]: :When $V_{ac}>0$, $D1$ and $D2$ conduct and when $V_{ac}<0$ the opposite switches will be turned on. (2) A switch mode DC-DC converter*:* By switching $M1$, the voltage over inductor can be controlled, so the grid current, I_s can be controlled in a way it is sinusoidal: When $V_{ac}>0$, if M1 is turned on, $V_L=V_{ac}$ and inductor current rises up. If $M1$ is off, $V_L=V_{ac}-V_d<0$ (remember that $V_d>V_{ac,max}$) and inductor current falls down. The same can be said for $V_{ac}<0$.

The rectifier together with the boost converter forms an active PFC. For charging mode, $M2$ is turned off for all times and only its body diode conducts.

Switch Mode Rectifier, SMR (Fig.3. 8 (B)): As the inductor is placed in the primary side, this converter is inherently a boost converter.

By controlling the magnitude and phase angle of $V_{r(1)}$[2] desired values for the real power supplied by the ac source to the converter, P and absorbed reactive power by the converter, Q can be obtained. For the desired magnitude and direction of power flow, the magnitude and phase angle (with respect to the line voltage) of $V_{r(1)}$ should be controlled [4]. V_d must be greater than the peak of the input ac voltage.

For the rectification, diodes of $MD1$ and $MD2$ are utilized and V_r can be controlled by simultaneous switching of $MD2$ and $MD4$ (to guarantee that the inductor current flows during zero crossing transient) When $V_{ac}>0$, if $MD2$ is off, the body diode of $MD1$ and $MD2$ conduct ($V_r=V_d$). If $MD2$ & $MD4$ are turned on, the current direction would be through $MD4$ and body diode of $MD2$, as it can be seen in fig.3. 8 (B) In this condition $V_r=0$ and $V_L=V_{ac}$, so L is charged.

3.3.2.2 Inversion mode (V2G)

Line frequency inverters: In order to transfer power to the grid, the inductor current should be applied to the grid in anti-phase with the grid voltage. In this way, power can be fed back to the ac power supply. *MD1* and *MD2* are turned on in the positive half cycle of Vac while $MD3$ and $MD4$ are turned on in the negative half cycle.

The main drawback of this method is that the grid current (with opposite direction) is distorted and have a very high THD.

Switch mode inverter: In order to limit the harmonics to the grid, switch-mode inverters are widely used. The most well-known switching pattern is PWM switching. There are two methods of PWM switching, unipolar and bipolar. Due to advantages of unipolar switching, in this thesis unipolar PWM is used. The principle of operation is to control the magnitude and phase angle of $V_{r(1)}$ in anti-phase with I_{s1}. In chapter 18 of [4] different PWM switching patterns and a method to implement the controller for inversion and rectification mode is given.

---

[1] MD1 to MD4 can be seen in Fig. 3. 8. M1 refers to the switch, while D1 refers to the switch body diode.

[2] $V_{r(1)}$ is the fundamental frequency component of V_r in Fig. 3 .8

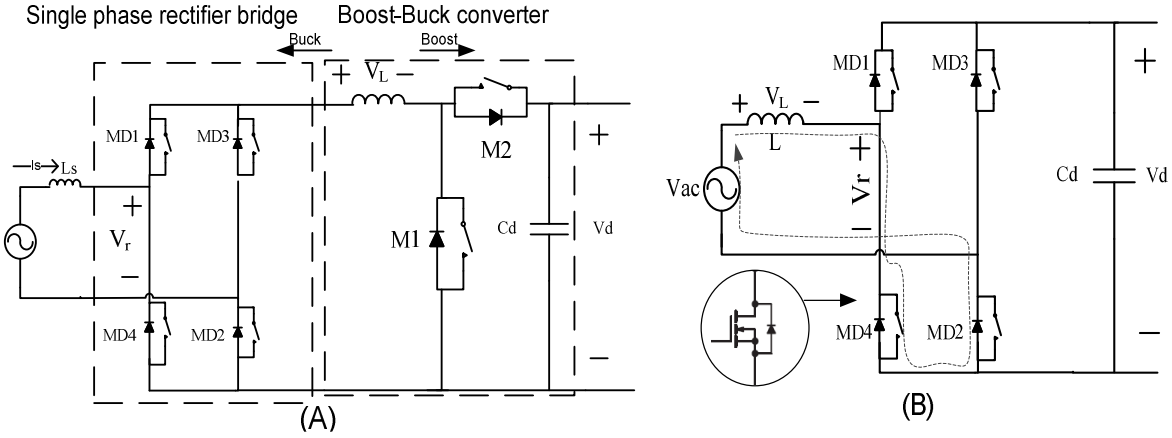


Fig.3. 8 Two different bidirectional APFC circuits. (A) Power Frequency Rectifer (PFR): single phase bridge rectifier +Buck-Boost Converter both will form a Bidirectional ac-DC converter, (B) Switch Mode Rectifer (SMR)

3.3.3 Space state equations for single phase rectifier

The grid voltage is rectified to half sine wave by the diode rectifier. By choosing an appropriate DC-link capacitor, this wave is smoothed more and an acceptable stiff DC voltage is provided for buck-boost converter.

The diode rectifier in Fig 3. 7(A) can be simplified to the equation circuit in Fig.3. 9(A). By applying KVL and KCL on this circuit, (3.4) and (3.5) will be obtained:

$$V_{ac} = L_s \frac{di_d}{dt} + V_d \tag{3.4}$$

$$i_d = C_d \frac{dV_d}{dt} + \frac{V_d}{R_{load}} \tag{3.5}$$

By rearranging the above equations in the state variable form for a half cycle, the state matrix equation will be obtained:

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{dV_d}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{Ls} \\ \frac{1}{C_d} & -\frac{1}{C_d R_{load}} \end{bmatrix} \begin{bmatrix} i_d \\ V_d \end{bmatrix} + \begin{bmatrix} \frac{1}{Ls} \\ 0 \end{bmatrix} V_{ac} \tag{3.6}$$

This matrix can be implemented in MATLAB.

By increasing the size of the capacitor the output voltage will be smoother. But as this capacitor is huge and expensive, there is always a tradeoff between the desired ripple and capital cost. By assuming a ripple around 25~30% and by trial and error, a capacitor value is found to be around $C_d = 1\,mF$. The effect of such a dc-link capacitor to build a DC output voltage can be seen in Fig.3.9(B) will be obtained. As it can be seen the output voltage average is increased to 311.5V. Without the capacitor, the average voltage of the half sine wave, V_{avg} with amplitude of V_m was:

$V_{avg} = V_d = 2V_m/\pi = 2 \times 230\sqrt{2}/\pi \cong 206V$

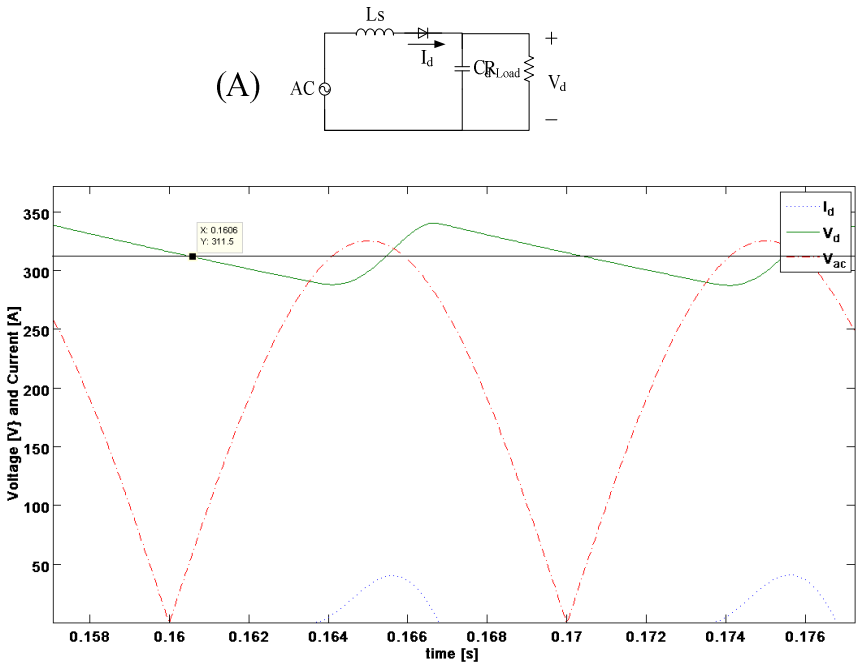


Fig3. 9 (A) Simplified equation circuit of a Bridge Rectifier, (B)Output Voltage and current of a diode rectifier in presence (green line) and absense (red dashed line) of Capacacitor

By providing the DC link voltage output by the diode rectifier, using the state space averaging and linearizing the DC-DC boost converter a small signal transfer function between output and duty cycle, $\tilde{v}_d(s)/\tilde{d}(s)$ can be obtained.

A common approach is to: (1) find a circuit state for switch on and one for switch off and write a space state equation for each of them (2) average the state-variables in a period (3) introduce small signal (4) and finally transform the equations in Laplace domain.(P:323 [4])

Although Space state equations can describe the power frequency rectifier behavior, it is difficult to implement them for switching mode rectifiers, as linearization cannot be done easily. The averaged state matrix[1] includes duty cycle and for each d, it varies and makes this approach impossible. In Chapter 9, with a simple solution, the model is linearized.

3.3.4 The whole onboard charger topology

There are some reasons to choose the switch mode rectifier APFC circuit (Fig.3. 8(B)). First, the numbers of switches are reduced (from six switches in power frequency rectifier to four switches in switch mode rectifier). This means the lower capital cost and control circuit for SMR. Switch losses comparison is not investigated in this thesis.

The final topology can be seen in Fig.3. 10. It includes two modules:

1. An ac <-> DC rectifier that converters $220Vac$ to around $400VDC$.

2. A Full Bridge Buck-Boost DC-DC converter (with the Inductor in secondary side) that steps down the DC voltage from $400V$ to $300\sim 400V$ to supply the battery terminals.

[1] $A = A_1 D + A_2(1-D) = \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ -\frac{1-D}{C_d} & -\frac{1}{C_d R_{load}} \end{bmatrix}, \dot{x} = \begin{bmatrix} \dot{I_L} \\ \dot{V_C} \end{bmatrix}$ So the places of two poles in [SI-A] is varied by D

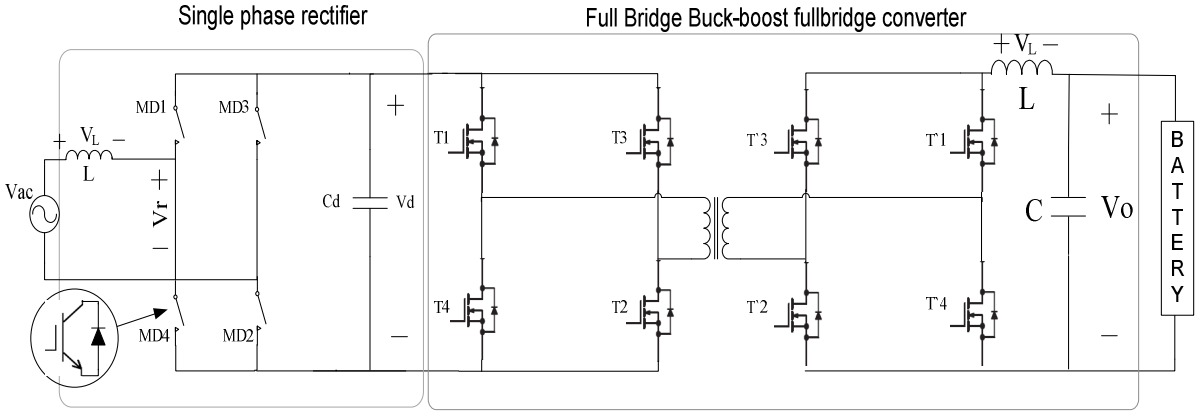


Fig.3. 10 The whole onboard charger topology, including an APFC module and a Bidirectional Full-Bridge DC-DC Converter module

3.4 Output filter calculation for full-bridge converter

3.4.1 Buck full-bridge converter

As we know *L* and *C* in the output of DC-DC converter of Fig.3. 2 create a low pass filter with cut off frequency:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.7}$$

We also know that:

$$V_L = -Vo \qquad t_{on} < t < (t_{on} + \Delta_t T_s)(= 0.5) \tag{3.8}$$

$$V_L = \frac{N2}{N1} V_d - V_0 \qquad 0 < t < t_{on}(= DT_s) \tag{3.9}$$

Output voltage ripple is calculated based on basic equation of capacitor:

$$\Delta V_0 = \frac{\Delta Q}{C} = \frac{1}{C}\frac{1}{2}\frac{\Delta I_L}{2}\frac{1}{2}\frac{Ts}{2}$$

$$\Delta I_L = \frac{\Delta_t T_s}{L} Vo \tag{3.10}$$

$$\Delta V_0 = \frac{\Delta_t V_0}{16 f_s^2 LC} = \frac{(0.5 - D)V_0}{16 f_s^2 LC} \tag{3.11}$$

Δ_t : Off time, Δ_t for a buck converter is equal to $\Delta_t = 1 - D$ and for a full-bridge buck converter is equal to $\Delta_t = (1 - 2D)/2$

As it can be seen, the voltage ripple is two times lower than the voltage ripple in a buck converter with the same *L* and *C* ($\Delta V_{0_{buck}} = \frac{\Delta_t V_0}{8 f_s^2 LC}$), which depicts a good advantage of the full bridge converter.

L calculations:

We assume that all the output ripple currents (harmonics) will pass through Capacitor and only DC (average value of) current will be delivered to load. This assumption enables us using basic equation of inductors.

The reason is that by assuming infinite C, $Z = \frac{1}{jC\omega}$ will be so small and is a short circuit pass for harmonics. By the help of Fig.3. 3, we can write:

$$\Delta I_L = \frac{\Delta_t T_s}{L} Vo = \frac{(0.5 - D)T_s}{L}\frac{N2}{N1} 2DV_d \tag{3.12}$$

$$\Delta I_L(D) = \frac{N2}{N1}\frac{(D-2D^2)}{Lf_s}V_d \quad (3.13)$$

Δ_t: is defined as the ratio of the time that all switches are off over a period Ts. For a full-bridge buck converter is equal to $\Delta_t = (1-2D)/2$

The derivative of $\Delta I_L(D)$ with respect to D equals to zero at $D = 0.25$ suggesting that we have the highest current ripple at that duty cycle[1]. It should be noted that we calculate the inductor based on desired 10% current ripple (at max current)

C calculation:

Now by assuming huge inductor, L (these assumptions are valid only if $f_c << f_s$) $Z = j\omega L$ will be infinite and all voltage harmonics only see this huge impedance and will be over the inductance.

So we can assume all voltage harmonics (ripple) are over the inductor V_L and so Vo will be purely DC:

Based on $\Delta V_0 = \frac{\Delta_t V_0}{16 f_s^2 LC}$ by defining the desired voltage ripple and having all the parameters and L from previous calculations, C can be found.

In order to filter the switching frequency ripple, we need to have $f_c << f_s$ so f_c is set less than 0.2 of f_s. Based on (3.7) by having the inductance value, L, capacitance can be recalculated. By inserting new C and L in to (3.11) new voltage ripple which should be less than required voltage ripple is obtained.

3.4.2 Boost Full-bridge converter

In Boost operation the inductor size is different from the buck operation.

Referring to wave forms of Fig.3. 4, and parameters defined in Fig.3. 5 we can write:

$$\Delta I_L = \frac{\delta_t T_s}{L} Vd \xrightarrow{yields} L = \frac{\delta_t T_s}{\Delta I_L} Vd \quad (3.14)$$

Where:

δ_t: is defined as the ratio of the time that all switches are on over a period Ts and is equal to $\delta_t = D - 0.5$

Vd: Battery side voltage.

For Continuous conditions, ripple current, as a function of D can be obtained by (3.15)

$$\Delta I_L(D) = -\frac{\frac{N1}{N2} Vo(2D-1)(1-D)}{f_s L} \quad (3.15)$$

Where:

Vo: Converter's output voltage which is the inverter input voltage

N1, N2: Number of Transformer turns in primary and secondary side respectively (as defined in Fig.3. 5)

Equation (3.15) suggests that the maximum current ripple happens at $D = 0.75$

We can go further and see in which duty cycle, D we will have the highest output current in boundary condition.

From (3.3) and by assuming $P_o = P_{in}$ we can write:

$$\frac{Id}{Io} = \frac{N2}{N1}\frac{1}{2(1-D)} \quad , \quad D > 0.5 \quad (3.16)$$

1 Later on we will see that our range of duty cycle is more than 0.25 , $0.2813 \leq D \leq 0.375$, suggesting that the current ripple is even less that the expected value and this is proven in chapter 8

Considering boundary conditions ($\Delta I_L = I_{L,peak}$, $I_{LB,av} = 0.5\, I_{L,peak}$) and remembering that $I_{LB,av} = Id$ and by using equations (3.14, 3.15 , 3.16), I_o can be expressed as a function of D.

$$I_o(D) = \left(\frac{N1}{N2}\right)^2 \frac{T_s V_o}{L}\, 2\,(1-D)^2\,(D-0.5) \qquad (3.17)$$

(3.17) shows the maximum transferred current to the output occurs at D=0.666 as depicted in Fig.3. 11

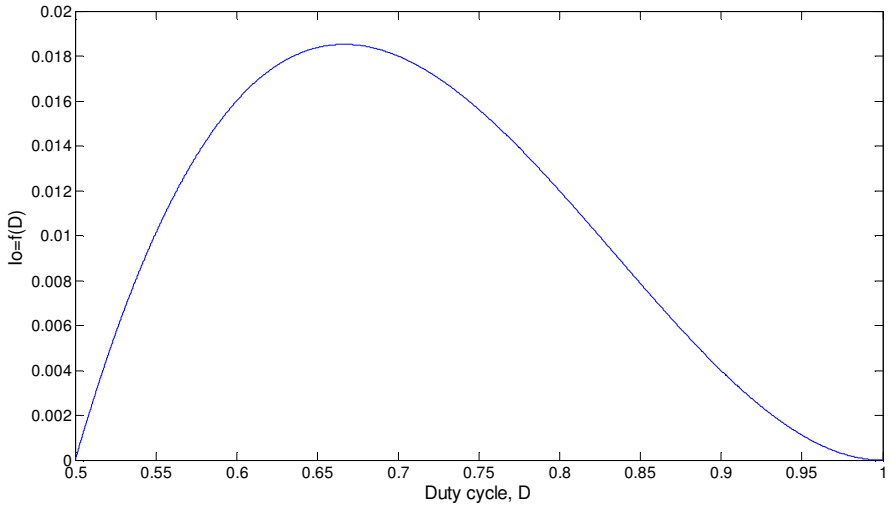


Fig.3. 11 Output current as a function of D in full bridge boost converter (boundary conditions)

3.5 Filter Inductor (choke) design

3.5.1 Introduction and basic concepts

A simple inductor is shown in Fig.3. 12 (c). If leakage inductance is neglected electrical and magnetic equivalent circuit can be found in Fig.3. 12 (b) and (a) respectively.

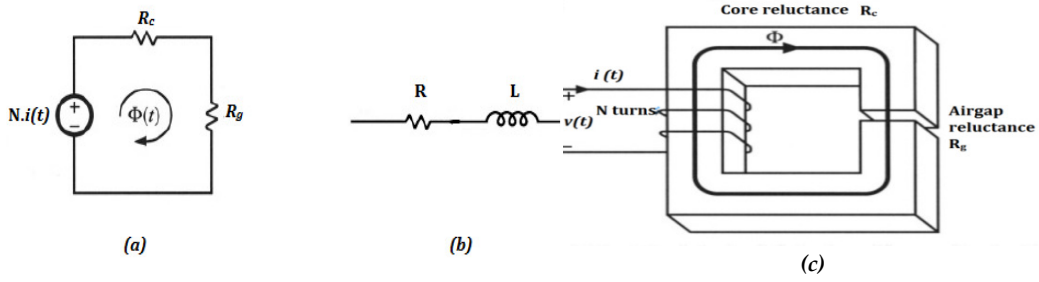


Fig3. 12 Inductance: (a) Magnetic circuit, (b) Electric circuit model of inductor, (c) Simplified structure of filter inductance.

Air gap reluctance, $\mathcal{R}_g$ and core reluctance, $\mathcal{R}_c$ can be calculated by (3.18) and (3.19) respectively:

$$\mathcal{R}_g = \frac{L_g}{\mu_0 A_g} \qquad (3.18)$$

$$\mathcal{R}_c = \frac{L_c}{\mu_0 \mu_r A_c} \qquad (3.19)$$

Also from basic electromagnetic courses we know that:

$$N.i(t) = \varphi.(R_g + R_c) \quad (3.20-1)$$

$$\varphi = B.A_g \quad (3.20-2)$$

Where

L_g: Length of airgap

L_c: Length of the flux path inside the core which is called magnetic path

μ_0: 1.25e -6: air permeability

μ_r: Permeability of the material

$A_g = A_c$: Core cross sectional area which if fringing flux is neglected it can be assumed is equal to airgap cross section.

φ: Flux in the core

B: Flux density

3.5.2 Four design Constraints

Maximum flux density

Based on I_{Max} and with the help of (3.18) and (3.19), B_{Max} can be found:

$$B_{Max} = N.\frac{I_{Max}}{A_g(\mathcal{R}_g + \mathcal{R}_c)} \quad (3.21)$$

B_{Max} should be lower than saturation flux density of the material.

We will see later that for inductor design, to have a low flux density we need either huge core (large A_C) or using airgap (adding $\mathcal{R}_g$) . Using airgap will increase number of turns and this, leads to higher copper losses.

Inductance value

The calculated inductance value must be obtained by:

$$L = \frac{N^2}{\mathcal{R}_g + \mathcal{R}_c} \quad (3.22)$$

For transformers this formula gives Magnetizing inductance (L_M).

Winding area (please refer to Appendix B)

Winding resistance (will be discussed later)

3.6 Transformer design:

3.6.1 Modeling of Non Ideal transformer

Ideal transformer: In Ideal transformer, Core reluctance is assumed to be zero. MMF will be zero as well and $F_c = \varphi.\mathcal{R} = 0 = n_1 i_1 + n_2 i_2$

Consequently, as there is no passive element, input power will be equal to output power: $v_1 i_1 = v_2 i_2$

The ideal model is not accurate enough most of times and for our simulations we have to use non Ideal transformer model. Fig.3. 13 shows a simple structure of a non Ideal transformer.

3.6.1.1 The Magnetizing Inductance

Magnetizing inductance can be calculated by:

$$L_M = \frac{N^2}{\mathcal{R}} \quad (3.23)$$

Where

$\mathcal{R}$ equivalent core reluctance
N: number of turns, if secondary number of turns is used, it means we move L_M to secondary side and vice versa.

3.6.1.2 Leakage inductance and Eddy currents in winding conductors (winding parasitics)

Due to externally-applied magnetic field over each winding (from primary winding on secondary and from secondary on primary), and non ideal magnetic field coupling, eddy currents will be induced and flow in a conductor. This non ideal coupling results in leakage inductances and eddy current power losses in a conductor. (Fig.3. 13(left)). Leakage inductances are inevitable but there are some methods to reduce their effects. In addition to leakage inductance, there is a capacitance between windings themselves which is called inter-winding capacitance. We neglect the effect of these capacitances in our model.

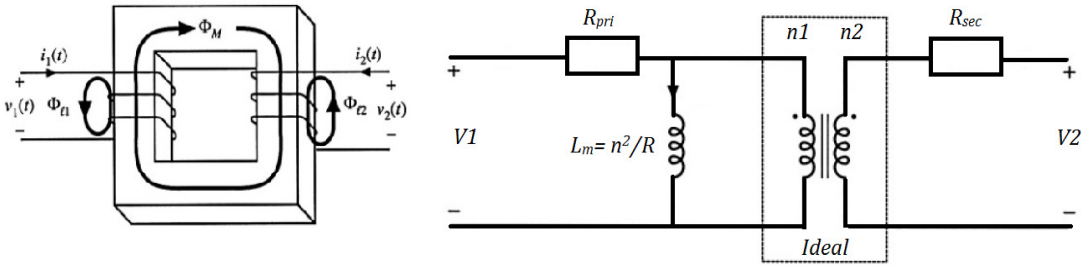


Fig.3. 13 Left: A transformer, windings and core, φ_L is the result of leakge inductance . Right: Non ideal model of transormer (including an ideal model)

For simplicity, we assume that leakage only occurs on winding. This assumption is especially correct when relative permeability of a material (such as ferrites) is much higher than air's. Too much Increase of the airgap will introduce a large flux leakage (flux fringing). Flux pollution can result in Electromagnetic Interference (EMI)

Sectioning the windings can reduce the leakage inductance and using LITZ wires will reduce Eddy current loss [8].

Generally speaking, in isolated converters, leakage inductance leads to switching loss, increased peak transistor voltage, and that degrades cross-regulation, but otherwise, has no influence on basic converter operation [9], [10] . We will see later that leakage inductance can highly influence the transformer core losses.

By coupling coefficient, the degree of magnetic coupling between primary and second windings can be evaluated. This coefficient is between 0 (total coupling) and 1 (no coupling). Construction of low voltage transformers having coefficients in excess of 0.99 is quite feasible [11].

3.6.1.3 Transformer Design Constraints:

The Constraints are the same as Inductor constraints. The only difference is that in order to have a lower copper losses, it is desirable to have a lower number of turns and this leads to lower magnetizing inductance. But this also means that higher current passes through L_M and lower current enters the ideal transformer which means we will have lower current at output than we expected before. (Distorted output current) so between these two, a compromise should be reached.

3.7 Output capacitor design

3.7.1 Simplified capacitance model

The output capacitor is also a source of energy dissipation, but as the current ripple through this capacitor is not so high, we don't expect huge power losses. Fig.3. 14 shows a conventional capacitor modelling.

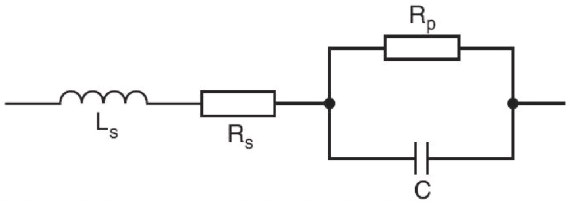


Fig3. 14 Conventional capacitor modelling.

Instead of all the resistances of a capacitor, the Equivalent Series Resistance (ESR) is obtained in datasheets. The ESR sums up all the losses in the capacitor (resistive and dielectric losses). The ESR is a temperature and frequency dependent. Another useful parameter for a capacitor is the dissipation factor (tan δ) which relates capacitance at a certain frequency to the ESR. By definition the dissipation factor is the ratio between the ESR and the reactance of the capacitor.

The power losses in a capacitor can be calculated by (3.24):

$$P_{cap} = i_{C,rms}^2 . (ESR) \quad (3.24)$$

i_c is the current of the capacitor. The current ripple of the inductor flows in the capacitor and the DC current flows to the load. So, the DC link Capacitor current does not have a DC value.

There are several types of capacitors in the market with their own advantages and usage areas[1] such as:

Aluminum Electrolytic Capacitors, Capacitors for AC Motor Run Applications, Capacitors for Power Factor Correction, Capacitors for Power Electronics, EMI Suppression Capacitors, Film Capacitors (Metallized Polyester (MKT), Metallized Polypropylene (MKP/MFP)) and Multilayer Ceramic Capacitors.

For this study, among above capacitors two of them are selected. Each of these two capacitors (table 1 and 2) can be suitable:

Table. 3. 1 Metalized Polypropylene (MKP/MFP)

MODEL	V_{RMS}	V_{DC}	C_R (uf)	I_{RMS}	ESL (nH)	ESR (10kHz,mohm)
B32794	250	630	2.5	4	24	14.1

Table. 3. 2 Aluminium electrolytic capacitor. Axial-lead capacitors

MODEL	V_{DC}	C_R (uf)100 Hz	I_{ac},10 kHz	ESR(100Hz,ohm)	ESR (10kHz,ohm)
B43698	450	6.8	1.26	7.2 -12	5.5

Both of these capacitors exhibit very low power losses, thus in future calculations the effect of Capacitor losses will be neglected.

[1] www.epcos.com

3.8 Battery study: Importance and technologies[1]

3.8.1 Introduction

The very first step to design a battery charger controller is to find the battery type that can satisfy the required specifications. I.e. an electric vehicle battery should contain high and constant energy density during the discharge cycle, long working cycle and life time, without having memory effect.

After choosing the battery, in order to increase the life time and the efficiency of that certain battery type, its charge /discharge characteristics should be known and based on these characteristics, a specific charging control strategy should be applied.

There are several types of batteries available in the market. But in Automotive industries, Lithium-Ion batteries are replacing other types of batteries especially Lead-Acid batteries. The reasons can be summarized as below:

1. Lithium-Ion cells have a fairly flat discharge curve which means delivering a permanent power over 80% of discharge cycle. If the delivered power during the discharge cycle falls progressively, for high power applications like HEV this can be problematic at the end of cycle. (Li-Ion delivered power at the end of the cycle falls down drastically and this is the reason we should never let the battery discharge completely).

2. Lithium-Ion shelf life time is much longer than other types (Zinc Carbon (Leclanché) 2 to 3 years, Alkaline 5 years, Lithium 10 years or more)

3. Lithium-Ion cells discharge rate are lower (Lead Acid 4% to 6% per month, Nickel Cadmium 15% to 20% per month, Nickel Metal Hydride 30% per month, Lithium 2% to 3% per month)

4. Fast charge and discharge is possible. I.e. for discharge, up to 40C rate is possible. (Very good for accelerating)

5. No memory effect

6. Partial charges and micro-cycles make the battery last even more than full charges that makes it perfect candidate for hybrid use.

7. By changing basic cell chemistry, a desired performance can be obtained such as capacity or rate performance.

8. the most important advantage of this type of battery is its superior energy density at a certain power density as it can be seen in the Ragone chart[2] (Fig.3. 15). This means that for the same capacity Li-ion batteries are generally much lighter than other types. For instance despite containing nearly identical energy (16kWh), the Chevrolet Volt's Li-ion battery pack (with the weight of 170 kg) is over 70% lighter than the EV1's original 590 kg AC Delco lead-acid battery pack.

[1] This thesis's focus is not on batteries so a brief but necessary section is dedicated to it.

[2] Ragone chart is a chart used for performance comparison of various energy storing devices. On such a chart the values of energy density (in Wh/kg) are plotted versus power density (in W/kg)[Source:Wikipedia.org]

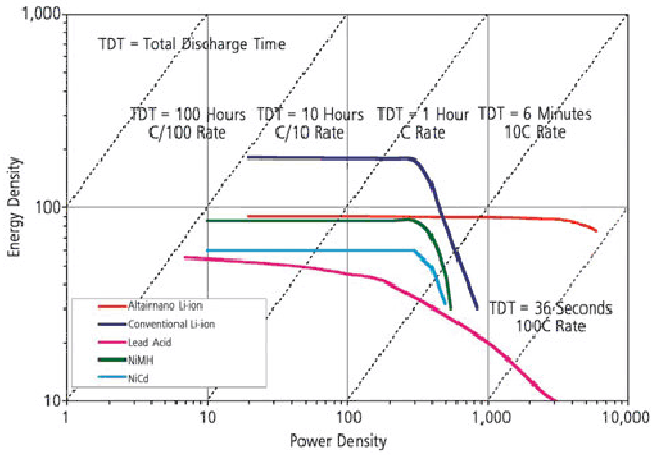


Fig.3. 15 Ragone chart, superior energy density at a certain power density of Li-ion battery

3.8.2 Cell modelling

Inside the battery cell, the voltage between two electrodes (for simplicity) can be assumed to be fixed by electrochemical characteristics of the active chemicals (constant voltage source). But the actual voltage depends on several variables such as load current and internal impedance which is changed by temperature, state of charge (SOS) and age of the cell.

The simplest way to model a Battery is to use a linearized mode. It means that a Li-ion battery can be viewed as an ideal voltage source with a series resistance proportional to the slope of the middle region of V-I. Fig. 3. 16 shows the battery V-Ah profile. The value of the resistance and the Voltage source can be seen in that figure. In order to provide a time constant for the voltage source a small capacitance is sometimes added to the model [12]. Thus a battery can be modelled as RC circuit (or in other words, first order system).

Maximum current carrying capacity of a battery is determined by its internal resistance. There are several types of resistances but their equivalent resistance is replaced with them. As higher current capacity is desired there are several manufacturing techniques to reduce the internal resistance. A high internal resistance causes high losses during charging and discharging which means lower available capacity of a cell especially at high power rates that demands high current. But lower internal resistance causes the self discharge rate to increase. Li-ion has relatively high internal impedance. One individual Li cell voltage is typically around 4V (higher than NiMH (1.2V) and Lead acid (~2V)) and this, makes this type suitable for high voltage and power applications as it draws lower current which means less losses. By paralleling and putting these cells in series, the required voltage and internal impedance can be achieved.

An equivalent resistance in series with constant voltage source is the most convenient model which can be implemented. Fortunately in SIMULINK the battery block model is developed which can ease the effort.

3.8.3 Different charging rates

3 different charging strategies have been introduced in recent years.

1. Slow charging (230V, 15A and charging time~6-8 hours, charging rate~0.1 C[1])

2. Semi-fast charging (400V, 53A and charging time~100 min)

3. Fast charging (400V, 600A and charging time~10 min)

The advantage of strategies two and especially three is its convenience for owners as battery charging does not take several hours. But it cannot be available at any household. Also as of high power demand, if a few car owners at the same time charge their batteries there would be a stability problem at LV and MV substations. Cell chemical constraints are also another obstacle and advanced and expensive charging methods such as Burp charging (or Negative Pulse Charging) are needed. As a basic rule, if electrical energy is pumped into the battery faster than chemical process can react to it, it will damage the battery (depending on Battery type around 20C).

On the other hand, with ordinary outlets, slow charging is possible. Researches also show that for Li-Ion cells, effective capacity is increased if the cell is charged (or discharged) at slow rates [12]. This means if we charge (discharge) the battery in a long period of several hours the effective capacity can be doubled the specified capacity at C rate. A battery in EHV can be charged/discharged by other sources (breaking=charge, accelerating=discharge) and that can affect the effective capacity too, but as we just study the charger, we don't consider their effects. I.e. if high current rates for hard acceleration and hill climbing are used, the range of vehicle will be reduced. Super capacitors in this case can be helpful in future as they contain very high power (though low energy) density.

3.8.4 Battery charging safety precautions

In order to understand charging schemes, we need to know what the worst conditions are that should be avoided all the times.

Deep discharge: Cycle life decreases severely with Depth of Discharge *(DOD).* A cell can be permanently damaged if it is fully discharged.

Overcharging: A good charger should detect the moment that a battery is fully charged. If not, especially for Li-ion, charging a fully charged battery can seriously damage the battery and reduce its life time because charging current generates great heat and this, releases some gases that are not good for the battery.

For slow chargers, which are the simplest types, charge termination is set when a certain upper voltage limit (termination voltage) has been reached.

Charging has 3 phases:

1) Charging the battery

2) Charging rate optimization (based on battery type)

3) Charge Termination (prevent overcharging)

[1] C is the charge (and discharge) current of a battery. 1C means that a 1000mAh battery would provide 1000mA for one hour (1C=1Ah)

3.8.5 Charging methods

There are several charging methods such as Constant Voltage, Current, Taper current, Pulsed, Burp, Trickle, float, Random or IUI charging. But as it is not the purpose of this thesis, only relevant charging methods are introduced.

Constant Voltage Charger is the simplest charger: A DC power supply. Basically simple Li-ion chargers use constant voltage method, with some circuitry to protect the battery and the user [13]. This charger is a circuit that charges a battery by supplying only enough current (as variable) to force the battery voltage to a fixed value.

Constant Current Charger is a circuit that charges a battery by supplying a fixed current into the battery (by varying Duty cycle). In this method, battery voltage increases linearly.

Combined method is the most popular method of charging that combines two above methods and is generally used in the fast Charging. As it can be seen in Fig.3. 19 Li-ion battery charging has two stages:

Stage1. The greatest possible constant current is supplied to the battery while voltage increases to termination voltage.

Stage2. Constant termination voltage is maintained while current decreases to trickle charge.

*Random charging (*also: *opportunity charging):* Applications that the energy to the battery is not controllable Like regenerative braking, can generate large power spikes which the battery has to withstand. For these, special techniques have to be applied to limit the charging current/voltage.

Constant Power Charging: in this charging method the product of the battery current and the voltage remains constant. This is typically suitable for hybrid vehicle slow chargers with huge and expensive battery capacity. In the slow charging, the main limitation is the single phase outlet fuse current, so the maximum possible current from the outlet must be exploited.

3.8.6 Battery requirements for this thesis

The Constant Power Charging method is used in this thesis: While the battery voltage terminal increases gradually from 300V to 400V during the charging time, the current is reduced from around 12A to 9A to keep the injected power to the battery continuously around 3600W. This can be seen in Fig.3. 17.

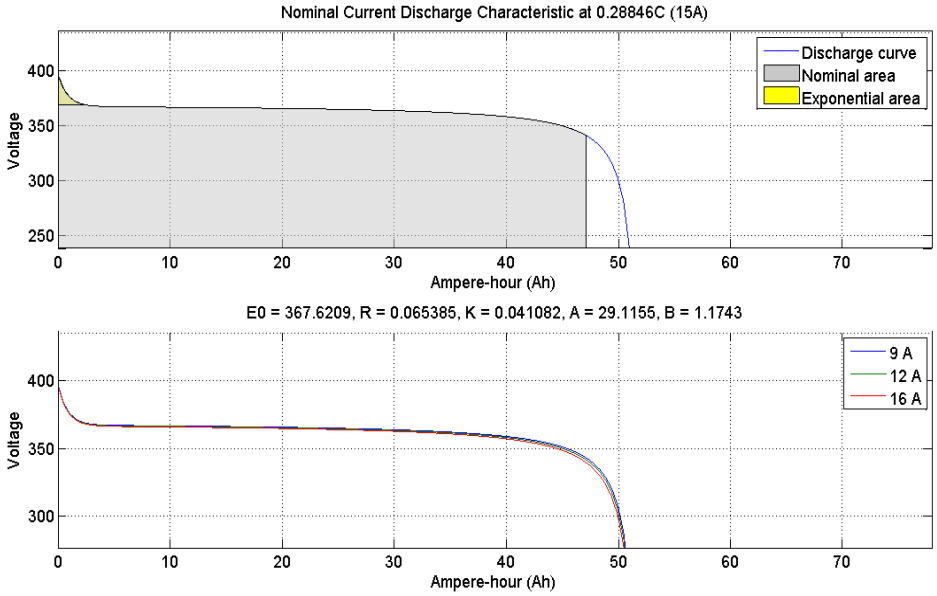


Fig.3. 16 The battery discharge characteristics for 3 different discharge current (9A, 12A, 16A). The gray Area depicts the extractable battery energy (which we chose to be around $17kW.h$, this value is less than total battery energy). Charge characteristics will be the opposite if we neglect the hysteresis effect of the battery

The battery capacity, like today's conventional hybrid vehicles (like Toyota Pirus or Chevrolet Volt's or EV1) is selected to be around 18kWh. This means that with constant power of 3.6 kW, it takes around 5 hours to charge the battery with slow charging method. The red line in Fig.3 .17 shows the charged capacity of battery (in Ah). It should be noted that the battery should be never depleted completely.

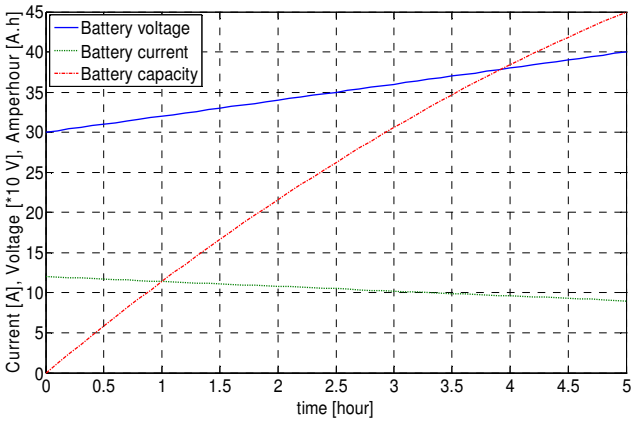


Fig.3. 17 Constant Power Charging method for a 18kW.h Li-ion battery

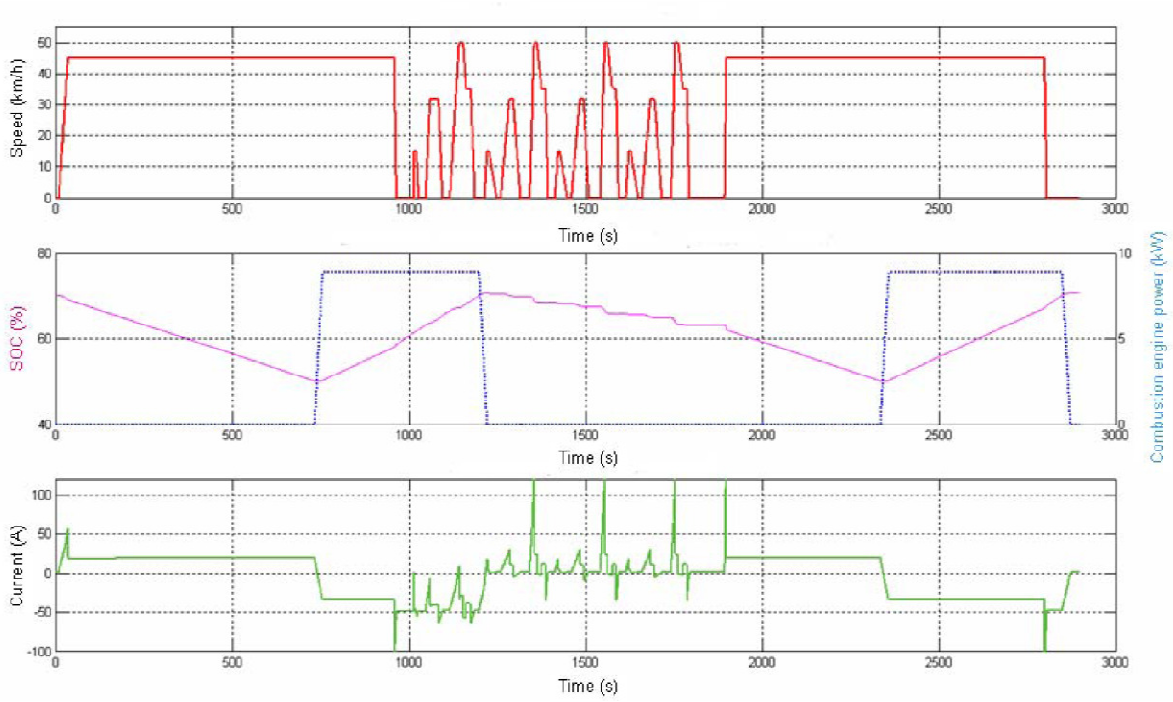


Fig.3. 18 Speed variation and current drawn from the battery by the Electric motor. With regenerative breaks SOC can fall more slowely. By courtesy of Dr. Felipe Jimenez , EPISOL project ,Polytechnic University of Madrid (UPM)

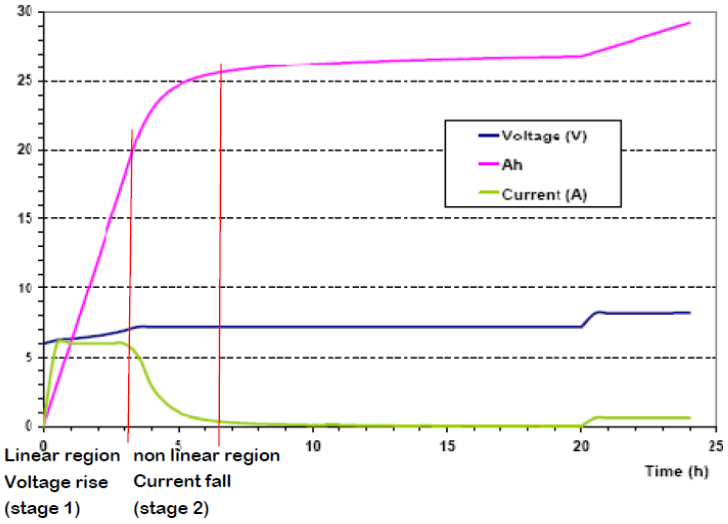


Fig.3. 19 Li-Ion recharging curve of Orvital 6V/24Ah Module. Different Charge stages of a lithium-ion battery can be seen. By courtesy of Dr. Felipe Jimenez , EPISOL project, Polytechnic University of Madrid (UPM)

4 Sources of Losses in a converter

4.1 Switch losses

4.1.1 Introduction:

After some investigations, it is realized that for this power and voltage level and for frequencies higher than 10 KHz MOSFETs[1] are good options. At low power applications and voltages up to 400 or 500 V, the forward voltage drop is superior to the forward voltage drop of minority carries devices and there is no need to mention that because of lower t_{on} and t_{off}, lower switching losses are deduced. Silicon used in power MOSFET plays important role on reduced on-state resistance.

Without going deep in physics behind a MOSFET structure, some basics are illustrated here.[2]

Although MOSFETS can be used for signal amplifying, it is the switching characteristic of MOSFET that a power electronics designer is looking for. In Fig.4. 1 the elements that have the highest influence on a switching event and switching loss can be observed. Each of these elements effects will be discussed later. Also a simple driving circuit with important parameters is depicted in Fig.4. 1.

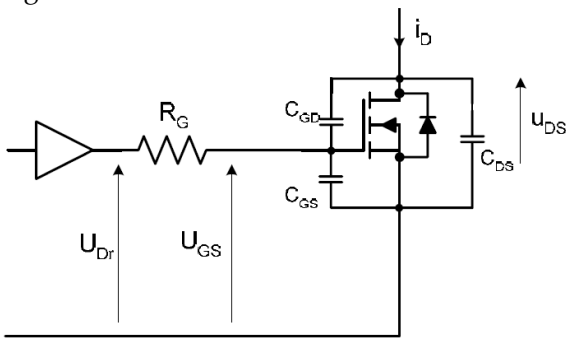


Fig.4. 1 Elements that have the highest influence on switching even of MOSFET. Driving circuit dictates the gate current which charges/discharges the MOSFET capacitances and these capacitances (esp. C_{GD}) determine the switching time. The larger the capacitances, the higher switching time thus switching losses.

4.1.2 Conduction losses

Losses on a MOSFET can be divided in 2 major losses: conduction and switching losses.

Based on Fig.4. 2 we can model a MOSFET output characteristic with a resistance ($R_{DS(on)}$). Due to *on*-resistance of MOSFET, the forward current through MOSFET leads to conduction losses. The resistance increases dramatically by increasing the temperature.

[1] Metal–Oxide–Semiconductor Field-Effect Transistor

[2] More information can be found in literatures such as chap22 of [4] and [9]

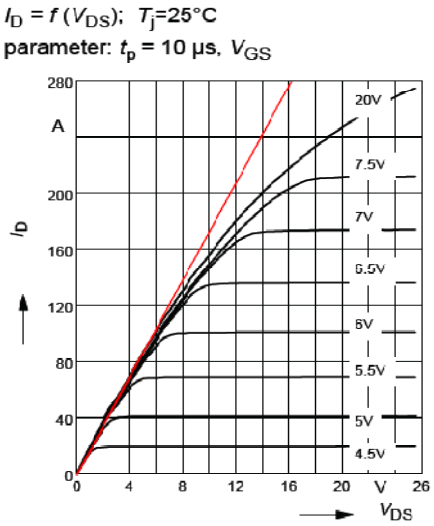


Fig.4. 2 Straight red line: linearized model of MOSFET. We wish the MOSFET operates only in this line in Power electronics applications. the reverse of the red line slope is $R_{DS(on)}$ (www.Infineon,.com *SPW47N60C3)*

For a switching mode buck converter, Provided that the current ripple is negligible, RMS current can be calculated by (4.1)

$$I_{d,rms} = I_o\sqrt{D} \tag{4.1}$$

Conduction losses of MOSFET can be calculated by (4.2) and alternatively (4.3)

$$P_{on} = I_{d,rms}^2 r_{DS(on)} \tag{4.2}$$

$$P_{on} = I_o^2 . D . r_{DS(on)} \tag{4.3}$$

Where:

$R_{DS(on)}$: On- state resistance of MOSFET, It is function of I_D and V_{gs}: by increasing I_D and V_{gs}, $R_{DS(on)}$ increases and decreases respectively. This resistance is highly dependent on temperature.

$I_{d,rms}$: RMS value of the MOSFET on-state current

D: Duty cycle

Also the conduction losses of the body anti parallel diode of a MOSFET can be calculated by modelling a diode with a DC voltage source (u_{D0}) and on-state resistance, R_D as it can be seen from Fig.4. 3

In MOSFET datasheets, there is a graph that describes the anti parallel diode behaviour. This graph for *IRFPS40N50L* can be seen in Figure below. The Figure self explains how to find R_D and u_{D0}.

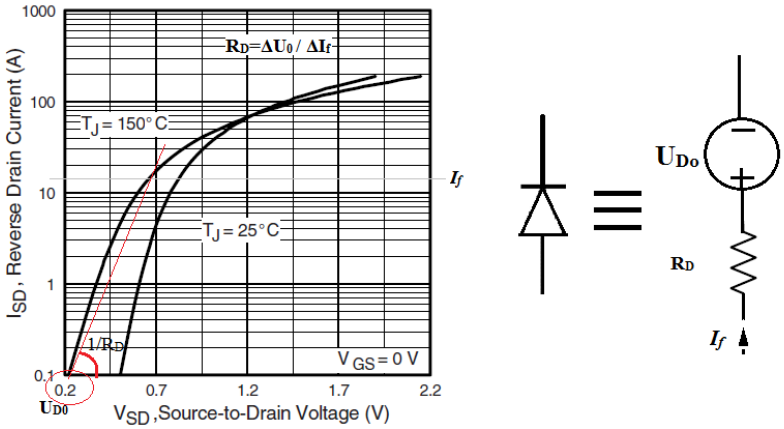


Fig.4. 3 Modelling a diode with DC voltage source (u_{D0}) and on-state resistance. Cortesy of Infineon (www.infineon.com)

4.1.2.1 Typical Source Drain Diode Forward Voltage and equivalent Diode model

Based on the equivalent diode model from Fig.4. 3 the following equations for conduction losses can be found:

$$U_D = U_{Do} + R_D i_F \quad (4.4)$$

$$P_{on} = U_{Do} i_{F,av} + R_D . I_{rms}^2 \quad (4.5)$$

Where

u_{D0} : Diode on-state zero-current voltage (Temperature dependent voltage source)
R_D : Diode on-state resistance.

4.1.3 Switching losses

Generally speaking, due to complexities and lots of conditions such as the effect of the parasitic inductive components, an accurate evaluation on switching losses is impossible [14]. Here we try to have a fair estimation of switching losses. The switching losses in a MOSFET depend on some parameters such as the voltage /current of MOSFET when a gate-source voltage, V_{gs} is applied and also the gate current and voltage (driving circuit).

This thesis does not cover transient behavior explanations and physics of switches. In order to understand the source of switching losses, it is recommended to study the transient behavior of a MOSFET during a switching event.

In each topology, the dynamics of transient behavior may be varied. In the first step, a simple buck converter with a MOSFET and its free-wheeling diode in parallel with an inductive load (that can be assumed as a constant current source, *Io*) is presented in Fig.4. 4.

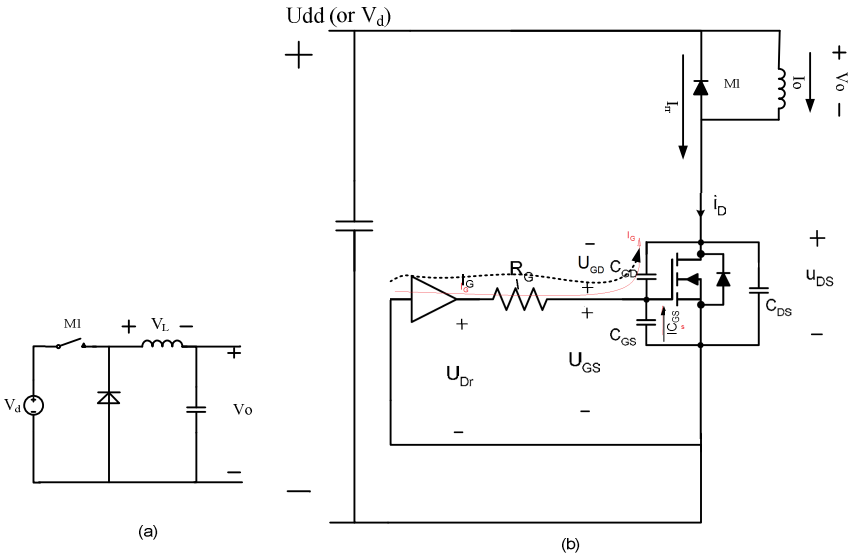


Fig.4. 4 a) Conventional Buck converter. b)The equivalent dynamic test circuit, suitable for studying the transient analysis and the role of body diode, M1, note that we assume Io=cte for all the times.

Although different configuration of elements, the principle of operation of such a Buck converter is similar to the conventional Buck converter studied before.

The waveforms of switching transient are illustrated in Fig.4. 5 and 4. 6

4.1.4 Turn-on losses and dramatic effect of Reverse Recovery Charge

Switching losses in most DC-DC converters which the p-n diode also takes current in some portion of a cycle are highly influenced by reverse recovery characteristics of the diode. Unfortunately RR characteristics of MOSFET body diodes are not so good (at the moment) Later on we will see that the reverse recovery charge can contribute a large amount of losses of a converter.

From Fig.4. 4 we can say that during the current rise time interval, the drain current, i_D increases to $I_o + I_{rr}$ instead of I_o due to the reverse recovery current of the body diode and this, in turn increases U_{gs} beyond the expectedU_{gs,I_o}. When I_{rr} starts to reduce to zero, U_{gs} starts to reduce to its expected value,U_{gs,I_o} and by referring to equation $i_{c_{gs}} = C\frac{dU_{gs}}{dt}$ as the voltage derivative is negative now, it can be inferred that this current will be added to i_g to flow to C_{gd} which (based on polarity definition in Fig.4. 4) it can be said that V_{DG} and V_{DS} decrease very rapidly during the recovery interval, $trr2$ (Fig.4. 6). $trr2$ is generally shorter than tfu. Vds may or may not reach to zero during $trr2$. The average value of C_{gd} affects $trr2 + tfu$ (It will be explained in the next section &Fig.4. 7)

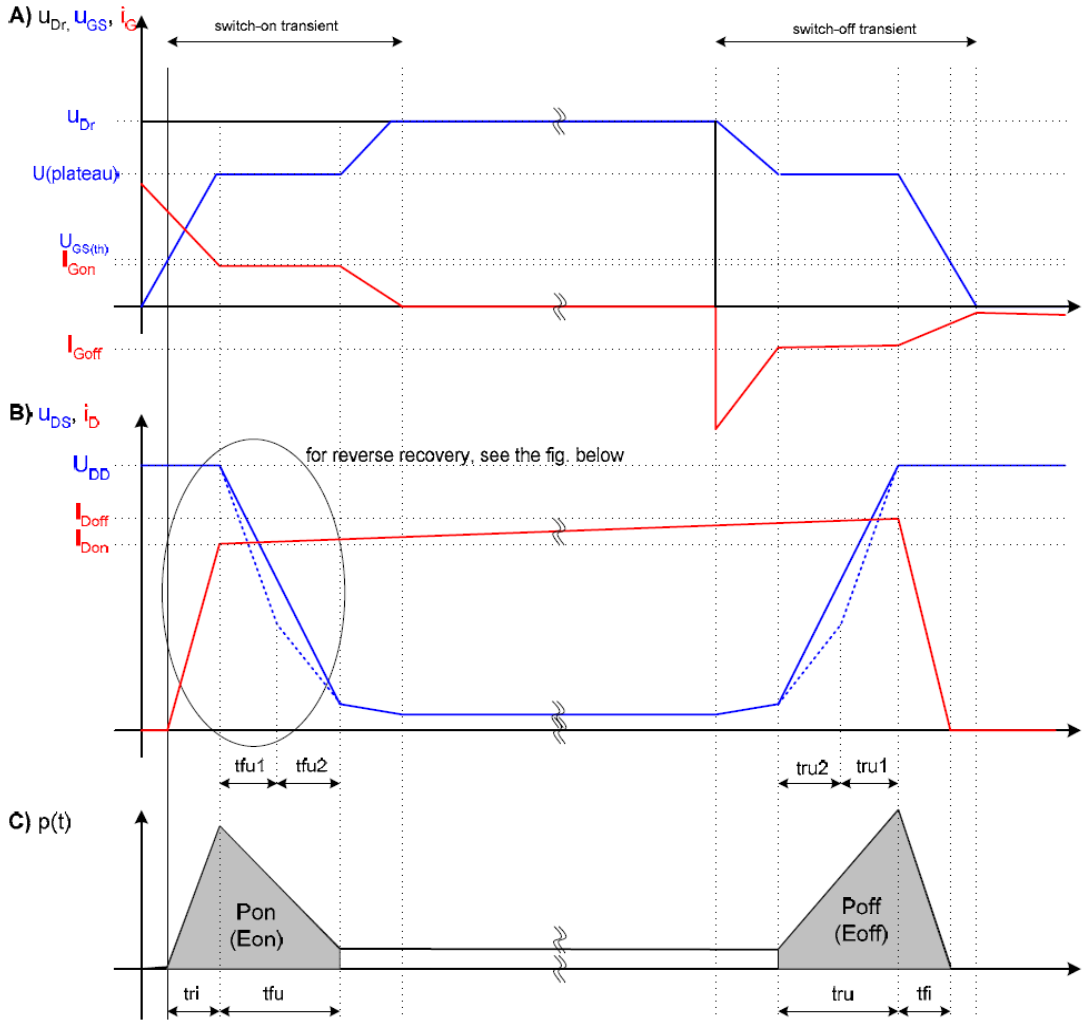


Fig.4. 5 Switching turn-on and turn-off transient and Losses of a MOSFET (without considering Reverse recovery)

4.1.4.1 Simplified estimation of Reverse Recovery (RR) losses (With no dv_f/dt optimization)

In Fig.4. 6, a simplified method for calculating RR losses is presented. In this method, we assume that the diode voltage falls instantaneously from zero to its blocking voltage (here U_{DD}) (green line in Fig.4. 6) while MOSFET voltage falls during t_{fu} to its conduction voltage ($V_{DS(on)} = R_{DS(on)}I_L$). Although this assumption obviously violates the Kirchhoff Voltage Law (KVL) it will help us to have the worst case losses calculation. (For both diode and MOSFET losses)

Fig.4. 6 explains this transient process. The energy losses caused by RR can be divided in 2 parts:

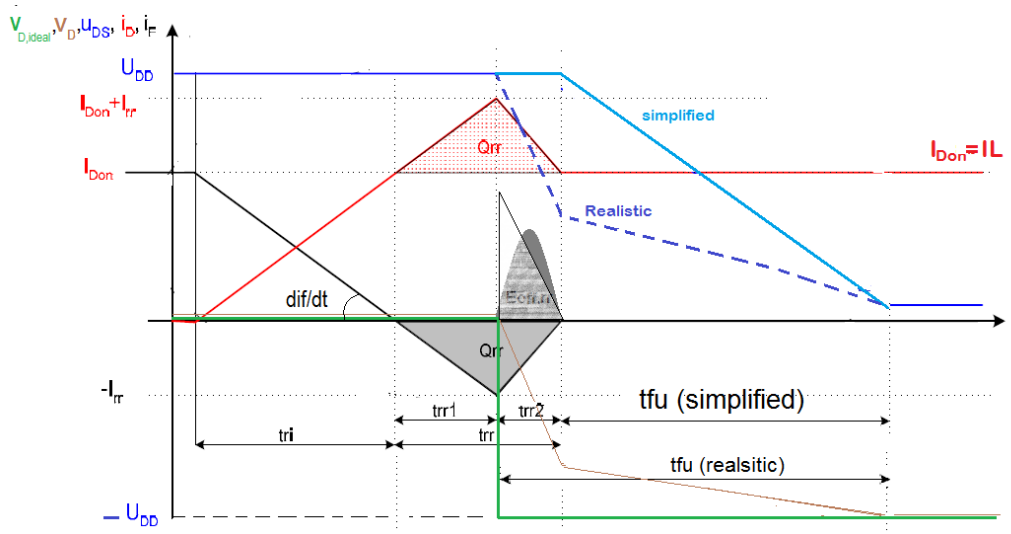


Fig.4. 6 MOSFET voltage (dark blue) and current(red) turn on transient and Diode turn-off voltage (Brown) and current (black) turn-off transient. When Reverse recovery effect is taken to the account, the MOSFET/Diode voltage /current waveforms change as it can be seen here. Then the equation $U_{DD}I_{Don}\frac{t_{ri}+t_{fu}}{2}$ cannot solely describe the total switching losses. The diode also introduces some extra losses; triangular shaded area: the worst case overestimated diode energy loss[1] ($Udd = Vd$). In reality, I_{Gon} affects t_{fu} just after the current starts to decrease (realistic model) but for simplicified model t_{fu} is assumed from the time t_{rr2} is finished

1. Diode turn-off , $E_{off,D}$ (corresponding to MOSFET turn-on, E_{onMrr}) can be calculated by multiplying the diode voltage, V_D and the diode current, I_{Don} during this transient.

Based on MOSFET waveforms in Fig.4. 6 we can extract practical equations for switching losses. For simplification, we assume that in the diode, the reverse blocking voltage happens simultaneously as is shown in green in Fig.4. 6

An interesting and important factor which is determinant in diode switching losses is soft factor, S which is defined as the ratio of t_{rr2} to t_{rr1}: $S = \frac{t_{rr2}}{t_{rr1}}$

Based on Fig.4. 6 and the triangular shaded area which represents the energy losses, we can write:

[1] As it can be seen from the Figure, dv/dt is finite in the real case, but in order to have the worst case condition, dv/dt is assumed to be infinitive.

$$Qrr = \frac{t_{rr} I_{rrm}}{2} => I_{rrm} = \frac{2Q_{rr}}{t_{rr}} \quad (4.6)$$

$$E_{off,D} = \int_0^{t_{rr}} V_d I_{rr}(t)\, dt = V_d \int_{t_{rr1}}^{t_{rr}} I_{rr}(t) dt = \frac{V_d I_{rrm}}{2} t_{rr2} \quad (4.7)$$

$$=> E_{off,D} = \frac{V_d Q_{rr} t_{rr2}}{t_{rr}} = V_d Q_{rr} \frac{S}{S+1} \quad (4.8)$$

Only if $t_{rr1} = t_{rr2}$ $(or\ S = 1)$ *then:*

$$E_{off,D} = \frac{V_d I_{rrm}}{2} \frac{t_{rr}}{2} =>\ E_{off,D} = \frac{V_d Q_{rr}}{2} \quad (4.9)$$

Where for (4.6) to (4.9):

Qrr: Diode Reverse Recovery charge
E_{offD} : Diode turn-off energy losses
I_{rrm} : Max Reverse Recovery current
t_{rr} : Reverse Recovery time, defined in Fig.4. 6

The switching losses can be divided to 3 different losses.

1. Turn-on energy losses in power MOSFET (E_{onM}): As it can be seen from Fig.4. 6, a MOSFET turn-on energy loss is sum of MOSFET energy losses without considering reverse recovery energy loss, E_{onMi} (during $tri + tfu$) and the reverse recovery energy loss during trr, $E_{onM(trr)}$:

$$E_{onM} = E_{onMi} + E_{onM(trr)}$$

Where:

$$E_{onMi} = V_d\, I_L \frac{t_{ri} + t_{fu}}{2} \quad (4.10)$$

Voltage fall time, t_{fu} can be calculated by (4.11):

$$t_{fu} = \left(U_{DD} - R_{DS,on} I_{Don}\right) \frac{C_{GD}}{I_{Gon}} = \left(U_{DD} - R_{DS,on} I_{Don}\right) R_G \frac{C_{GD}}{U_{Dr} - U_{(plateau)}} \quad (4.11)$$

By changing the time origin to the beginning of t_{rr}, MOSFET losses during t_{rr} can be found:

$$E_{onM(trr)} = \int_0^{t_{rr}} V_d I_{rr}(t)\, dt = \frac{V_d I_{rrm}\, trr}{2} + I_L V_d t_{rr2} = V_d Q_{rr} + I_L V_d t_{rr2} \quad (4.12)$$

Where for (4.10) to (4.12):

I_{Gon}[1]: Gate current; $I_{Gon} = (U_{Dr} - U_{plateau})/R_G$
U_{DD}: Converter DC (and blocking) voltage (here the same as Vd)
I_{Don}: Drain current when switch is on (=I_L)
tri (tfi): Current rise time (fall time) during switch-on (off) transient (in datasheet: tr (tf))
tfu (tru): Voltage fall (rise) time
Q_{rr}: Reverse recovery charge
R_{dson}: Drain-source on-state resistance
U_{Dr}: Driver output voltage (Fig.4 .1)
$U_{plateau}$: Plateau voltage (from datasheet)
C_{GD} (or Crss): Gate-drain capacitance, also known as Miller capacitance, which provides the feedback loop between the output and the input

We saw that our calculations are based on the worst case. As for our case $I_L t_{rr2} \ll Q_{rr}$ the second term of $E_{onM(trr2)}$ in future calculations will be neglected.

From (4.11) and Fig.4. 7 it can be deduced that the gate-drain capacitance affects voltage rise/fall time and is strongly nonlinear. $Crss$ is estimated by two-point approximation, C_{GD1} and C_{GD2}: If $U_{DD}/2 \le U_{DS} \le U_{DD} \rightarrow C_{GD1=}f(U_{DD})$ and if $0 \le U_{DS} \le U_{DD}/2 \rightarrow C_{GD2=}f(I_{Don} R_{DS,on})$

[1] The gate current, I_{Gon} through C_{GD} is calculated by the capacitance basic equation $I_{Gon} = C_{GD} dV/dt$. see [16]

Then approximated value for gate-drain capacitance C_{GD} will be the average value of C_{GD2} and C_{GD1}: $C_{GD} = \frac{C_{GD1}+C_{GD2}}{2}$

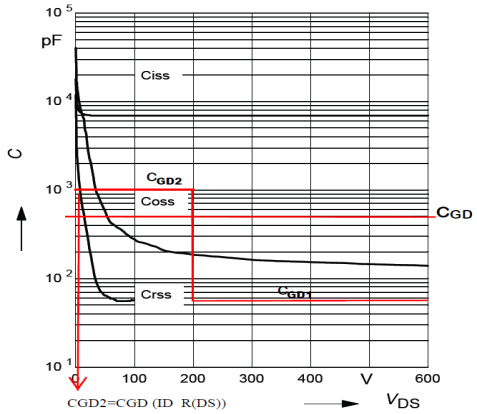


Fig.4. 7 Drain-gate Capacitance as a function of V_{DS}; two point demonstration and final selected value: C_{GD}

4.1.4.2 More realistic estimation of Reverse Recovery (RR) losses, with optimized dv/dt

This method differs from previous method in two ways. Here

1. in time interval *trr1,* the MOSFET (IGBT) switch losses are not neglected.
2. It is assumed that during $trr2$, V_{DS} dramatically falls (green solid line in Fig.4.8). This can be true if dv/dt is high enough that can drag the MOSFET voltage down to somewhere around zero during $trr2$ ($tfu = trr2$). As it was illustrated before, tfu can be controlled by Gate driving circuit (eq.(4.11)). The optimum value for dv/dt is when MOSFET voltage drops to zero just at $trr2$. Shorter tfu will increase diode turn-off losses (like previous method) and longer tfu will result in larger MOSFET turn on losses. (As it was assumed in previous method)

From Fig.4. 8 we can divide the losses in 3 regions. The followings show how to find RR losses which is the sum of all losses of all regions.

Region1:

Diode Losses=0

MOSFET energy losses**:**

$$E_{onM1} = U_{DD} I_{Don} \frac{t_{ri}}{2} \tag{4.13}$$

But we can write (4.13)

$$t_{ri} = \frac{I_L}{\frac{di_f}{dt}} \xrightarrow{I_{Don} = I_L} E_{onM1} = U_{DD} \frac{I_L^2}{2\frac{di_f}{dt}} \tag{4.14}$$

Region2:

Diode Losses=0

MOSFET energy losses: As before:

$$E_{onM2} = (\frac{I_{rrm}}{2} + I_L)\, V_d\, t_{rr1} \tag{4.15}$$

But for $trr2$ we can write

$$\frac{di_f}{dt} = \frac{I_{rrm}}{t_{rr1}} => t_{rr1} = \frac{I_{rrm}}{\frac{di_f}{dt}} \tag{4.16}$$

So we can rewrite (4.15) as below:

$$E_{onM2} = \left(\frac{I_{rrm}^2}{2} + I_L\, I_{rrm}\right)\frac{V_d}{\frac{di_f}{dt}} \tag{4.17}$$

Region3:

Diode energy Losses: (time offset: beginning of *trr2*)

The diode current and voltage equation valid during t_{rr2} are:

$$I_D(t) = -I_{rrm} + \frac{I_{rrm}}{t_{rr2}}\, t \tag{4.18}$$

$$V_D(t) = \left(-\frac{V_d}{t_{rr2}}\right) t \tag{4.19}$$

By integrating the multiplication of (4.18) and (4.19) Energy losses will be obtained:

$$E_{offD3} = \int_0^{t_{rr2}} I_D(t)\; V_d(t)dt = \frac{I_{rrm}}{t_{rr2}}\frac{t^2}{2}\, V_d - \frac{V_d I_{rrm}}{t_{rr2}^2}\frac{t^3}{3} \xrightarrow{t=t_{rr2}}$$

$$E_{offD3} = \frac{V_d I_{rrm} t_{rr2}}{6} = \frac{1}{3} V_d Q_{rr}\frac{S}{S+1} \tag{4.20}$$

Where:

I_D: Diode current

MOSFET energy losses:

With the same procedure MOSFET losses for region3 can be calculated:

$$E_{onM3} = V_d\left(\frac{I_L}{2} + \frac{I_{rrm}}{3}\right) t_{rr2} \tag{4.21}$$

4.1.4.2.1 The Turn-off transient time and regions of activity [15]

Based on KVL and KCL we know that

$V_D = V_{DS} + V_D$

$I_L = I_D + I_M$

It is important to find out in each region which element influences the current of the other element.

During $tri + trr1$, *Switch current* dictates the slope of the diode *current* (should be found in datasheet and be corrected by rescaling the value)

During $trr2$ the diode *current* dictates the slope of the switch current.

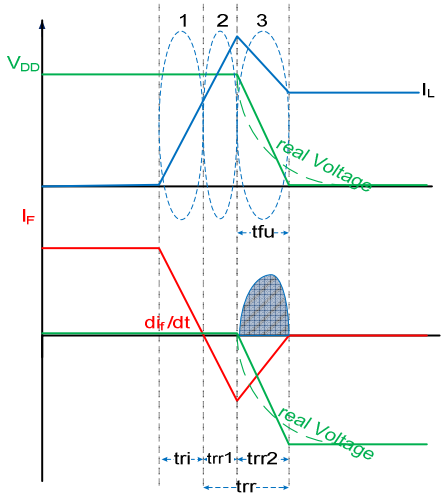


Fig.4. 8 Up: MOSFET Voltage and current during turn-on transient. Down: Diode voltage and current transient during MOSFET turn-on(=Diode turn-off)

4.1.5 Turn-off energy losses in power MOSFET, E_{offM}

Switch Turn-off in most cases corresponds to diode turn-on. Diode turn-on energy losses, $E_{on,D}$ in most cases is neglected as we do not have reverse recovery on diode turn on. Thus it is only MOSFET turn-off energy losses which can be found by (4.22):

$$E_{offM} = U_{DD}\, I_{Doff}\, \frac{t_{ru} + t_{fi}}{2} \tag{4.22}$$

Again like t_{fu} in previous part, t_{ru} is calculated based on C_{GD1} and C_{GD2} . The formula is more or less the same. The only difference is in I_{Goff} :

$$I_{Goff} = -\frac{U_{(Plateau)}}{R_G} \tag{4.23}$$

4.1.5.1 Scaling the current time from reference (datasheet) value to case value

In MOSFET datasheets, only current rise and fall time (t_r and t_f respectively) are provided which these values are measured in a certain operating point (v_{ref} and I_{ref}) [16]. In order to find correct time values at desired voltage and current level, an approximation should be done. By assuming constant slope during the switching transient (Fig.4. 9.(B)), we can find new current rise and fall time.

From Fig.4. 9.(B) , new current rise time, t_{new} can be expressed as below:

$$\frac{V_{ref} I_{ref}}{t_{ref}} = \frac{V_{new} I_{new}}{t_{new}} \Rightarrow$$

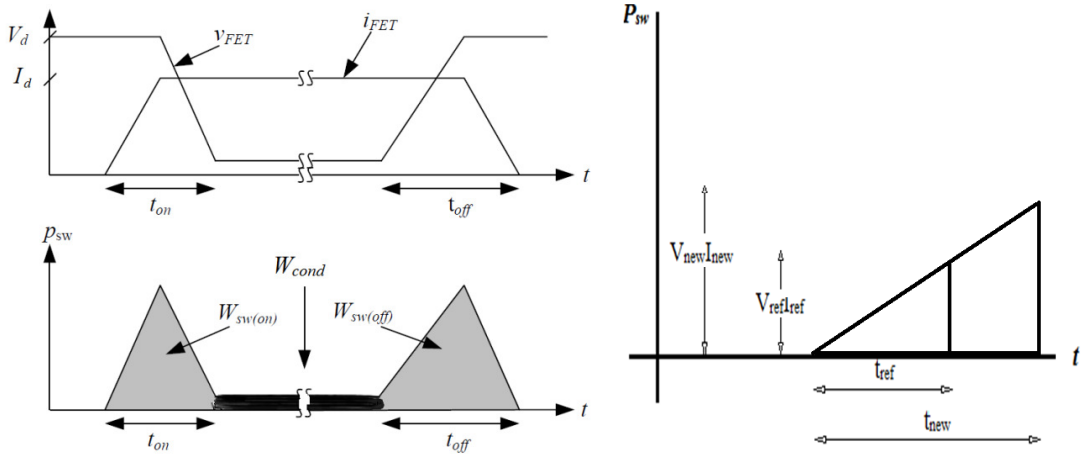
$$t_{new} = \frac{V_{new} I_{new}}{V_{ref} I_{ref}}\, t_{ref} \tag{4.24}$$

Where:

t_{ref} : Current rise time in datasheet under the condition of V_{ref} and I_{ref}

t_{new} : New current rise time when $V_{new} = V_{DD}$ and $I_{new} = I_D$

With the same method current fall time can be found as well.



(A) (B)

Fig.4. 9. (A) Switch waveforms and energy losses ($t_{on} = t_{fu} + t_{ri}$, $t_{off} = t_{fi} + t_{ru}$) , (B) Scaling of current rise time based on reference value, t_{ref} switching losses

4.2 Inductor / transformer Losses

4.2.1 An introduction to available core materials

4.2.1.1 Choice of core material:

Most of magnetic core materials are made of Iron alloys; consequently they are good electrical conductors. This means ac magnetic fields will lead to electrical eddy current which in turn this eddy current causes $R.I^2$ losses in the resistance of the core material. Eddy currents are dominant especially at high frequency applications [11].

Generally four types of materials can be used for inductor and transformer cores:

Silicon steel and similar materials: they have a high saturation flux density (between 1.5 and 2 T) but they have a high core loss because they have low resistivity. Even with laminated or ribbon cores still exhibit high power losses especially at high power applications. [11]

Iron alloys contain ferromagnetic particles. Diameters of the particles are small enough to limit eddy currents. Powdered iron and molybdenum Permalloy powder cores saturate at flux densities around 0.6 to 0.8 T. These materials show lower core losses than silicon steel laminated materials. These cores have relatively low permeability. Powder cores can be used as filter inductors in high frequency (100 kHz) switching converters.

Amophous alloys have lower hysteresis and eddy current losses than two upper materials but still have higher losses than Ferrites.

Ferrite Materials are ceramic materials with low saturation flux density (0.3 to 0.5 T) Due to their higher resistivity; they have much smaller eddy current losses. Manganese-zinc (MnZn) ferrite cores are widely used in power inductor and transformer application with switching frequency of 10 kHz up to 1MHz. Nickel- zinc materials can be used at even higher frequencies. Ferrite materials are widely used in power applications these days. These materials most advantage is their lower power losses. Especially at high magnetic flux levels, hysteresis losses for these materials are minimized.[1] By nature, this causes an increase in the permeability level of such a material. In power applications, this will usually have positive effects. The price and low saturation is the reason they cannot be used in high power applications.

4.2.2 Core losses

In any magnetic cores two types of losses happened. One is due to the material characteristic which is generally referred to core losses and one is based on flowing current on copper wires and is called copper losses. Each of these two types of losses is caused by naturally different phenomenon.

4.2.2.1 Hysteresis losses

When an external magnetic field is applied to a ferromagnet, the atomic dipoles align themselves with the external field inside the magnet. Then if the direction of magnetic field changes, these dipoles need to rotate to align to new direction and this rotation is associated with friction which is the source of hysteresis losses. So the main reason is the changing of

[1] http://ferroxcube.com/appl/info/3C94.pdf, Introducing the new power ferrite 3C94

magnetic field (variable source). Generally the area under B-H curves is equal to Hysteresis losses *if* H variations are so slow (i.e. very low frequency)

4.2.2.2 Eddy current and Eddy losses

Magnetic core materials are relatively good electric current conductors. Due to the flow of the flux inside the core, a current is induced perpendicular to the flux direction to (according to Lenz low) oppose the changes in the core flux. This current, known as Eddy current tends to prevent the flux to penetrate into the core.

In addition to frequency and flux level, eddy losses depend on molecular structure of the core material. Although ferrite cores have high resistivity, but their resistivity is not infinite so eddy currents are induced into the core by changing the magnetic flux. As described before adding semi conducting grain crystallites with a thin isolated layer (such as 0.001 Ωm for MnZn, and 30 Ωm for NiZn) reduce eddy currents. Resistivity and permeability of grain crystallites are strongly dependent on frequency and temperature. The reason is that by increasing temperature and frequency, grain crystallites and insulation are bypassed by the capacitances between grains and in practice their effect is reduced. An example is 3F3 ferrite which its resistivity increases severely from 0.3Ωm to 2.1Ωm and relative permeability reduces from 110000 to 60000 by increasing frequency and temperature from 10kHz to 1MHz and 25 ^{0}c to 100 ^{0}c, respectively [8]. This makes this material more suitable for higher frequencies. (as we will see later)

4.2.2.3 Total core losses

Total core Losses (Hysteresis and Eddy losses) in ferrite materials depend on frequency (f in Hz), flux density (B in T)) and temperature (T in ^{o}C). The relation between total core power losses (with sinusoidal excitation) and these quantities can be found by Steinmetz equation [8] , [17], [18]:

$$P_{core} = C_m f^x B_{peak}^y (ct_0 - ct_1 T + ct_2 T^2) \ [mW/cm3] \quad (4.25)$$

Every material has its own C_m, x, y, ct_0, ct1 and ct_2 which have been found by curve fitting of measured power loss data and in some cases are obtained in the data sheet of the particular material (Table.4.2). ct_0, ct_1 and ct_2 are dimensionised in such a way that at $T = 100^oC$, $(ct_0 - ct_1 T + ct_2 T^2)$ will be equal to 1. For simplicity for further calculations we assume that $T = 100^oC$ and (4.25) Can be simplified as (4.26) (for $T = 100^oC$)

$$P_{core} = C_m f^x B_{peak}^y \quad [mW/cm3] \quad (4.26)$$

Equations (4.25) and (4.26) are only valid if the excitation is sinusoidal without DC component. But later on we will see that transformer and core flux density more or less look like Fig.4. 12

Mulder in [18] modified Steinmetz equation in a way that it can be used for different types of flux density wave forms. For a piecewise linear current shape, the modified equation is expressed as (4.27,28) [8], [19]

$$P_{core} = 1000 \frac{1}{T_s} C_m f_{eq}^{x-1} B_{peak}^y V_e \quad [W] \quad (4.27)$$

$$f_{sin_{eq}} = \frac{2}{\pi^2} \sum_{k=2}^{K} \left(\frac{B_k - B_{k-1}}{B_{max} - B_{min}} \right)^2 \frac{1}{t_k - t_{k1}} \quad (4.28)$$

Where

B_{max} : Maximum flux density during switching period (without considering DC part) (T)
B_{min} : Minimum flux density during switching period (T)
B_k :Flux density at t_k (T)
t_k : time instant k (s)
K number of sub periods in the switching period
T_s: Switching period
V_e: Core effective volume [m3]
F_sin_eq:Equivalant frequnecy of sine
B_{peak}: half of the peak to peak value of the ac wave form

It should be noted that the hysteresis losses depend on both B_{ac} and B_{dc}. But B_{ac} has a dominant influence on core losses in actuality as it is shown in [20] (Fig.4. 10). This can be explained in Fig.4. 11, where minor *B_H* loop area (ac part of *B*) indicates the total core losses. Referring to Fig.4. 12.(a) , B_{ac} is defined as a peak to peak value of the ac wave form .If the flux density has time average B_{dc} then the appropriate value to use is $B_{ac} = B_{max} - B_{dc}$

In data sheets B_{peak} is widely used and it is half of the peak to peak value of the ac wave form and shouldn't be mistaken with total peak flux , $B_{max}(= B_{dc} + B_{ac})$

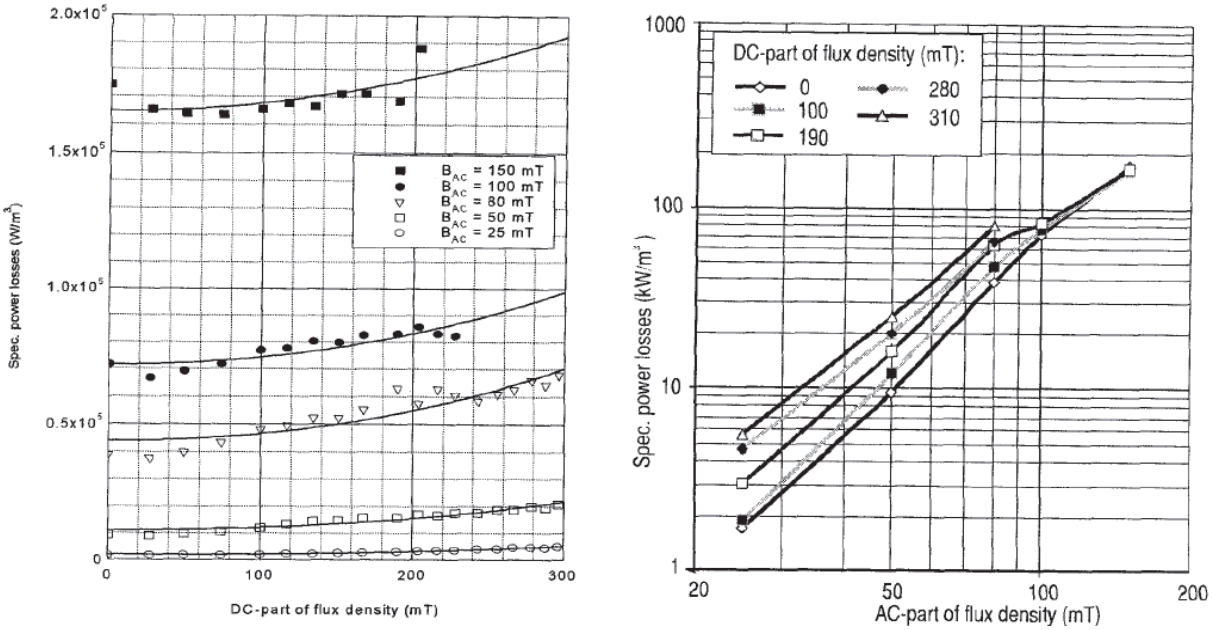


Fig.4. 10 Left: Low loss dependency on the DC part of flux (esp. at low B_{ac}) Right: high dependency on *ac* part of flux. From Figures 6 and 7 of [20]

4.2.2.3.1 Inductor core losses

The reduced size formula which is valid for the inductor of a full bridge DC-DC converter (without considering the DC component of flux density) can be extracted from (4.27) and (4.28), as (4.29) and (4,30):

$$f_{sin_{eq}} = \frac{2}{\pi^2}\left(\left(\frac{B_{ac}}{B_{ac}}\right)^2 \frac{1}{DTs} + \left(\frac{-B_{ac}}{B_{ac}}\right)^2 \frac{1}{(0.5-D)Ts} + \left(\frac{B_{ac}}{B_{ac}}\right)^2 \frac{1}{DTs} + \left(\frac{-B_{ac}}{B_{ac}}\right)^2 \frac{1}{(0.5-D)Ts}\right) \quad (4.29)$$

$$f_{eq} = \frac{2}{\pi^2} f_s \frac{1}{D(0.5-D)} \quad (4.30)$$

4.2.2.3.2 Transformer core losses

Despite the inductor core losses, the transformer core losses will be much more severe as equivalent frequency, $f_{sin_{eq}}$ is high. This can be testified by (4.31). The reason is due to a very sharp flux density during transient Δt (from Fig.4. 12.(b))

$$f_{sin_{eq}} \cong \frac{2}{\pi^2}\left\{4\left(\frac{B_{ac}/2}{B_{ac}}\right)^2\right\}\frac{1}{t_k - t_{k1}} = \frac{2}{\pi^2}\frac{1}{t_k - t_{k1}} \tag{4.31}$$

Here for simplicity it is assumed that the flux remains constant during DTs.

The leakage inductance $L_{leakage}$ mainly creates the transient time interval $\Delta t = t_k - t_{k-1}$

$$t_k - t_{k-1} = \Delta t = L_{leakage}\frac{i_{oDC}}{V_d}$$

$$f_{sin_{eq}} \cong \frac{2}{\pi^2}\frac{1}{t_k - t_{k1}} = \frac{2}{\pi^2}\frac{V_d}{L_{leakage}\, i_{oDC}} \tag{4.32}$$

Although higher leakage inductance can lead to higher switching losses (as we will see later) but regarding transformer core losses it will reduce the core losses.

In chapter 6 we perform Fourier analysis on the flux density waveforms and will find the main harmonic frequencies and their amplitude and then will plug these values to (4.26) to find the core losses of a given core material.

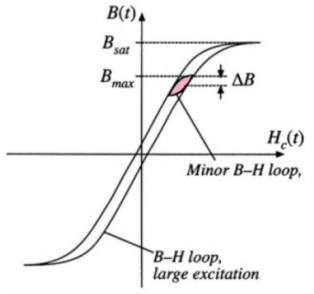


Fig.4. 11 Hysteresis loops: When B_{avg} is greater than 0, let's say 0.7 p.u, hysteresis loss is the shaded area known as asymetrical minor loops. Fluctuation of B creates the shaded area (Hysteresis losses)

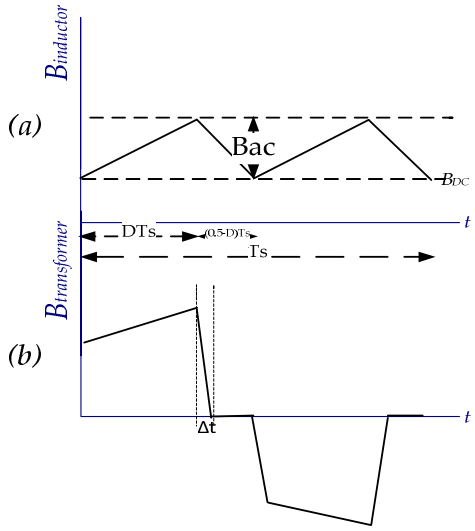


Fig.4. 12 Typical Flux density waveform of (a) inductor (b) transformer. In the inductor, the DC component of flux is neglected. For transformer, dB/dt in switching transients is so high. The effect of leakage inductance can be seen. (core permeability within its limits is considered as constant) The simulation results also complies with [10]

4.2.2.4 A glance into different ferrite materials:

In this part, different Ferrite materials and their characteristics is studied. Table.4. 1 shows different ferrite material specifications.

Table.4. 1 General Characteristics of Low and middle range frequency ferrite materials

Ferrite material	μ_i at 25 ° c	$\mu_a \pm 25\%$at 100 °c 25kHz, 200mT	B_{sat}(mT) at 25 °c (1200 A/m)	T_C (° C)	ρ(ohm.m)	Ferrite type	P_v (kW/m3) at 100 ° c 25kHz, 200mT
3C30	2100	5000	500	240	2	MnZn	80
3C90	2300	5500	470	220	5	MnZn	80
3C92	1500	5000	520	280	5	MnZn	50[1]
3C94	2300	5500	470	220	5	MnZn	?
3C95	3000	5000	530	215	5	MnZn	?

3C90: General purpose material (for low frequency application[2])

3C94: General purpose material with Lower power losses than 3C90 and 3C85.[3]

3C92 is a low frequency, high B_{sat} power material which can be used in power inductors. As inductors have mainly dc current with a small ac ripple, core losses are generally not the first worry. High saturation flux density makes high dc current possible without too much inductance loss. 3C92 for high flux density applications has an increased Curie temperature compared to the general purpose power material 3C94. Because of this, 3C92 has a higher saturation flux density. Losses are the same as for 3C94. [21]

3C95 is suitable for a broad range of temperature and power loss density versus temperature curve is very flat. (Lower dependency on temperature)

3F30 is optimized for high frequency applications. (Lower losses and leakage @ high frequencies)

Unfortunately for different materials, it is not easy to find their parameters (C_m, x, y, ct_0, ct_1 and ct_2) and most manufactures prefer using the graphs which are not so accurate. The best way to obtain these coefficients is by experimental setup. It should be considered that these formulae can't provide the exact value for power losses and it can be valid only in a limited range of frequencies and flux level. Table.4. 2 shows C_m, x and y for some Ferrite Materials.

Table.4. 2 Ferrite material parameters made by Feroxcube to calculate the core loss density [17]

Ferrite	f (kHz)	Cm	x	y
3C30	20-100	7.13e-3	1.42	3.02
3C90	20-200	3.2e-3	1.46	2.75
3C92	20-200	2.37e-3	1.42	2.75
3C94	20-200	2.37e-3	1.42	2.75
3F3	300-500	2e-5	1.8	2.5
3F3	<300	0.25e-3	1.63	2.45

[1] For 3C92 Pv at 100 ° c 100kHz, 100mT

[2] Here the frequency does not necessarily mean switching frequency but the frequency of flux variations.

[3] http://ferroxcube.com/appl/info/3C94.pdf

Based on material parameters on table.4. 2, Figs.4. 13 and Fig.4. 14 can be obtained. Plotting power losses versus B_{peak} shows that, 3C30 has the lowest losses at low peak flux densities below 0.15 T (which is our operating point for inductor)

We will see that inductor core losses are very low even independent of ferrite material. In transformer design which core losses are much higher, core material selection becomes an important factor in core losses. At $B = 0.2\,T$ and above, 3F3 is the material with the lowest core losses.

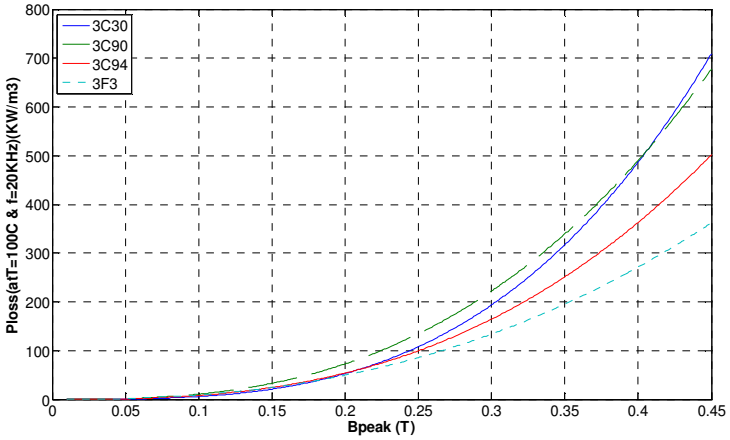


Fig.4. 13 core losses as a function of flux density

In general, for filter inductor design copper losses are dominant because in inductor, current variation is not so much and core losses can be neglected in continuous conduction mode in ferrite materials [9] as we will see soon.

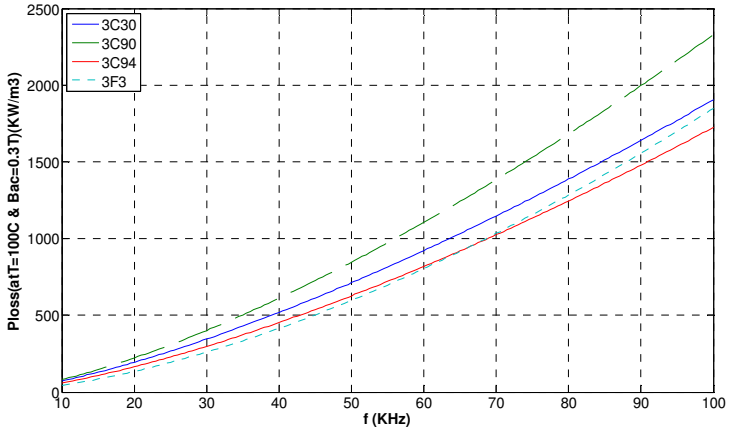


Fig.4. 14 core losses as a function of frequency (sine wave)

4.2.3 Winding losses

4.2.3.1 Low frequency copper power losses in inductors

Low frequency copper power losses (Winding losses) are the main losses in chocks.

$$P_{cu} = R.I_{rms}^2 \tag{4.33}$$

$$R = \sigma \frac{L}{A_{Cu}}$$

$$L = N \times Length\ of\ turn$$

Where:

N: Number of turns

$\sigma = 1.7e-6$ ohm. m : resitivity of copper

R : resistance

L: Length of copper wire

A_{Cu}: copper cross section

We will see later that increasing air gap leads to increasing number of turns and this, results in higher copper losses.

4.2.3.2 Transformer copper power losses

For transformer copper losses, (4.33) needs to be modified a bit:

$$P_{cu} = R_{pri}.I_{pri,rms}^2 + R_{sec}.I_{sec,rms}^2 \quad (4.34)$$

In order to find R_{pri}, number of turns in primary, N1 should be known. N1 can be expressed by

$$B = \frac{NI}{\mathcal{R}A_e} => N1 = \frac{\mathcal{R}\,B_{pri}\,A_e}{I} \quad (4.35)$$

Where:

R_{sec}, R_{pri}: secondary and primary resistance , their calculations are the same as inductor.

B_{pri}: the flux density for a particular material refered to primary side.

Equation (4.35) gives us the number of turns and subsequently the length of copper wire of primary side to be used for calculating the copper resistance and copper losses. Increasing *N1* results in higher copper and core losses (due to lower *B*). But *N1* should be high enough in order to have adequate magnetizing inductance.

4.2.3.3 Skin effect at high frequency and Litz wires

If the wire is carrying high frequency currents, depending on its diameter, the skin effect may affect the distribution of the current across the section by concentrating the current on the surface of the conductor. The reason is the eddy current that opposes the main current. The main current inside the core is cancelled to some extent in the center of conductor and moves towards the surface. This skin effect plays an important role in Switched-mode power supply transformers where the wires carry high currents and high frequencies (between 10kHz and 1MHz). Often in those transformers, the windings are made of multiple isolated wires in parallel with a diameter twice the skin depth and which are twisted together to increase the total skin area and to reduce the impact of the skin effect. These types of wires are called LITZ wire. Even properly constructed Litz wires will exhibit some skin effect due to the limitations of stranding. Wires intended for higher frequency ranges require more strands of a finer gauge size than Litz wires of equal cross sectional area but composed of fewer and larger strands.[1]

4.2.4 Total inductor and transformer losses and their dependency on core volume and geometry

For an inductor with inductance of *L*, for a certain core material with relative permeability, μ_r we can write:

[1] *MWS Wire Industries, http://www.mwswire.com/litzmain.htm*

$$\left.\begin{aligned}\varphi &= \frac{NI}{\mathcal{R}} \\ B &= \frac{\varphi}{A_e}\end{aligned}\right\} => B = \frac{NI}{\mathcal{R}A_e} \tag{4.36}$$

$$\mathcal{R} = \frac{L_e}{\mu_o \mu_r A_e} \tag{4.37}$$

$$N = \sqrt{L\mathcal{R}} \tag{4.38}$$

By plugging (4.37) and (4.38) into (4.36) we can extract (4.39):

$$B = \frac{NI}{\mathcal{R}A_e} = I\sqrt{L\,\mu_o\mu_r}\,\frac{1}{\sqrt{L_e A_e}} \tag{4.39}$$

$$B \propto \frac{1}{\sqrt{V_e}} \tag{4.40}$$

This relation for transformer is a bit different as the inductance value is not of interest and the number of turns is in our hand:

$$B = \frac{NI}{\mathcal{R}A_e} = \frac{NI}{\frac{L_e}{\mu_o\mu_r A_e}\,A_e} = \mu_o\mu_r\frac{NI}{L_e} \propto \frac{1}{L_e} \tag{4.41}$$

In case of the cores with circular cross sections (like EC70) the copper losses for an inductor can be expressed by

$$L_{cu} = N \times Length\ of\ turn = N\,2\pi\sqrt{\frac{A_e}{\pi}} = 2N\sqrt{\pi A_e} \tag{4.42}$$

$$P_{cu,ind} = R_{cu}I_{rms}^2 = \frac{\sigma L_{cu}}{A_{cu}}I_{rms}^2 = \frac{2\sigma\sqrt{\pi A_e}}{\frac{I_{rms}}{j}}\,N\,I_{rms}^2 = \frac{2\sigma\sqrt{L\,\pi\frac{L_e}{\mu_o\mu_r}}}{\frac{I_{rms}}{j}}\,I_{rms}^2$$

$$= 2\sigma j\sqrt{L\,\pi\frac{L_e}{\mu_o\mu_r}}\,I_{rms} \tag{4.43}$$

$$P_{cu,ind} \propto \sqrt{L_e} \tag{4.44}$$

While for transformer core losses:

$$P_{cu,trans} = R_{cu}I_{rms}^2 = \frac{\sigma L_{cu}}{A_{cu}}I_{rms}^2 = \frac{2\sigma\sqrt{\pi A_e}}{\frac{I_{rms}}{j}}\,N\,I_{rms}^2 = 2\sigma\,j\,N\,\sqrt{\pi A_e}\,I_{rms} \tag{4.45}$$

$$P_{cu,trans} \propto \sqrt{A_e} \tag{4.46}$$

Where:

R_{cu} Copper resistance
$\mathcal{R}$: Reluctance
N: Number of turns
L: Inductance [H]
L_{cu}: Copper length
A_{cu}: Copper wire cross section
V_e: Effective volume which is the multiplication of L_e and A_e
L_e: Effective length
A_e: Effective cross section
j: Current density (we assume J=3A/mm²)

For core losses of an inductor, in the previous section we found out that $P_{core} \propto B_{peak}^{y} V_e$. As in (4.40) we saw that $B \propto 1/\sqrt{V_e}$, we can write:

$$P_{core,ind} \propto V_e^{-\frac{y}{2}+1} \qquad 2.5 < y < 3.5 \tag{4.47}$$

Equation (4.47) suggests that for most Ferrite materials by increasing the volume the core losses of an inductor will be slightly reduced.

While for transformer core losses, it can be written

$$P_{core} \propto A_e \, L_e^{-y+1} \qquad 2.5 < y < 3.5 \tag{4.48}$$

So by increasing the volume, depending on the material core losses may change slightly or may not change at all (if y=3)

From above, we can deduce that the best way to reduce the total *transformer* losses is to increase L_e (to reduce core losses) while preserving A_e(to keep copper losses constant)

From *inductor* copper and core losses equations, it can be deduced that by reducing L_e (which results in lower copper losses) and increasing volume (by increasing cross section which leads to lower core losses) total core losses can be optimized. Just keep in mind that the winding area should be also considered as a constraint.

To illustrate inductor total losses using a numerical example can be helpful. Let's say we scale a particular core by factor of 2. This means each dimension increases twice and the weight (volume) increases 8 times. Reluctance $\mathcal{R}$ is halved and Flux density is reduced $2\sqrt{2}$ times. Depending on the level of the flux density this may or may not result in significant core losses changes but generally it should be expected that Core losses reduce (see Fig.4. 13). Also copper losses increase $\sqrt{2}$ times.

Adding an *airgap* can increase reluctance dramatically which this corresponds to reducing the equivalent permeability. In datasheets a new equivalent permeability, μ_i for each airgap is given. Increasing the air gap reduces the flux which results in lower *core* losses (for both transformer and inductor). But about copper losses, based on $N = \sqrt{\mathcal{R}L}$, in an inductor (with constant inductance) the airgap will cause higher copper losses, while transformer *copper* losses is not affected by the airgap length (in transformers as *N* is constant, *L* reduces)

4.2.4.1 Different Core shapes[1]

The shape of cores can affect the equivalent permeability and this can change the total core losses. As a rule of thumb, with the same material, the cores with circular cross-section have a slightly lower permeability. I.e. μ_i of EC70 (127g) and E552825 (130g) is 1580 and 1860 respectively (for 3C90). The reason is maybe due to the fact that EC cores do not have sharp ends, resulting more uniform flux inside the core.

There are different core shapes in the market that will be explained briefly:

EE: possibility to have huge airgaps. Simple, with high mass and volume, suitable for large inductances.

*EC***:** like EE cores air-gaps are provided, but in smaller sizes. Also winding leg has a circular cross section. They have large Winding area.

*ETD***:** like EC cores they have circular cross section. But no air gap is possible.

EI: No air gap is possible, but huge sizes are available

Planar ER: lower effective length and larger effective area which means much lower reluctance. It seems good option for especially high frequency applications.

PM cores: especially used for higher power ratings (high current). They are the biggest possible ferrite cores.

[1] based on www.ferroxcube.com

5 Switch losses: case setup

5.1 Introduction: case setup and investigated MOSFETs and IGBTs parameters-Buck operation

In chapter 3 the DC-DC converter topology was studied. It was decided that due to high power demand, it should be a fullbridge converter with galvanic isolation which is realised with a transformer. The final topology can be seen in fig.3. 12. In this chapter we are going to calculate losses of the DC-DC full-Bridge converter based on equations introduced in previous chapter. In order to do so, we need to fully understand the voltage and current that each element is exposed to.

Table.5. 1 demonstrates the case set-up that is applied in this section.

Table.5. 1 The specifications of the DC-DC full bridge converter

Parameter	Description
$Vd = 400\,V$	input dc link voltage from rectifier
$Pin = 3800\,W$	Input power from the rectifier
D_{max} (Buck operation)= 0.38	max duty cycle of each switch of full bridge
$n = N2/N1 = 4/3$	turning ratio of transformer: secondary/primary
$f_s = 20000\,Hz$	Switching frequency
$V_{p1} = 400V$	Max voltage over a Switch (during turn-off)
$Vo = 300{\sim}400V$	Battery side voltage variation

By referring the battery current and voltage profile (Chapter3), we can say that in the battery side, voltage increases from $300V$ to $400V$. In slow charging method, the current is well below the maximum battery current capacity and the only limitation is power drawn from the outlet[1]. The output power from an outlet should never violate its constraints and this can be done by varying the drawn current. By assuming 200W of losses during the operation (which means efficiency of 95% and later on we will find out is close to reality) the battery current, Io can be found:

$$Io,min = \frac{Po_{max}}{Vo_{max}} = \frac{P_{in} - P_{loss}}{Vo_{max}} = \frac{3600}{400} = 9\,A$$

$$Io,max = \frac{Po_{max}}{Vo_{min}} = \frac{P_{in} - P_{loss}}{Vo_{min}} = \frac{3600}{300} = 12\,A$$

After realizing our case static parameters, we compare the different MOSFETs based on their losses.

[1]A 20A mains fuse can deliver up to 4.5 kW and to be in safe margin and with considering peak current transients it is decided that the charger rating be below 4kW

These Switches[1] and their parameters can be found in Appendix A. All These MOSFETs are chosen among MOSFETs available in the market. Some of the available MOSFETs are disqualified at the very first look. After a long search on internet it can be claimed that they are among the best available MOSFETs, suitable for our case. All the data in Appendix A about the MOSFETs and IGBTs are extracted individually from their datasheets.

Current calculation in this part is based on $V_o = 400V$, which corresponds to $Io_{min} = 9A$

For MOSFET losses, we need to know their average and RMS current as well as voltage over a period. In order to have a good understanding of losses we need to equip ourselves with two tools: wave forms and formulas. In chapter 3, we discussed about the waveforms and the needed equations.

Fig.5. 1 shows the Buck Full-bridge converter topology. In Fig.5. 2 the waveforms for each diode and switch and also for the inductor is presented.

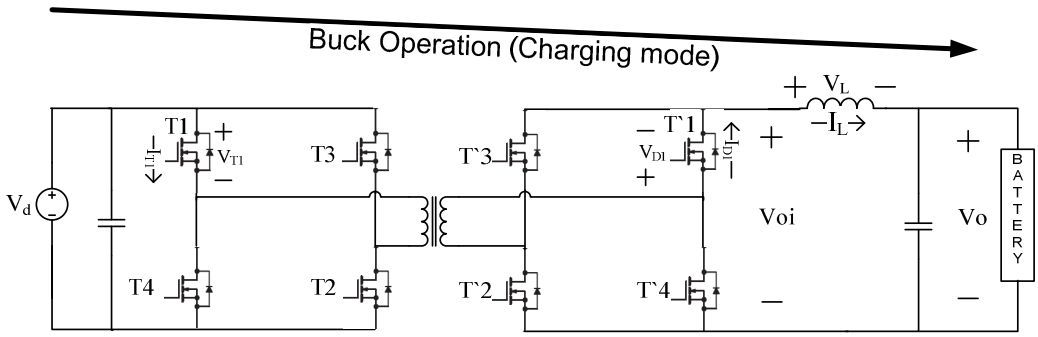


Fig5. 1 Full-bridge bidirectional converter, when it operates in buck (charging) mode

5.1.1 RMS and MEAN values of current of each Switch and Losses

5.1.1.1 Secondary side current calculation

The current waveform of each diode on secondary side (Fig.5. 2.c) during a period can be simplified to Fig.5. 3.

In previous chapters we saw that with ideal components[2] by choosing $n = 4/3 \Rightarrow D_{max} = 0.375$

Bear in mind that as we have two legs, the average current through each diode should be halved.

[1] The list of compared MOSFETs:

IRFPS43N50K	IRFPS40N60K	IRFPS40N50L	IRFPS38N60L	IRFP31N50L	IRFP460
FDH27N50	IRFPS37N50A	IRFP22N50A	IRFP32N50K	IRFP23N50L	STW26NM50
STF25NM50N	IRFP460A	SPW32N50C3	SPW52N50C3	IPW60R045CP	SPW47N60C3
IXFR48N60P					

[2] Full-Bridge Buck converter: $D = \frac{Vo}{2\,n\,Vd} = \frac{Pout}{2\,Io_{DC}\,n\,Vd}$

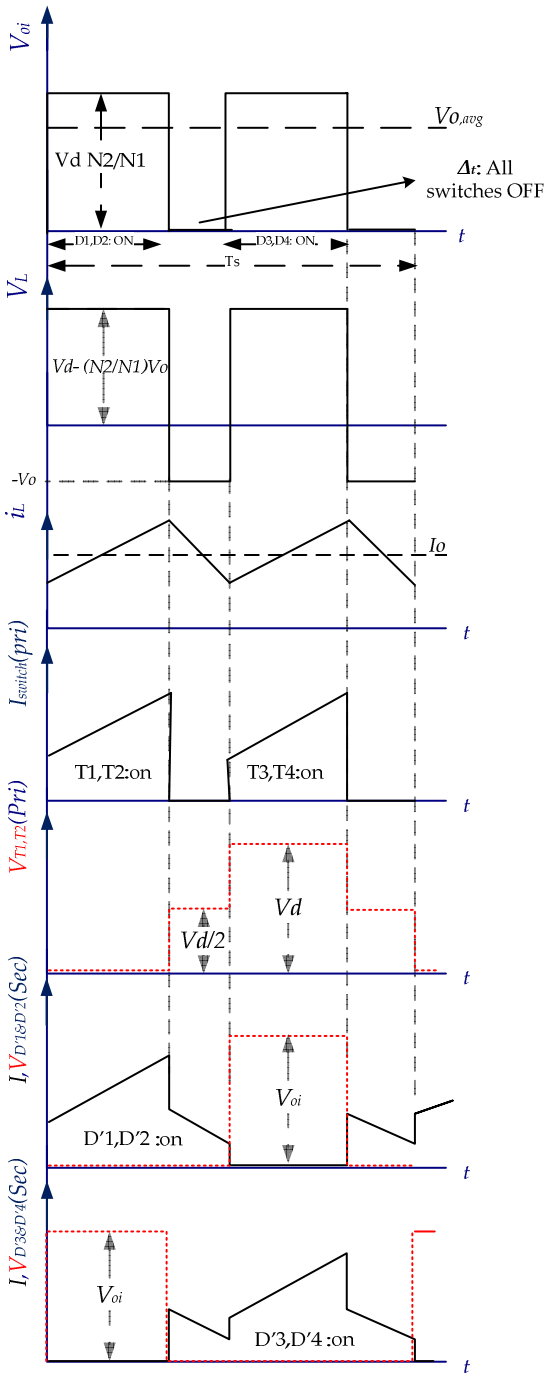


Fig.5. 2

DC-DC fullbridge buck converter waveforms. The topology can be seen in Fig.3. 2(unidirectional) and Fig.5. 1 (bidirectional). The principle of operation is explained in section 3.2.3

a)Inductor current (iL) and voltage (VL) waveforms

b)Switch current and voltage waveforms (on PRIMARY side)

c)Diode current and voltage (on SECONDARY side) waveforms

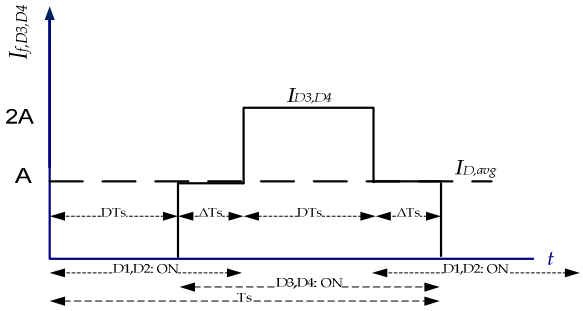


Fig.5. 3 The Simplified current profile of D3 & D4 on the Secondary side, a period can be expressed by $2\Delta + 2D = 1$

$$I_{f,D,avg} = \frac{Io_{DC}}{2} = \frac{9}{2} = 4.5A$$

As mentioned before, 10% output current ripple should be satisfied:

$\Delta Io = 0.1\ Io_{DC} = 0.1 \times 9 = 0.9A$

Based on Fig.5. 2, the instant current just before switch turn-off can be found to be

$$I_{off,D} = \frac{Io_{DC} - \frac{\Delta Io}{2}}{2} = I_{f,D,avg} - \frac{\Delta Io}{4} \quad (5.1)$$

$$\cong 4.5 - 0.22 = 4.22\ A$$

$$I_{on,D} = \frac{Io_{DC} + \frac{\Delta Io}{2}}{2} = I_{f,D,avg} + \frac{\Delta Io}{4} \quad (5.2)$$

$$\cong 4.5 + 0.22 = 4.72\ A$$

Based on Fig.5. 3, RMS forward current of each diode in secondary side, $I_{f_{rms}}$ can be calculated as follows:

$$I_{f,rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} I_{f,D}^2(t)\,dt} \Rightarrow\ {I^2}_{f,rms} = \frac{1}{T_s}(0 \times DT_s + 2A^2\Delta T_s + 4A^2 DT_s) = 2A^2(\Delta + 2D)$$

$$\leq\ 2A^2$$

$$\xrightarrow{I_{D,avg}=A} I_{f,rms} = \sqrt{2(\Delta + 2D)}\, I_{f,D,avg} = \sqrt{1 + 2D}\, I_{f,D,avg} < \sqrt{2}\, I_{f,D,avg} \quad (5.3)$$

$$I_{f,rms} < 4.5\sqrt{2} = 6.36A$$

The simulation shows that the real RMS current is around $6A$ which complies with (5.3). When $D_{max} = 0.375$, $I_{f,rms} = 4.5\sqrt{1 + 2 \times 0.375\mathrm{D}} = 5.96$

5.1.1.2 Secondary side: body diode power losses calculation[1]

As it was illustrated in Chapter3 and based on Fig.5. 1, on the secondary side MOSFETs are switched off for all the times, which means in the secondary side there is neither conduction nor switching losses regarding MOSFETs switching. In other words, only diode turn-on or turn-off and conduction losses occur in secondary side.

Turn-on Switching losses happen when the current in the diode rises to Io (and voltage falls to V_{fd}[2]) at turn off losses occur when the current goes down to zero and voltage rises up (to *Vo*).

5.1.1.2.1 Diode Conduction losses:

To have a numerical demonstration on the dimension of the diode losses lets pick SPW47N60C3 and check its anti parallel body diode chars and losses. The forward characteristics of the body diode can be seen in Fig.5. 4

Referring to chapter 4, we recall that conduction losses can be calculated by (4.5)

At high temperature of $T = 125°C$ we can write:

$$P_{cond_{sec,125}} = U_{D0}.I_{f,D,avg} + R_D\, I_{f,D,rms}^2 = 0.6 \times 4.5 + 0.025 \times 6^2 = 3.6W$$

For lower temperature ($T = 25°C$) however, conduction losses will be

$$P_{cond_{sec,25}} = U_{D0}.I_{f,D,avg} + R_D\, I_{f,D,rms}^2 = 0.8 \times 4.5 + 0.0044 \times 6 \times 6 = 3.76W$$

Where

1 Due to the lack of several parameters which are not provided in the datasheet, the reverse recovery losses calculation in this chapter is based on simplified model (chapter3) unless otherwise mentioned. However a comparison between these two models will be done at the end of this chapter

2 Diode forward voltage, that is mostly between 0.6 to 1.5V

U_{D0} Diode on-state zero-current voltage
R_D Diode on-state resistance
$I_{f,D,rms}$, $I_{f,D,avg}$: RMS and average current pathing through a diode during conduction

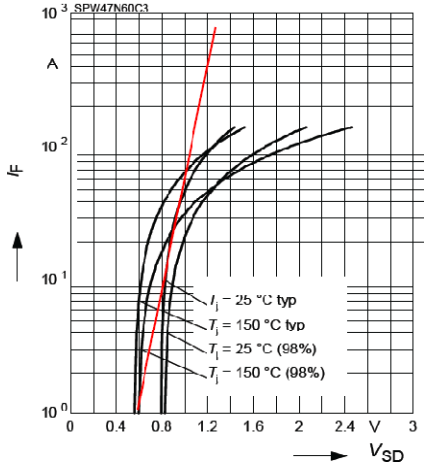


Fig.5. 4 Forward characteristics of body diode, T=150 => typical. $U_{d0} = 0.6,\ R_D = \frac{0.4}{16} = 0.025\ ohm$ .For T=25 => $U_{D0} = 0.8,\ R_D = \frac{0.04}{9} = 0.0044\ ohm$ Cortesy of Infineon (www.infinion.com)

This means that although the on-state resistance and constant voltage depend on temperature significantly, but the conduction losses don't vary so much with the temperature variation and this trend can be observed more or less in most diodes.

5.1.1.2.2 Diode switching losses

Turn-off energy losses (caused by switching of an opposite pair of switches in the primary side) in the anti parallel diode E_{offD} consists of the reverse recovery energy. From (4.9) diode turn-off losses can be found:

$$P_{offD,sec} = 0.5\ Q_{rr} U_{Drr} f_s = 0.5 \times 23 \times 10^{-6} \times 400 \times \frac{4}{3} \times 20000 = 122.6W$$

U_{Drr}:Diode blocking voltage which in sec side is equal to $V_{oi} = V_d$ N2/N1

But this value is just too high and maybe several times higher than real case. The reason is that Q_{rr} in datasheets is measured in certain condition and operating point. I.e for this MOSFET, Q_{rr} is $23uC$ for the diode continuous forward current, $I_{f_{ref}} = 47A$. Later on (in Fig.5.18) it will be seen that Q_{rr} in P-n diodes is highly dependent on I_f. Obviously it is not possible to find a general equation that describes this dependency for all the diodes, but it can be said that as our current is much lower than $I_{f_{ref}}$(around 10 times smaller) the actual turn-off energy losses will be smaller than what is calculated based on $I_{f_{ref}}$.This can be seen in Fig.5. 20.

It is such a pity that none of the MOSFETs manufacturers provide the accurate data regarding the body diode reverse recovery of their MOSFETs products and this lack of data makes the reverse recovery energy losses evaluation unreliable.

Diode turn-on energy losses generally are small and in most power electronics applications in industry are neglected [16]. In [22] the diode turn-on energy losses are discussed in more details and is explained that most of the turn-on energy in diode is stored in its package inductance and is delivered to the load during the diode turn-off and is not decapitated at all.

Thus the total power losses in the diode can be expressed as

$$P_D = P_{offD,sec} + P_{cond_{sec}} = 122.6 + 3.6 = 126.2\ W$$

5.1.1.3 Primary side current calculation

DC input current at highest input power can be simply expressed as

$$\frac{I_d}{Io_{dc}} = \frac{N2}{N1} => I_d = \frac{N2}{N1} Io_{DC} = \frac{4}{3} \times 9 = 12A$$

I_d is the transformer input current and Io_{DC} is the secondary transformer current that flows towards the transformer whenever each pair of primary switches conduct. Secondary side ripple current will be $\Delta Id \cong 1.2A$

Input current at the moment that a switch turns off is at its peak ($I_{d,off}$) and vice versa (as it can be seen from Fig.5. 2) the maximum and minimum input current can be expressed as (5.4) and (5.5) respectively:

$$I_{d,off} = Id_{max} = Id_{DC} + \left(\frac{\Delta Io}{2}\right) \quad (5.4)$$

$$= 12 + 0.6 = 12.6A$$

$$I_{d,on} = Id_{min} = Id_{DC} - \left(\frac{\Delta Io}{2}\right) \quad (5.5)$$

$$= 12 - 0.6 = 11.4A$$

Maximum RMS and average current of *EACH* switch in primary side, during a period can be calculated by (5.6) and (5.7) respectively:

$$Id_{rms} = I_d\sqrt{D_{max}} \quad (5.6)$$

$$= 12\sqrt{0.375} = 7.35A$$

$$Id_{DC} = D_{max}.I_d \quad (5.7)$$

$$= 0.375 \times 12 = 4.5\ A$$

5.1.1.4 Input-output Power balance in Duty Cycle Control method

The switching pattern used in this thesis is called "Duty Cycle Control". The reason is that the current to the output is controlled by duty cycle.

To verify that the current calculation is correct, we have to check if the input power, Pin is equal to output power $Pout$

For max Duty cycle (Corresponds to max Battery voltage, 400 V):

$$Pin_{(Dmax)} = I_d(2\ D_{max})Vd = 12 \times 2 \times 0.375 \times 400 = 3600\ W$$

$$Pout_{(Dmax)} = Io_{DC}.Vout = 9 \times 400 = 3600\ W$$

And for minimum Duty cycle (= minimum Battery voltage, 300 V):

$$Pin_{(Dmin)} = I_d(2\ D_{min})Vd = 16 \times 2 \times 0.2813 \times 300 = 3600\ W$$

$$Pout_{(Dmin)} = Io_{DC}.Vout = 12 \times 300 = 3600\ W$$

5.1.1.5 Total switch losses in primary side [1]

As it was shown in chapter 4, MOSFET losses in primary side can be expressed by:

MOSFET Conduction losses in primary side

The MOSFET we study in this part is *SPW47N60C3* ($R_{DS,on} = 0.05\ ohm$). Conduction losses can be calculated by (4.2)

$$P_{cond,M} = R_{DS,on}I^2_{d,rms} = 0.05 \times 7.35^2 = 2.75\ W$$

MOSFET switching losses in primary side

[1] In order to understand the equations in this part, it is recommended to skim chapter4

In Chapter 4, We found some suitable equations that can help us to calculate switching losses by each MOSFET datasheet. First we need to find voltage fall and rise time.

$U_{DD}, R_{DS,on}, C_{GD1}, C_{GD2}, U_{Dr}, t_{ri}$ And Q_{rr} all can be extracted from a MOSFET datasheet. (See Appendix A). Referring to Fig.5. 2.b we can see that before the turn-off transient, MOSFET voltage is $Vd/2$.

But what about I_{Gon}?

$I_{Gon} = V_{gs}/R_g = V_{dr}/\sum R_G$ is the current needed on a MOSFET gate that will turn it on. As (4.11) suggests, increasing I_{Gon} reduces the voltage fall time and this ultimately reduces the Switching losses. So we desire to have a relatively high gate current. But this current depends on the MOSFET driver circuits.

There are lots of available driver/buffers in the market. Here we introduce two of them, both from MICROCHIP Company. Both of them can deliver Supply Voltage (V_{GS}) up to 20V:

TC1411/TC1411N: The TC1411/TC1411N is 1A CMOS buffers/drivers.

MCP1415/16: The MCP1415/16 is high speed MOSFET driver capable of providing 1.5A of peak current.

So having $I_{Gon} = 1.2A$ is feasible; by tuning V_{dr} (up to 20V for some drivers) and total gate resistance, $\sum R_G$ (by adding series resistance to MOSFET gate resistance, R_g) we can produce $I_{Gon} = 1.2A$. From Fig.4. 7 C_{GD} is found to be 530 pF. For simplicity we assume $t_{fu} = t_{ru}$

By plugging our case values into (4.11), (5.8) is obtained:

$$t_{fu} = t_{ru} = \left(\frac{U_{DD}}{2} - R_{DS,on}\, I_{d,on}\right)\frac{C_{GD}}{I_{Gon}} \tag{5.8}$$

$$= \left(\frac{400}{2} - 0.05 \times 11.4\right)\frac{530 \times 10^{-12}}{1.2} \approx 87\ ns$$

The datasheet provides $t_{ri,ref} = 27\ ns$ based on its defined conditions. From (4.24) the new current rise time $t_{ri,new}$ is calculated based on our case values:

$$t_{ri,new} = \frac{V_{new} I_{d,on}}{V_{ref} I_{ref}}\ t_{ri,ref} = \frac{400/2 \times 11.4}{380 \times 47}\ 27 = 3.44ns$$

Total turn-on time consists of voltage fall time and current rise time:

$$t_{new,on} = t_{fu} + t_{ri,new} = 87 + 3.44 = 90.4\ ns$$

As discussed in chapter 4 and based on Fig.4. 6, RR charge influences significantly MOSFET turn-on switching losses. In full-bridge topology the maximum current through each switch will be $I_L + 2\frac{n2}{n1} I_{rrm}$ (doubled I_{rrm} is compensated with halved voltage of each switch in RR losses calculation) this will be explained in section 5.2.1. By the help of (4.10), (4.12), MOSFET turn-on losses for our topology can be expressed as (5.9)

$$E_{onM} = \frac{Vd}{2} I_{d,on} \frac{t_{new,on}}{2} + (2Qrr)\frac{Vd}{2} + \frac{Vd}{2} I_{d,on} trr \tag{5.9}$$

$$E_{onM} = \frac{400}{2} \times 11.4 \times \frac{90.4 \times 10^{-9}}{2} + 2 \times 23 \times 10^{-6} \times 200 + \frac{400}{2} \times 11.4 \times 580 \times 10^{-9}$$

$$= 0.0106\ [j]$$

On-state Power losses then can be calculated:

$$P_{onM} = E_{onM} f_{sw} = 0.0106 \times 20000 = 213\ W$$

Turn-off losses in power MOSFETs E_{offM} can be calculated with the same steps:

$$t_{fi,new} = \frac{V_{new} I_{d,off}}{V_{ref} I_{ref}}\ t_{fi,ref} = \frac{400/2 \times 12.6}{380 \times 47}\ 8 = 1.13\ ns$$

$$t_{new,off} = t_{ru} + t_{fi,new} = 87 + 1.13 = 88.13\ ns$$

$$P_{offM} = \frac{U_{DD}}{2} I_{d,off} \frac{t_{new,off}}{2} f_{sw} = 2.1\ W$$

As it can be seen, turn on losses are 100 times higher than turn off losses! Total MOSFET switching power losses then will be the sum of these 2 sources of energy losses:

$$P_{tot,sw} = P_{offM} + P_{onM} = 2.1 + 213 = 215\ W$$

And the total MOSFET losses, P_M is:

$$P_M = P_{tot,sw} + P_{cond,M} = 215 + 2.75 = 217.85\ W$$

Then total switch losses of the whole DC/DC stage will be:

$$P_{tot} = 4(P_M + P_D) = 4(217.85 + 126.2) = 1376\ W$$

This is of course much higher than our expectation and MOSFET thermal limitations will cause failure, suggesting that this cannot be a good MOSFET for this application. It should be noted that these calculations are overestimations and the real losses will be less than these Values. In the next part, we will compare different switches and will find the most suitable

5.1.2 A short presentation on IGBT losses calculation

5.1.2.1 Conduction losses:

In practice an IGBT can be modelled similar to a diode: a constant voltage source in series with a (variable) resistance. This is a linear model of output characteristics of an IGBT as can be seen in Fig5. 5 Based on the equivalent IGBT model the following relations can be found:

$$V_{IGBT}(i_c) = V_{CE,0} + R_{IGBT,on} i_C \quad (5.10)$$

$$P_{on} = V_{CE,0} I_{C,av} + R_{IGBT,on} . I_{C,rms}^2 \quad (5.11)$$

Where

$I_{c,av}$, $I_{c,rms}$: Average and RMS collector current during a period respectively
$V_{CE,0}$: IGBT on-state zero-current voltage (Temperature dependent voltage source) and
$R_{IGBT,on}$: IGBT on-state resistance.

Based on Fig.5. 5 conduction losses at $T_j = 125℃$ in primary side would be:

$$P_{on} = V_{CE,0} Id_{DC} + R_{IGBT,on} . Id_{rms}^2 = 0.75 \times 4.5 + 0.375 \times 7.35^2 = 23.6W$$

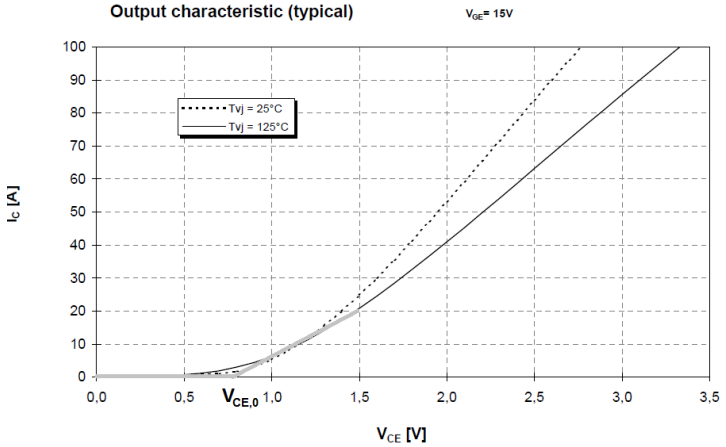


Fig.5. 5 Infineon BSM50GB60DLCL Gray line: linearized output characteristic, here $V_{CE,0}$=0.75 V, $R_{IGBT,ON}$=0.75/20=0.375 ohm (for Tvj=125) (www.infineon.com)

5.1.2.2 Switching losses

In previous part we saw that huge reverse recovery energy losses on secondary side is problematic.

In contrary with MOSFETs, IGBT datasheets provide adequate graphs that simply describe switching losses dependency on R_G, V_{CE} ,temperature and Collector current (Fig). IGBTs chosen in this study have $V_{CE_{ref}} = 400V$ which is the same as our case so we don't need to study the switching Energy losses as a function of V_{CE}.

Although reducing R_G (which means increasing of I_G) from its recommended value will reduces the switching losses, but sharp voltage and current transient may causes some oscillations and higher diode turn-off losses. It can be said that R_G in each datasheet is the optimized value thus we don't investigate on IGBT driving circuit.

Fig.5. 6 is taken from *BSM50GB60DLCL* datasheet. From there we see that for currents up to 20A, total switching losses will be:

$$E_{sw} = E_{on} + E_{off} + E_{rec} = 0.1 + 0.4 + 0.8 = 1.3 \times 10^{-3}[j]$$

$$P_{sw} = E_{sw} f_{sw} = 1.3 \times 10^{-3} \times 20 \times 10^{3} = 26W$$

So total losses in this IGBT is:

$$P_{tot,IGBT} = P_{sw} + P_{cond} = 26 + 23.6 = 49.6\ W$$

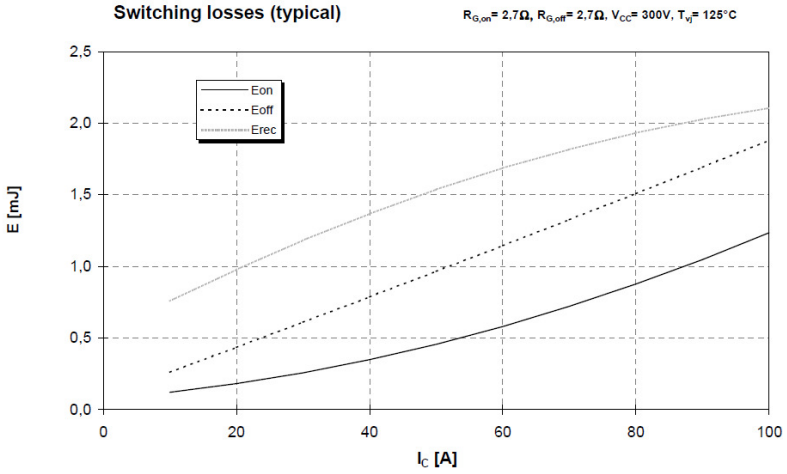


Fig.5. 6 Infineon *BSM50GB60DLC* switching losses as a function of collector current. E_{rec}: Recovery losses (www.infineon.com)

5.1.2.3 Switching losses and temperature dependency on IGBTs

In reality, switching losses depend on several parameters. The most important parameters that affect the switching losses are temperature and collector current. The 3D plot in Fig.5. 7 can show this fact.

The most important conclusion which is valid at least among investigated IGBTs (The list of IGBTs can be found in Appendix A) is that at low I_C, the energy losses dependency on Junction temperature is so low and for simplicity we can claim that at low currents switching losses is not dependent upon variations in junction temperature. However this claim is not true for high collector current. On the other hand, the energy losses are highly dependent on collector current variation especially at higher temperatures and can be neglected.

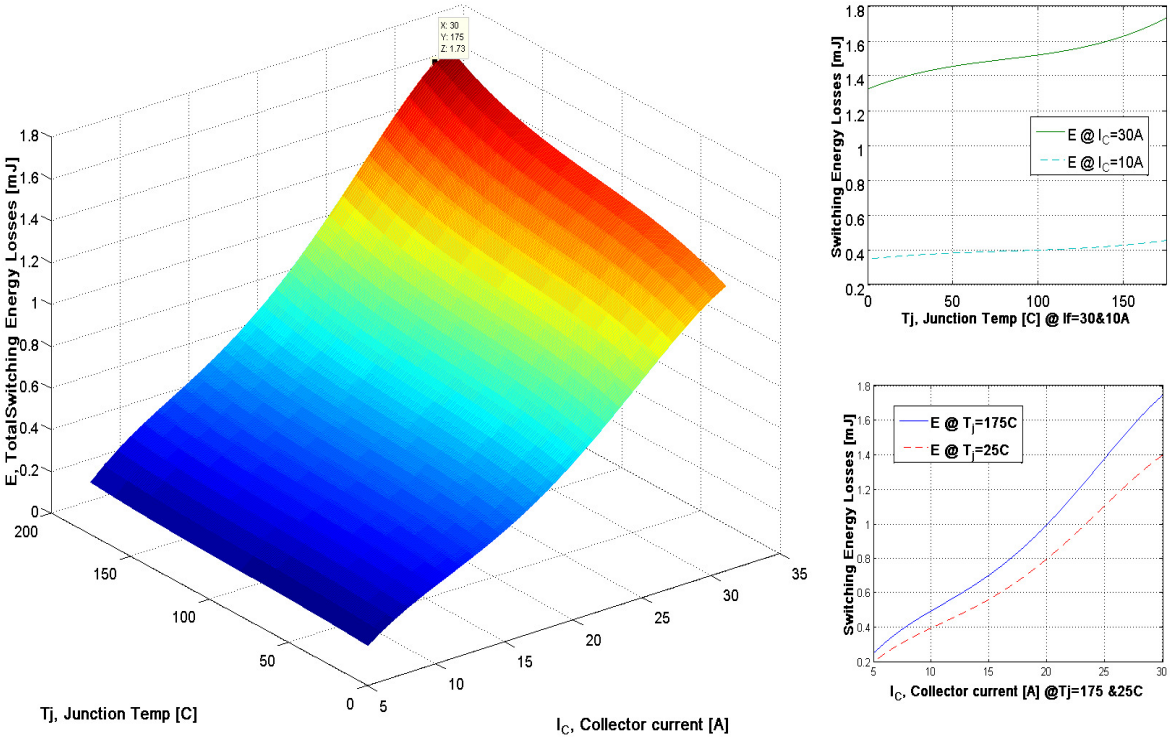


Fig.5. 7 Total switching energy losses as a function of collector current and temperature for the "IKW30N60H3" IGBT at $R_G = 10.5$

5.2 Transient current flow and other losses

Unfortunately it is difficult to fully understand the switching transients of complex topologies and there are few simulation softwares that can provide us with correct reverse recovery process simulations. In this part turn-off and turn-on transients will be discussed in more details.

5.2.1 Reverse recovery current propagation

During the turn-off of a secondary side body diode, its reverse recovery current can pass through on-state MOSFETS, *T3*, *T4* in primary side as it can be seen in Fig. 5. 8.

As $T1(D1)$ and $T2(D2)$ are reversely biased ($Vd/2$ over them), Current cannot pass through $D1$ or $D2$. So it will choose to pass through $T4$ and $T3$. As mentioned before it is the MOSFET who dictates $dif\ /dt$ of the body diode current turn-off. It is because of *T3* and *T4* turn-on event that $D'1$ and $D'2$ in secondary side are forced to turn off.

The difference between a full-bridge converter topology and a Buck converter studied in chapter 4 is that the maximum current through switch ($T4$) will be $I_L + 2I_{rrm}$ instead of $I_L + I_{rrm}$. This can be realized by referring to Fig.5. 8 (blue line indicates I_{rr}). This excessive current leads to higher switching losses as it was observed in previous parts.

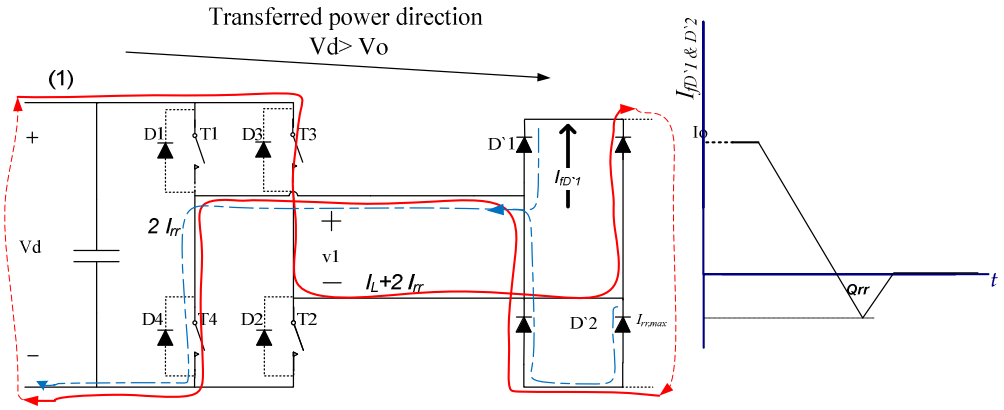


Fig.5. 8 The direction of reverse recovery current in primary side (blue dashed line) As the inductor current cannot change suddenly, the reverse recovery current dose not pass through the inductor in secondary side (see section 7.4.1)

5.2.2 Effect of leakage inductance on waveforms

After a pair of primary side switches in Fig.5. 9 are turned off, let's say T1 and T2, ideally no current has to pass through the transformer. But leakage inductance makes this assumption invalid. The leakage inductance causes current to flow for a while before it reaches zero. This can be seen in Fig.5. 9. While all the switches in the primary side are turned off, D4 and D3 should supply this leakage current. As $V_{sec} = 0$, $-Vd$ is applied over the leakage inductance, resulting a very steep current fall. It also means that primary body diodes experience turn-off losses. (reverse recovery losses) Simulation observations verify this process. (Chapter 8)

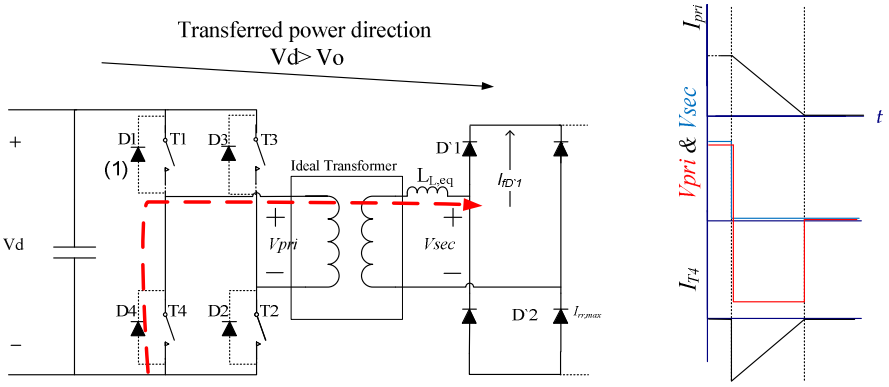


Fig.5. 9 Transformer leakage inductance forces the diodes of primary side to turn-on

5.2.3 Gate losses

There is another source of losses associated with MOSFET driving circuit: gate losses [23]. (5.12) describes this type of losses:

$$P_G = Q_G \frac{U_{Dr}}{R_{Dr}} f_{sw} \tag{5.12}$$

Where

Q_G Total gate charge[1]
R_{Dr} External gate drive resistance
U_{Dr} Gate drive voltage

[1] range: 70~250 nC depending on MOSFET model

By reducing R_{Dr}, P_G increases, but at the same time the MOSFET switching losses decrease. We neglect Gate losses as Q_G is so minute.

5.3 MOSFETs or IGBTs; Comparison and Conclusion

A comparison between Turn-on and Turn-off energy losses in MOSFETs shows that the contribution of term $Q_{rr}U_{DD}$ in switch losses in MOSFET is so high. i.e. for MOSFET *SPW47N60C3* more than 80% of switching losses is because of the reverse recovery charge, Q_{rr} and body diodes with lower Q_{rr} are more suitable for applications that the anti parallel body diode is involved in losses. The calculations illustrated in Fig.5. 10 and 5. 11 support this claim. This is also in accordance with [24].

In the power and voltage range of some kilo watts and some hundred Volts and in applications that the anti-parallel diode conducts (like full bridge case) the reverse recovery charge of MOSFET becomes problematic. On the other hand IGBTs, in general have slightly higher conduction losses due to their constant voltage source as it can be seen in Fig.5. 10.

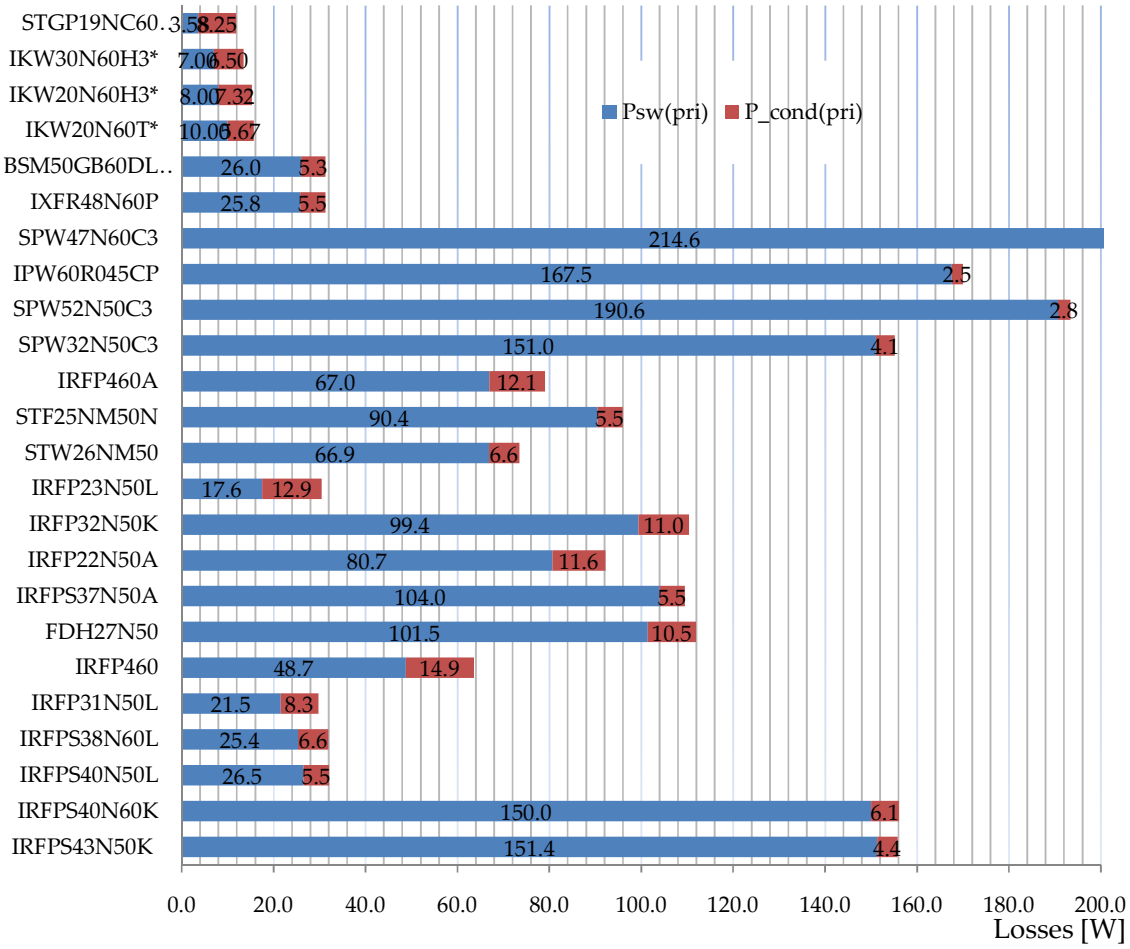


Fig.5. 10 Primary side, switching losses (Switch turn-on and off) and Conduction losses for a single switch (* represents IGBTs) (Pout=3600W). Switching losses based on $I_{Gon} = 1.2A$ for all switches(simplified model)

Another interesting issue is that MOSFETs should not be judged by their glamorous trademarks. An obvious example is COOLMOS Power Transistors (such as SPW47N60C3 or

SPW35N60C3) Some models of these transistors despite the claim of having very low conduction and switching losses exhibit huge switching losses. This proves that they should be used in the switching frequencies much lower than 20kHz. In applications where no reverse current occurs, just based on MOSFET conduction and switching losses, COOLMOSs are better than other MOSFETs as it can be seen in Fig.5. 10.

Yet it is possible to find MOSFETs with good body diodes. Referring Appendix A, It can be seen that Q_{rr} varies dramatically in different MOSFET models i.e. in *IRFP23N50L*: $Q_{rr} = 9.8 \times 10^{-7}\mathrm{C}$ and in *SPW52N50C3*: $Q_{rr} = 2.0 \times 10^{-5}\mathrm{C}$. Q_{rr} In latter model is more than 20 times bigger than the former. Fig.5. 11 shows that some IRF MOSFETS (IRF31N, IRFP32N, IRFPS40 and IRFPS38 from International Rectifier with their "Super Fast Body Diode" can effectively reduce RR losses.

Fig 5. 12 shows the total switch losses of a single switch in primary and the same switch on secondary side of the DC-DC converter. (* in their name represents that the switches are IGBT). This Figure is the sum of Fig.5. 10 and 5. 11

The total switch losses of the DC-DC converter for the best MOSFETs and IGBTs with the lowest losses can be seen in Fig.5. 13. We can claim that *IRFP31N50L* is the MOSFET with the lowest losses and *STGP19NC60W* has the lowest losses among IGBTs. The total efficiency (and losses) of the DC-DC converter will be assessed and compared based on these two switches.

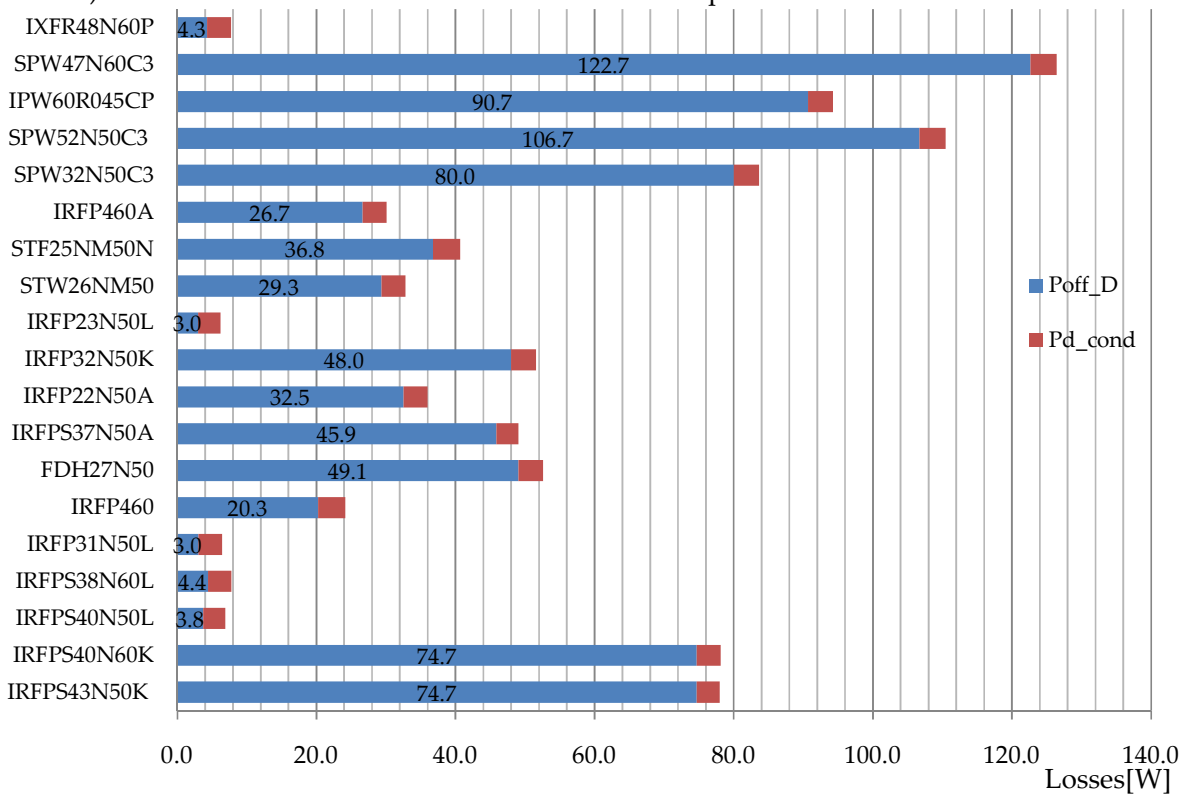


Fig.5. 11 conduction losses and turn-off losses of diode in secondary side, the sum will be total secondary losses. (Pout=3600W) Switching losses based on $I_{Gon} = 1.2A$ for all switches (simplified model)

From Fig 5.13 it can be said that even the MOSFET with the lowest losses has larger switch losses than most investigated IGBTs.

It should be reminded that the output power (voltage and current) for all of these topologies assumed to be constant (3600W) and the input power is the sum of output power and total losses. On the other words, switch losses are based on constant current and voltage for each switch.

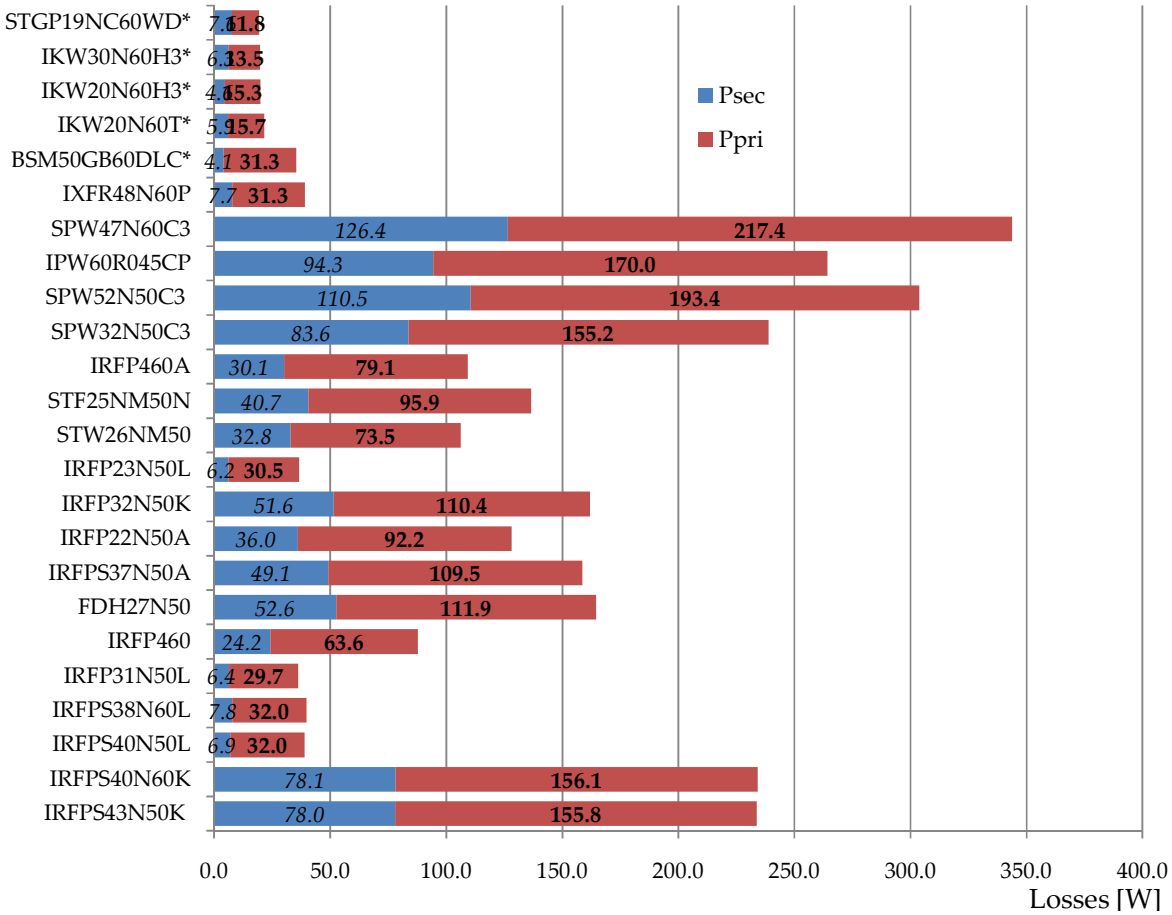


Fig.5. 12 The total switch losses of a single switch in primary and the same switch on secondary side (*represents IGBT) (Pout=3600W(Switching losses based on I_{Gon} = 1.2A for all switches (simplified model)

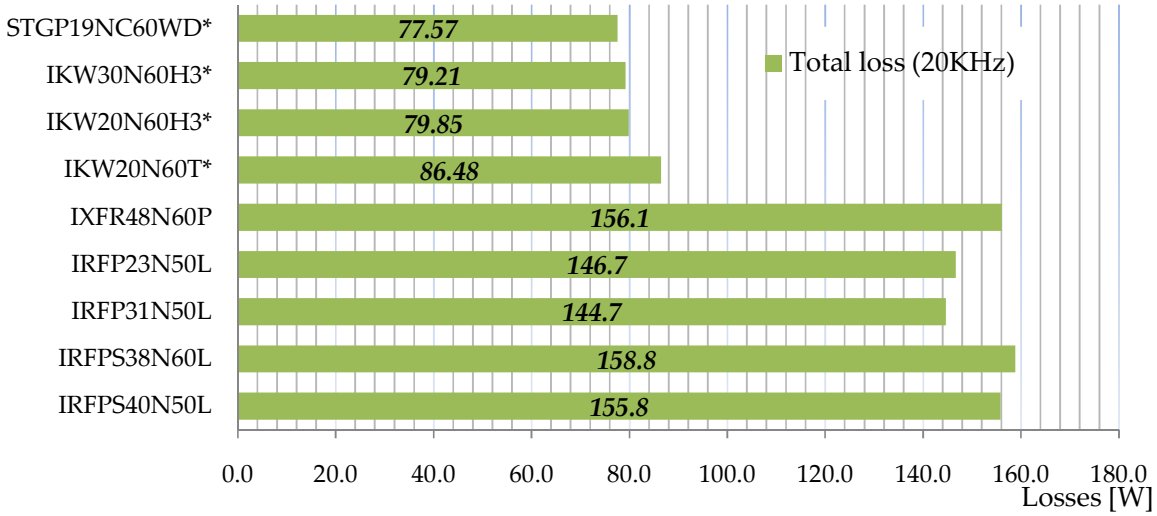


Fig.5. 13 Total switch losses of DC-DC full bridge converter (* represents IGBTs) (Pout=3600W) Switching losses based on I_{Gon} = 1.2A for all MOSFETs

5.4 Bidirectional vs. Unidirectional: losses comparison

By studying the previous part and observing the huge losses caused by body diode, other solutions for bidirectional functionality may cross readers mind:

1) Instead of one bidirectional circuit, we can have 2 unidirectional (one quadrant) converters that the rectification is done with the diodes, (two separate circuits: one for buck operation and one for boost operation) with a common transformer and inductor. Obviously, this solution is too expensive.

2) Using an external diode ($D1$) instead of switch body diode, anti parallel with each switch as demonstrated in Fig 5. 14. Please note that we need a small diode in series with each switch (in each side) to prevent the reverse current flow through the switch body diode. Generally switch body diodes have very small Vo and in absence of *D2*, reverse current prefers to pass through body diode. *D2* can be a small Schottky diode[1] (which needs to have a blocking voltage of few volts) which is protected by a Zener diode in parallel with it. This topology has one drawback: during switch turn-on, in addition to *M1*, *D2* exhibits conduction losses too.

3) Utilizing synchronous rectification on Secondary side switches (will be explained in the next part

In this part we try to analyze the external diode power losses in secondary side instead of MOSFET body diode.

We study two types of diodes and compare their losses with MOSFET body diode.

a) SiC power Schottky diode

b) P-n junction Power diode (with Silicon ultra fast soft recovery)

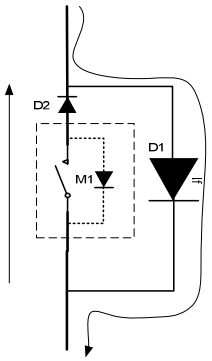


Fig.5. 14 A circuit to prevent current passes through body diode

5.4.1 Schottky diodes

Advantages:

+ No reverse recovery: No reverse recovery time, t_{rr} due to the absence of the minority carrier injection, which means the switching losses are negligible.

+ The wide band-gap of SiC allows higher operating temperatures.

+ No significant voltage overshoots during device turn-on.

Disadvantage:

- This type of diode is not ideal for high-voltage applications, where the leakage current and the forward-voltage drop can be much higher (may have higher conduction losses)

The proposed Silicon Carbide Schottky diodes can be seen in table.5. 2

Table.5. 2 Two Silicon Carbide Schottky diodes

MODEL	IDT16S60C (Infineon)	STPSC1206
$\mathbf{I_{f_{max}}}$(avg)	16A	12A
$\mathbf{V_f}$ (T=25)	600 V	600V

[1] I.e. *STPS15L25D/G*

5.4.1.1 CONDUCTION LOSSES

Fig.5.15 a) represents a typical diode forward characteristic. As discussed before, for secondary side, the conduction losses for diodes can be calculated by

$$P_{cond_{sec}} = U_{D0} \cdot I_{f,D,avg} + R_D I^2_{f,D,rms}$$

For *IDT16S60C* (Infineon) conduction losses would be:

$$P_{cond_{sec}} = 0.9 \times 4.5 + 0.025 \times 6 \times 6 = 4.95\,W$$

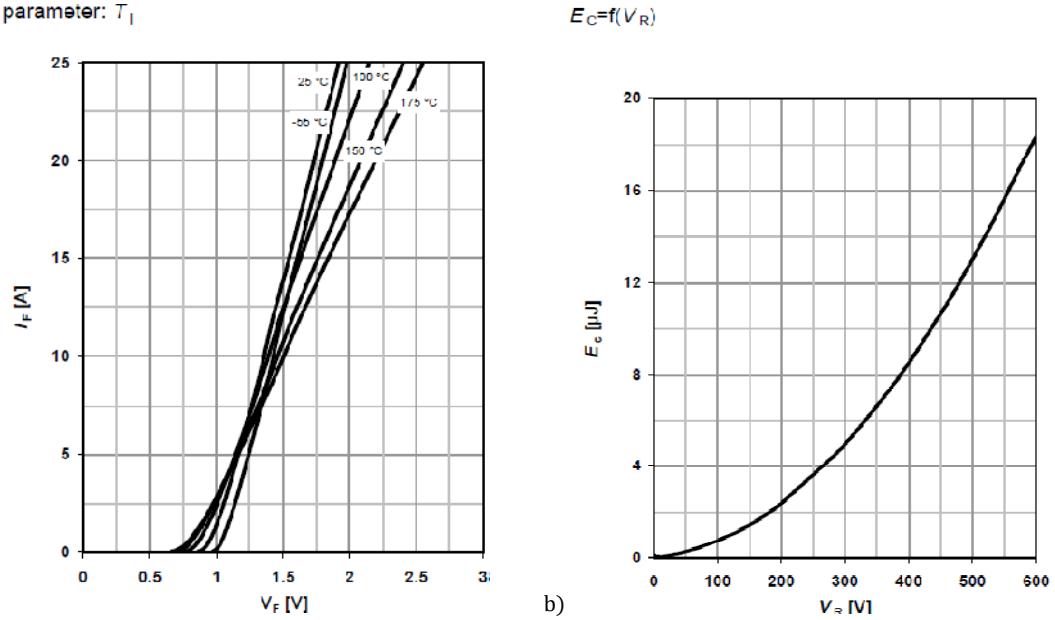
Similarly, the conduction[1] losses for *STPSC1206* is 8.1W

For our Small Schottky diode in primary side and in series with the switch (see Fig.5. 14) the losses will be:

$$P_{cond_{pri}} = 0.275 \times 4.5 + 0.01 \times 7.35 \times 7.35 = 1.8\,W$$

5.4.1.2 Switching losses in Schottky diodes

The switching losses in Schottky diodes are due to the energy loss caused by the junction capacitance charge at given operating voltage over one switching cycle and multiplying by the switching frequency. But in most references it is neglected [24], [25]. Referring Fig.5. 15 b) this can be proven: Based on Fig.5. 15 b) the diode switching losses at $f = 20KHz$ is only 0.18W, which is much smaller that the conduction losses.



a) b)

Fig.5. 15 a) $U_{D0} = 0.9V, R_D = 0.04$ ohm (T=25°C) b) switching losses in Schottky is only because of junction charge (capacitor). For $(V_R, E_c) = (400V, 8\mu J) \rightarrow Psw = 0.16W$ (*STPSC1206*, Infineon)

5.4.2 P-n junction power diode (with Silicon ultra fast soft recovery)

Normally Power diodes are oversized due to the excessive reverse recovery energy loss.

Models and their specifications that are studied in this part can be seen in Table.5. 3.

Table.5. 3 P-n power diodes which are studied in this section

Model (company)	$\mathbf{V}, \mathbf{I_{f,avg}(25°C)}$	$\mathbf{R_D = dV_f/dI_d}$	$\mathbf{V_{D0}}$
IDB30E60 (Infineon)	600V, 30A	0.35/10=0.035	0.8

[1] The datasheet of STPSC1206 suggests to use the following equation for conduction losses evaluation: $P_{cond} = 1.2\, I_{f,avg} + 0.075 I^2_{f,rms}$

STTH12R06 (ST)	600V, 12A (@ all temperatures)	$P_{cond} = 1.16\ I_{f,avg} + 0.053\ I^2_{f,rms}$	
IDB23E60 (Infineon)	600V, 41A	0.2/10=0.02	1
IDB09E60 (Infineon)	9	0.5/10.5=0.048	1

5.4.2.1 P-n diode switching losses and its dependency on di_F/dt[1]

In previous parts we discussed about MOSFETs and IGBTs body diodes and their turn-off losses. On MOSFETs, due to the lack of information about the body diode behaviour especially at turn-off, we had no choice but to use simplified equations to estimate the body diode turn-off energy losses. Despite MOSFETs and IGBTs datasheets, most diodes datasheets provide adequate information about the diode switching time, Q_{rr}, I_{rr} and even Softness factor, S all as a function of turn-off current slope, di_F/dt. This also can be seen in Fig.5. 16

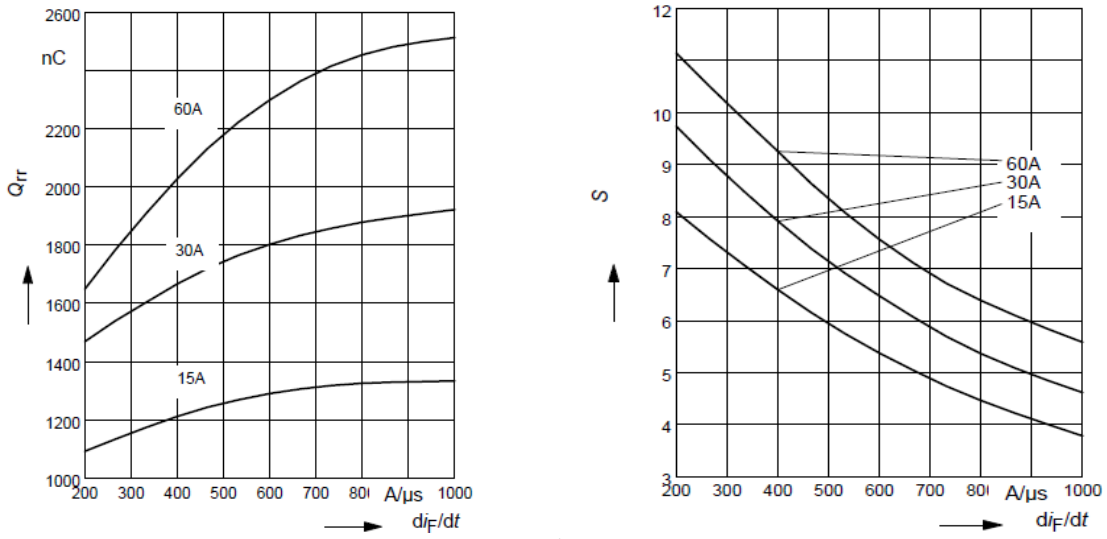


Fig.5. 16 Qrr and S as a function of dif/dt for *IDB30E60.* Courtesy of infinieon (www.infineon.com) Adition to S and Qrr, Irr and trr are also affected by dif/dt. By increasing dif/dt, Irr increaes while trr decreases. This can be observed for all p-n diodes.

5.4.2.2 Determining turn-off current slope, di_F/dt

di_F/dt can affect the total losses and even the current and voltage noise of the whole converter. As it was discussed in chapter 4, the turn-off energy losses can be calculated by (5.13):

$$E_{off,D} = \frac{V_d Q_{rr} t_{rr2}}{t_{rr}} = V_d Q_{rr} \frac{S}{S+1} \tag{5.13}$$

Please note that this equation is not accurate in high di_F/dt as the current and voltage cannot be assumed linear anymore and both diode current and voltage experience oscillations at high di_F/dt. This can be observed in [22]

From Fig.5. 16 it can be simply understood that by increasing the di_F/dt, Q_{rr} increases and at the same time S decreases; the two opposite elements in (5.13). By having these two graphs, we have to be able to calculate the energy losses as a function of di_F/dt .

Although not easy to predict, it can be claimed that at lower i_F/dt , diode turn-off energy losses are minimized. Fig.5. 17 can validate such a claim. Lower di_F/dt also prevents what it is

[1] di_f/dt also known as Current Slew Rate, Rate of Diode Forward Current Change Through Zero Crossing

called "snappy recovery" that leads to voltage and current oscillation after diode turn-off which increases the generated EMI [22].

But it is only half of the story: The diode turn-off current and current slope in most transient time regions during a switch turn-on time interval (in Primary side) is dictated by the switch current on the primary side. In other words, it is the switch current that dictates the slope of the diode turn-off current (di_F/dt) [15].

$$\frac{di_{sw}(on)}{dt} = -\frac{di_f(off)}{dt} \tag{5.14}$$

We will later see that for the fullbridge topology (with duty cycle control) (5.14) looks like this:

$$\frac{di_{sw}(on)}{dt} = -2\frac{n2}{n1}\frac{di_f(off)}{dt} \tag{5.15}$$

So lower value of di_F/dt means it takes more time for opposite pair of switches in primary to turn-on and this, in turn increases the MOSFET/IGBT switching time and so turn-on energy losses [26].

What is behind the formation of $di_{sw}\ (on))/dt$ is the drain lead inductance of a switch in series with the switch (which is around a few tens of nH) [27] . In [28] it is mentioned that although it may be possible to reduce $di_{sw\ (on)}/dt$ by introducing an external inductance in series with a switch, in full and half bridge power modules it may not be feasible.

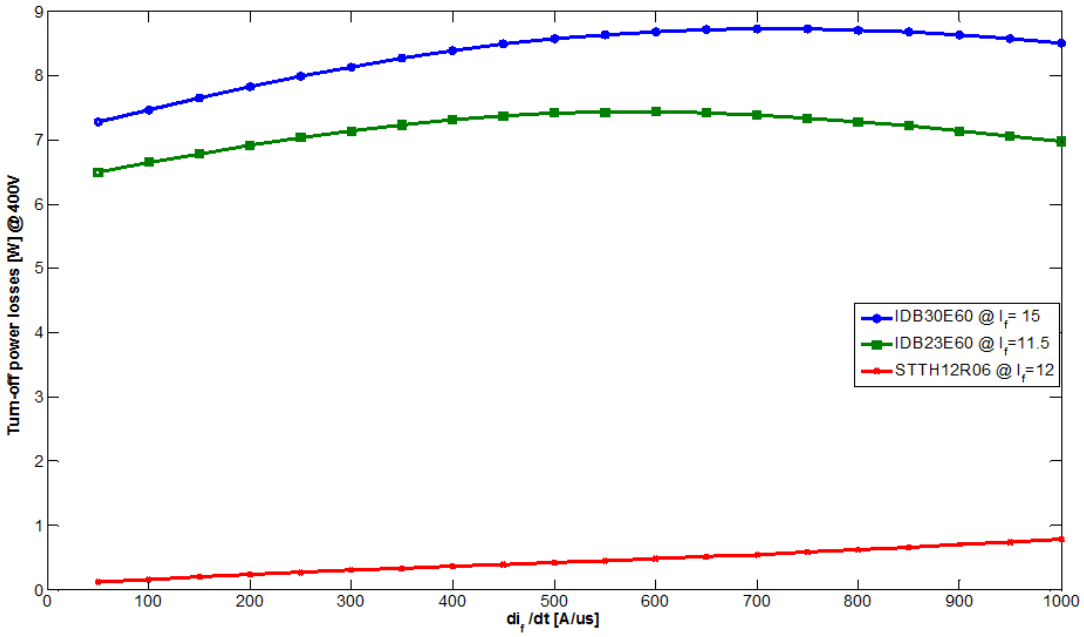


Fig.5. 17 turn-off power losses of 3 different diodes as a function of di_f/dt

Finding the best value of di_F/dt requires a precise modelling of switches and whole topology in a certain operating point which is beyond the scope of this thesis. What we use for diode current derivative comes from some papers which suggest that the optimum commutation point should be between 200 to 300 A/us ([22], [29])

The rest of this part and future analysis is based on $di_F/dt = 200$ A/us

In Fig.5 .18 Q_{rr} for 5 different diodes (listed in table.5. 3) as a function of diode forward current, I_f (at $di_F/dt = 200$ A/us) from their datasheet is extracted. This shows that by increasing I_f, Q_{rr} will significantly increase. This is also true for Softness factor, S as it can be seen in Fig.5. 19.

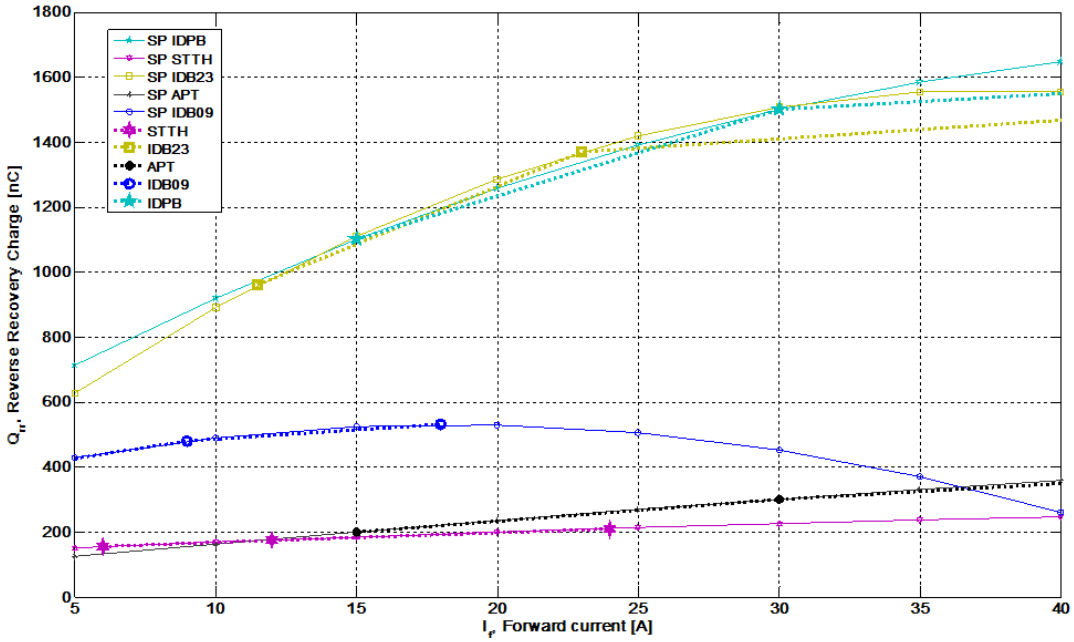


Fig.5. 18 Reverse recovery charge as a function of diode forward current at $di_F/dt = 200$ A/us (SP: extrapolated lines for $I_f = 5{\sim}10A$)

Fig.5. 20 obviously suggests the diode that has the lowest turn-off losses and that is *STTH12R06*. A very interesting feature of this diode is that its switch losses are not so much dependent on di_f/dt as it can be seen in Fig.5. 17. For this diode turn off losses (at $I_f \cong 5A$) will be:

$$E_{off,D} = V_d Q_{rr} \frac{S}{S+1} = 400 \times 175 \times 10^{-9} \times \frac{0.2}{0.2+1} = 1.17 \times 10^{-2}\ [mj]$$
$$P_{off,D} = f_{sw} E_{off,D} = 0.2333\ W$$

Table.5. 4 shows the conduction and switching losses of the investigated diodes. It can be seen that STTH12R06 (ST) has a slightly lower total losses.

Table.5. 4 Switching losses (turn-off) and conduction losses of 4 investigated diodes (Vd=400V)

Model (company)	Conduction losses [w]	Switching losses (@ $I_f = 5$ A) [w]
IDB30E60 (Infineon)	4.64	5
STTH12R06 (ST)	7.13[1]	0.233
IDB23E60 (Infineon)	5.2	4.5
IDB09E60 (Infineon)	6.21	3

[1] The datasheet suggests to use the following equation for conduction losses evaluation: $P_{cond} = 1.16\ I_{f,avg} + 0.053\ I^2_{f,rms}$

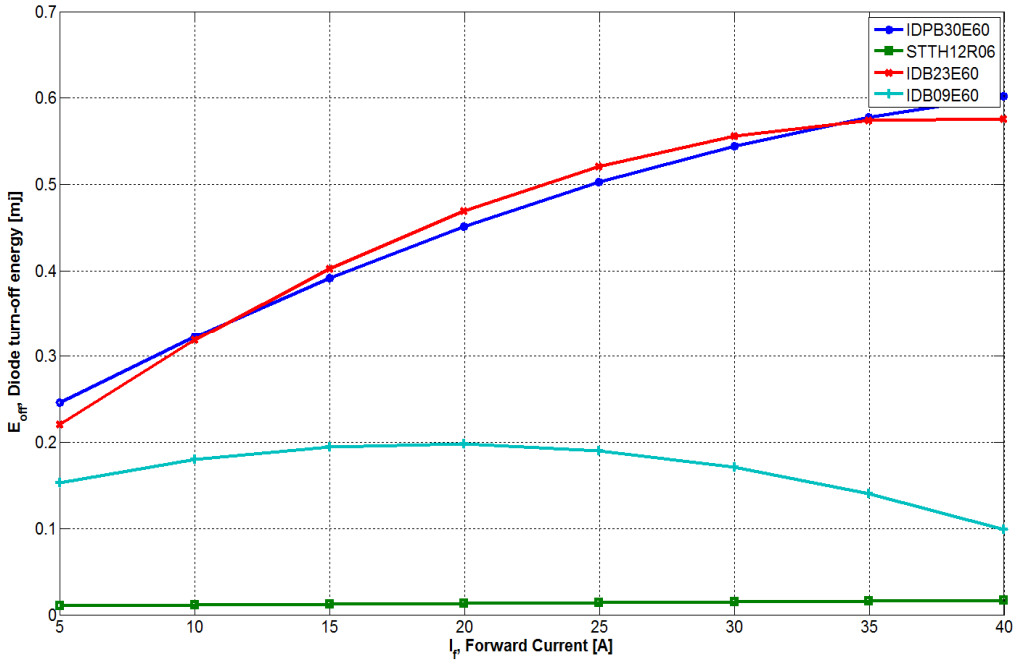


Fig.5. 19 Diode turn-off energy losses of 4 differet p-n diodes as a function of forward current @ dif/dt=200

5.5 Comparing the RR losses with 2 methods presented in chapter 4

Findings in section 5.4 enable us to have a better understanding on di_f/dt effect and improve the calculation method of reverse recovery losses.

Fig.5. 20 can help us to understand the current and voltage transient during a switching instance for the full-bridge converter.

In this part, MOSFET *IRFP31N50L* which is proven to have very low losses is chosen for the comparison of different methods of calculating RR losses.

First, based on t_{ri} (= 115 ns) of the current reference, I_D (=31 A) , the slope of the switch current turn-on in primary side, $di_{sw}(on)\ /dt$ is calculated:

$$\frac{di_{sw}(on)}{dt} = \frac{31}{115} = 269\ A/us$$

For this switch, $Qrr = 570\ [nC]$, $trr = 170[nS]$, $7.9 < Irrm < 12A$ @ $i_D = 31A$

By the help of (5.15), we see that the slope of diode current on secondary side

$di_f(off)\ /dt = 269/2\ (3/4) \cong 100\ A/us$

For region3, as discussed before, the diode dictates t_{rr2} and this time as was seen before, is highly dependent on current slope dif/dt. Quite luckily in this MOSFET datasheet, the values for $dif/dt = 100\ A/us$ are also provided: $trr = 220\ ns$, $Qrr = 1200\ nC$. So new I_{rr} would be:

$$I_{rrm_{new\ condition}} = 2\frac{Q_{rr}}{trr} = 10.9\ A$$

The maximum current, I_{max}can be found:

$$I_{max} = I_{d,on} + 2\frac{n2}{n1}\ I_{rrm} = 11.4 + 2\frac{4}{3}\ 10.9 = 11.4 + 29 = 40.4\ A$$

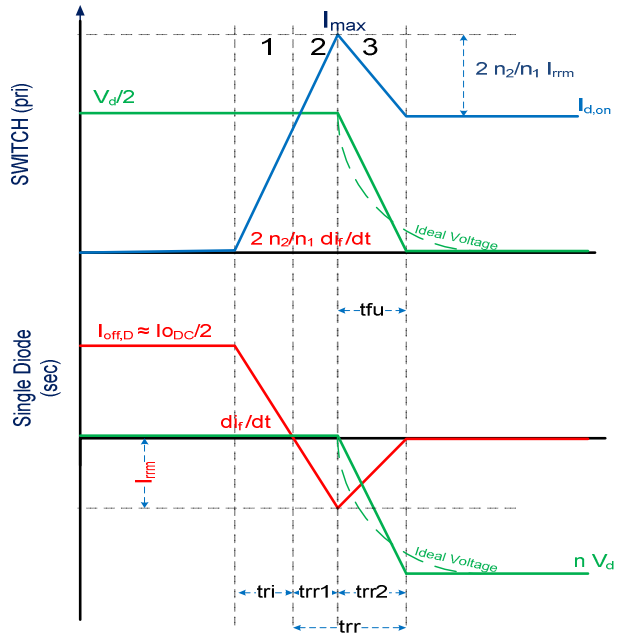


Fig.5. 20 MOSFET Voltage and current during turn-on transient. Down: Diode voltage and current transient during MOSFET turn-on(=Diode turn-off) secondary side of full bridge DC-DC converter

First, we need to find t_{rr1} and t_{rr2}. (5.16) can be deduced from Fig.5. 20.

$$t_{rr1} = \frac{I_{rrm}}{\frac{dif}{dt}} = \frac{10.9}{100} = 109\ ns \tag{5.16}$$

t_{rr1} can be calculated as follows as well, with similar result:

$$t_{rr1} = \frac{2\frac{n2}{n1}\ I_{rrm}}{\frac{di_{sw}}{dt}} = \frac{29}{269} = 108\ \ ns$$

$$t_{rr2} = trr - t_{rr1} = 220 - 109 = 111\ ns$$

Based on Fig.5. 20, equations (4.13) to (4.23) will be modified as below:

Region1&2 :

MOSFET energy losses in primary side (caused by RR, in secondary side)

In Region 1 and 2, the diode losses is zero. The switch dictates the rise time of the current in regions 1 and 2, $t_{ri} + t_{rr1}$, which can be calculated by (5.17)

$$t_{ri} + t_{rr1} = \frac{I_{max}}{\frac{di_{sw(on)}}{dt}} = \frac{40.4}{269} = 150\ [ns] \tag{5.17}$$

$$E_{onM1,2(pri)} = \frac{1}{2}\frac{V_d}{2} I_{max}(t_{ri} + t_{rr1}) \tag{5.18}$$

$$E_{onM1,2(pri)} = \frac{1}{2}\frac{400}{2} \times 40.4 \times 150 = 606\ [uj]$$

5.5.1 Gate current control to mitigate the switching losses (dv_f control)

Region3:

In the simple method introduced in section 4.1.4.1 we made a simplification which can be quite wrong, but will give us the worst case losses. t_{fu} starts just after $Irrm$ reaches it peak and starts to recover to zero, thus the assumption that it occurs after t_{rr2} is wrong. In fact,

when the current during t_{rr2} decreases to zero, V_{gs} starts to decrease rapidly and this causes extra current, more than I_{Gon} passes through C_{gd} resulting a very rapid drain source voltage drop during t_{rr2}. So as it can be seen, during t_{rr2} drain source voltage has a faster voltage drop than it was anticipated [4]. Thus assuming that t_{fu} begins when reverse current reaches its peak is quite correct.

By controlling the gate signal, $I_{G,on}$ with the help of (4.11) we can make $t_{fu} = t_{rr2}$, thus the time that the switch/diode *current* reaches its final value (=t_{rr2}) and the time that the switch/diode *voltage* (=t_{fu}) reaches its final value become equal. Then region3 looks like what is seen in Fig.5. 20. Thus in region 3, both diode and switch exhibit losses, but after that, the switching event is finished (no more losses after that). The current duration, $t_{rr2}$is dictated by the body diode of the secondary side, while the voltage duration, t_{fu} is dictated by gate current of the switch in primary side. From (5.8) we can write:

$$I_{Gon} = \left(\frac{U_{DD}}{2} - R_{DS,on}\, I_{d,on}\right)\frac{C_{GD}}{t_{fu}} = \frac{(200 - 0.15 \times 11.4)}{111} = 1.78A$$

So the gate current pulse amplitude must be 1.78A. But as discussed before, an additional current more than I_{Gon} passes through C_{gd} during t_{rr2}, meaning that for satisfying $t_{fu} = t_{rr2}$, I_{Gon} must be less than 1.78A. Here, we assume that by trial and error, the correct gate current is found and is applied to the switch.

Diode turn-off energy Losses in Secondary side (from (4.20))

$$E_{offD3,sec} = \frac{1}{3}\frac{n2}{n1}\frac{V_d Q_{rr} t_{rr2}}{trr} \tag{5.19}$$

$$P_{offD3,sec} = \frac{1}{3}\frac{4}{3}\,400 \times \frac{1.2 \times 111}{220} 20000 = 2.15\ W$$

MOSFET energy losses (caused by RR, in primary side) (from (4.21))

$$E_{onM3,pri} = \frac{V_d}{2}\left(\frac{I_{d,on}}{2} + 2\frac{n2}{n1}\frac{I_{rrm}}{3}\right)t_{rr2} \tag{5.20}$$

$$E_{onM3,pri} = \frac{400}{2}\left(\frac{11.4}{2} + 2\,\frac{4}{3}\frac{10.9}{3}\right)111 = 341\ [uj]$$

Then total *MOSFET* turn-on energy losses in the primary side would be:

$$P_{onM} = f_{sw}E_{onM} = f_{sw}(E_{onM1,2(pri)} + E_{onM3,pri}) = 20000(606 + 341) = 18.9W$$

While with the *simplified method*[1], when $I_{Gon} = 1.2A$ (ref: Chapter 5, equation (5.9)) from Fig.5. 10 we saw that MOSFET turn on losses was:

$$P_{onM,pri} = f_{sw}(\frac{V_d}{2} I_{d,on}\frac{t_{ri} + t_{fu}}{2} + (2Qrr)\frac{Vd}{2} + \frac{Vd}{2} I_{d,on}\, trr) = 21.5W$$

From (4.9) , as can be seen in Fig.5. 11, diode turn off losses was:

$$P_{offD3,sec} = f_{sw}\,\frac{\frac{n2}{n1}V_d Q_{rr}}{2} = 3.04\ W$$

The conduction losses and the MOSFET turn-off losses would not be changed. So in the simple method, the total switch turn-on energy losses (equal to sum of diode turn-off in secondary side and MOSFET turn-on energy losses in primary side) would be:

$$P_{rr\,simple} = P_{onM,pri} + P_{offD3,sec} = 947 + 107.5 = 21.5 + 3.04 = 24.54\ W$$

While with the more realistic model introduced here, we can write:

$$P_{rr_{realistic\,model}} = P_{onM} + P_{offD3,sec} = 18.9 + 2.15 = 21.05$$

[1] Please note that in simplified method, typical values are read from datasheet.

5.6 Synchronous Rectification (a unidirectional solution)

In Synchronous Rectification, SR, the switches operate as diodes. In other words, the switches are turned on just like diodes. This method is especially used for low voltage applications when the constant voltage drop of a diode during the conduction can affect the total efficiency and functionality of a circuit significantly, or when reverse recovery losses in body diode is excessive. By utilizing MOSFETs and firing them in the right moment, this problem can be resolved as MOSFETs do not have constant voltage drop.

SR can also be used in our full-bridge DC-DC converter, when secondary side diodes cause huge RR losses. By SR, we can get rid of RR losses.

Although from the physics electronic point of view, may using a single MOSFET as a bidirectional switch (ability to turn on at any moment) be feasible, it was not possible to find any source which validates such functionality. Although MOSFETs can conduct in both directions, it is only one direction that can have a switching mode .In some sources a configuration presented in Fig.5. 21 was the proposed solution. This configuration doesn't solve our RR losses problem and it also introduces MOSFET losses. So we drop this solution.

From above, we can conclude that SR cannot be used in bi-directional circuits. So it is classified as unidirectional solution. The switch loss calculation on the Secondary side obeys the same principle as primary side with some minor differences in switching voltage and current. Just bear in mind that we don't have the reverse recovery charge as diodes don't conduct.

MOSFET conduction losses in secondary side

The MOSFET we study in this part is *SPW47N60C3* ($R_{DS,on} = 0.05\ ohm$)

$P_{cond,M,sec} = R_{DS,on} I_{f,rms}^2 = 0.05 \times 6^2 = 1.8\ W$

MOSFET switching losses in secondary side

Based on equations found in chapter 4 and secondary side current and voltage waveforms in Fig.5. 2 (c) we can write:

For turn-on switch losses, t_{fu} with $I_{Gon} = 1.2A$ can be found as below:

$$t_{fu\_sec} = \left(n\, U_{DD} - R_{DS,on} I_{on,D}\right) \frac{C_{GD}}{I_{Gon}}$$

$$= (533.3 - 0.05 \times 4.72)\ \frac{530 \times 10^{-12}}{1.2} \approx 235\ ns$$

$$t_{ri,new\_sec} = \frac{n\, U_{DD}\, I_{on,D}}{V_{ref} I_{ref}}\ t_{ri,ref} = \frac{533.3 \times 4.72}{380 \times 47}\ 27 = 3.8\ ns$$

$$t_{new,on\_sec} = t_{fu\_sec} + t_{fi,new\_sec} = 238.8\ ns$$

$$E_{onM_s} = n\, U_{DD} I_{on,D}\ \frac{t_{new,on\_sec}}{2}$$

$$E_{onM\_sec} = 400 \times \frac{4}{3} \times\ 4.72 \times \frac{238.8 \times 10^{-9}}{2} = 0.3\ [mj]$$

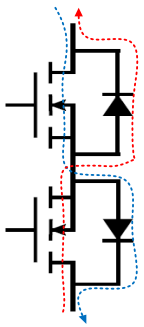


Fig.5. 21 bidirectional switching

On-state Power losses then can be calculated:

$P_{onM\_sec} = E_{onM\_sec} f_{sw} = 0.3\ [mj]\ \times 20[KHz] = 6\ W$

Turn-off losses in power MOSFETs E_{offM} can be calculated with the same steps:

$$t_{ru\_sec} = \left(n\, U_{DD} - R_{DS,on} I_{off,D}\right) \frac{C_{GD}}{I_{Gon}} = (533.3 - 0.05 \times 4.22)\ \frac{530 \times 10^{-12}}{1.2} \approx 235\ ns$$

$$t_{fi,new\_sec} = \frac{nU_{DD}I_{off,D}}{V_{ref}I_{ref}}\, t_{fi,ref} = \frac{533.3 \times 4.22}{380 \times 47}\, 8 = 1.01\, ns$$

$$t_{new,off\_sec} = t_{ru\_sec} + t_{fi,new\_sec} = 236.1\, ns$$

$$P_{offM\_sec} = n\, U_{DD}I_{off,D}\, \frac{t_{new,off}}{2} f_{sw} = 5.31\, W$$

Total secondary side MOSFET switching power losses then will be the sum of these 2 sources of energy losses:

$$P_{tot,sw\_sec} = P_{offM\_sec} + P_{onM\_sec} = 5.31 + 6 = 11.31\, W$$

The MOSFET losses in the *primary side* will be the same as before with one major difference; as there is no reverse recovery charge, E_{onM} would be:

$$E_{onM} = \frac{U_{DD}}{2} I_{d,on} \frac{t_{new,on}}{2}$$

$$P_{onM} = 200 \times 11.4 \times \frac{90.4 \times 10^{-9}}{2} \times 20000 = 2.06\, W$$

Turn-off and conduction losses were calculated in previous parts:

$$P_{offM} = 2.1\, W\, , P_{cond,M} = 2.75\, W$$

$$P_{tot,sw\_pri} = P_{offM} + P_{onM} = 2.1 + 2.06 = 4.16\, W$$

The total switch losses of the whole DC-DC converter with utilizing synchronous rectification would be:

$$P_{tot} = 92.3W$$

5.7 Summery and conclusion

5.7.1 The results, comparison and conclusion about SR method

The total losses of *SPW47N60C3* with SR method are around 7% of the total losses of when the body diode was used in the secondary side. While this MOSFET losses was the worst (highest) in the bidirectional circuit (when the body diode conducts) due to the very low conduction losses, this switch is among the best choices for SR function.

Fig.5. 22 shows a comparison between the body diode switch losses (sum of switching losses and conduction losses) and the switch losses when SR is utilized, in the secondary side. It can be seen that for most of the switches, SR results in lower losses. But it cannot be generalized. I.e *IRFP31N50L*, suffers higher losses with SR method.

SR reduces the switching losses of MOSFETs in primary side significantly. Fig.5. 22 studies only the secondary side losses. Fig.5. 23 compares the total switch losses of SR method with switch losses of body diode.

SR requires a complicated control system to detect zero crossings and to control the secondary side switches. The driving circuits also exhibit losses which we did not take to account. Additionally these control circuits will increase the weight of the whole charger which is important. More importantly we lose bidirectional functionality with SR. Fig.5. 23 shows that despite the fact that with the SR method, the total switch losses for most cases are reduced, but there are still some switches that are good enough. For instance, the 3.6kW DC-DC converter with *IRFP31N50L* MOSFETS exhibits 144W switch losses (corresponds efficiency of 96%), while this value for *IPW60R045CP* with RF method is 88.5 W (corresponds

efficiency of 97.5% without considering control circuit and gate losses on secondary side). Thus it is not worth to use SR in this application.

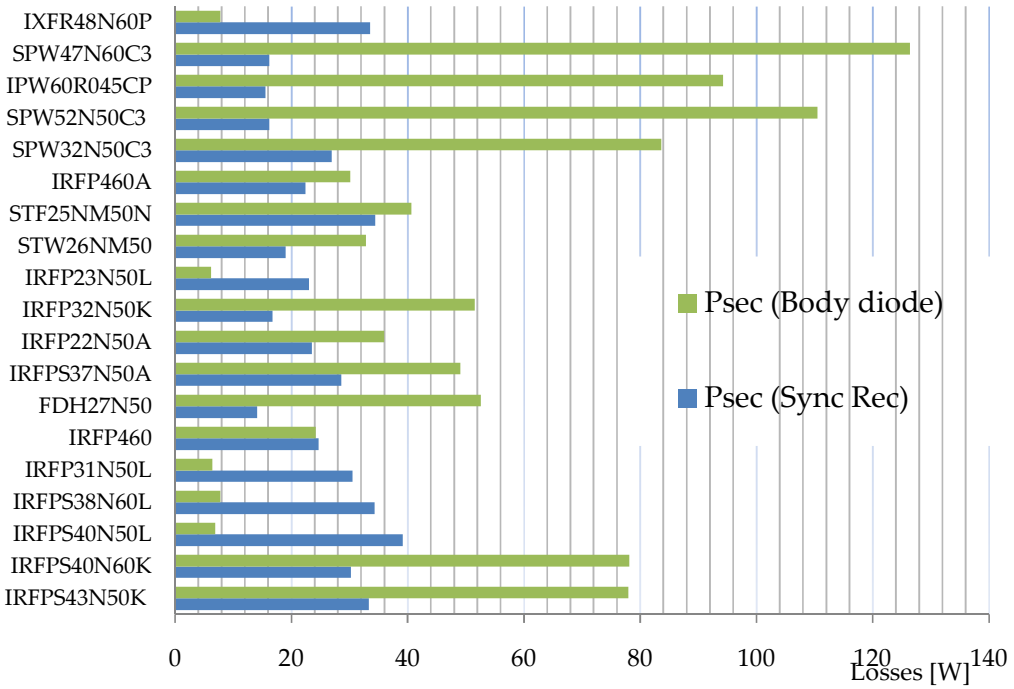


Fig.5. 22 comparison of synchronious rectification switch losses and body diode losses in the secondary side, for a DC-DC full-bridge converter (output power:3.6 KW)

It should be noted that this conclusion was possible to draw only after studying of large verity of switches.

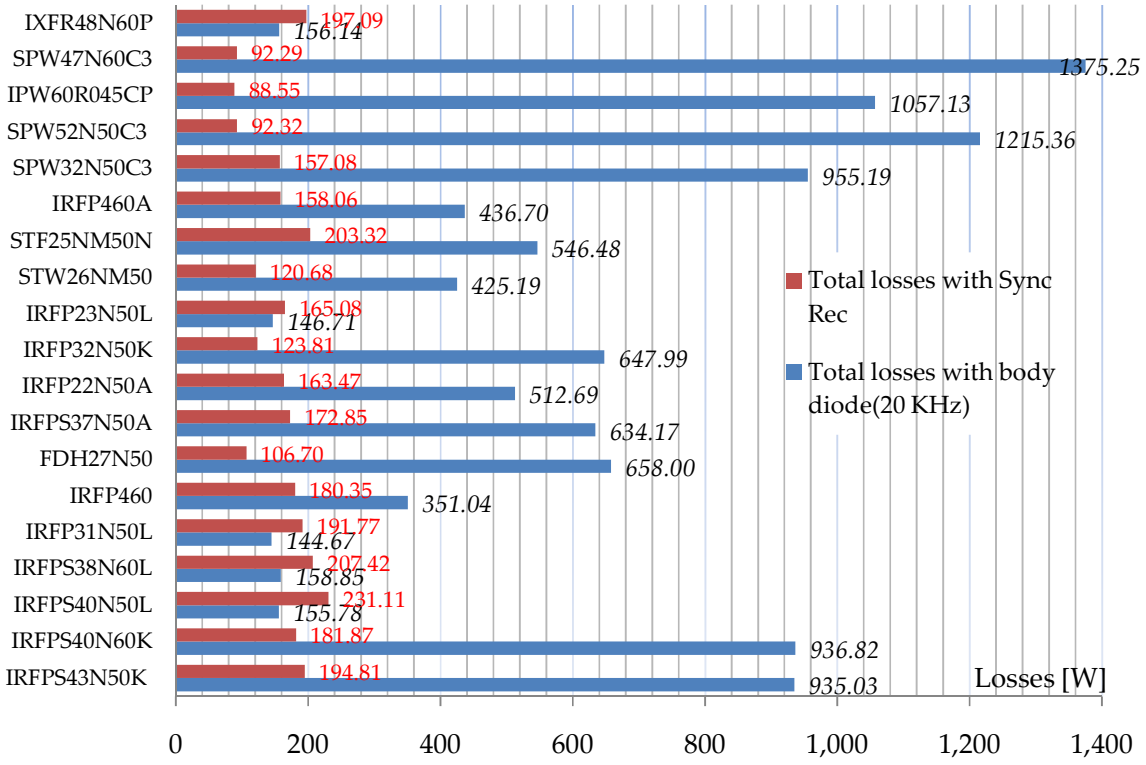


Fig.5. 23 Total switch losses of the DC-DC full-bridge converter with and without Sync. Rec (output power:3.6 KW)

5.7.2 Findings

Switch losses of 19 MOSFETs and 5 IGBTs were compared and the best MOSFET and IGBT were found. It was realized that generally, IGBTs for this application have lower total losses.

Losses of these MOSFET body diodes were compared with external Schottky and p-n diodes. It was found out that although Schottky diodes do not have RR charge and are better than p-n diodes, still some MOSFETs with very low losses can compete with them[1]. Also it was seen that Synchronous Rectification method can be a solution but still some MOSFETs' body diodes exhibit lower losses than the SR method. These can be seen in Fig.5. 24

Two different methods for calculating the reverse recovery losses were presented. It was realized that with dv_f/dt control the losses can be reduced. Also in section 5.5 we showed that realistic model shows lower losses than simplified model.

RR losses dependency on dif/dt was studied and it was revealed that increasing dif/dt generally results in higher turn-off losses and also diode turn-off losses can be minimized by optimized the gate drive as it is the switch that dictates the diode turn-off time.

IGBT switching losses dependency on temperature was studied and found out that at *low temperatures*, the energy losses is independent upon junction temperature. The switching losses in IGBT are highly dependent on the collector current.

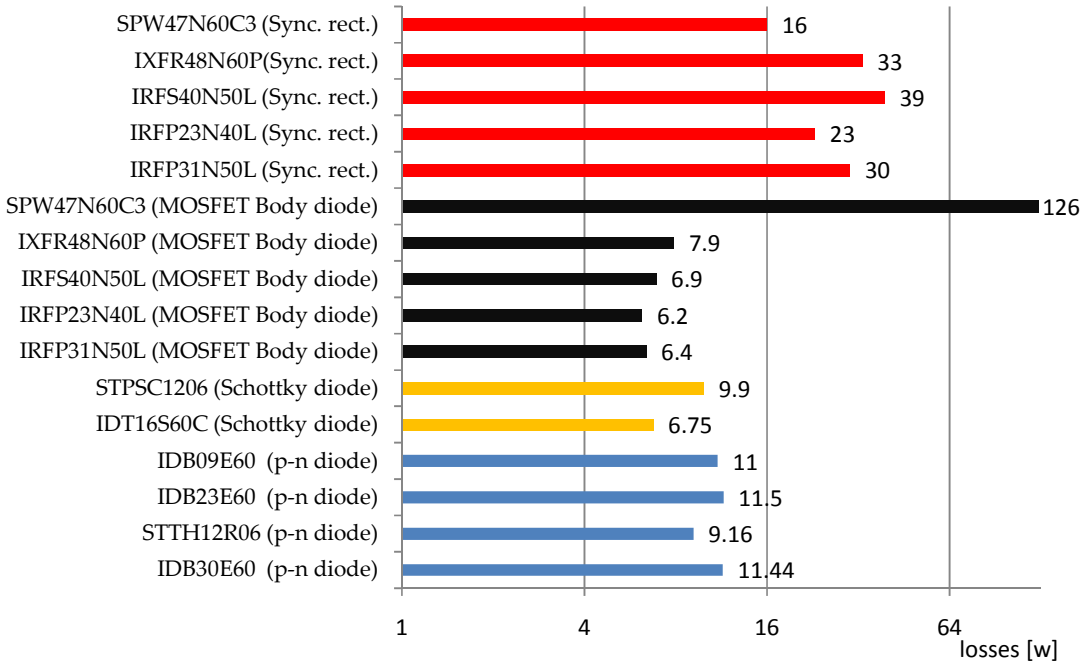


Fig.5. 24 Single switch losses comparison (on secondary side) between SR method, p-n Diodes, Schottky diodes, and MOSFET body diodes (Vd=400V)

From Fig.5. 24 it can be seen that on the secondary side between SR method, p-n Diodes, Schottky diodes, and MOSFET body diodes, body diode of IRFP family MOSFETs exhibit the lowest losses, while Cool MOS can be very good for Sync.Rect. method. One important note is the effect of RR charge on turn on switch losses which cannot be seen in Fig.5.24 (Ref: Fig.5.23)

[1] For diodes, the blocking diode losses on primary side is also included.

6 Total DC-DC converter losses: Buck operation

6.1 Inductor losses

6.1.1 Inductance value for BUCK and BOOST operation

In section3.5, we saw how to calculate the inductance. If 10% of current ripple is desired, it means $\Delta I_L = 0.1\ Io = 0.1 \times 9 = 0.9A$ we saw that at $D = 0.25$, maximum ripple occurs. So by using (3.13) we can write

$$L = \frac{N2}{N1}\frac{(D - 2D^2)}{\Delta I_L(D) f_s} V_d = \frac{4}{3}\frac{(0.25 - 2 \times 0.25^2)}{0.9 \times 20000} 400 = 0.0037\ H$$

With this value of inductance, it is guaranteed that the ripple current is always less than $0.9A$.

Examining this inductance value in the boost converter shows that ripple current is almost half of the criteria (at maximum value, less than 0.5 A as it can be seen in Fig.6. 1)(refer to (3.15))

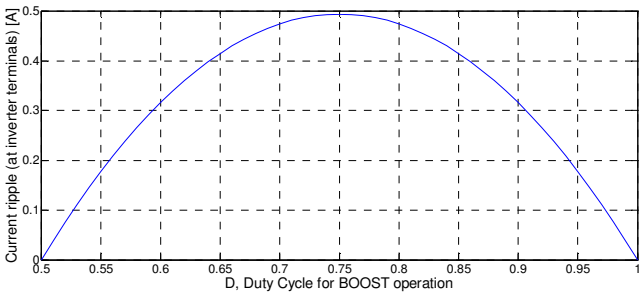


Fig.6. 1 Current ripple in boost operation as a function od duty cycle, when $L_{ind} = 0.0037\ H$

This shows that inductor current of buck operation should be used to guarantee that ripple current, both in boost and buck operation is always below its limits.

6.1.2 Effect of length and cross section of a core on inductance losses

As discussed in section 4.2.4 the inductor losses is highly dependent on the core geometry. Core geometry in theory means effective length, L_e and cross-section A_e. The product of these two is effective volume, V_e. Some people think that by increasing the whole volume (thus weight) with a certain scale factor the lower losses may be obtained. However It is not completely true. In Fig.6. 2 we see that by increasing L_e, core losses decrease, while at the same time copper losses increase. The result in Fig.6. 2 (down) shows that core-cross section is a determined factor of total inductor losses so there is no need of increasing L_e (unless for other constraints like winding area, flux density etc). By only increasing A_e, the

lower core losses can be obtained. (so apply a certain scale factor for all the dimensions is a bit naive!)

It should be noted that there are some manufacturing constraints regarding A_e/L_e ratio. Thus not all A_e and L_e in Fig.6. 2 are feasible to manufacture in practice. As we will see, maximum allowable flux density, B_{max} is the main constraint that should be satisfied and this is done by widening the cross section.

Core losses in Fig.6. 2 is somehow mountainous, esp. at very small volumes. The reason is the quantitative value of number of turns: Referring to (4.39) and (4.47) we see that by increasing A_e at constant N, flux density and so core losses reduce. But when N reaches the next quantitative value, suddenly flux density jumps up resulting higher core losses. (Esp. at low number of turns)

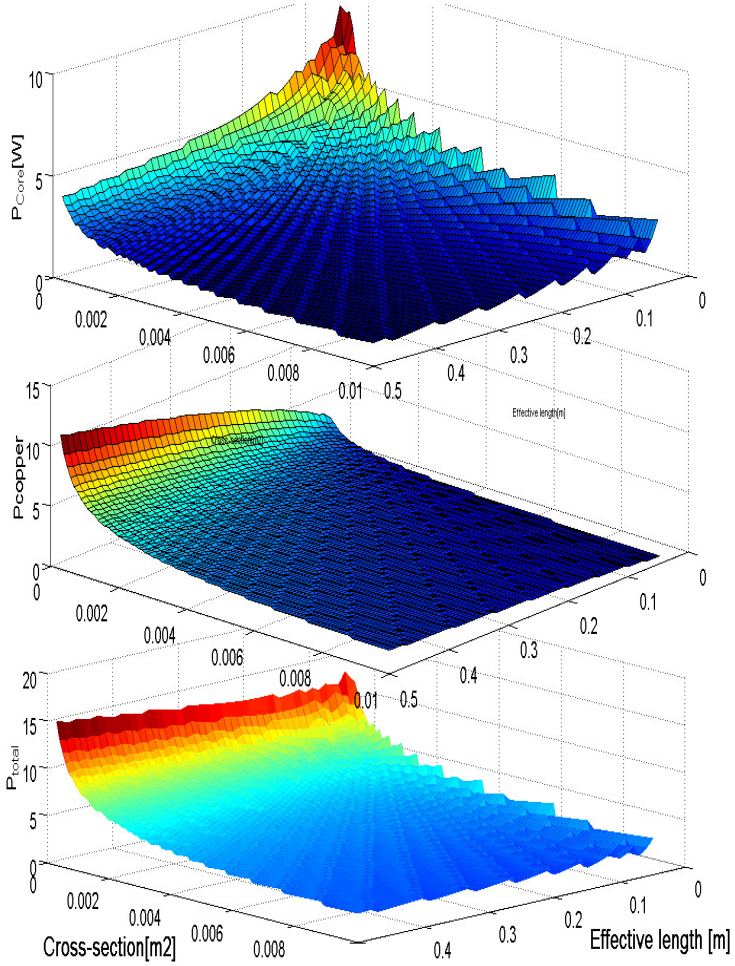


Fig.6. 2 Inductor losses vs. Cross-section and Effective length, for $\boldsymbol{L_{ind} = 0.0037\ H}$, Material: 3C90

6.1.3 Inductor losses calculation procedure and core selection

Fig.5. 2 shows inductor current and voltage waveforms.

Two problems make the finding of the appropriate core for this inductor difficult:

1. Relatively high current, means higher flux and also higher needed winding area.

2. Relatively high inductance value which means higher number of turns (higher flux) and also higher needed winding area. By increasing the frequency, L can be reduced.

In this study in order to find a core with the lowest losses, a comprehensive and massive research over most available cores in the market has been done. From 54 cores (different core shapes and air-gaps can be seen in appendix B), the ones that could satisfy $B < B_{sat}$ are presented in table.6. 1. Then the core with the lowest power losses is selected.

For all the cores based on each core geometry and airgap, core total reluctance can be found [1]. Then, the number of turns can be calculated by $N = \sqrt{L\,\mathcal{R}}$.

At the next step based on each core geometry the length of each turn is found. By knowing N and length of turns, copper losses can be found. For copper losses calculation, there is one technical consideration. Generally, to be in the safe side, assuming current density of around $J = 3\ A/mm^2$ is reasonable.

By $N.i(t) = \varphi\,(\mathcal{R}_g + \mathcal{R}_c)$, Flux density and flux variation can be calculated. In chapter 4 different losses, their nature, concepts and equations were thoroughly discussed. It was observed that the core losses vastly depend on the flux variations (ac flux) and also core geometry and volume.

Table.6. 1 Inductor losses for the cores with the lowest total losses. The full list of cores can be found in Appendix B

Core	E552825E100	E653227E100	E713332E250	E713332E160	E713332E100
Airgap (mm)	0.01044	0.01438	0.00528	0.00962	0.01780
$\mathcal{R}_{tot}$[2]	20011674.3	21420788.5	6277312.2	11360767.6	20942026.7
B (T)	0.394	0.297	0.434	0.322	0.237
dB (T)	0.03284	0.02473	0.03615	0.02681	0.01979
P_{fe} (W)	0.04	0.03	0.10	0.04	0.02
R_{cu} (ohm)	0.147	0.182	0.105	0.141	0.192
P_{cu} (W)	23.195	28.842	16.673	22.374	30.442
P_{tot} (W)	23.232	28.868	16.769	22.417	30.460

The most challenging part of filter inductor design with high values of *L* is to keep the DC Flux density in the acceptable range. If it is done correctly, the flux variation which is the main reason of core losses can be neglected as ac Flux density is always a small fraction of the DC Flux density (ac part based on requirements in this theses is around 10% of DC flux).

It is important to mention that empirical core losses equations introduced in chapter 4, cannot be verified for high flux densities and are only valid within acceptable flux density range. (No saturation)

6.1.3.1 Voltage variation and inductor losses

As it could be seen in table.6. 1 copper losses are the main source of losses in an inductor. *E713332E250* is chosen as the inductor core. We expect an inverse linear correlation between the losses and output voltage (higher voltage corresponds to lower copper losses) and this can be seen in Fig. 6. 3.

[1] For equations and description refer to chapter4

[2] Total core reluctance, $\mathcal{R}_{\text{tot}}$ which is sum of $\mathcal{R}_{\text{fu}} + \mathcal{R}_{\text{gap}}$

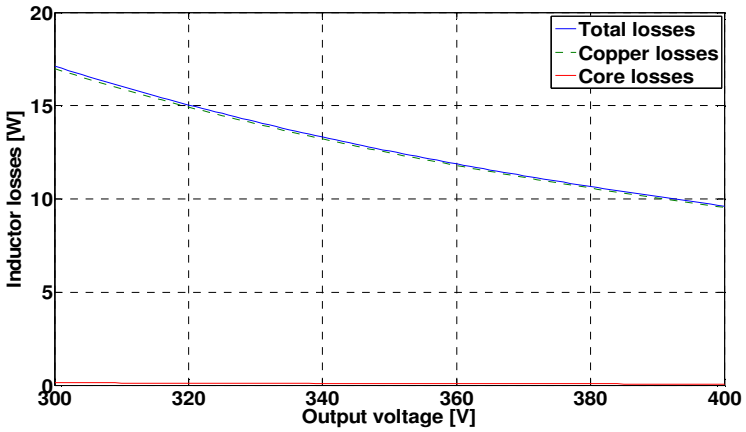


Fig.6. 3 Inductor losses as a function of output voltage (Core*: E713332E250*, Airgap: 5.28mm) at $P_{out} = 3600W$ and $fsw = 20kHz$ (core losses are close to zero)

6.1.4 Frequency and inductor value

By referring (3.13), it can be seen that by increasing the frequency, the value of the inductance is reduced and as a consequence, the number of turns and accordingly core and copper losses will be reduced. This can be seen in Fig.6. 4. (On the other hand, the switching losses and transformer losses will be higher.)

Respective inductance values for $f = 20,\ 60,\ 100kHz$ can be seen in table below.

Table.6. 2 inductance values for different frequencies.

f=20 KHz	L= 0.0037 H
f=60 KHz	L= 0.0012 H
f=100KHz	L= 0.0007 H

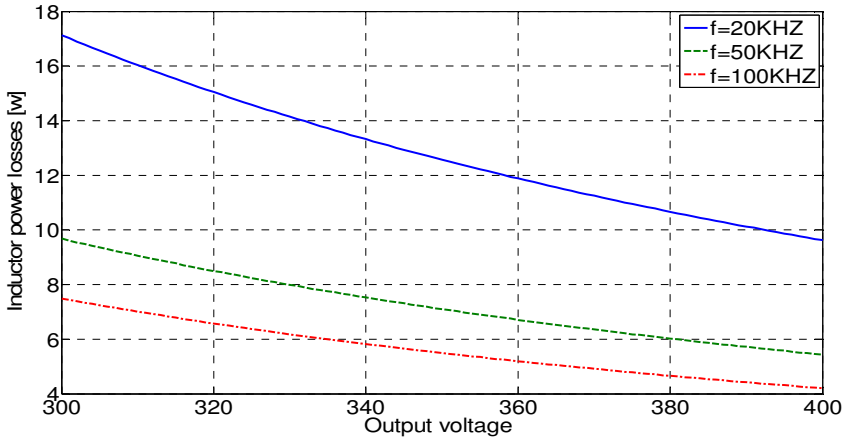


Fig.6. 4 Total inductor losses as a function of output voltage in 3 different frequencies (Core: *E713332E250*, Airgap: 5.28mm) at $P_{out} = 3600W$

6.1.5 Conclusions and deductions on inductor losses

1. Unless the zero airgap case, (which due to the very high flux density is not a practical case for Inductor cores) copper losses are the dominant reason of losses So by increasing the

core size, the length of copper wire, L_{cu} is increased and this leads to higher copper losses. This validates the calculations of chapter 4 (4.2.6).

2. Increasing the air gap leads to increasing Reluctance and hence the number of turns and this, results in higher copper losses. While core losses maybe reduced a little but it does not have any effect on inductor efficiency. In this application airgap is needed to reduce the flux density below B_{sat}.

3. Core material can affect on the total (copper) losses a little. Core materials with higher permeability increase the copper losses like what airgap does. But as the reluctance is highly affected by the airgap, it can be said that core materials have a very minute influence in inductor losses.

6.2 Transformer design

6.2.1 Finding an appropriate turning ratio, N

As observed in chapter 3, for a Buck Full Bridge DC-DC converter we can say:

$$\frac{Vo}{Vd} = \frac{N2}{N1}\, 2D$$

For practical limitations, we have to consider a dead band to prevent the parallel switching which can cause a high short circuit current. Normally $D_{max} < 0.45$ this means:

$$n = \frac{N2}{N1} = \frac{400}{400} \cdot \frac{1}{2 \cdot 0.45} = 1.11$$

Which means N can be equal to $N2/N1 = 4/3 = 1.33$ or 5/4=1.25 or 6/5=1.2. For example for N=4/3, the difference between 1.11 and 4/3 will be corrected by tuning the duty cycle.

Then with N=4/3, the minimum duty cycle (for steady state) will be when the Battery is in its minimum voltage:

$$D_{min} = \frac{Vo,min\ N1}{2.Vd\ N2} = \frac{300 \times 3}{2 \times 400 \times 4} = 0.2813$$

$$D_{max} = \frac{Vo,max\ N1}{2.Vd\ N2} = \frac{400 \times 3}{2 \times 400 \times 4} = 0.375$$

6.2.2 Transformer losses

In chapter 4, core and copper losses were thoroughly discussed. It was realized that the transformer core losses become problematic especially at the beginning of each switching event when the inductor current should vary with a very high rate (which will cause high voltage jumps). This will cause a very high equivalent frequency ($f_{sin_{eq}}$) for modified Steinmetz equation. The transformer current waveform with leakage inductance of $1uH$ can be seen in Fig.6. 5.

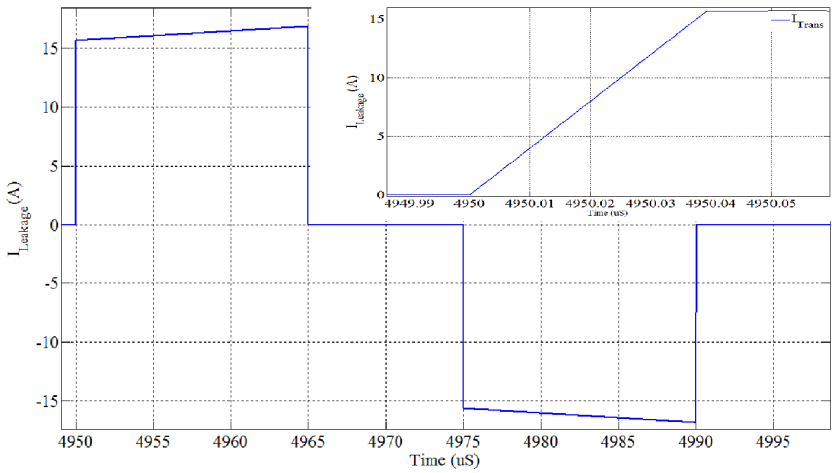


Fig.6. 5 Transformer current (flux density) waveform and the switching transient (leakage=1uH)

As it can be seen, equation below which is used in some publications, is not applicable for finding the transformer flux in fullbridge configuration as the flux doesn't build up during DT_s. This can be seen in Fig.6. 5 and Fig.4. 12

$$B_{max} = \frac{V_d D\, T_s}{A_e N_{min}} \tag{6.1}$$

What we do is to use Fourier transformer on the transformer current (by assuming a constant permeability) the flux waveform is proportional to transformer current as it can be seen in (6.2). For four voltage levels, the main current harmonics are found (only harmonics higher than 9% of fundamental) and are presented in Table.6. 3. As it can be seen for each duty cycle the harmonics spectrum may differ significantly.

Table.6. 3 Transformer current harmonics for 4 different voltages.

V=306 (D=0.3)	Fundamental(@ 20KHz) = 16.19 peak (11.45 rms) Total Harmonic Distortion (THD) = 34.36% 60000 Hz (h3): 12.08% 100000 Hz (h5): 24.49% 180000 Hz (h9): 10.40% 220000 Hz (h11): 9.3%
V=334.5 (D=0.326)	Fundamental = 15.54 peak (11.0 rms) Total Harmonic Distortion (THD) = 30.72% 100000 Hz (h5): 21.06% 140000 Hz (h7): 13.28% 220000 Hz (h11): 9.86%
V=361 (D=0.35)	Fundamental = 15.2 peak (10.75 rms) Total Harmonic Distortion (THD) = 28.12% 100000 Hz (h5): 15.34% 140000 Hz (h7): 15.79%
V=399 (D=0.385)	Fundamental = 14.45 peak (10.22 rms) Total Harmonic Distortion (THD) = 28.00% 60000 Hz (h3): 16.68% 140000 Hz (h7): 12.44% 180000 Hz (h9): 11.70%

As the frequency spectrum shows, harmonics frequencies even 10 times larger than fundamental still contribute a large portion of THD. So it is important to choose a core material suitable for $200\ kHz$ and higher. That is the reason we choose $3F3$ for transformer core material. From Fig. 4.13 and Fig. 4. 14 (at 20 kHz) it can be said that $3F3$ exhibits lower core losses.

Flux density for each harmonic can be found by:

$$B(h) = \frac{N\ I(h)}{\mathcal{R}A_e} = \mu_o\mu_r \frac{N\ I(h)}{L_e} \tag{6.2}$$

By plugging (6.1) into (4.24) for each voltage level, core losses can be calculated by:

$$P_{core} = C_m \sum_{h=1}^{n} f(h)^x\ B(h)_{peak}^y \quad \left[\frac{mW}{cm3}\right] \tag{6.3}$$

Where:

h: Harmonic order

$B(h)$ and $I(h)$: Flux density and current for each harmonics

Although (6.3) utilizes the summation rule which means the linearization of losses and this is maybe not quite correct (i.e. the area under hysteresis loop of a signal with several harmonics is not equal to the summation of the areas of each harmonic of that signal), but the author believes this method gives the worst case losses. Still the experiment should support this claim.

There are several mathematic models that try to predict the losses, like modified Steinmetz equations, or more recently [30], but all of these models fail to give a correct values of losses when the time that flux is built-up becomes minute. For example, in [30] the model error can reach to 40% and more.

In appendix B we compare losses of 50 cores at 400V (assuming sine wave flux, Steinmetz equation is used for core losses). Based on that, the core with lowest losses is selected which is EC70. This core has a large winding area that can house up to 87 turns in primary and 96 turns in secondary side (with filling factor of 0.7, for more details refer to appendix B)

6.3 Total losses of DC-DC Buck Converter

In the full-bridge DC-DC converter with galvanic isolations, three source of losses were investigated in previous parts: (1) Transformer core and copper losses, (2) Inductor core and copper losses, (3) Switch losses (switching and conduction losses of four switches in primary and four switches in secondary side, totally 8 switches.)

For each of these elements the one with the lowest losses were selected as it can be seen in Table.6. 4. Information about all these elements can be found in Appendices A and B

The total losses for the best MOSFET, *IRFP31N50L* and the best IGBT, *IKW30N60H3* are calculated and presented in Fig. 6. 6.

Table.6. 4 final chosen components for the DC-DC converter

Transformer core	EC70
Inductor core	E713332E250
IGBT switch	IKW30N60H3
MOSFET switch	IRFP31N50L

With these components the total converter losses and efficiency when the output voltage varies from 305V to 400V is presented Fig.6. 6.

As it can be seen, with IGBT IKW30N60H3, efficiency is improved around 1% at 300V while at higher voltage the efficiency improvement is only 0.5%.

When the battery voltage is 400 V, The total switch losses for the best MOSFET and IGBT are respectively 144W and 78W which corresponds to 78% and 67% of total DC-DC buck converter losses.

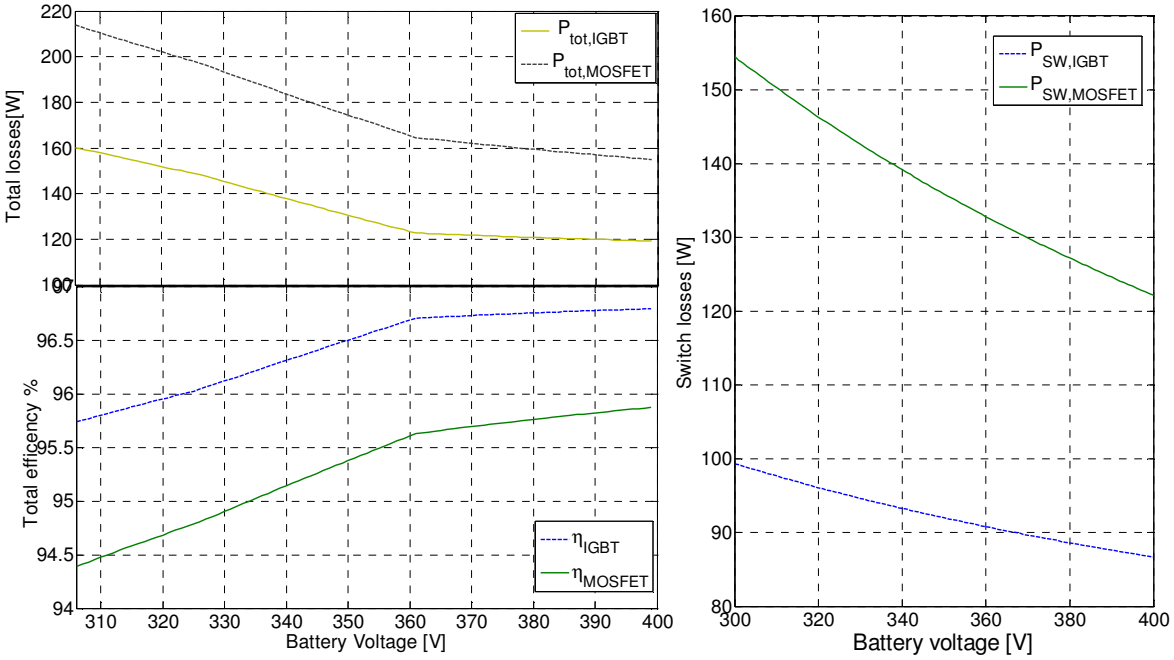


Fig.6. 6 (left-up): DC-DC full bridge buck converter losses. (left -down): Total efficiency of the converter. (right):total switch losses as a function of voltage with two different switches. One IGBT (IKW30N60H3) and one MOSFET (IRFP31N50L)

7 Total DC-DC converter losses: Boost operation

7.1 Prerequisites and assumptions

After choosing elements with lowest losses for buck full-bridge converter in previous chapters, in this chapter the designed converter is exposed to boost operation mode and the losses for this mode will be estimated. It should be noted that the buck operation (charging mode) is the common operation mode, so elements are selected based on buck mode.

As now the direction of the power/current flow is from the battery towards the grid, the transformer primary and secondary side is defined based on this new direction, meaning that the winding connected to the battery side is now primary and the other is secondary. It must be remembered that the number of turns and turning ratio was selected for buck operation and based on the opposite current direction.

The specification of the DC-DC converter for the boost operation can be seen in table.7.1. It is assumed that if the battery can deliver 4kW. With around 150-200W power loss in DC-DC stage and 100W losses in the inversion stage, around 3750-3700W is expected to be delivered to the grid. These values, later on will be checked and modified. The elements which were selected for the buck operation can be seen in Table.6. 4.

The topology of the DC-DC full-bridge boost converter (current source converter) can be seen in Fig.7. 1.

Table.7. 1 The specification of the full bridge DC-DC converter for boost operation

Parameters	**Description**
$Vo = 400\ V$	Output dc link voltage to the inverter
$Pin = P_{bat} = 3950\ W$	Power from the Battery
D_{max} (Boost op.)= 0.72	Max duty cycle of each switch corresponding $Vin = 300V$
D_{min} (Boost op.)= 0.63	Min duty cycle corresponding $Vin = 400V$
$n_{boost} = N2/N1 = 3/4$	Turning ratio of transformer: secondary/primary
$f_s = 20000\ Hz$	Switching frequency
$V_{p1} = 400V$	Max voltage over a Switch (during turn-off)
$Vin = V_{bat} = 300{\sim}400V$	Battery side voltage variation
$P_{loss} = 200W$	Assumed power losses of boost full-bridge stae
Current ripple=10%	Battery current ripple (preferably 5%)
Voltage ripple=20%	Battery voltage ripple (preferably 10%)

The principle of operation is discussed in chapter3, so the repetition is omitted here. Based on parameters introduced in Fig.7. 1, different voltage and current waveforms are displayed in Fig.7. 2

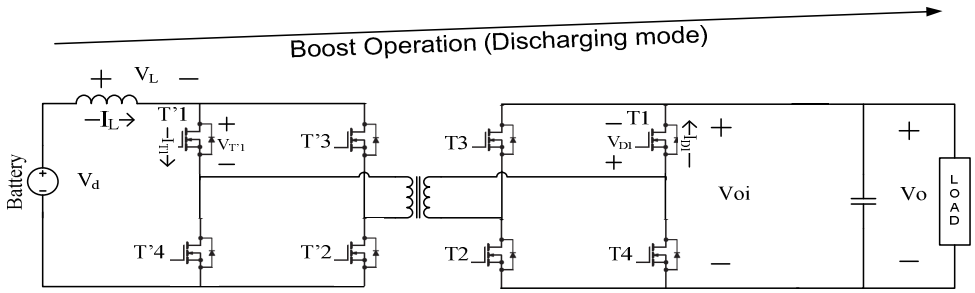


Fig.7. 1 Full-bridge bidirectional converter, when it operates in boost (discharging) mode

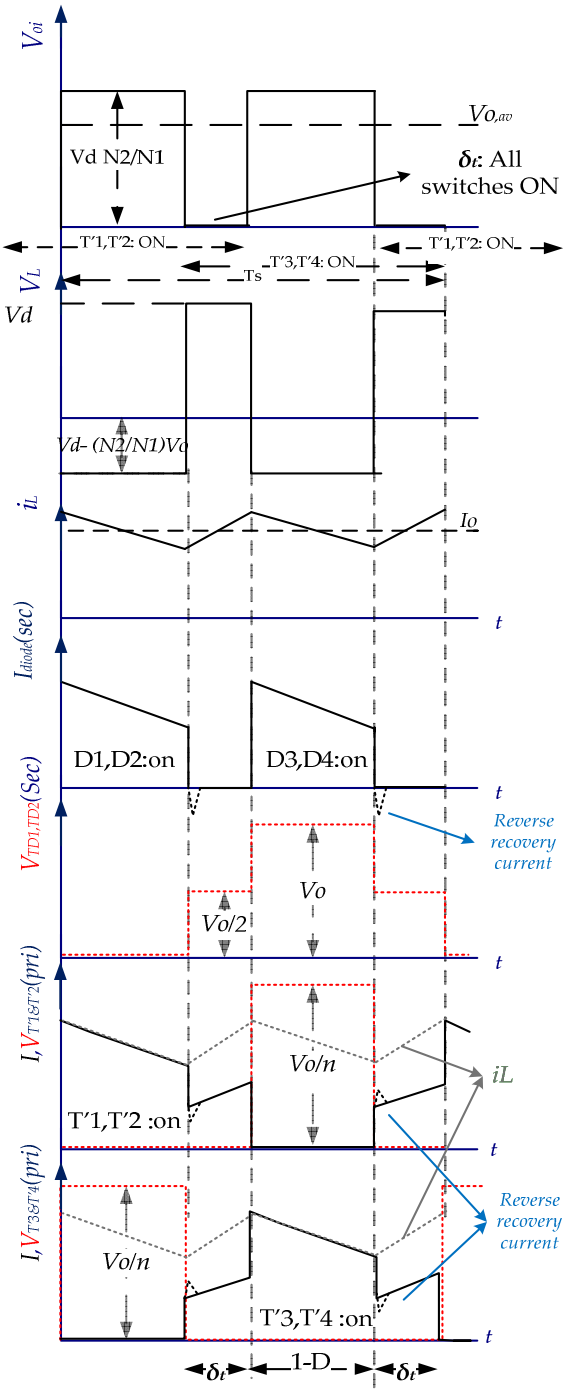


Fig.7. 2 DC-DC fullbridge Boost converter waveforms. The topology can be seen in Fig.7. 1
the principle of operation is explained in chapter 3

a)Inductor current (iL) and voltage (VL) waveforms

b)Body diode current and voltage waveforms (on secondary side)

c)Switch current and voltage waveforms (on primary side)

7.1.1 Current calculation for each element

7.1.1.1 Switch current in primary side

As it can be seen in Fig.7. 2 (c) a switching period can be divided in four intervals.

$(1-D)Ts$ which a pair of switches are off, $(1-D)Ts$ which another pair of switches are off, and $2\delta_t T_s$ which all the switches conduct. δ_t can be defined as:

$$\delta_t = D - 0.5 \tag{7.1}$$

Inductor average current would be:

$$I_{L_{avg}} = \frac{P_{bat}}{V_{in}} \tag{7.2}$$

From Fig.7 2(a) ripple current would be

$$\Delta I_T = \frac{V_{in}\delta_t}{f_s L} \tag{7.3}$$

The maximum and minimum current of the inductor would be

$$I_{T_{max}} = 2\, I_{T_{off}} = Id + \left(\frac{\Delta I_T}{2}\right) \tag{7.4}$$

$$I_{T_{min}} = 2\, I_{T_{on}} = Id - \left(\frac{\Delta I_T}{2}\right) \tag{7.5}$$

Current value just before the switch turn-off and turn-on transient respectively would be:

$$I_{T_{off}} = \frac{I_{T_{max}}}{2} \tag{7.6}$$

$$I_{T_{on}} = \frac{I_{T_{min}}}{2} \tag{7.7}$$

Average value of the switch current would be:

$$I_{T_{avg}} = \frac{I_{L_{avg}}}{2} \tag{7.8}$$

RMS current can be calculated by its classic equation. Just bear in mind that current ripple is neglected.

$$I_{T,rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} I_{f,D}^2(t)\, dt} \Rightarrow \quad I^2{}_{f,rms} = \frac{1}{T_s}\left(2\delta_t T_s\, I_{T_{avg}}^2 + 4\, I_{T_{avg}}^2 (1-D)T_s\right)$$

$$\rightarrow \qquad I_{T,rms} = I_{T_{avg}}\sqrt{3-2D} \tag{7.9}$$

7.1.1.2 Switch current in secondary side

In secondary side, anti parallel diodes conduct. So based on Fig.7. 2 (b) output current towards the inverter can be found:

$$Io = \frac{I_{L_{avg}}}{n} \tag{7.10}$$

Ripple current in secondary side (output) would be:

$$\Delta Io = \frac{\Delta I_T}{n} \tag{7.11}$$

Diodes turn on and turn off current would be:

$$Io_{max} = I_{d_{on}} = Io + \left(\frac{\Delta Io}{2}\right) \tag{7.12}$$

$$Io_{min} = I_{d_{off}} = Io - \left(\frac{\Delta Io}{2}\right) \tag{7.13}$$

In the secondary side during $(1-D)Ts$ diodes conduct. So we can say that the average current of the body diode in secondary side can be found by (7.14)

$$I_{d_{avg}} = Io\,(1-D) \tag{7.14}$$

Also RMS current of body diode in secondary side would be:

$$Io_{rms} = Io\,\sqrt{1-D} \tag{7.15}$$

7.1.1.3 Transformer current

The average value of primary and secondary current is zero.

During $(1-D)Ts$, the current is flown towards transformer windings. So the RMS current value of the primary side would be:

$$I_{pri} = I_{L_{avg}}\,\sqrt{2(1-D)} \tag{7.16}$$

7.2 Inductor losses

With assuming around 4kW output power of the battery, the average value of the inductor current can be found between:

$$I_{L,min} = \frac{P_{Bat}}{V_{Bat,max}} = \frac{4000}{400} = 10A \tag{7.17}$$

$$I_{L,max} = \frac{P_{Bat}}{V_{Bat,min}} = \frac{4000}{300} = 13.3A$$

Inductor losses calculations were discussed in previous chapters. When the battery voltage reduces (discharging) the current (in constant power) increases which leads to increasing the total inductor losses.

Core losses can be found out by (4.27) and (4.28). The only difference between buck and boost is the equivalent frequency that is needed to be calculated based on new conditions. From (4.28) the equivalent frequency can be found to be:

$$f_{sin_{eq}} = \frac{2}{\pi^2}\left(2\left(\frac{B_{ac}}{B_{ac}}\right)^2\frac{1}{(1-D)Ts} + 2\left(\frac{B_{ac}}{B_{ac}}\right)^2\frac{1}{(D-0.5)Ts}\right)$$

$$= \frac{2}{\pi^2}\,f_s\,\frac{1}{(1-D)(D-0.5)} \qquad 1 > D > 0.5 \tag{7.18}$$

By plugging required values into (4.27) the core losses can be obtained. The result in Fig.7.3 shows that like the buck operation, core losses are so low and can be neglected for our case.

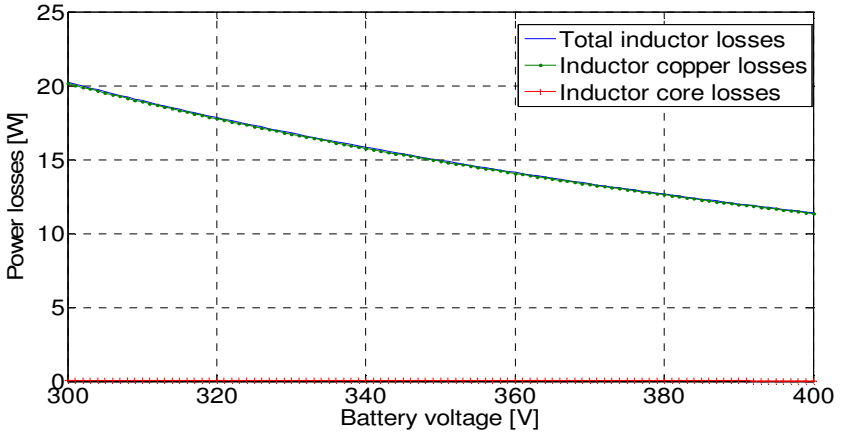


Fig.7. 3 Inductor losses as a function of battery voltage (Core*: E713332E250*, Airgap: 5.28mm) at $P_{bat} = 4000W$ and $fsw = 20kHz$ (core losses are close to zero)

7.3 Transformer losses

Transformer losses were discussed in previous chapters. In chapter 6 we found out that the best transformer core is EC70.

Copper losses for boost operation can be seen in Fig.7. 4(right). Core losses with two different methods, Steinmetz equation (based on sine wave) and with harmonics summation method as explained in chapter 6 are compared and the results can be seen in Fig.7. 4(left)

In order to implement the harmonics summation method, for 5 different battery voltage, a Fourier table of transformer current harmonics is established as it can be seen in table.7. 2

Table.7. 2 Transformer current harmonics for 5 different voltages (boost operation)

Vbat=400, V0=400, D=0.63	Fundamental = 11.78 peak (8.327 rms) 60000 Hz (h3): 13.06% 60000 Hz (h5):9.15% 60000 Hz (h7):14.63% 60000 Hz (h9):10.76% 60000 Hz (h15):7%
Vbat=375, D=0.652,	Fundamental = 12.06 peak (8.525 rms) THD = 29.11% 60000 Hz (h3): 6.18% 100000 Hz (h5): 15.70% 140000 Hz (h7): 15.83% 260000 Hz (h13): 8.45%
Vbat=350, D=0.68	Fundamental = 12.62 peak (8.921 rms) THD = 31.87% 100000 Hz (h5): 22.02% 140000 Hz (h7): 12.27% 220000 Hz (h11): 10.53% 260000 Hz (h13): 5.26% 340000 Hz (h17): 6.87%
Vbat=325, D=0.703	Fundamental = 12.9 peak (9.119 rms) THD = 35.65% 60000 Hz (h3): 12.83 100000 Hz (h5): 24.70% 140000 Hz (h7): 5.47% 180000 Hz (h9): 11.09% 220000 Hz (h11): 9.06% 300000 Hz (h15): 8.18%
Vbat=300, D=0.726	Fundamental = 13.14 peak (9.293 rms) THD= 40.52% 60000 Hz (h3): 22.13% 100000 Hz (h5): 24.44% 180000 Hz (h9): 14.48% 260000 Hz (h13): 9.50% 340000 Hz (h17): 6.03%

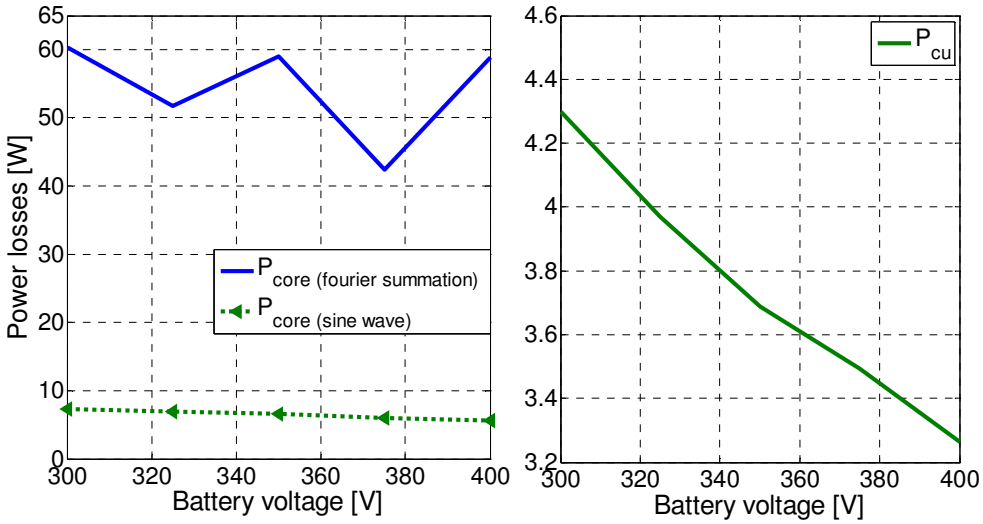


Fig.7. 4 Transformer losses as a function of battery voltage (Core*: EC70*, Airgap: 1.83mm) at $P_{bat} = 4000W$ and $fsw = 20kHz$ (Left) core losses with two different method (Right) copper losses

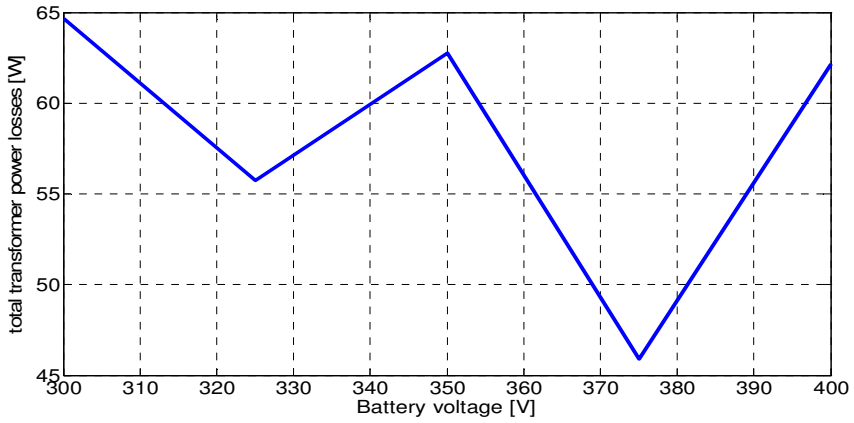


Fig.7. 5 Transformer total losses as a function of battery voltage (Core*: EC70*, Airgap: 1.83mm) at $P_{bat} = 4000W$ and $fsw = 20kHz$

7.4 Total losses

7.4.1 Reverse recovery and switch losses in boost operation

The reverse recovery current occurred during the body diode turn-off time interval, finds its way to the primary side as it is shown in Fig.7. 6.

Like the buck operation, inductor current cannot be changed suddenly. As $D'1$ is reversely biased, the reverse recovery current, I_{rr} in the primary side can only pass through $T'1$. But as it can be seen in Fig.7. 6 and Fig.7. 2, when $D1$ and $D2$ in the secondary side are turned off, $T'1$ and $T'2$ are still conducting, meaning that no switching losses will occur in $T'1$ and $T'2$. But in $T'3$ and $T'4$ the turn on losses will significantly be affected by $D1$ and $D2$ turn-off.

As before, the MOSFET we study is *IRFP31N50L*. In chapter 5 it was seen that for this MOSFET, $di_{sw_{pri}}/dt = 269\ A/us$, meaning that the current derivative in the secondary side , dif_{sec}/dt is:

$$\frac{dif_{sec}}{dt} = \frac{di_{sw_{pri}}}{n} = 358.6\frac{A}{us} \qquad (7.19)$$

This current derivative can be too high and there is a risk of snappy recovery and EMI problems. As it was studied in chapter 5, by increasing the current derivative, Q_{rr} increases slightly, I_{rrm} also increases, while trr and S reduces (Ref. to diode data sheets and Fig.5. 16)

The MOSFET datasheet only provides the value of $Q_{rr}, trr\ or\ I_{rr}$ for $\frac{dif}{dt} = 100\ A/us$ and it forces us to use such values for $dif/dt = 358\ A/us$. Unfortunately this will result in some errors in power losses calculations. The values for the boost operation power losses calculation are:

$t_{rr} = 170\ ns$
$Q_{rr} = 1.2\ uC$
$I_{rr} = 14A$

The equations for calculating the switching losses for the boost operation are quite similar to the buck operation (5.18 - 20) By the help of Fig.7. 2 and Fig.7. 6 we can find the turn-on switching losses of the MOSFETs in the boost operation. Turn-on losses in the switches of the primary side in the regions 1,2 and 3 (see Fig.5. 20)would be:

$$E_{onM1,2} = \frac{1}{2}\left(\frac{Vo}{n}\right)\left(I_{T_{off}} + n\,I_{rrm}\right)(tri + trr1) \qquad (7.20)$$

$$E_{onM3} = \left(\frac{Vo}{n}\right)\left(\frac{Id}{2} + n\frac{I_{rrm}}{3}\right)trr2 \qquad (7.21)$$

On the secondary side, diode turn off losses would be:

$$E_{offD3} = \frac{1}{3}\left(\frac{Vo}{2}\right)Q_{rr}\left(\frac{t_{rr2}}{trr}\right) \qquad (7.22)$$

Where:

$I_{T_{off}}$ Current value just before the switch turn-off
n: turning ratio, for the boost operation it will be n=3/4
Vo: output voltage of the DC-DC converter that is kept constant: (400 V)

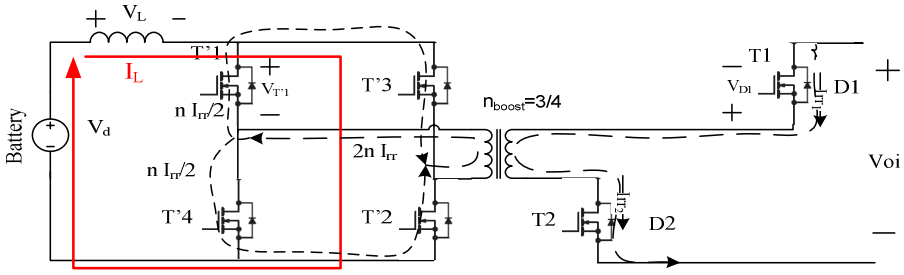


Fig.7. 6 the reverse recovery current propagation from secondary side towards primary and the direction of it.

Two switches from chapter 6 were selected and compared for boost operation. These two switches are MOSFET *IRFP31N50L* and IGBT *IKW30N60H3*. Their specifications can be found in appendix A

The total losses of these two switches as a function of battery voltage can be found in Fig.7.6 (right) as it can be seen, the MOSFET exhibits more switching losses.

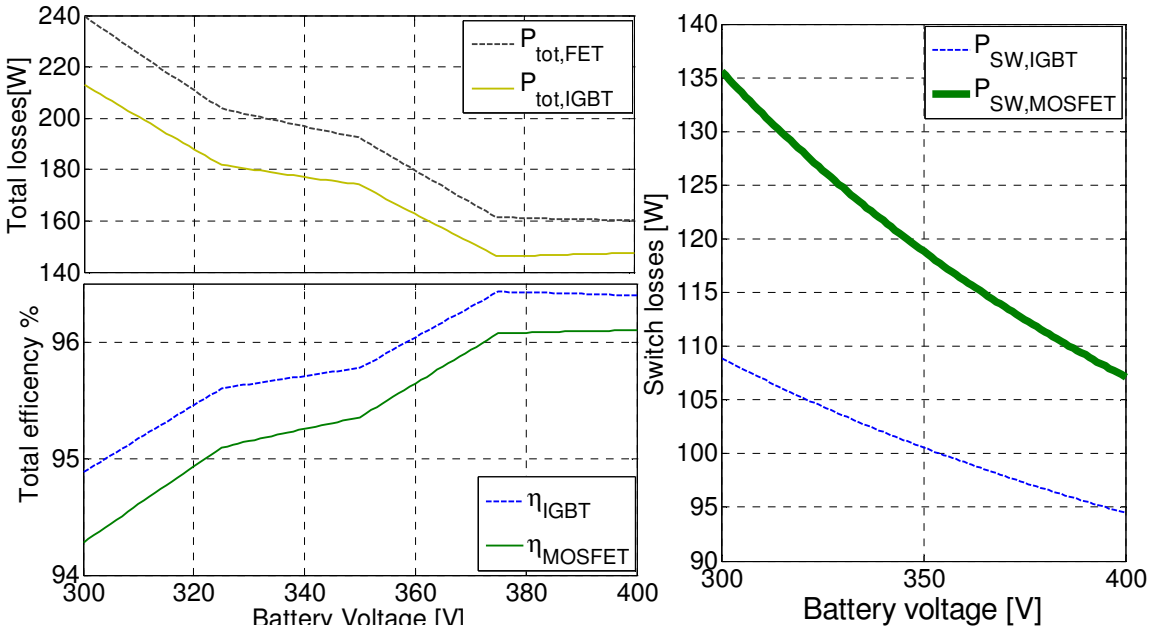


Fig.7. 7 (left-up): DC-DC full bridge boost converter losses. (left -down): Total efficiency of the converter. (right):total switch losses as a function of voltage with two different switches. One IGBT (IKW30N60H3) and one MOSFET(IRFP31N50L)

7.5 Conclusion

It was observed that like buck operation, in the boost operation, inductor losses are mostly due to the copper losses, while an opposite can be observed for transformer losses.

It is interesting to see that in boost operation the MOSFET exhibits higher losses. Totally utilizing IGBTs can improve the total efficiency of around 0.5% in the boost operation as it can be seen in fig.7. 6(left)

Fig.7. 6(left) also shows that at lower battery voltage, when the battery energy is depleting, the losses are higher than when the battery is fully charged. This difference is around 60W for the IGBT and 80W for the MOSFET (corresponding ~1.5% of the efficiency)

Another interesting result arises when the total efficiency (and losses) of boost operation (Fig.7. 6) is compared with the total efficiency (and losses) of buck operation (Fig.6. 12).

It can be seen that that total loss for the boost operation vary between 150W and 210 W ($P_{in_{converter}} = 3950\,W$), while for the buck operation this value (for IGBT) switch is between 140W and 200W ($P_{in_{converter}} = 3600W$), suggesting that the total efficiency for the buck operation is only around 0.25% to 0.5% higher. Thus it can be claimed that generally the operation mode does not influence the total losses significantly.

8 Controller design and Simulations

8.1 DC-DC converter

8.1.1 Buck operation, Open loop operation

Simulation results of the full bridge buck converter operation can be seen in Fig.8. 1. The waveforms comply with what is expected. An undesirable overshoot of 30% in output voltage can be observed.

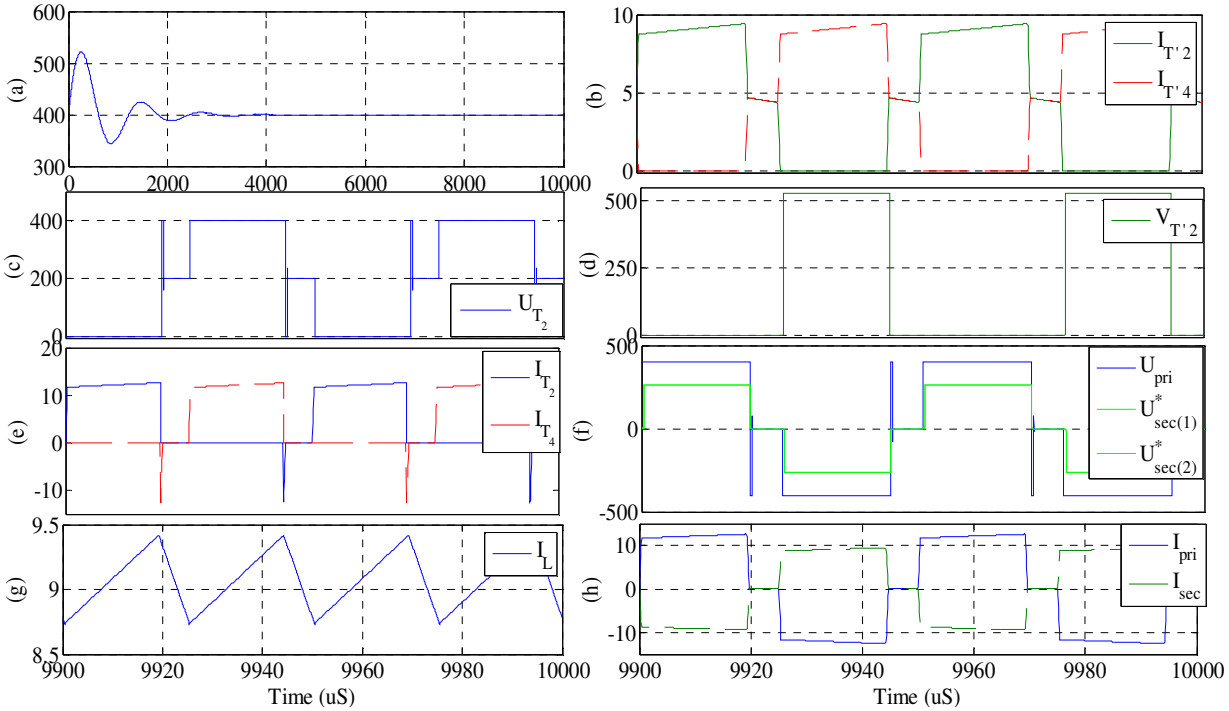


Fig.8. 1 Simulation result of the DC-DC converter and its waveforms, in buck operation mode (charging) when the battery voltage and input voltage are 400V. (Input power from rectifier is around 3650W) (resitive load)(a) Battery voltage, (b) Sec-side body diode current, (c) pri-side switch voltage, (d) Sec-side body diode voltage , (e) pri-side switch current (f) Transformer pri & sec side voltages, (g) Inductor current, (h) Transformer pri & sec side currents (currents are in A and voltages are in V)

* the transformer in this simulation has two windings in series in secondary side and in Fig.8. 1.(f), the voltage of each of the secondary windings is presented. The actual secondary side voltage is the summation of these two voltages. (twice the appeared voltage in Fig.8. 1.(f))

As it was mentioned in chapter3, the output voltage (battery side) was a function of duty cycle. This equation can be seen below:

$$\frac{Vo}{Vd} = 2D\frac{N2}{N1} \quad , \quad D < 0.5$$

But in reality due to switch, inductor and transformer resistance, and also constant voltage drop of diodes, equation above is not quite correct. This can be seen in Fig.8. 2(left) It

is also worth mentioning that the converter should never work beyond D=0.5 because it leads to simultaneous switching which can short circuit the capacitance (primary side).

In chapter 3, we proved that the maximum current ripple occurs at D=0.25 and this can be verified in Fig.8. 2(right).

One interesting point about buck operation is that it is always stable, making the controller design simple and robust.

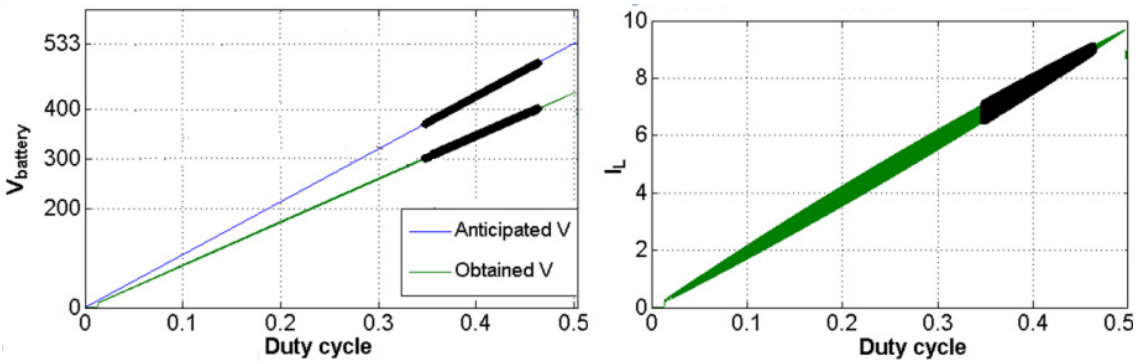


Fig.8. 2 Open loop performance of buck DC-DC converter. Black area indicates the operation area in which the battery voltage may vary (from low SOP to full charge) The width of I_L represents the expected ripple at corresponding duty cycle

8.1.2 Boost operation, Open loop operation

Eq. (3.3) describes the output voltage as a function of duty cycle. But Fig.8. 3 shows that (3.3) is only valid for the duty cycles less than 0.7 (500V). Beyond D=0.7 the output voltage fails to follow the required voltage, thus a control system should be implemented.

Simulation results for the boost operation can be seen in Fig.8. 4. The waveforms comply with the calculations.

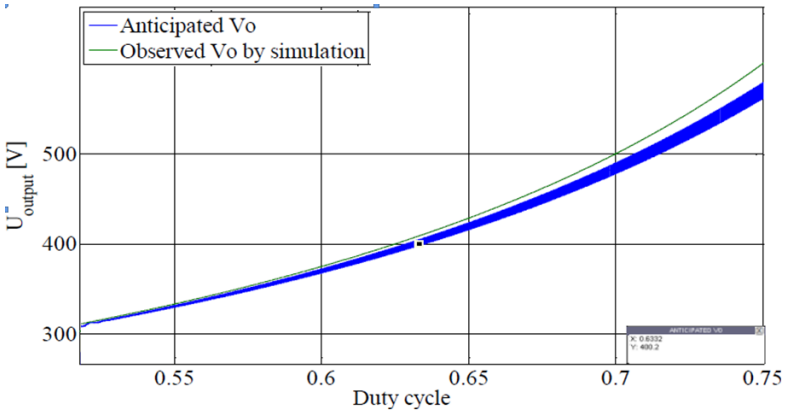


Fig.8. 3 Open loop performance of fullbridge boost DC-DC converter in a range of duty cycles ; The observed output voltage diverges from anticipated output voltage esp. At higher duty cycles.

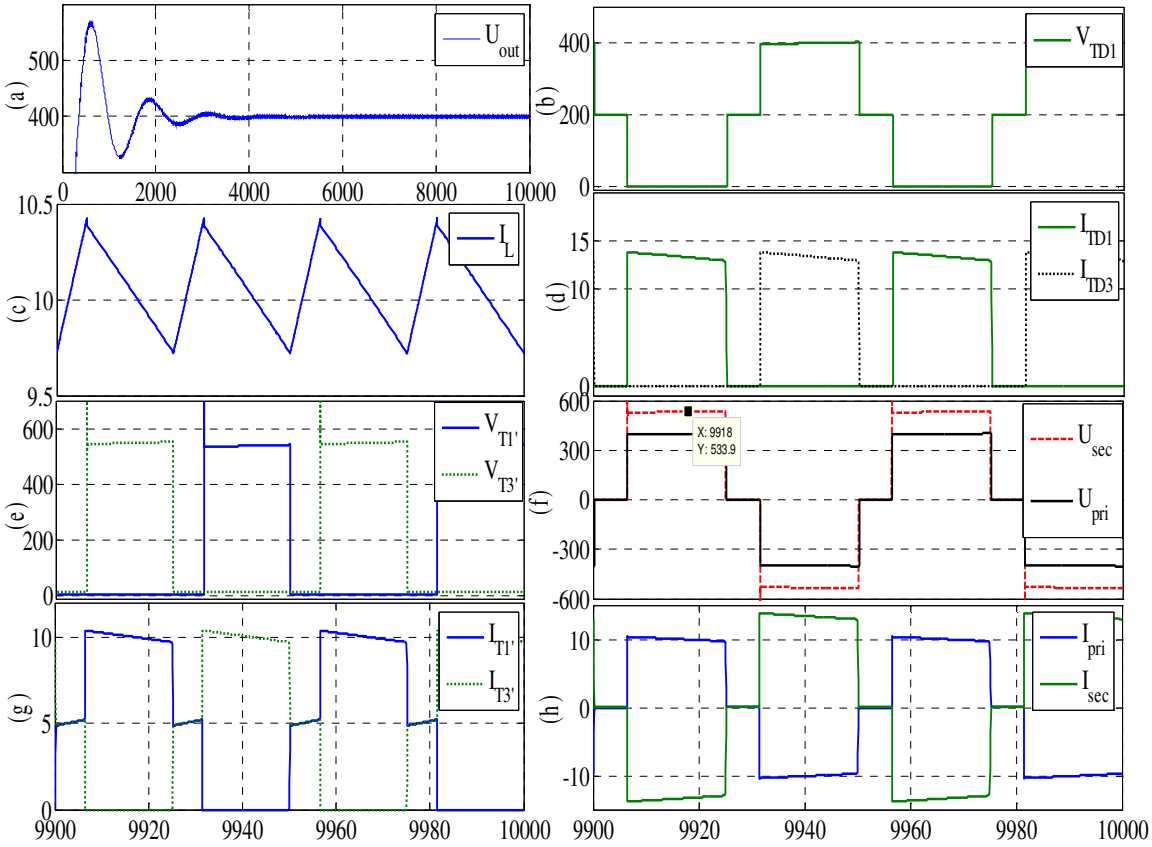


Fig.8. 4 Simulation result of the DC-DC converter and its waveforms, in boost operation mode (dicharging) when the battery voltage and output voltage are 400V. (input power from battery is around 3950 W) (resitive load) In absense of any compensation, large voltage overshoot is abserved.
(a) Capacitor /output voltage, (b) sec-side body diode voltage, (c) Inductor current (in pri-side), (d) Sec-side body diode current, (e) pri-side switch voltage, (f) Transformer pri & sec side voltages, (g) pri-side switch current, (h) Transformer pri & sec side currents (currents are in A and voltages are in V)

8.2 DC-DC fullbridge converter- Buck operation

In previous part we saw that although the plant (and buck converters in general) is stable, it cannot follow the desired output voltage very well. Fig.8. 2 and Fig.8. 3 show that the Steady State Error, ESS increases by increasing the output voltage.

8.2.1 Transfer function of DC-DC converters

NOTE!

For simplicity some assumptions have been made:

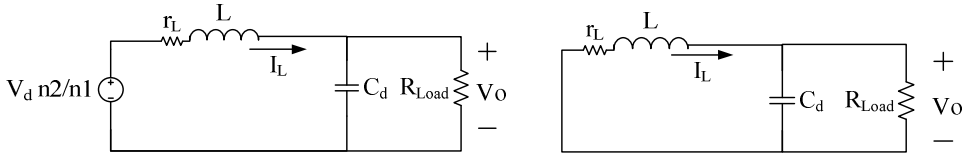
(1) Transformer leakage inductance and resistance, on-state resistance of switch and inductance and ESR of capacitance, all are neglected due to very small values. I.e. ESR will introduce a zero on transfer function but as it is very small, the place of the zero can be assumed to be in infinite and this does not have any obvious effect at practical gain.

(2) The battery load is assumed to be purely resistive.

In order to design a robust controller for the converter, the first step is to find the plant transfer function. There are several methods for doing this such as Mason method which is implemented in [31], but as we are only interested in $\tilde{v}_o(s)/\tilde{d}(s)$, the small signal method which was briefly explained in section 3.3.3 will be used.

In [4], a step by step procedure of obtaining the power stage and output filter transfer function of a DC-DC converter, $T_p(s) = \tilde{v}_d(s)/\tilde{d}(s)$ is explained. A common approach is:

1. For each state (switch on and switch off), find the corresponding circuit state and state-space matrix equations. The circuit state for switch on and off can be simplified to Fig.8. 5



A1) Each pair of switches on: 2DTs A2) All switches off: (1-2D)TS

Fig.8. 5 circuit state of (A1) switch-on, and (A2) switch-off

Based on Fig.8. 5.(A1) and by assuming (8.1) and (8.2) we can write (8.3) , (8.4):

$$x1 = i_L \tag{8.1}$$

$$x2 = v_c = V_0 \tag{8.2}$$

$$-\frac{V_d n2}{n1} + L_s\dot{x}1 + r_L x1 + R_{load}(x1 - C_d\dot{x}2) = 0 \tag{8.3}$$

$$-x2 + R_{load}(x1 - C_d\dot{x}2) = 0 \tag{8.4}$$

By rearranging the above equations in the state variable form as (8.5), for a half cycle the state matrix equations (8.6-8) will be obtained:

$$\left.\begin{aligned} \dot{x} &= Ax + Bv_d \\ V_0 &= Cx \end{aligned}\right\} \tag{8.5}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} \dot{x}1 \\ \dot{x}2 \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C_d} & -\frac{1}{C_d R_{load}} \end{bmatrix} \begin{bmatrix} x1 \\ x2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L}\frac{n2}{n1} \\ 0 \end{bmatrix} V_d \tag{8.6}$$

Where

$$A1 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C_d} & -\frac{1}{C_d R_{load}} \end{bmatrix} \; and \; B1 = \begin{bmatrix} \frac{1}{L}\frac{n2}{n1} \\ 0 \end{bmatrix}$$

As the only difference between Fig.8. 5.(A1) and Fig.8. 5.(A2) is the voltage source, we can directly write:

$$A2 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C_d} & -\frac{1}{C_d R_{load}} \end{bmatrix} \; and \; B2 = 0$$

For both circuits:

$$V_0 = R_{load}(x1 - C_d\dot{x}2) \;, \qquad V_0 = x2 \tag{8.7}$$

So we can write:

$$v_c = V_0 = [0 \quad 1]\begin{bmatrix} x1 \\ x2 \end{bmatrix} \tag{8.8}$$

Comparing (8.5) and (8.8) we can find $C1$ and $C2$

$$C1 = C2 = [0 \quad 1]$$

2. Average the state-variables in a period. To average description of the circuit over a switching period, the two state equations obtained above should be time weighted and averaged. The results can be seen in following equations:

$$\left.\begin{array}{c} A = A_1 2d + A_2(1-2d) => A = A1 \\ B = B_1 2d + B_2(1-2d) => B = 2d\,B1 \\ C = C_1 2d + C_2(1-2d) => C = C1 \end{array}\right\} \quad (8.9)$$

d: duty cycle.

So (8.5) can be written as follows:

$$\left.\begin{array}{c} \dot{x} = A_1 2d + A_2(1-2d) + 2dB1\,V_d \\ V_0 = C1\,x \end{array}\right\} \quad (8.10)$$

3. Introduce a small signal. **S**mall ac perturbations for state variables,$x1$ and $x2$, output voltage, V_0 and duty cycle, d are introduced. So each of these variables contain a DC value (capital letter) and ac value, (with "tilde" ~ above them).

$$\left.\begin{array}{c} x = X + \tilde{x} \\ v_c = V_c + \tilde{v_c} \\ d = D + \tilde{d} \end{array}\right\} \quad (8.11)$$

Using (8.10) and (8.11), the steady state equation (8.12-1,2) can be obtained by (below):

$$\left.\begin{array}{l} \dot{x} = \dot{X} + \dot{\tilde{x}} = AX + BV_d + A\tilde{x} + [(A1-A2)X + (B1-B2)V_d]\tilde{d} \\ \qquad = AX + BV_d + A\tilde{x} + [(B1)V_d]\tilde{d} \\ \\ \tilde{v_c} = C\tilde{x} + [(C1-C2)X]\tilde{d} = C\tilde{x} \end{array}\right\} \quad (8.12-1,2)$$

So we can divide $\dot{x}$ to DC and ac values as is expressed in (8.13) and (8.14):

$$\dot{X} = AX + BV_d \quad (8.13)$$

$$\tilde{\dot{x}} = A\tilde{x} + [(B1)V_d]\tilde{d} \quad (8.14)$$

But as X is a DC value, we can say:

$$0 = AX + BV_d \quad (8.15)$$

Using (8.15) and (8.5) the steady state dc transfer function is obtained:

$$\frac{V_0}{V_d} = -CA^{-1}B \quad (8.16)$$

By plugging the parameters in (8.16), (8.17) is obtained:

$$\frac{V_0}{V_d} = \frac{D}{1 + \frac{r_L}{R_{load}}}\,2\frac{N2}{N2} \quad (8.17)$$

(8.17) is more accurate than what was found earlier and can explain why there is a difference between our anticipated output voltage and what we observed.

4. Transform the equations in Laplace domain. By using Laplace transformation in (8.14) and with the help of (8.12-2) we can write:

$$\tilde{x}(s) = \frac{\tilde{v_c} - [(C1-C2)X]\tilde{d}}{C} = \frac{\tilde{v_c}}{C} = [sI - A]^{-1}[(A1-A2)X + (B1-B2)V_d]\tilde{d}\,(s) \quad (8.18)$$

where I is a unity matrix. So from (8.18) the desired transfer function $T_P(s)$ in general term can be obtained:

$$T_P(s) = \frac{\tilde{v}_d(s)}{\tilde{d}(s)} = C[sI - A]^{-1}[(A1-A2)X + (B1-B2)V_d] + (C1-C2)X \quad (8.19)$$

And for this case $T_P(s)$ would be:

$$T_P(s) = \frac{\tilde{v}_d(s)}{\tilde{d}(s)} = C[sI - A]^{-1}[B1\,V_d] \quad (8.20)$$

8.2.1.1 Power stage and PWM transfer function

Using $A = A1$, $[sI - A]^{-1}$ can be obtained. This term is especially important as it gives the places of poles.

$$[sI - A]^{-1} = \frac{1}{S^2 + S\left(\frac{1}{C_d R_{load}} + \frac{r_L}{L}\right) + \frac{1}{C_d L}} \begin{bmatrix} S + \frac{1}{C_d R_{load}} & -\frac{1}{L} \\ \frac{1}{C_d} & S + \frac{r_L}{L} \end{bmatrix} \tag{8.21}$$

Finally the power stage transfer function (including the output filter):

$$T_P(s) = \frac{\tilde{v}_d(s)}{\tilde{d}(s)} = \frac{\frac{n2}{n1} Vd}{L\, C_d} \frac{1}{S^2 + S\left(\frac{1}{C_d R_{load}} + \frac{r_L}{L}\right) + \frac{1}{C_d L}} \tag{8.22}$$

(8.22) can be written in the standard form of second order systems. Cut-off frequency, ωo and damping factor, ζ are defined as (8.23) and (8.24) respectively.

$$\omega o = \frac{1}{\sqrt{L\, C_d}} \tag{8.23}$$

$$\zeta = \frac{\frac{1}{C_d R_{load}} + \frac{r_L}{L}}{2\omega o} \tag{8.24}$$

So the standard form of $T_P(s)$ can be expressed as (8.25)

$$T_P(s) = \frac{\tilde{v}_d(s)}{\tilde{d}(s)} = \frac{n2}{n1} Vd \frac{\omega o^2}{S^2 + 2\,\zeta S + \omega o^2} \tag{8.25}$$

The theoretical transfer function of PWM is startlingly simple as it can be seen in (8.26). (While in practice, it always comes with some time delay) [4]

$$T_m(s) = \frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\widehat{V}_r} \tag{8.26}$$

Where:

$\widehat{V}_r$: Peak saw-teeth voltage; In this work: $\widehat{V}_r = 1$

$\tilde{v}_c(s)$: Control voltage (which is always $0 < \tilde{v}_c(s) < \widehat{V}_r$

$T_m(s)$: The transfer function of PWM modulator.

The open loop block diagram of the system, without compensator ($T_1(s)$) can be seen in Fig.8. 6.

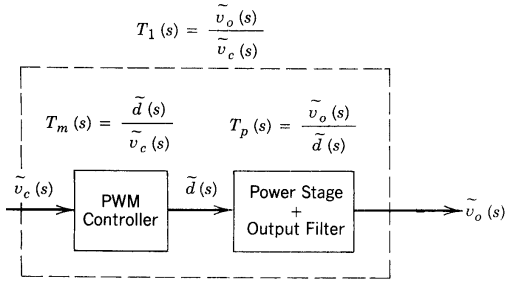


Fig.8. 6 The open loop block diagram of the DC-DC converter

8.2.2 Open loop analysis of the system

8.2.2.1 Some basic concepts[1]

Open loop Transfer function, $T_{OL}(s)$ is defined as follows:

[1] For more details refer to the corresponding literatures.

$$T_{OL}(s) = T_C(s)\,T1(s) = T_C(s)T_P(s)T_m(s)$$

Closed loop transfer function, $T_{CL}(s)$ based on Fig8. 7 would be

$$T_{CL}(s) = \frac{T_{OL}(s)}{1 + T_{OL(s)}}$$

Where $T_C(s)$ is the amplifier transfer function.

Cross over Frequency is the frequency in which $|Tol(s)| = 1$, (the crossover which magnitude of bode diagram meets frequency axis). This frequency should be a fraction of switching frequency (between 1/5 to 1/10 of switching frequency is recommended) [31] but also not so low to slow the system response.

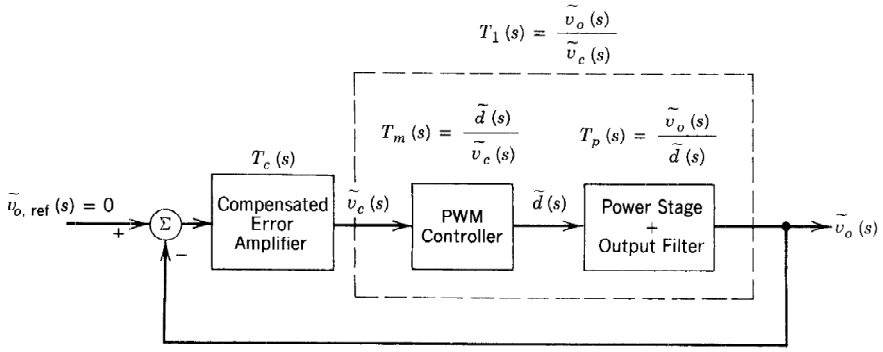


Fig.8. 7 Closed loop block diagram

Bandwidth is related to the cross over frequency. It is inversely related to the transient response time.

Phase margin (PM) is the difference between the phase of an output signal and 180°, as a function of frequency. Positive PM is a "safety margin" that ensures proper operation of an amplifier [32]. PM is related to the damping of the system. Low PM causes oscillatory transient response. Generally, PM should be higher than 45 to be immune to system turbulences.

Gain Margin: Gain is changed according to the variation of circuit components and it shows the robustness against gain variations.

8.2.2.2 Observations and objectives

By plugging the corresponding values to the transfer function obtained in the previous part, the open-loop transfer function can be obtained by (8.27):

$$T1(s) = T_P(s)T_m(s) = \frac{\tilde{v}_0(s)}{\tilde{v}_c(s)} = \frac{1.44e10}{S^2 + 4030\,S\, + 2.71e7}$$
$$= \frac{1.44e10}{(S\, + 2013 - 4800j)(S + 2013 + 4800j)} \qquad (8.27)$$

Two complex poles mean a high oscillation in the step response. This can be seen in Fig.8.8(down). The bode diagram of the open loop and closed loop system (without any compensator) can be seen in Fig.8. 8. Based on Figs.8. 8 and Fig.8. 9, we can observe that:

Observations:

- Very low phase margin (1.93°)

- Magnitude of the closed loop bode diagram is much higher than 1 dB, esp. at switching frequency, while it shouldn't. (rectangular area should be eliminated)

- Very high oscillation of the closed in the step response.
- High open loop overshoot (~35% overshoot)

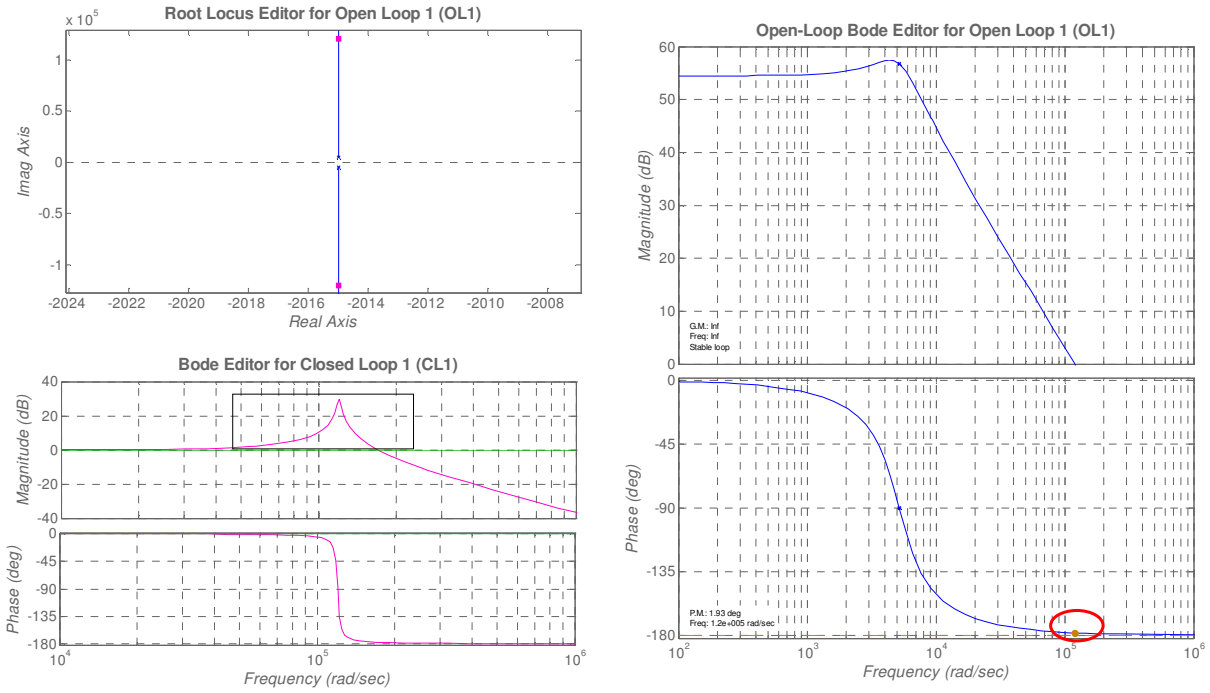


Fig.8. 8 Top left: Root locus plot of the plant when K=1, The red squares are the closed-loop poles; x indicates open loop poles. Right) Open loop bode diagram. $P.M = 1.9°$, $w_{cross} = 1.2e5\ rad/sec$. Down left) closed loop bode diagram of the system.

The open loop gain at relatively low frequencies is $Vd\ n2/n1$. So the final value would be 533.3. (i.e. when $D = 0.5$, the frequency in theory would be zero). This proves that the calculated transfer function is correct. I.e. at $D = 0.375$ the output voltage would be $V_o = 2D\ Vd.n2/n1 = 0.375 \times 2 \times 533 = 400$ which is what we expected to have for such duty cycle.

By using a closed loop system, the gain is reduced to unity, (refer to closed loop transfer function equation)

We desire to have a system with following specifications:

Objectives:

+ Phase margin higher than 60°
+ Gain margin higher than $20dB$
+ Over shoot less than 5%, (high overshoot is not suitable for batteries)
+ Steady state error less than 1%
+ Appropriate bandwidth

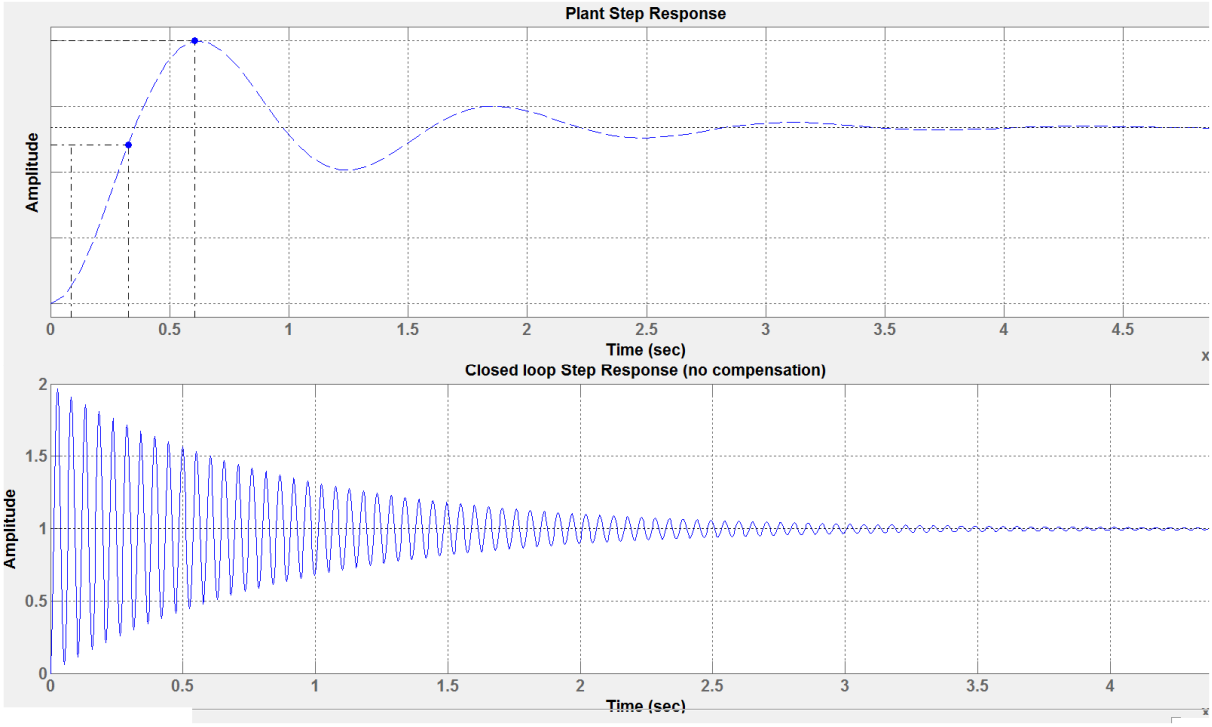


Fig.8. 9 The step response of the transfer function of the full-bridge DC-DC converter, $T1(s)$ when $T_C = T_m(s) = 1$

8.2.3 Compensator design

Using a proportional compensator can improve the system performance significantly but it is not possible to satisfy all the objectives with only a proportional gain.

A very poor phase margin shows that the phase should be boosted preferably more than 150°

This "phase bump" can be achieved by "type 3 compensators" [33]. The method we design our compensator is called K-factor method which is widely used in industry.

8.2.3.1 Type 3 amplifiers

A Type 3 amplifier has a pole at the origin, but in addition to the integrator, it has two zero-pole pairs, both poles and zeros are coincident. The pole in the origin maximizes the gain at frequencies below the crossover frequency (to minimize the steady state error in power supply output) and minimizes it above crossover frequency (this doesn't allow the high frequency noise and switching to pass). So the frequency of zeros should be before the cross over frequency to create a boost in phase and poles should be located after the crossover to reduce the gain immediately. This means that the compensator is a LEAD type. Each pole-zero pair in theory can boost the phase up to 90 degrees (if they are located far from each other) but in practice not more than 75 can be expected to be boosted. With type 3 amplifier, in theory the phase boost of 180 is possible. The voltage transfer function of type 3 amplifiers can be seen below:

$$T_C(S) = K\frac{1}{S}\left(\frac{S+Z}{S+P}\right)^2 \tag{8.28}$$

The bode diagram of the amplifier we used can be seen in Fig.8. 10.

8.2.3.2 Venable K-Factor Calculation

The preliminary steps to design a compensator are well explained in reference [33]. We briefly mention and implement them here:

1. Make Bode Plots of the Modulator, $T1(S)$

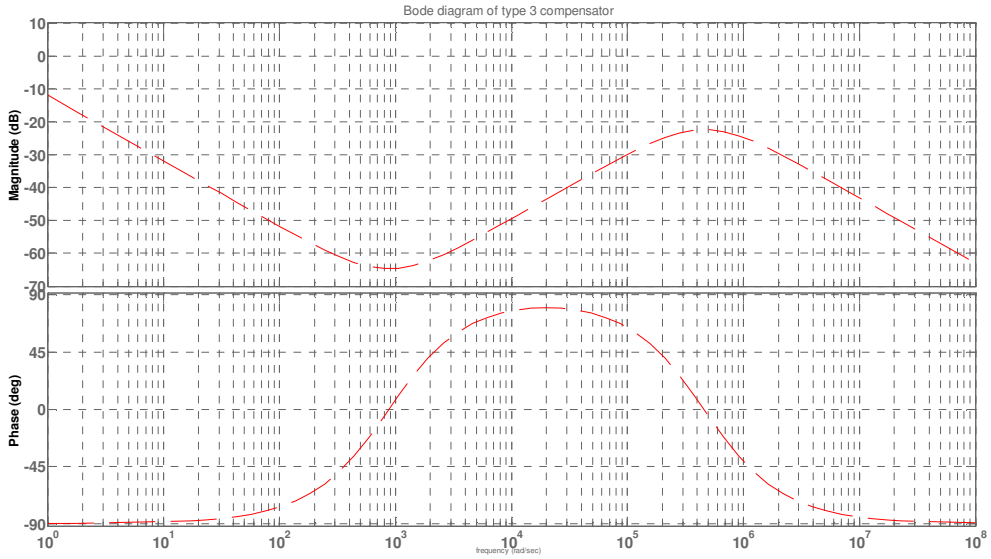


Fig.8. 10 The bode diagram of the type 3 amplifier as a function of frequency (rad/sec), based on the final values found and plugged in (8.36)

2. Choose a Cross-over Frequency: By trial and error it is found that the best cross over frequency is $\omega_{cross} = 20000\, rad/sec$. This is well below the angular switching frequency $\omega_s = 2\pi f_s = 1.25e5\, rad/sec$ but still high enough.

3. Choose the Desired Phase Margin. The desired phase margin is set to be $PM = 100°$

4. Calculate the Required Phase Boost: The Phase Boost, $Ph.B$ can be found by (8.29)

$$Ph.B = PM - P - 90° \tag{8.29}$$

Where:

PM: desired phase margin

P: Phase margin of modulator T1(s) which based on Fig.8. 8 is -179°

So the required phase boost would be:

$$Ph.B = 100 - (-179) - 90 = 189°$$

5. Find the Venable K-factor: The K factor for type 3 compensators can be calculated by (8.30)

$$K = tan^2(\frac{ph.B}{4} + 45) \tag{8.30}$$

So, $K = 625$, $(\sqrt{K} = 25)$

6. Place the zeros and poles around the crossover frequency: By (8.31) & (8.32) each zero-pole pair is placed around the crossover frequency. This can also be seen in Fig.8.11

$$\omega_z = \frac{\omega_{cross}}{\sqrt{K}} \tag{8.31}$$

$$\omega_z = \frac{20000}{25} = 800\, rad/sec$$

$$\omega_p = \omega_{cross}\sqrt{K} \tag{8.32}$$

$$\omega_p = 20000 \times 25 = 5e5\, rad/sec$$

$$\omega_{cross} = \sqrt{\omega_p \omega_z} \;\; = 20000\, rad/\,sec \tag{8.33}$$

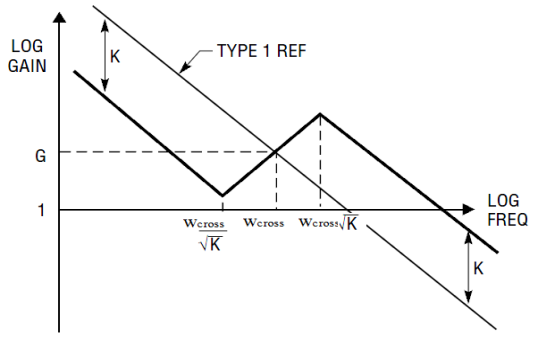


Fig.8. 11 The location of zero–pole pairs, as well as cross over frequency in type 3 amplifier

7. Determine the required amplifier gain at cross-over.

If the gain is expressed in dB, then the amplifier gain should be simply the negative of the modulator gain. In the other words, the open loop gain in dB should be zero at cross over frequency. This is expressed by (8.34) and (8.35)

$$|T_C(j\omega)|\ \Big|_{\omega_{cross}} = \frac{1}{|T1(j\omega)|\Big|_{\omega_{cross}}} => \tag{8.34}$$

$$Log|T_{ol}(j\omega)|\Big|_{\omega_{cross}} = Log|T_C(j\omega)|\Big|_{\omega_{cross}} + Log|T1(j\omega)|\Big|_{\omega_{cross}} = 0 \tag{8.35}$$

By the help of SISOTOOL toolbox in MATLAB different amplifier gains and pole-zero locations around the designed values were examined and finally the one which was fast enough and didn't have any overshoot was selected. The controller parameters and transfer function can be seen in (8.36) (fig.8. 10)

$$T_C(S) = 7e4\ \frac{1}{S}\ \frac{(S+873)^2}{(S+4.58e5)^2} \tag{8.36}$$

As it can be seen, the location of poles and zeros are close to the values found earlier. But cross over frequency (by changing the gain) is now $\omega_{cross} = 8000$

In another attempt, cross over was set to $\omega_{cross} = 8000$ and based on this value, the compensator was designed but in the SIMULINK, a very slow response proved that the location of zeros and poles should be as it was found in (8.36).

This amplifier can be implemented by an op-amp (assumed to be ideal) and sets of resistances and capacitances as it can be seen in Fig.8. 12. The corresponding parameters in Fig.8. 12 can be found by (8.37) to (8.41) [33] :

$$C2 = \frac{1}{\omega_{cross}\ G\ R1}\ [Farad] \tag{8.37}$$

$$C1 = C2(K-1)\ [Farad] \tag{8.38}$$

$$R2 = \frac{\sqrt{K}}{\omega_{cross}\ C1}\ [ohm] \tag{8.39}$$

$$R3 = \frac{R1}{K-1}\ [ohm] \tag{8.40}$$

$$C3 = \frac{1}{\omega_{cross}\ \sqrt{K}\ R3}\ [Farad] \tag{8.41}$$

Where:

ω_{cross}: chosen cross-over frequency in rad/sec
G: Amplifier gain at cross-over (a dimensionless ratio (not dB)) (based on Fig.8. 10, this value is $-50 = 20\log G \Rightarrow G = 0.0032$
K: K factor (dimensionless ratio)
R1: amplifier input resistance, it is inverse proportion to the current. All componetes scale in direct proportion to R1.

For the initial guess we set $R1 = 1000\,ohm.$ By plugging the corresponding values to (8.37) to (8.41) the suitable values of resitances and capacitances can be obtained:

$$C2 = \frac{1}{8000 * 0.0032 * 1000} = 3.9e-5\,, \qquad C1 = 0.024\,, \qquad R2 = 0.1302\,, \qquad R3 = 1.6,$$
$$C3 = 3.12e-6$$

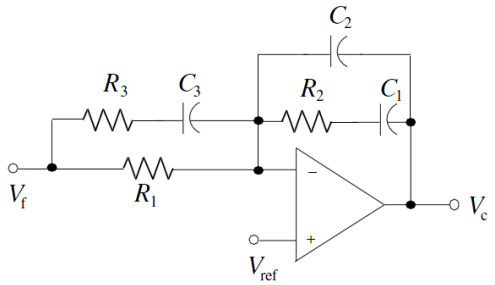


Fig.8. 12 Electrical implementation of type 3 amplifier

The Bode diagram and Root locus of T_{oL} as well as the bode diagram of T_{CL} in presence of the amplifier can be seen in Fig.8. 13.

From Bode diagram of open loop it can be seen that the $P.M$ and $G.M$ are as expected ($P.M = 103\,, G.M = 45.7\,dB$). From the bode diagram of the closed loop it can be seen than the closed loop gain before the crossover frequency (which due to the reduction of the over shoot is set to be $8000\ rad/sec$) is around or less than zero and unlike Fig.8. 8 we don't have any gain bump. From Root locus diagram in Fig.8. 8, we can see that there is no more complex closed loop poles.

8.2.4 Voltage controller response in presence of non ideal DC-DC converter

As it was observed in Fig.8. 2, a steady state error was inevitable in open loop control. The main objective of the control system is to obtain a correct duty cycle to compensate this voltage error. As it was discussed before:

$$d = D + \tilde{d}$$
$$D = \frac{V_{ref}}{2\,n\,V_d}$$

$\tilde{d}$ should be generated by the output of error amplifier and D is the direct duty cycle. These two values will be added and will generate the corrected duty cycle, d to be compared with a saw teeth wave (with amplitude of unity.)
Fig.8. 14 shows the voltage control method and block diagrams.

In order to observe the system behavior, at $t = 300\,uS$, a step with magnitude of $300V$, and at $t = 3600us$ another step with the total magnitude of $100V$ are applied. The system response can be seen in Fig.8. 15. From Fig.8. 15 it can be said that there is no overshoot. Other specifications are $tr = ts = 700\,us,\ ESS = 0$

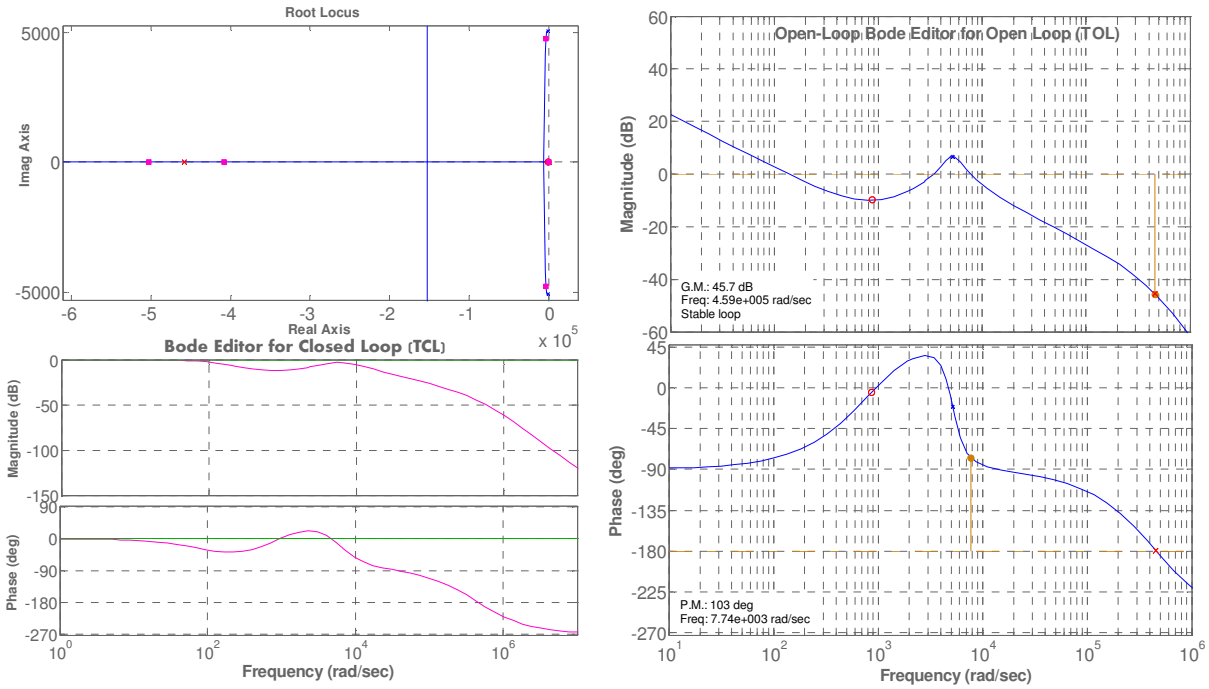


Fig.8. 13 top left: Root locus plot of the system with the compensater, The red squares are the closed-loop poles; x indicates open loop poles. Right) Open loop bode diagram. $P.M = 103°$, $G.M = 45.7dB, w_{cross} = 7.7e3\ rad/sec$ Down left) closed loop bode diagram of the system.

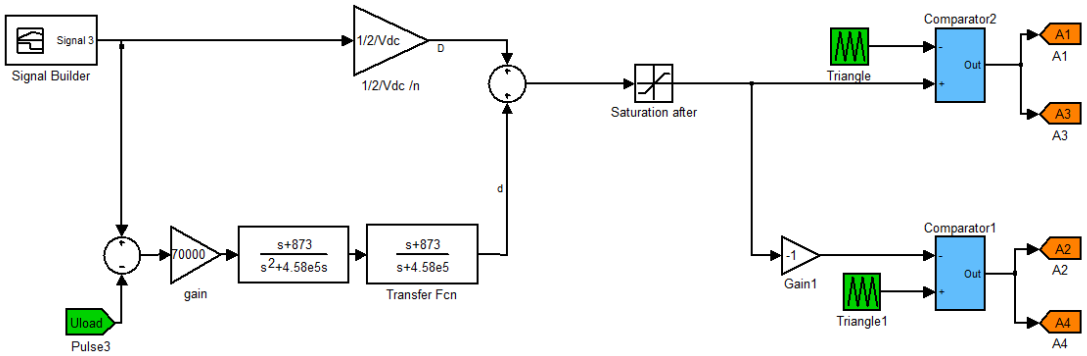


Fig.8. 14 The block diagrm and implementation of the type 3 compensator for the DC-DC converter

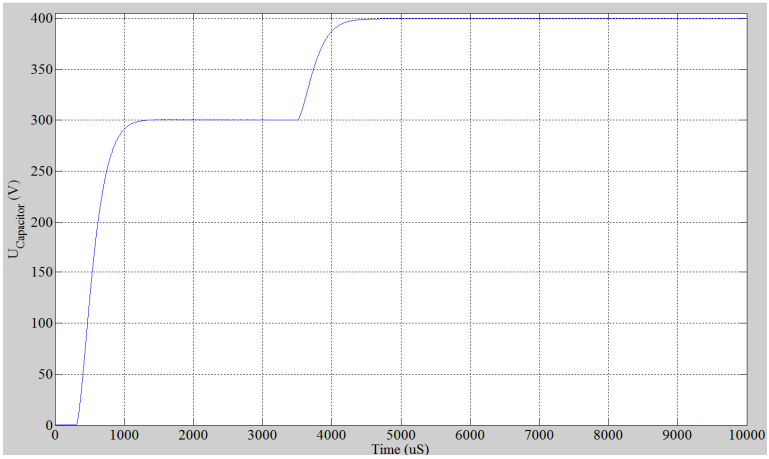


Fig.8. 15 Output voltage Step response of the DC-DC converter, at $t = 300\ us$ a step of 300 V is applied. At $t = 3700\ us$, another step, with amplitude of 100V is applied. No overshoot can be observed.

9 ac<->DC bridge: Control and simulation

9.1 ac -> DC bridge rectifier (Active PFC)

9.1.1 Control design and nonlinearity

The principle of operation of a power frequency and a switch mode rectifier was discussed in section 3.3.2. For the bidirectional onboard charger, the switch mode rectifier, as it can be seen in Fig.9. 1(A) is chosen. In section 3.3.3 it was discussed that as the state matrix of the converter is dynamic, linear control theories should be slightly modified.

The equation circuit of the switch frequency bridge rectifier can be seen in Fig.9. 1(B). Based on that we can write:

$$V_S = V_L + V_r = L\frac{di_s}{dt} + V_r \Rightarrow V_r = V_S - L\frac{di_s}{dt} \quad (9.1)$$

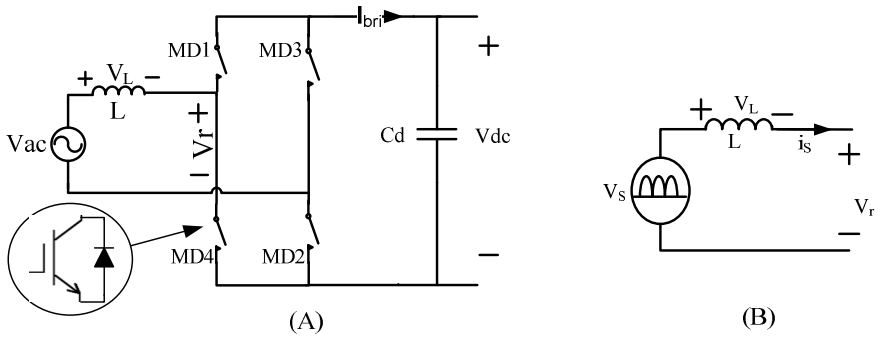


Fig.9. 1 (A) ac -> DC bridge rectifier (B) The equation circuit of the switch frequency bridge rectifier

By the help of the equation circuit, the rectifier block diagram can be found out as it can be seen in Fig.9. 2. $f(d)$ is the transfer function of the switching stage that its input is ac inductor current and the output is bridge current (ref to fig.9. 1(A)) and this is the nonlinear part that we should deal with. If we can linearize the topology in a way that the controller does not see the nonlinearity (by cancelling out the nonlinear part) the problem is solved. The output of the current controller produces only the inductor voltage drop required to maintain the sinusoidal source current [34]. So the output of the current controller should be linearized in order that the output current of the converter becomes a first order linear system. This can be done as follows:

The input voltage of the rectifier V_r can be expressed by the duty cycle and the output voltage, V_{dc} (refer to section 3.3.2). If $MD2$ & $MD4$ are off, $V_r = V_d$ (body diodes conduct) and if $MD2$&$MD4$ are turned on, $V_r = 0$. So we can write:

$$V_r = (1-d)V_d \Rightarrow$$
$$d = 1 - \frac{Vr}{V_{dc}} \quad (9.2)$$

By (9.2), linearization is possible. Now we can apply linear control theory (with some additional parts for cancelling the nonlinear part). This can be seen in Fig.9. 2

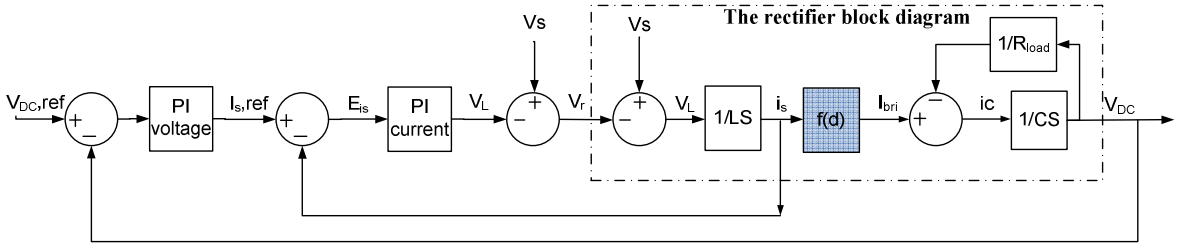


Fig.9. 2 The rectifer block diagram and the linear control system by assuming linear transfer function of rectifer

The controller is divided in 3 parts: the current controller, the voltage controller; and the linearizer. The controller is cascaded suggesting that the inner controller, being a current controller, should have a higher bandwidth than outer controller, which is a voltage controller. In this manner, it can be assumed that the inner control loop is ideal and the outer control loop cannot see it. (The outer control loop sees the gain of inner loop as 1)

The output of the current controller produces the inductor voltage drop to maintain the sinusoidal source current. From the output of the current controller, by utilizing (9.1) and (9.2) the linearizer can be formed. The output of linearizer is compared with a saw teeth career waveform and PWM switching pattern is generated.

The voltage controller input is the output voltage error (the difference between the reference and the measurement) and the output would be inductor current reference which should be then becomes half sine wave in phase with the voltage, and the reference inductor current should be compared with the measured inductor current to be fed to the input of the current controller.

9.1.1.1 PI current controller parameters

A rule of thumb suggests that:

$$\omega_s \gg a_{ci} \gg a_{cv} \tag{9.3}$$

Where:

ω_s: Switching angular frequency
a_{ci}: Current controller bandwidth
a_{cv}: Voltage controller bandwidth

From (9.1) it can be said that the transfer function of the input current over the bridge voltage for the converter,$T_{C,i}$ is in order of one as it can also be seen in Fig.9. 2. So a PI controller works well. With assuming that the linearizer can linearize the system, we make the closed loop system to be a first order low-pass filter. Then the PI controller transfer function, T_{cc} would be:

$$T_{C,i} = \frac{T_{cc}\cdot\frac{1}{L.S}}{1 + T_{cc}\cdot\frac{1}{L.S}} = \frac{a_{ci}/S}{1 + a_{ci}/S} \tag{9.4}$$

$$T_{cc} = K_{pc} + \frac{K_{ic}}{S} = a_{ci}L \tag{9.5}$$

Where

K_{pc}, K_{ic} : proportional and integral coefficient respectively.
$T_{C,i}$: Current closed loop transfer function
L: ac inductor value [H] like the DC-DC converter inductance is chosen to be 0.003 H
a_{ci}: Current controller bandwidth

Current controller bandwidth, a_{ci} by trial and error is chosen to be $a_{ci} = \frac{\omega_s}{50} = 2512$, so $K_{pc} = 7.5398$. Also K_{ic} is introduced which can improve the system speed. (Although too high K_{ic} can cause oscillation and even instability.)

9.1.1.2 PI voltage controller parameters

As the voltage controller bandwidth is much smaller than the current closed loop first order system, it cannot see it (much slower). From Fig.9. 2 it can be seen that the output voltage (V_{DC}) to the output current (I_{bri}) transfer function,$T_{C,v}$ is in order of one. If the voltage controller is slow enough (with smaller bandwidth than the current controller) it can be assumed that the closed loop system should be a first order low-pass filter with bandwidth of a_{cv}. Then the PI voltage controller transfer function, T_{vc} would be as (9.7).

$$T_{C,v} = \frac{T_{vc}\,\frac{R_{load}}{1+R_{load}C\,S}}{1+T_{vc}\,\frac{R_{load}}{1+R_{load}C\,S}} = \frac{a_{cv}/S}{1+a_{cv}/S} \tag{9.6}$$

$$T_{vc}\frac{R_{load}}{1+R_{load}C\,S} = \frac{a_{cv}}{S} =>$$

$$T_{vc} = a_{cv}C\ + \frac{a_{cv}}{R_{load}}\frac{1}{s} = K_{pv} + \frac{K_{iv}}{S} \tag{9.7}$$

Where

K_{pv}, K_{iv} : proportional and integral coefficient respectively.
$T_{C,v}$: Voltage closed loop transfer function
R_{load}: the load is assumed to be purely resistive. $R_{load} = 40$
C_d: output capacitor

By trial and error, the best value for a_{cv} is found to be 39. Thus $K_{pv} = a_{cv}\,C_d = 39 \times 1.9e-3 = 0.0754$. $K_{iv} = \frac{a_{cv}}{R_{load}} = \frac{39}{39} = 1$ which works well, but at K_{iv}=9, the response time will be improved, so the final value for K_{iv} is 9.

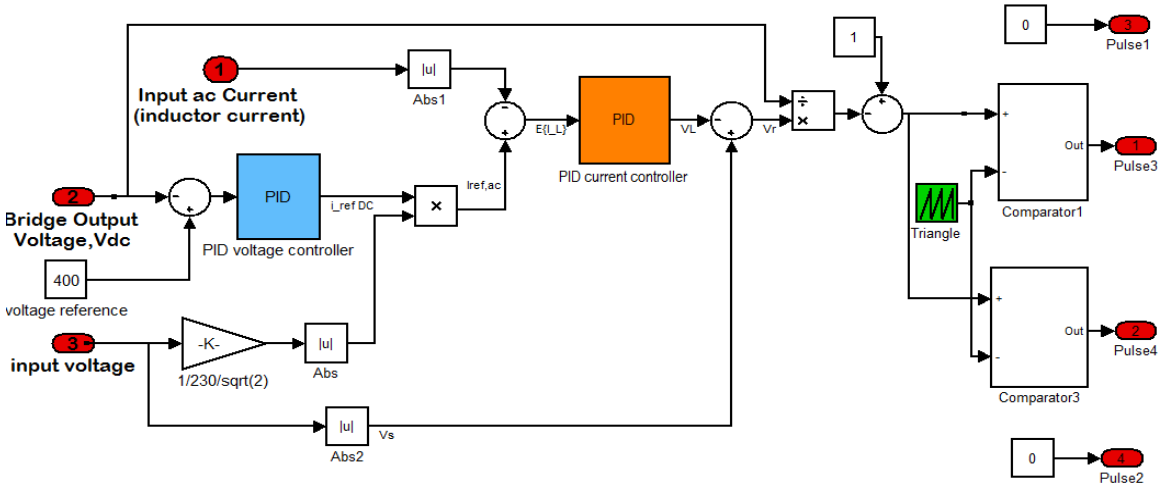


Fig.9. 3 The block diagrm of the cascaded controller of the rectifier, the inner loop: PI current contoller, outer: PI voltage controller

9.1.2 Losses evaluation of rectifier

Bu investigating IGBTs on table A-5 in Appendix A, it can be realized that IGBT *BSM50GB60DLC* has the lowest conduction losses. To find the total losses of the fullbridge

rectifier, the easiest way is to subtract the input and output power, the result would show the total rectifier losses. The losses at two different output voltage can be seen in table.9. 1

Table.9. 1 Total losses of the rectifier based on different output voltage and constant input voltage

Output power at 400V (Output power: 3800 W)	Input power: 3890 W Losses:90 W Efficiency: 97.7%
Output power at 450V (Output power: 3800 W)	Input power: 3900 W Losses:100 W Efficiency: 97.4%

This suggests that the rectifier total losses, including the resistive losses of the inductor, are around 100 W which means the rectifier efficiency is more than 97% when the output power is 3800W.

9.1.3 The results and performance

The RMS value of the fundamental inductor current is found to be $i_{s,1_{rms}} = 24.83\ A$

Total Harmonic Distortion, THD is found to be 2.5%. By knowing the THD and with the help of (9.8) Distortion Power Factor, $DiPF$ can be found as below:

$$DiPF = \frac{1}{\sqrt{1+THD^2}} = \frac{i_{1,rms}}{i_{rms}} \tag{9.8}$$

$$DiPF = \frac{1}{\sqrt{1+0.025^2}} = 0.9997$$

This definition of $DiPF$ assumes that the voltage stays undistorted (sinusoidal, without harmonics). This simplification is often a good approximation in practice too.

With $\varphi = \left(\measuredangle \mathrm{V_s} - \measuredangle \mathrm{i_{s(1)}} \right) = 5.4$, the Displacement Power Factor, $DpPF$, which is the cosine of the angular displacement of the input current waveform from the grid voltage waveform can be calculated as expressed below:

$$DpPF = Cos\ \varphi = Cos\left(\measuredangle V_s - \measuredangle i_{s(1)} \right) = 0.995$$

$DpPF$ is often incorrectly referred to PF. As power quality plays more of a role in power engineering, total power factor, PF will become more common. The PF can be found by (9.9)

$$PF = DpPF \times DiPF \tag{9.9}$$

$$PF = 0.9997 \times 0.9955 = 0.995$$

This PF is well above most standards. But we should also take a look on harmonics magnitudes and check if the rectifier can beat the standards. IEC 61000-3-2, being used wildly for household appliances, is the best choice here. This standard assesses and sets the limit for equipment that draws input current ≤ 16A per phase. The onboard charger is classified as class-A household appliances. Allowable maximum harmonic currents under IEC 61000-3-2 class-A regulations are shown in Table.9. 2 [35]. In this table, the rectifier current harmonic order is also presented.

Table.9. 2 harmonic currents limits of class A equations under IEC 61000-3-2

	H order	Max. permissible harmonic current [A]	Obtained
Odd Harmonics	3	2.3	1.19
	5	1.14	0.485
	7	0.77	0.42

	9	0.4	0.36
	11	0.33	0.30
	n<39	0.15 * 15/n	
Even Harmonics	2	1.08	0.004
	4	0.43	~0
	6	0.3	~0
	n<40	0.23*8/n	

In comply with the standard, the waveforms also show the excellent behavior of the converter. This can b seen in Fig.9. 4. As discussed in chapter 18 of [4], the capacitor (and output) voltage ripple is inevitable and its frequency is twice the line frequency. The magnitude of the output ripple can be reduced to the desired value by increasing the output capacitor. Fig.9. 4 shows that the selected capacitor can reduce the ripple voltage to less than 5% (18V ripple) which satisfies the criteria defined in Table.7.1. Maximum input current ripple is around 4% (less than 1A) as it can be seen below.

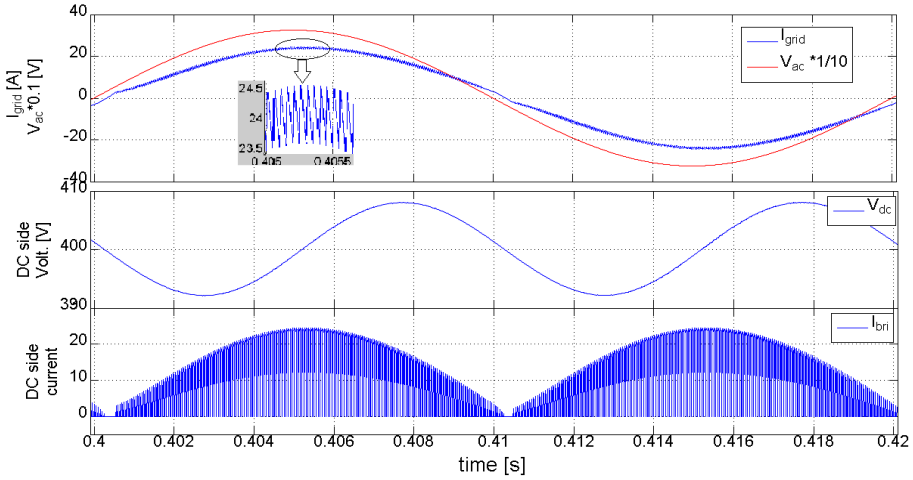


Fig.9. 4 (Up) the input current and grid voltage, (middle) output DC current, (down) Bridge current in DC side, (ref Fig.9. 1.(A)

9.2 DC->ac bridge inverter

The principle of operation of a switch mode full bridge inverter is discussed in [4]. From [4] and [36] it can be realized that unipolar switching pattern has several advantages over bipolar switching mode. (I.e. lower harmonics, lower current ripple in zero crossing, lower switching losses and half voltage jumps). Thus we also use PWM unipolar switching pattern. Fig.9 .5 shows the inverter topology.

In unipolar switching pattern, two opposite sine waves are compared with a saw teeth carrier wave and each switch will be turned on and off separately (in contrast with bipolar switching that switches are turned on and off in pairs). As a consequence, in unipolar PWM, anti-parallel diodes also conduct (in contrast with bipolar switching)

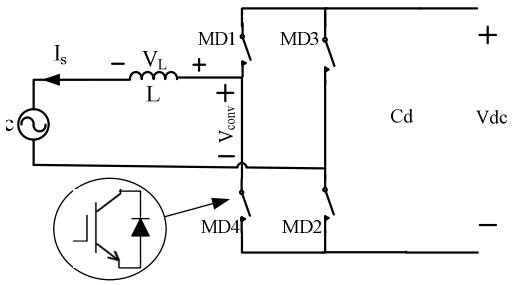


Fig.9. 5 the topology of the inverter in discharing more, when the power is transmitted from DC side to the grid

9.2.1 Controller design: PI current controller

Similar to ac-> DC rectifier, an inverter also has a nonlinear transfer function. To design an inverter controller, there are different control methods such as *d-q*, online trained neural network controller, Predictive Control Method, hysteresis Control Method and *PID* controller [36], [37]. As the inverter is a grid- tide inverter, meaning that the ac side voltage is dictated by the grid, a PI controller can work perfectly and there is no need of voltage controller. The benefits of PI controller are its robustness, simplicity, inexpensiveness and lightness which all are important factors for an HEV onboard charger [37]. The main drawback is lack of reactive power controllability which is not the case as the HEV owners' willing to deliver reactive power to the grid (which ages the car battery without any tangible benefit) is a question.

The steps of the design of PI controller were discussed earlier in this chapter. Here we just set the parameters. As it was seen in (9.3), a rule of thumb suggests that the current controller bandwidth should be smaller than the switching frequency:

$$\omega_s \gg a_{ci}$$

From (9.5) , we saw that a PI controller transfer function, T_{cc} would be:

$$T_{cc} = K_{pc} + \frac{K_{ic}}{S} = a_{ci} L$$

Although the PI current controller parameters of the rectifier can work here, but by trial and error it is found out that $K_{pc} = 37.5$ results in better waveforms (Proportional coefficient of PI current controller of the rectifier was $K_{pc} = 7.5$). K_{ic} for both of inverter and rectifier remains the same.

Based on the desired output power, the reference peak current is determined. Later on we will see that when the battery input power to the onboard charger is 4kW, the losses of the charger is around 250W, suggesting that the onboard charger output power is around $P_{out} = 3750W$

$$\widehat{I_{s_{ref}}} = \frac{P_{out}\sqrt{2}}{V_s} = \frac{3750\sqrt{2}}{230} = 23A$$

Fig.9. 6 shows the block diagram of the controller, including the PWM switching pattern generator of the inverter.

Referring Fig.9. 7, it can be said that the output current is quite sinusoidal. The ripple current is only $0.15A$, while for rectification, it was around $1A$. This shows that the rectifier requires higher value of the inductance and if the inductor is designed for the rectifier, it will work well for the inverter. The measurements verify that the inductor value is calculated correctly.

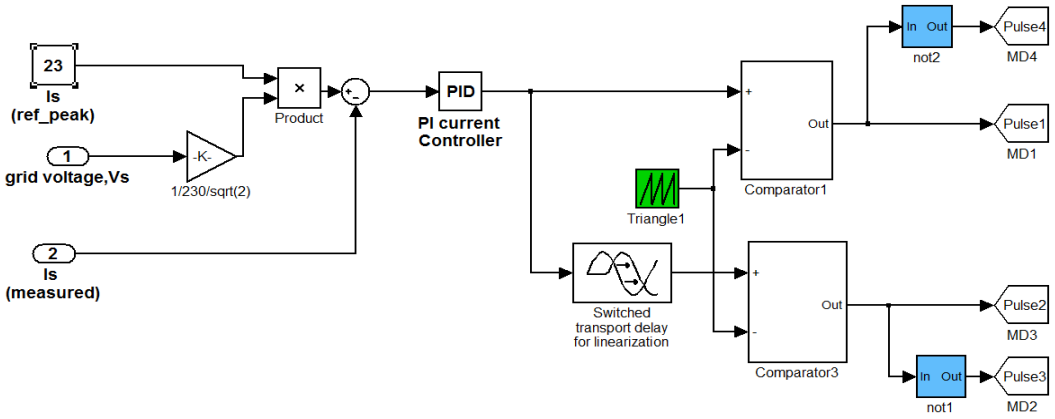


Fig.9. 6 The block diagram of the controller including PWM switching pattern generator of the inverter.

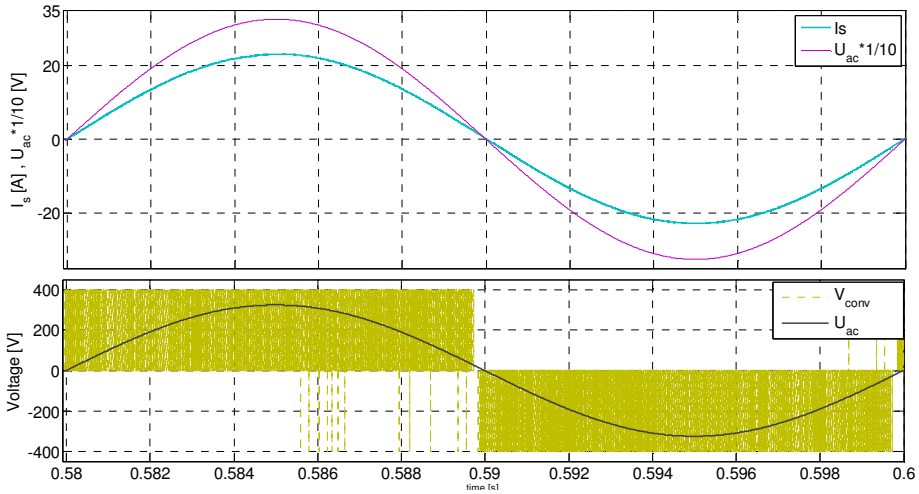


Fig.9. 7 (up) Output current $i_s$and grid voltage. I_s is sinosidal, but 180 ° behind the voltage but for comparing it is multiplied by -1 here, also grid voltage is 0.1 of its real value. (down) PWM unipolar switching patern

9.2.2 The performance and losses evaluation of inverter

The RMS value of fundamental inductor current is found to be $I_{s,1_{rms}} = 22.8\,A$. Total Harmonic Distortion, THD is found to be 0.6%. With the help (9.8), $DiPF$ can be found as below:

$$DiPF = \frac{1}{\sqrt{1+THD^2}} = \frac{i_{1,rms}}{i_{rms}} = \frac{1}{\sqrt{1+0.006^2}} = 0.999$$

With $\varphi = \left(\measuredangle \mathrm{V_s} - \measuredangle \mathrm{i_{s(1)}} \right) \approx 0$, the Displacement Power Factor, $DpPF$, can be calculated:

$$DpPF = Cos\ \varphi \approx 1$$

The PF can be found by (9.9):

$$PF = DpPF \times DiPF = 0.999 \times 1 = 0.999 \approx 1$$

To find the losses of the inverter, input and output power is read. The difference between these two quantities represents the total losses of inverter.

With the input power of $P_{ac} = 3766W$ (the power injected to the grid) and inverter input power of $P_{DC} = 3708\,W$ (in DC side), the total losses, including switch losses and inductor losses, would be 57.3 W, which corresponds to the efficiency of 98% in the inverter.

10 Conclusion and future work

10.1 Conclusion and the charger performance

The objectives of the thesis and the outcome will be discussed in the last chapter.

Firstly, the feasibility of the scheme was a question. The simulations showed that the charger can work in both directions.

The simulations approve the back to back operation of the rectifier and DC-DC converter. The waveforms are more or less the same as before, for each separate module.

The charger performance is highlighted below:

1. PF and THD in charging and discharging mode:

Charging mode (rectification): Current THD of 2.5% and PF of 0.99

Discharging mode (inversion): Current THD of 0.5 % and PF of ~1

2. Efficiency of the onboard charger, in both directions is between 93.5% and 94.8% depending on the battery voltage. This can be seen in Fig.10. 1

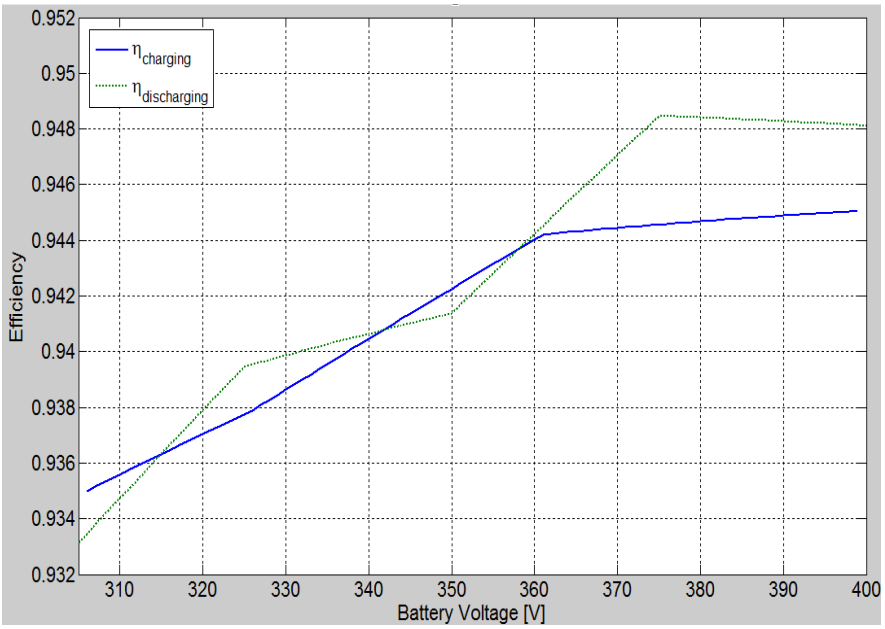


Fig.10. 1 The total efficiency of the onboard charger in both directions, depending on the battery voltage

3. The DC-DC converter efficiency for the both directions is between 94.5% and 96.5% (Depending on the battery voltage)

4. ac > DC rectifier efficiency is around 97.4% and this, for the inverter is 98.4%. This means that the rectifier contributes 38~45% of the total onboard charger losses (in charging mode). The contribution of the inverter losses is around 20~30% of the total onboard charger losses (in discharging mode). Thus it can be said that the DC-DC fullbridge converter is the main source of losses in the onboard charger.

5. In the DC-DC converter, transformer losses conduce to 30%, Switch losses (of eight IGBT switches) to more than 60%, and nductor losses to less than 10% of total losses.

MOSFET or IGBT?

It is found that although IGBTs exhibit a bit less losses in power rating of 3.7 kW and voltage of 300- 400 V, but there are some MOSFETs with ultra fast body diodes, namely IRFP models that are also good. On the other hands, COOL MOS MOSFETs are not suitable for this application. Generally it can be said that for these ratings, IGBTs have lower switching losses while MOSFETs have lower conduction losses. (Fig.5. 10)

10.2 Future work

The software used for this study was MATLAB SIMULINK. This software had some limitations: (1) Different solvers can lead to quite different results, making the selection of proper solver difficult. (2) In the diodes, reverse recovery current (charge) cannot be set, thus the effect of this on losses, as well as on the waveforms cannot be studied. The same can be said for MOSFETs as well. I.e. it is not possible to set C_{gd} or drain lead inductance in the parameters settings. MATLAB scripts were written to find the losses. Thus for the future work it is not recommended to use SIMULINK SIMPOWER for the losses assessment, as the result could be unrealistic. But the control tools are handy, accurate and easy to use.

A lack of an accurate mathematic model of transformer core losses, especially at short time transients, suggests that the core losses is better to be analyzed by FEM softwares, where the role of more elements can be considered in the losses.

Furthermore the newer transformer materials, like Nono-crystalline may reduce the transformer losses significantly and can be a good topic to study.

It was shown that the switching losses are a big problem, as the usage of snubbers is not easy. In [4] it is explained why the diode turn-off snubbers cannot be used in fullbridge configuration. Capacitive snubbers, suitable only for reducing EMI and dv/dt in fullbridge configuration, cannot be used, as the diodes in secondary side in discharging mode short circuit the paralleled capacitors.

One of the main topics of this work was to investigate the reverse recovery effect in MOSFET switch losses, while for the IGBTs, the switch turn-on, turn-off, and diode turn-off losses are only given based on switch current. But besides switch current other elements also affect the losses. The investigation of accurate switch losses of IGBTs can be done by following this thesis.

The last but not least, the implementation and practical issues are the most important and challenging parts and we are looking forward to see the day of its implementation and hope this report can be helpful.

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Appendix A) List of MOSFETs and IGBTs

Table A-1 List of investigated MOSFETs

Model	IRFPS43N50K	IRFPS40N60K	IRFPS40N50L	IRFPS38N60L	IRFP31N50L
V-I(25)-I(100C)	500-47-29	600-40-24	500-46-29	600-24-38	500-20-31
$\mathbf{R_{ds_{on}}}$[1]	0.08	0.11	0.1	0.12	0.15
$\mathbf{V_{dd,ref}}$	250	300	250	300	250
$\mathbf{I_{d,ref}}$	47	38	46	38	31
$\mathbf{R_G}$	1	4.3	0.85	1.2	4.3
Crss[2]	1.25e-09	1.050e-09	1.50e-09	1.250e-09	1.0e-09
$\mathbf{t_{ri}}$	140	110	170	130	115
$\mathbf{t_{fi}}$	74	60	69	69	53
Qrr (typ@ 25C)	1.40E-05	1.40E-05	7.05E-07	8.30E-07	5.70E-07
$\mathbf{V_{plat}}$	5	5	5	5	5
$\mathbf{V_{GS}}$	10	10	10	10	10
$\mathbf{R_D}$ [3]	0.02	0.015	0.025	0.03	0.025
$\mathbf{V_{D0}}$[4]	0.58	0.65	0.5	0.5	0.55

Table A-2 List of investigated MOSFETs

Model	IRFP460	FDH27N50	IRFPS37N50A	IRFP22N50A	IRFP32N50K
V-I(25)-I(100C)	500-12-20	500-19-27	500.000	500-22-14	500-32-20
$\mathbf{R_{ds_{on}}}$	0.27	0.19	0.1	0.21	0.2
$\mathbf{V_{dd,ref}}$	250	250	250	250	250
$\mathbf{I_{d,ref}}$	21	27	36	22	32
$\mathbf{R_G}$	4.3	2.15	4.3	4.3	4.3
Crss	5.0e-10	1.5e-10	1.0e-09	5.5e-10	2.5e-10
$\mathbf{t_{ri}}$	81	54	98	94	120
$\mathbf{t_{fi}}$	65	54	80	47	54
Qrr (typ @ 25C)	3.80E-06	9.20E-06	8.60E-06	6.10E-06	9.00E-06
$\mathbf{V_{plat}}$	5	5	5	5	5
$\mathbf{V_{GS}}$	10	10	10	10	10
$\mathbf{R_D}$	0.033	0.01	0.02	0.02	0.0175
$\mathbf{V_{D0}}$	0.6	0.7	0.55	0.6	0.65

Table A-3 List of investigated MOSFETs

Model	IRFP23N50L	STW26NM50	STF25NM50N	IRFP460A	SPW32N50C3
V-I(25)-I(100C)	500-23-15	500-30-18.9	500-22-14	500-20-13	560-32-20

[1] MOSFET On-state resistance obtained from output characteristics graph at Junction temperature, $T_j = 25°C$

[2] Crss is derived from its respective graph as explained in chapter 4 (two-point approximation method)

[3] Body diode on-state resistance Obtained from respective graph at Junction temperature, $T_j = 25°C$

[4] Body diode on-state Constant voltage source Obtained from respective graph at Junction temperature, $T_j = 25°C$

$\mathbf{R_{ds_{on}}}$(25)	0.235	0.12	0.1	0.22	0.075
$\mathbf{V_{dd,ref}}$	250	250	250	250	380
$\mathbf{I_{d,ref}}$	23	13	11	20	32
$\mathbf{R_G}$	6	4.6	4.7	4.3	2.7
Crss	5.0e-10	5.0e-10	1.25e-09	5. 0e-10	1.0e-09
$\mathbf{t_{ri}}$	94	15	23	55	30
$\mathbf{t_{fi}}$	45	19	22	39	10
Qrr (typ @ 25C)	5.60E-07	5.50E-06	6.90E-06	5.00E-06	1.50E-05
$\mathbf{V_{plat}}$	5	5	5	5	5
$\mathbf{V_{GS}}$	10	10	10	10	10
$\mathbf{R_D}$	0.02	0.0025	0.02	0.02	0.026
$\mathbf{V_{D0}}$	0.55	0.75	0.7	0.6	0.6

TableA-4 List of investigated MOSFETs

Model	SPW52N50C3	IPW60R045CP	SPW47N60C3	IXFR48N60P
V-I(25)-I(100C)	560-52-30	650-60-38	650-47-30	600-32-?
$\mathbf{R_{ds_{on}}}$	0.05	0.045	0.05	0.1
$\mathbf{V_{dd,ref}}$	380	400	380	300
$\mathbf{I_{d,ref}}$	52	44	47	32
$\mathbf{R_g}$	1.8	3.3	1.8	2
Crss	5.0e-10	5.0e-10	5.0e-10	1.25e-09
$\mathbf{t_{ri}}$	30	20	27	25
$\mathbf{t_{fi}}$	10	10	8	22
Qrr (typ @ 25C)	2.00E-05	1.70E-05	2.30E-05	8.00E-07
$\mathbf{V_{plat}}$	5	5	5.5	0
$\mathbf{V_{GS}}$	10	10	10	0
$\mathbf{R_D}$	0.005	0.0125	0*	0.015
$\mathbf{V_{D0}}$	0.8	0.7	0	0.65

Table A-5 List of investigated IGBTs

Model	BSM50GB60DLC	IKW20N60T	IKW20N60H3	IKW30N60H3	STGP19NC60WD
V-I(25)-I(100C)	600-75-50	600-40-20	600-40-20	600-60-30	600-40-22
$\mathbf{R_{IGBT,on}}$	0.034	0.02	0.05	0.035	0.15
$\mathbf{V_{dd,ref}}$	380	380	380	380	380
$\mathbf{I_{d,ref}}$	47	47	47	47	47
$\mathbf{V_{CE,0}}$	0.75	1	1	1	0
Etot [mj][1]	0.1+0.4+0.8=1.3	0.5	0.4	0.35	0.18
$\mathbf{R_D}$	0.0125	0.04	0.035	0.05	0.085
$\mathbf{V_{D0}}$	0.8	1	0.75	1	1

[1] Total switching losses, E_{sw} is the sum of turn-on, turn-off and reverse recovery energy loss of an IGBT: $E_{sw} = E_{on} + E_{off} + E_{rec}$ at $T_j = 25°C$ and $I_C = 7{\sim}10A$

Appendix B) Transformer cores and losses

B. 1 Some useful concepts

Current density

In the domain of electrical wiring (isolated copper), maximum current density can vary from 4A/mm² for a wire isolated from free air to 6A/mm² for a wire in free air. However in our calculations in order to prevent excessive temperature rise, we assume j= 3 A/mm²

Fill factor

Number of turns, N times copper cross section; A_{Cu} will give us total copper area. For some reasons $A_w > N.A_{Cu}$: first, most of times the cross section of wire is circular and this makes impossible to completely fill winding area because there are some spaces between circles. Second, each wire has to have a thin insulation layer and this layer occupies some space of winding area. Fill factor, k_{Cu} is a ratio of total copper area to core winding area [4]

$$k_{Cu} = \frac{N.A_{Cu}}{A_w}$$

Normally Fill factor for round conductors is around 0.5 – 0.6. But after studying different Litz wire manufacturers, we decide to use Profile Litz wires in square or rectangular section. This makes optimum use of the available winding space and cut wasted space in windings. (Fig.3.14)

Fig.B. 1 an example of Profile Litz wire with 65-80% copper fill factor which enables winding without bobbin (self bonding enamel / acetate silk) with max available cross section of 1 mm² Cortesy of RUPALIT®[1]

Scale Factor, SF

Sometimes the cores we are looking for are not available in the market. With SF, we scale the available cores to fit our needs. It means each dimension is multiplied with SF, so the new volume/ weight of the core is proportional to cube of SF.

Core datasheet:

Core Datasheets provide useful information on effective length, volume, airgap length $(L_{air} or\ L_g)$, cross section and material permeability. With effective Length (L_e) and cross

[1] http://www.pack-feindraehte.de/en/products/litzwire/produkt.php?produkt_id=7

section (A_e), a core can simplified to a cylinder with L_e length and A_e cross section. For example for *E71/33/32-E250* core (material: 3C90):

Table B. 1

Core	Ve (m^3)	Le (m)	Ae (m^2)	m(kg)	μr	Lair(um)	d(mm)	b(mm)	h(mm)	c(mm)
E713332E250	0.000102	0.149	0.000683	0.26	1880	5280	48	22	21.9	32

B.2 Finding the winding area, length of turn and maximum winding turns

Winding window area depends on the core shapes. For example, according to Fig.4.16 winding area for E type core can be calculated as follows (without considering bobbin area):

$$a = (d - b)/2$$

$$A_w = 2ah$$

A_w : Winding area

Considering SF, the new winding area would be:

$$A_{w,new} = 2ah\,SF^2$$

Copper wires are winded around the Bobbins and in fact they are coil formers. Bobbins, while in most cases seem necessary have the drawback that they reduce the winding area. They also increase the length of each turn (and so copper losses).

Unfortunately in most core datasheets, the area that a Bobbin occupies is not mentioned. Here, a method to estimate the occupied space is introduced and applied to all the cores that the winding area is not given.

To check the validity of the method, the result of the method is tested with the E55/28/21 core. Based on the data sheet, length of turn is 116 mm (table...):

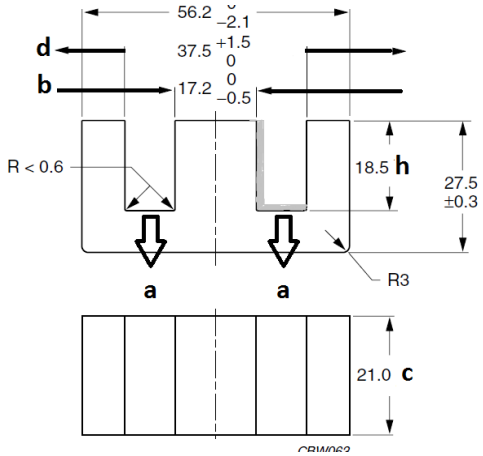

Fig.B. 2 Gray area, Bobbin area. These values are for half core. For full core h should be doubled. From the E55/28/21 datasheet

$$Average\ Length\ of\ turn = 2[(b + a) + (c + a)] = 2b + 2c + 4a$$

$$a = \frac{d - b}{2} = \frac{37.5 - 17.2}{2} = 10.15\ mm$$

$$Length\ of\ turn = 2(c + d)$$

$Length\ of\ turn = 117\ mm$

Bobbin area: Bobbin occupies certain space. It is supposed that the difference between data sheet and our calculated area is occupied by Bobbin (gray area in Fig.B. 2)

We assume bobbin reduces the actual size of winding area, A_w which is:

$A_w = 2ah = 375.5\ mm2$

In the data sheets, generally the winding area is for total core not half core.

winding area in data sheet = 250~277 mm^2 (Depending on the chosen bobbin) For the worst case calculation we can find bobbin area, S_{Bobbin} to be:

$S_{Bobbin} = 375.5 - 250 = 125.5\ mm^2$

By assuming the same thickness x in all the bobbin sides, we can estimate x:

$S_{Bobbin} = 2x(a + h) \approx 125.5\ mm2$

$x = 2.18\ mm$

In this thesis it is assumed that this width is applicable for all the cores that the winding area on the datasheet is not given.

Let's check *E65/32/27* core ($d = 44.2, b = 20, h = 22.2\ mm$)

The winding area without considering bobbin can be calculated by:

$A_w = 2ah = a(d - b) = (44.2 - 20)\ 22.2 = 537mm2$

Based on previous calculations and the same bobbin thickness for all cores, bobbin area would be:

$S_{Bobbin} \approx 2ax + 2hx = 2x(a + h)$

$= 2 \times 12.1 \times 2.18 + 2 \times 22.2 \times 2.18 = 149.5\ mm^2$

So available winding area should be:

$S_{winding} = A_w - S_{Bobbin} = 537 - 149.5 = 387.5\ mm2$

The Winding area in data sheet is 394 mm^2.

In the cores with rounded cross section (like ETD, PM and EC cores) we add thickness x *to* the radius, r and calculate the winding area based on the new increased radius.

B.2.1 Finding the Maximum number of turns

Winding area provides the space for primary and secondary windings of a transformer. By assuming constant current density, j for both primary and secondary side, we can say:

$$N_1 I_1 = N_2 I_2 \Rightarrow N_1 j_1 A_1 = N_2 j_2 A_2 \xrightarrow{j_1 = j_2 = 3A/mm^2} N_1 A_1 = n N_1 A_2$$

A_1(A_2): copper cross section needed on primary(secondary)

S, Needed winding area, can be calculated:

$$S = \frac{N_1 A_1 + N_2 A_2}{K_{cu}}$$

K_{cu}: Filling factor that can be up to 0.8 for chosen type of LITZ wire. Here we assume K_{cu}=0.75

And the maximum number of turns that can be fit in available winding area is:

$$N_{1,Max} = \frac{2\acute{S}K_{cu}}{A_1 + nA_2}$$

Ś is a winding area of a half core that can be found in most datasheets. For EC70 , Ś = 465 mm^2

For EC70, which is the chosen core for the transformer, $N_{1,max}$can be found:

$$N_{1,Max} = \frac{2\acute{S}K_{cu}}{A_1 + nA_2} = \frac{2 \times 465 \times 0.75}{4 + \frac{4}{3}\ 3} = 87$$

B.3 Initial transformer losses calculation

Initially, more than 50[1] cores were investigated to have a general understanding about the dimension of transformer losses. The flux density is found by (6.1) and Steinmetz equation is used to find the core losses. As we saw in chapter 6, the losses obtained by (6.1) and Steinmetz equation, for transformer losses is not quite correct, but at least it can be a good guide to find the cores with the lowest losses, as are presented in table

Table B.2 Comparison of transformer cores and their losses with two different materials

	E552821	**E653227E100**	**ETD59**	**ETD54**	**EC70**
$P_{cu,T}$[2]	8.96	7.63	7.84	9.32	9.45
$P_{fe}(3C90)$	75.02	134.69	87.80	60.53	34.18
$P_{tot}(3C90)$[3]	83.98	142.32	95.65	69.85	43.63
$P_{fe}(3C92)$	36.25	65.09	42.43	29.25	16.52
$P_{tot}(3C92)$	45.22	72.72	50.27	38.57	25.97

Comparing Core losses, based on two materials, 3C90 and 3C92, shows that in contrast with inductor losses, in transformers, material can affect the core losses dramatically.

Table B.2 suggests that EC70, with its large winding area is a good candidate for this project.

In the next section, the parameters of a transformer core which affect the transformer losses will be studied. The losses in the next section are found based on the summation method, introduced in chapter 6.

B.4 Transformer parameters and core losses

Number of turns and transformer losses

Both core and copper losses increase by increasing the number of turns. For copper losses this increase (as was proven in chapter 4) is linear. While for core losses, as it can be seen in (6.2) increasing N will increases B and this will increase total core losses.

On the other hand, magnetizing inductance, $L_{m_{pri}}$ is desired to be high enough to not distort the transformer output current. So $N1$ should be high enough.

Fig.B. 3 shows transformer power losses as a function of $N1$ for four different voltages. It can be seen that copper losses can be neglected esp. at $N1 > 20$. Based on Fig.B. 4 $N1$ is chosen

[1] The list of these cores are:
E552821-E315 E552821-E250 E552821-E160 E552821-E100
E552825 E552825-E400 E552825-E315 E552825-E250 E552825-E160 E552825-E100
E562419 E562419-E400 E562419-E315 E562419-E250 E562419-E160 E562419-E100
E653227 E653227-E630 E653227-E400 E653227-E250 E653227-E160 E653227-E100
E713332 E713332-E630 E713332-E315 E713332-E250 E713332-E160 E713332-E100
E803820 E803820-E630 E803820-E315 E803820-E160 E803820-E100 E1006028 ETD59
ETD54 EE641050 EE641050A2500 EE641050-E1000 EE641050 E630-E630 EC70
EC70-A1000 EC70-A630 EC70-E400 EC70E250 ER641351 PM7459 PM8770_3C90
PM8770_3C94 PM11493_3C90 PM11493_3C94 TX7849

[2] Total copper losses: $P_{cu} = P_{cu_{pri}} + P_{cu_{sec}}$

[3] $P_{tot} = P_{fe} + P_{cu}$

to be 30 (so $N2 = 40$). Depending on the output voltage total losses will be between 20 and 45W.

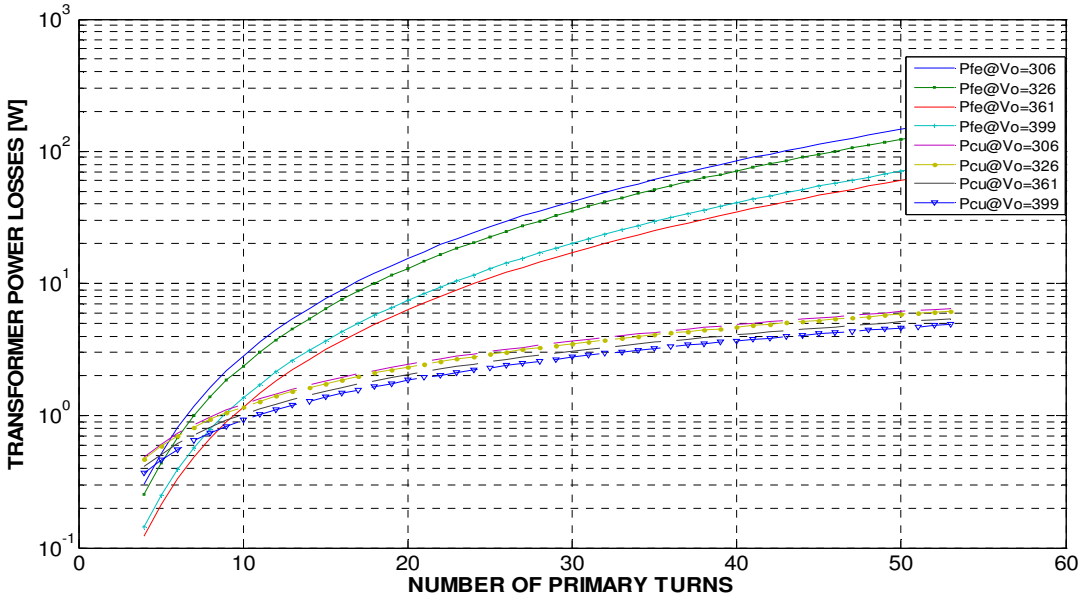

Fig.B. 3 Transformer core and copper losses as a function of number of primary turns when the core is EC70 ($airgap = 1830\ \mu M$, $\mu r_{3F3} = 2000$) (log scale)

It should be noted that with $N1 < 55$ flux never exceeds 0.4T as it can be seen in (6.2). (Decreasing N reduces the flux density.)

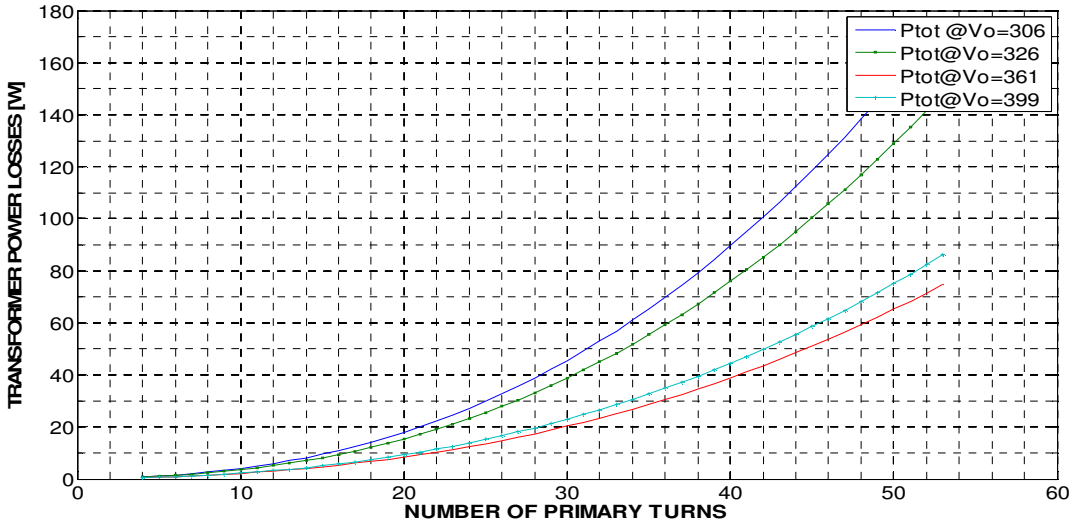

Fig.B. 4 Transformer total losses as a function of number of primary turns when the core is EC70 ($airgap = 1830\ \mu M$, $\mu r_{3F3} = 2000$) (linear scale)

Airgap and core losses

As discussed in chapter4, airgap length highly influences the (DC) flux density. This can be seen in Fig.B. 5. Fig.B. 5 shows that in order to prevent the core saturation (that results in very high current) which for 3F3 is around $0.4T$, airgap should be higher than 1mm.

Even if the airgap is 1mm, still core losses are so high. This can be seen in Fig.B. 6 (although copper losses are not affected by airgap as N is constant)

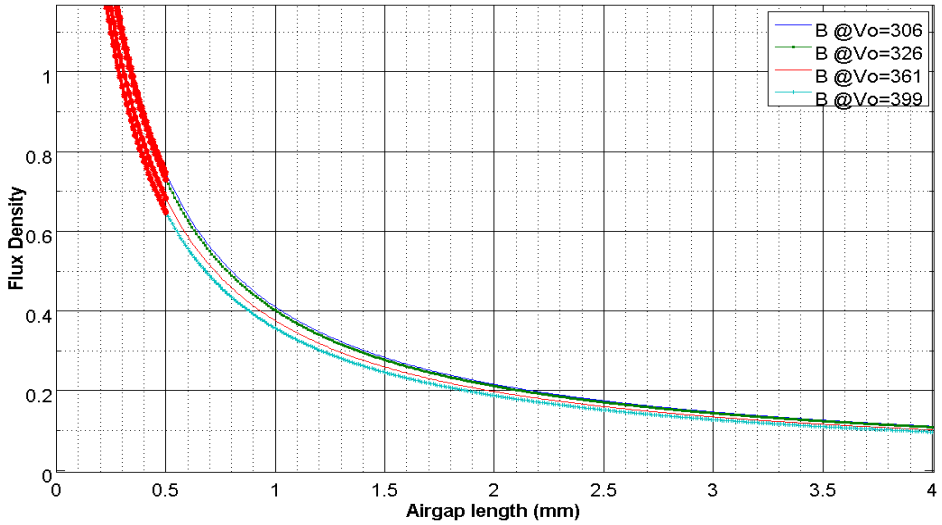

Fig.B. 5 Flux density as a function of airgap length when the core is EC70 ($N1 = 30, \mu r_{3F3} = 2000$)

EC70 manufacturer[1] doesn't provide airgap wider than 1830mm for this core. Large airgaps increase flux leakage and this may cause EMI problems.

Also as it can be seen, beyond 2mm, the losses reduction is not that significant. So the chosen airgap is 1830mm.

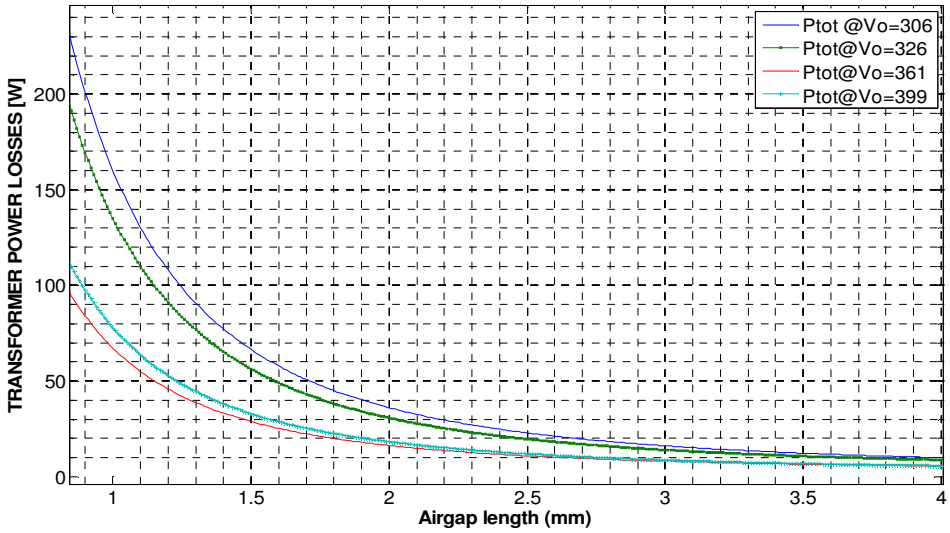

Fig.B. 6 Total transformer losses as a function of airgap length when the core is EC70 ($N1 = 30,\ \mu r_{3F3} = 2000$)

[1] Feroxcube.com

Core size and core losses

As discussed in section 4.2.4, one way to reduce the total transformer losses is to increase the effective length, L_e (to reduce the core losses) while preserving A_e(to keep copper losses constant). Fig.B. 4 depicts that by increasing the effective length (half core weight) from $144mm$ $(127g)$(original values) to $720mm$ $(1016g)$ transformer losses will reduce to half.

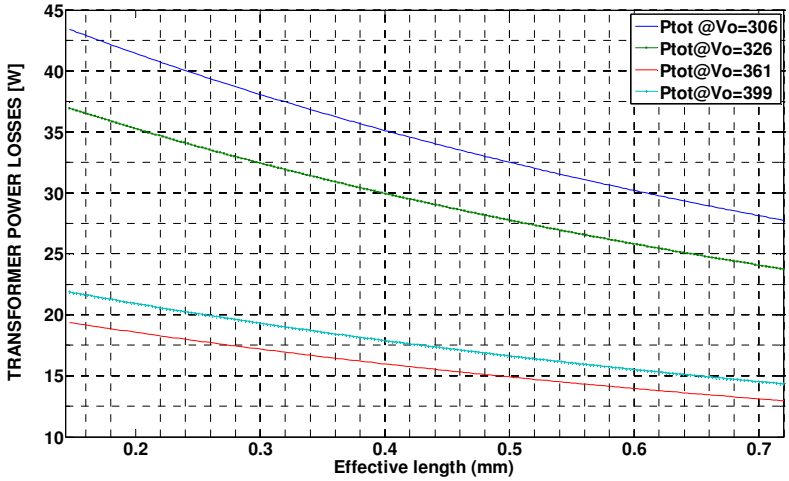

Fig.B. 7 Total transformer losses as a function of core effective length when the core is EC70 ($N1 = 30,\ airgap = 1830\mu m,\ \mu r_{3F3} = 2000$)

Effect of Frequency and output voltage on transformer losses

By increasing the frequency, the harmonics spectrum will not change. In this part, 3 different frequencies will be studied: $f_{sw} = 20, 40\ and\ 60kHz$. It is obvious that by increasing the frequency the total losses will increase. This can be seen in Fig.B. 8.

Increasing the voltage should generally reduce the transformer losses as the current (≈flux) will reduce in higher voltages. But core losses depend on harmonics order and their amplitude corresponding to each voltage level as well. I.e. when $V_{bat} = 399V$ the harmonics orders are higher than when $V_{bat} = 361V$ and this causes slightly higher core losses at $V_{bat} = 399V$. (Although the THD is more or less the same)

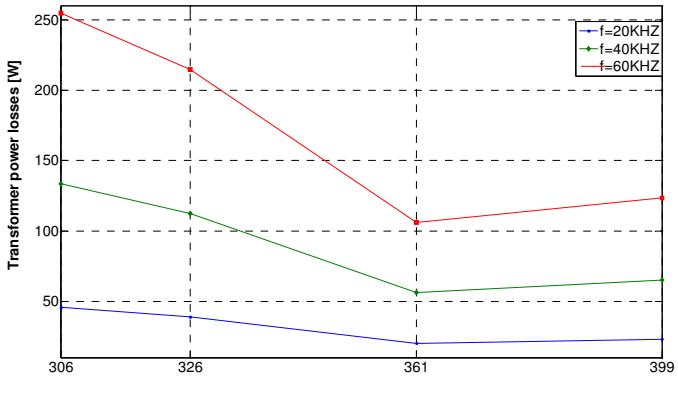

Fig.B. 1 Transformer losses as a function of output voltage (Battery voltage) for different frequencies